Past and Future of Mirco/Nano-Electronics

Nov 4, 2009

@S.K.P ENGINEERING COLLEGE,
Thiruvanmalail, Tamilnadu, India

Hiroshi Iwai,
Tokyo Institute of Technology

Tokyo Institute of Technology

Founded in 1881, Promoted to Univ. 1929

Institute Overview

Einstein Visit

Established in 1881→ 130th anniversary in 2011

3 undergraduate schools

School of Science, School of Engineering, School of Bioscience and Biotechnology

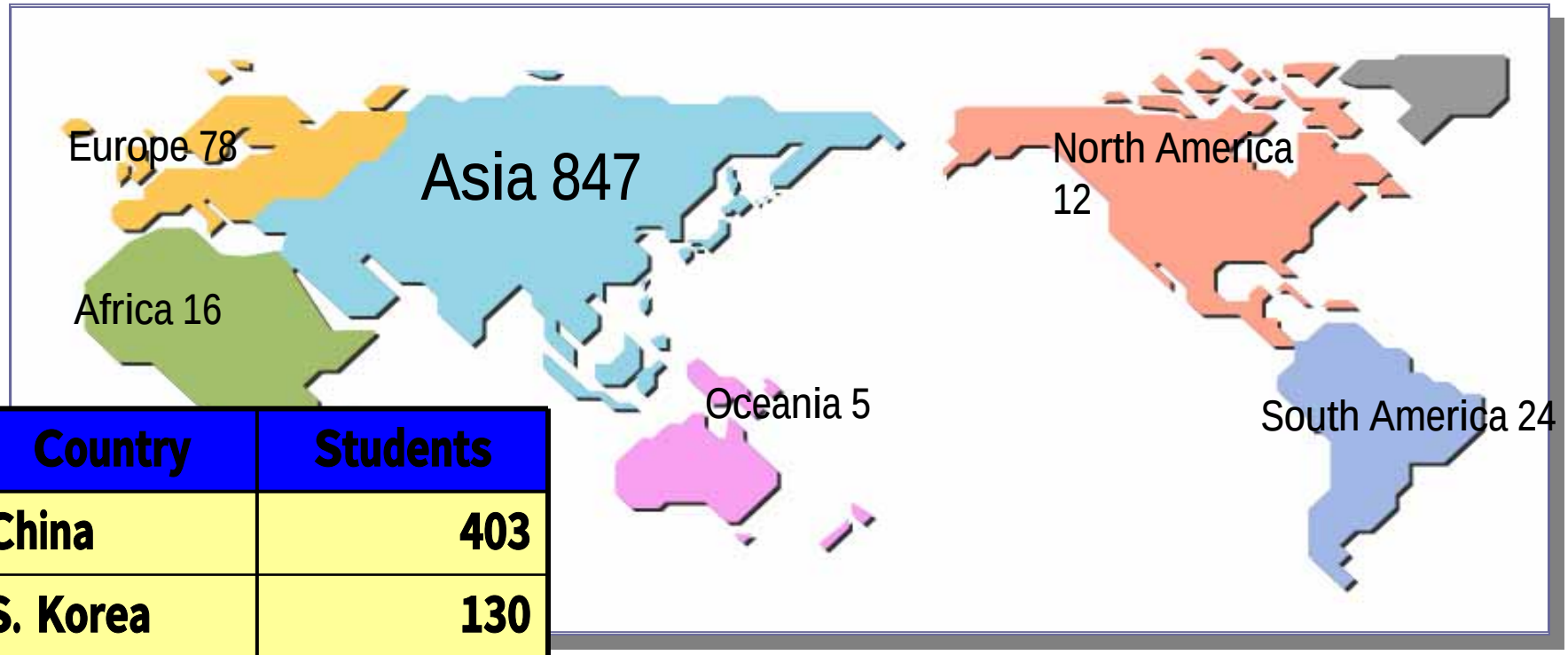
7 graduate schools

Science and Engineering Science, Science and Engineering Technology,
Bioscience and Biotechnology, Interdisciplinary Graduate School of Science and Engineering,
Information Science and Engineering, Decision Science and Technology, Innovation Management

Total Number of Students

	Undergraduate	Graduate	Master's	Doctoral	Teaching Staff	Student/Instructor	Staff
Tokyo Inst.	5,000	5,000	3,500	1,500	1,200	8.3	550
Per Year	1,200		1,800	500			

International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982

(As of May. 1, 2005)

岩井研メンバー

(2009年04月1日現在)


教授
岩井洋


准教授(共同研究)
筒井一生


客員教授
服部健雄


特任教授
名取研二


連携教授
杉井信之


連携教授
西山彰


助教
Parhat Ahme


助教
角嶋邦之

博士研究員


ﾐﾗﾝ･ﾍﾞﾗ

博士課程


D3
佐々木雄一朗


D3
ﾍﾝﾄﾞﾘｱﾝｼｬｰ･ｻｳｯﾃﾞｨﾝ


D3
下村浩


D3
宋在烈


D3
舘喜一


D2
川那子高暢


D2
佐藤創志


D2
冨田隆治


D1
Maimaitirexiati Maimaiti


D1
Abudukelimu Abudureheman


D1
幸田みゆき


筒井研 D3
小林勇介

修士課程


M2
新井英朗


M2
李映勲


M2
中山寛人


M2
船水清永


M2
細田亘


M2
又野克哉


M1
ﾀﾘｳｽ･ﾊｻﾝｻﾞﾃﾞ


M1
Mokhammad Sholihul Hadi


M1
小柳友常


M1
小澤健児


M1
神田高志


M1
澤田剛伸


M1
茂森直


M1
向井弘樹


筒井研 M2
横田知之


筒井研 M2
星野憲文


筒井研 M2
横手義智

学部


B4
来山大祐

スタッフ


松本昭子

辛川美琴

西澤　正子

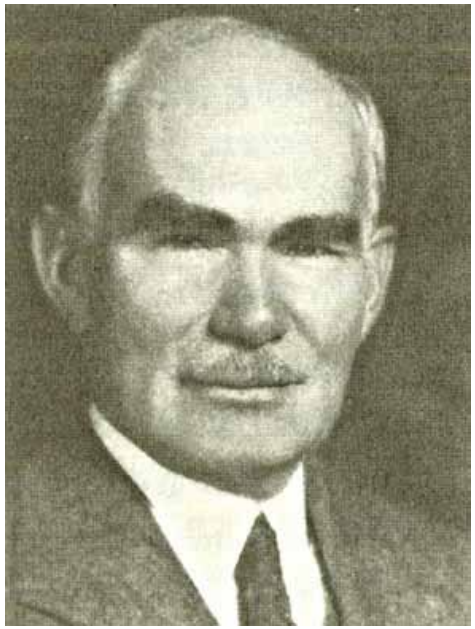
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

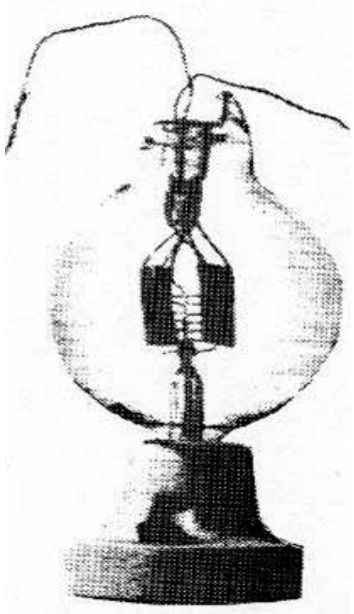
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

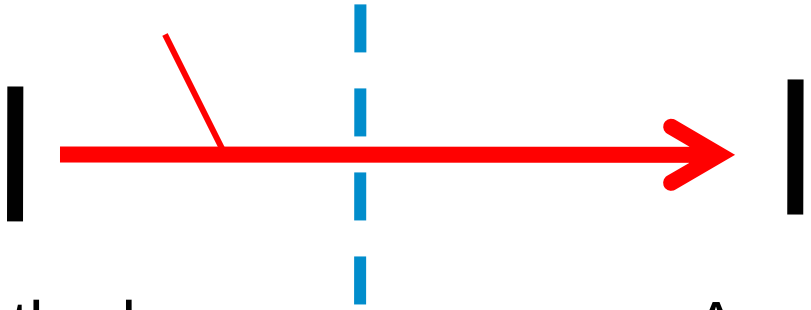


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

4 wives of Lee De Forest

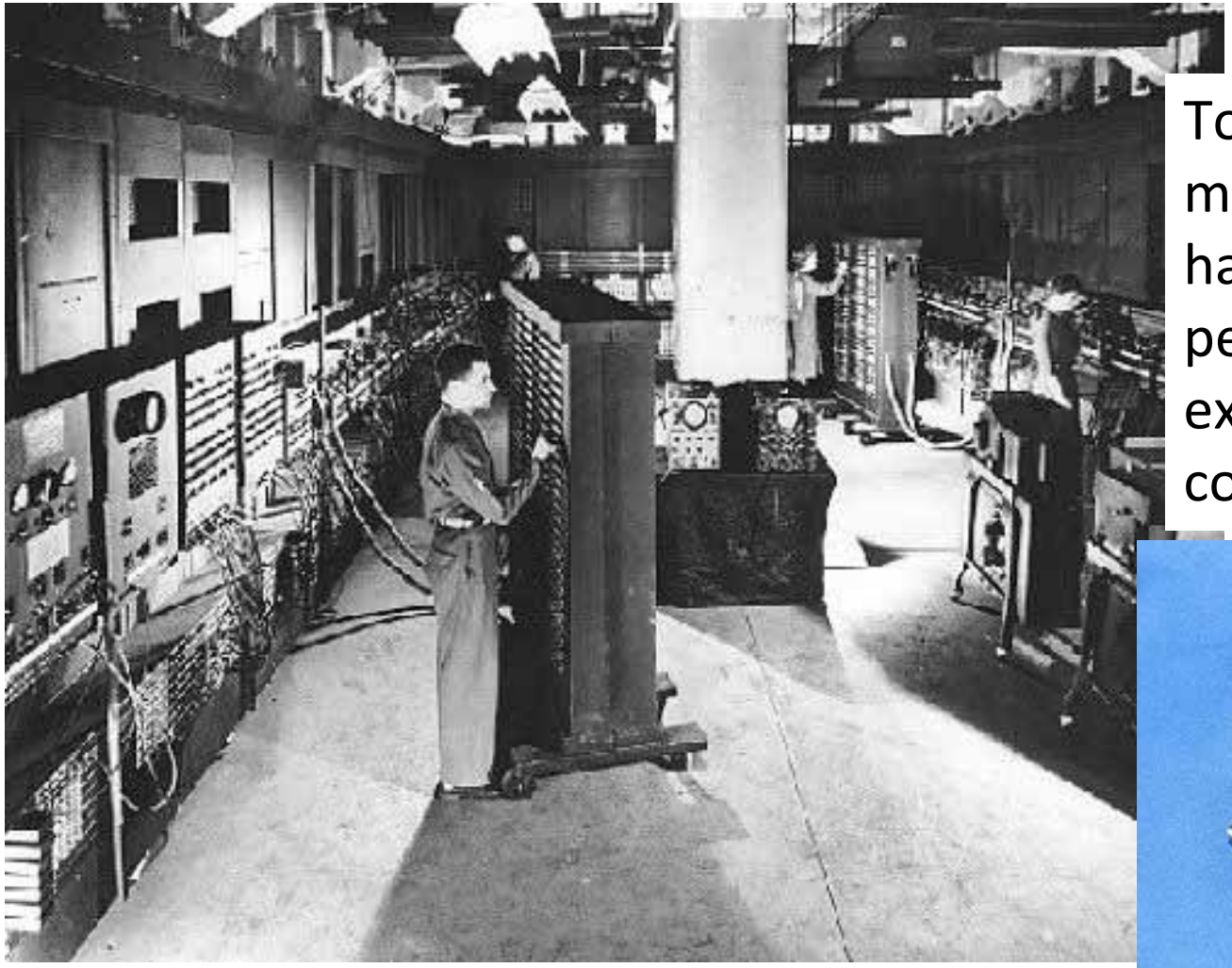
1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress

Mary

Marie

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor:
Ge Semiconductor, Bardeen, Brattin
→ Nobel Prize

1948, 1st Junction Bipolar Transistor,
Ge Semiconductor, Schokley
→ Nobel Prize

1958, 1st Integrated Circuits,
Ge Semiconductor, J.Kilby → Nobel Prize

1959, 1st Planar Integrated Circuits,
R.Noice

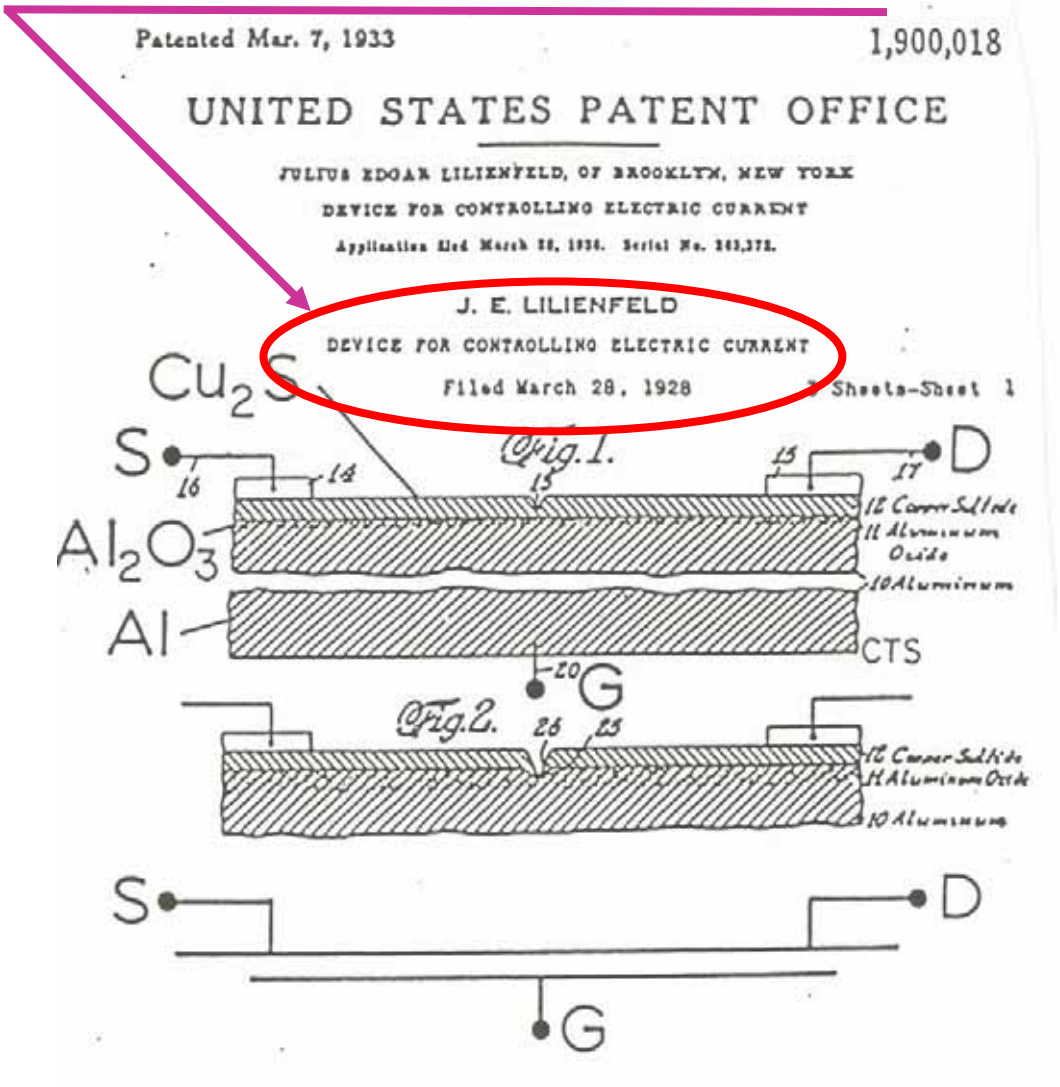
1960, 1st MOS Transistor, Kahng,
Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 263,372.

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 2 Sheets-Sheet 1

Cu_2S

S

D

Al_2O_3

Al

CTS

G

Fig. 1.

Fig. 2.

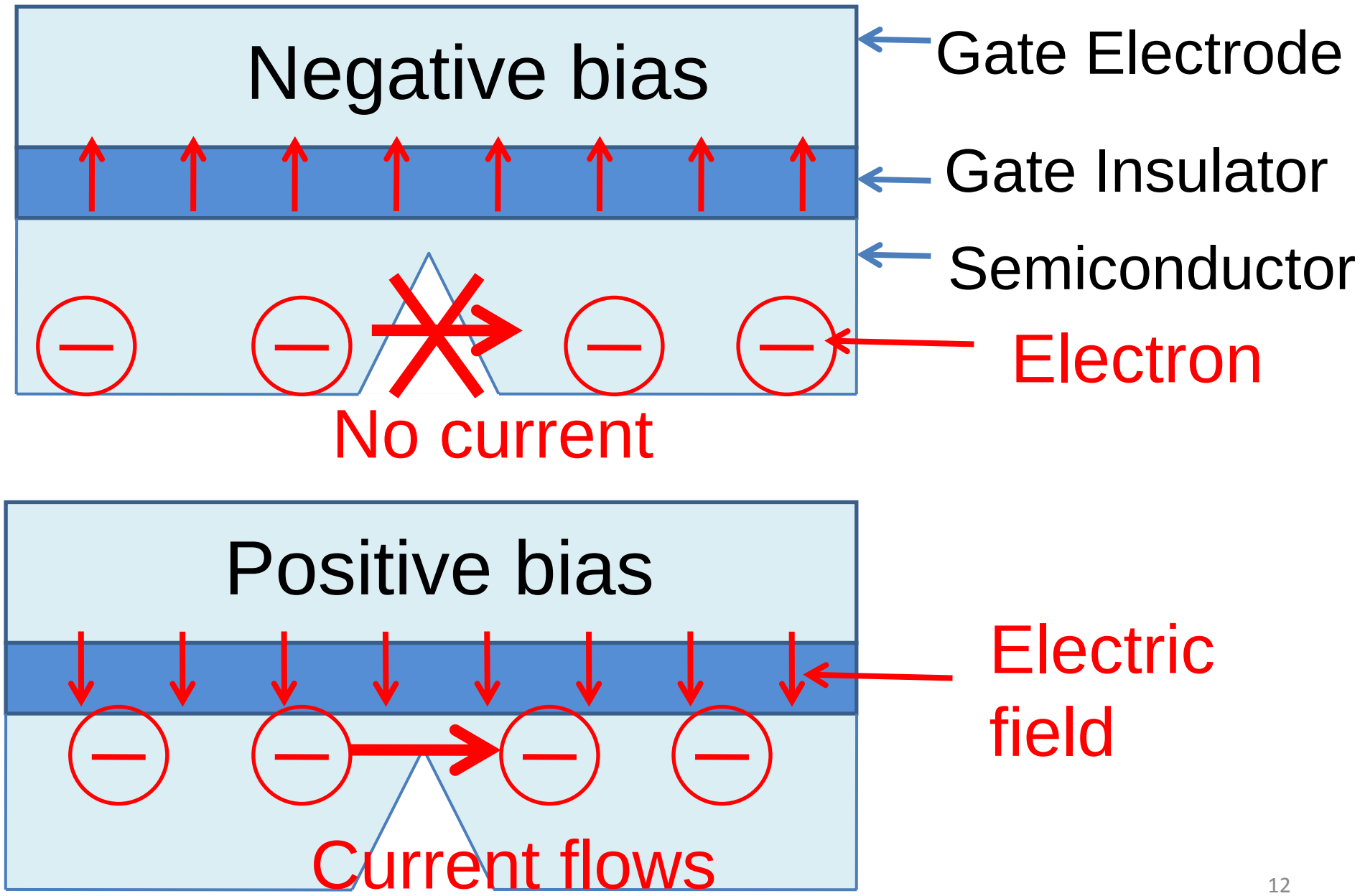
S

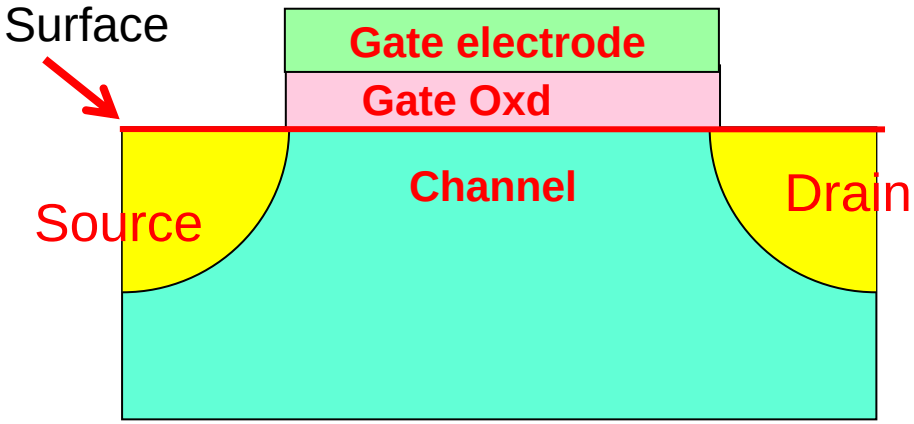
D

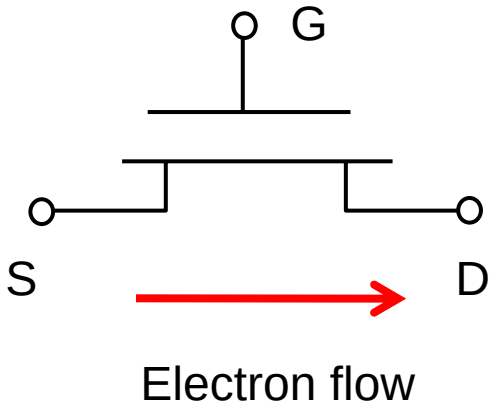
G

J.E.LILIENFELD

Capacitor structure with notch

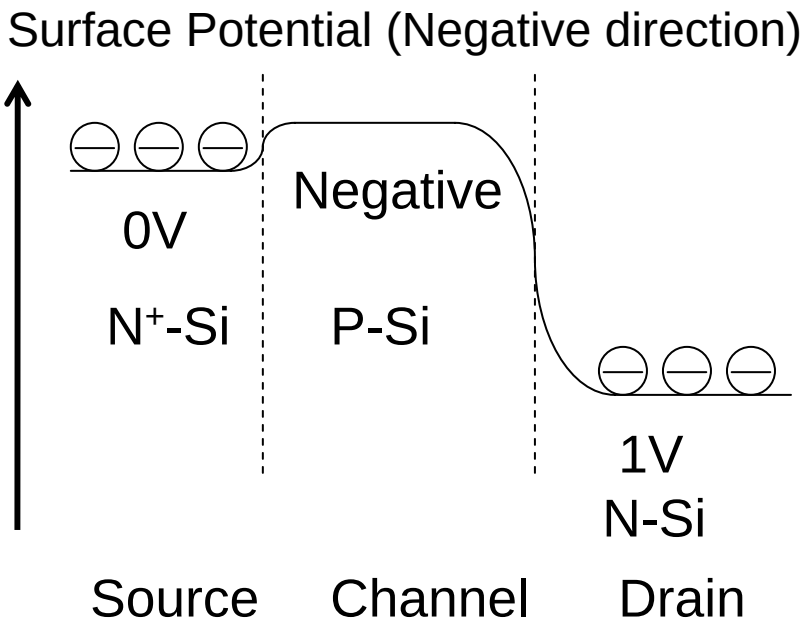


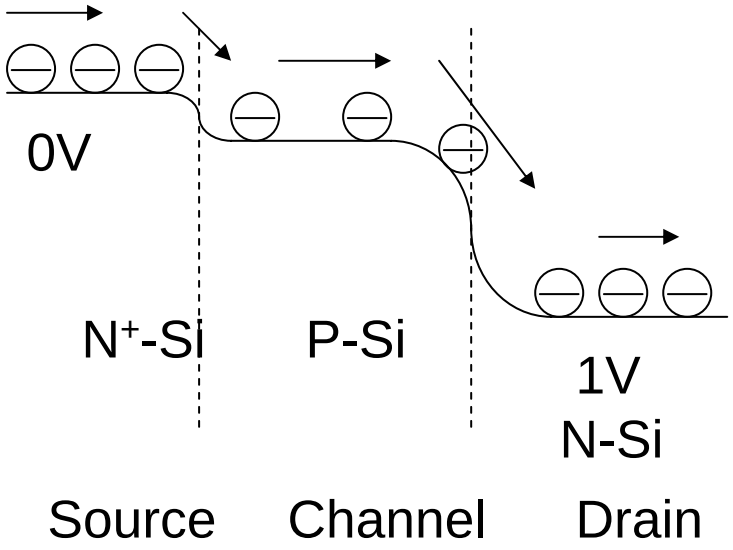




0 bias for gate

Positive bias for gate



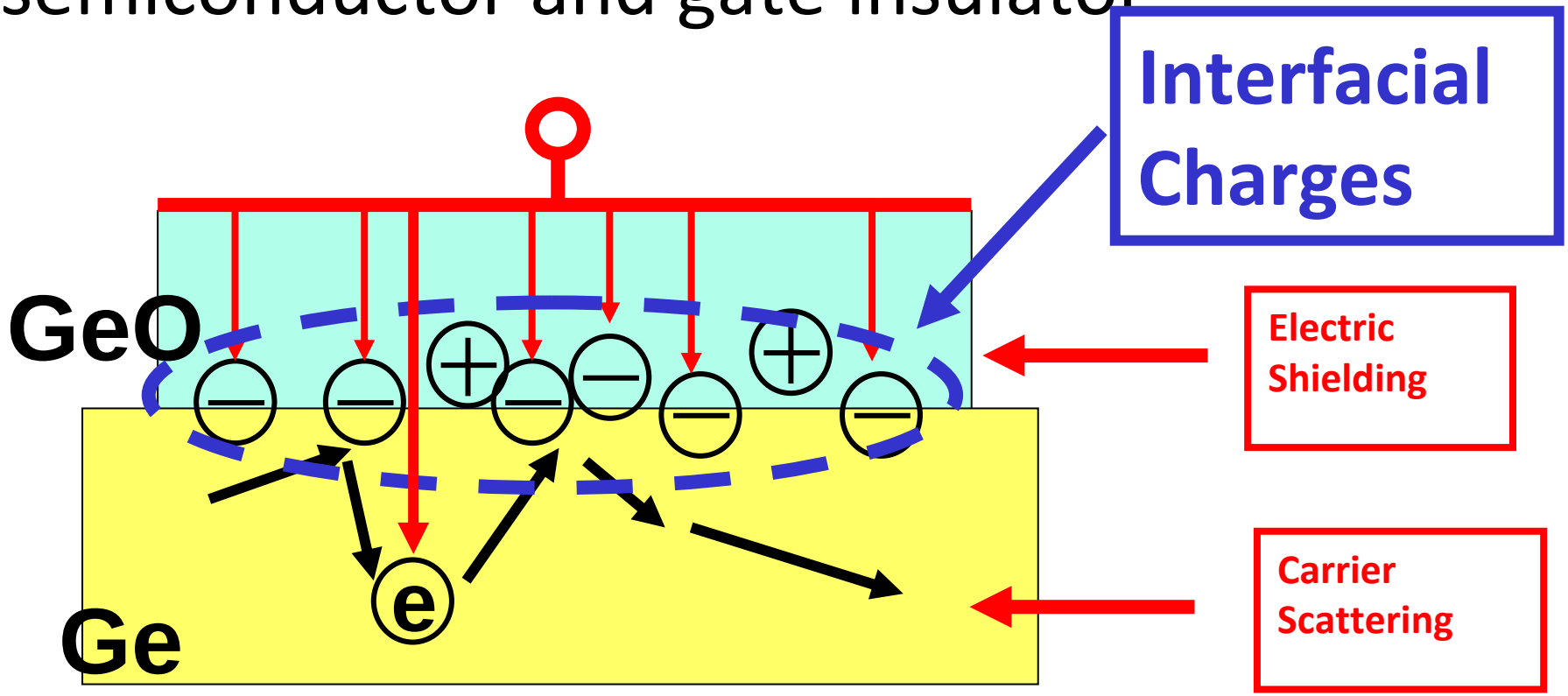


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator

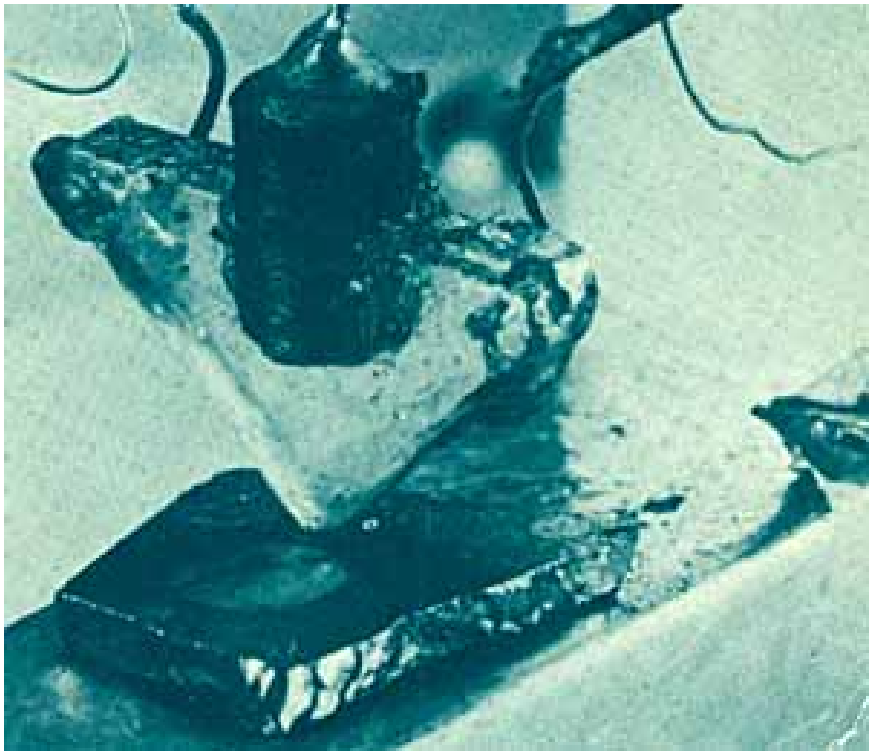


Drain Current was several orders of magnitude smaller than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor



Bipolar using Ge

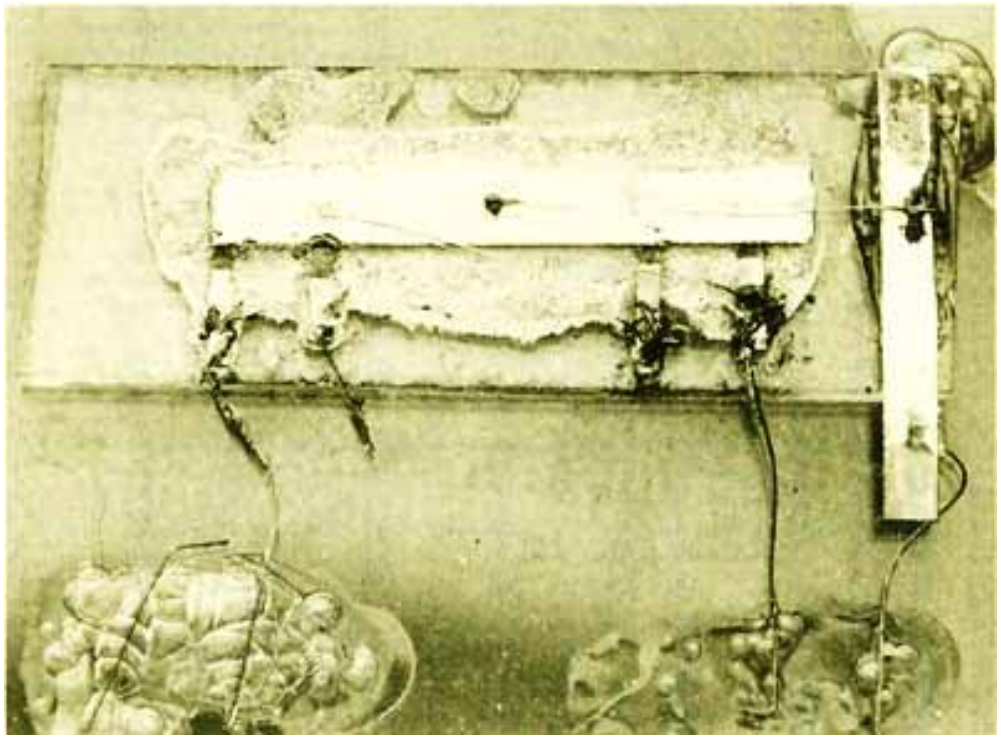
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

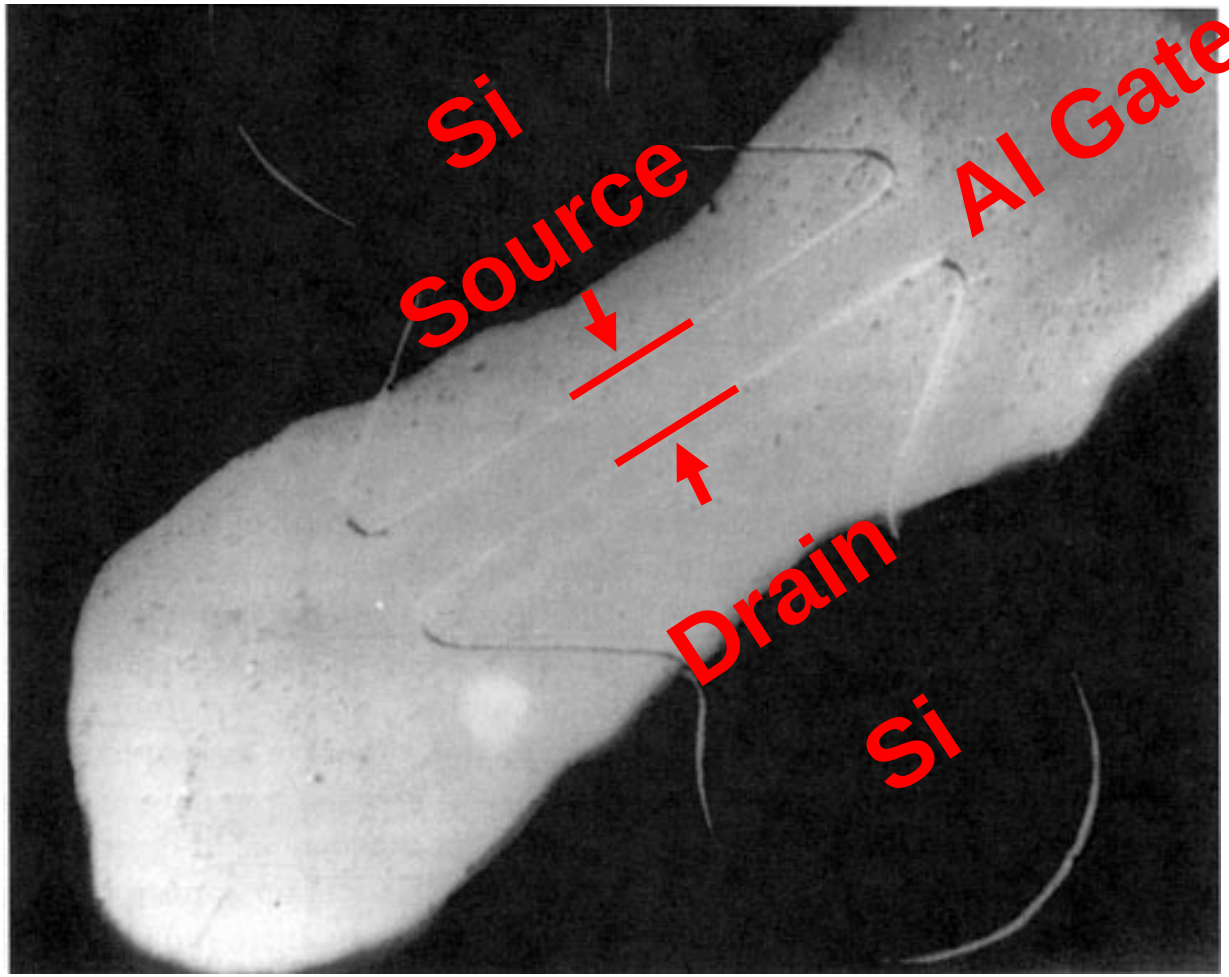
Jack S. Kilby

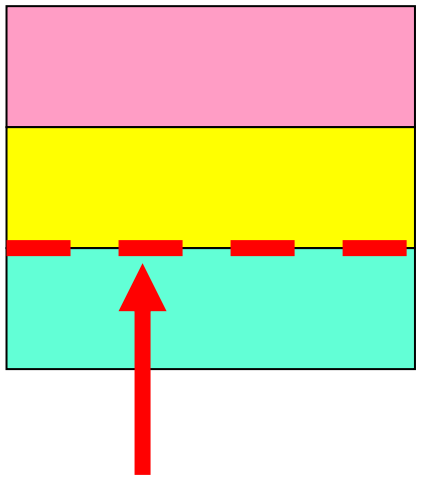
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

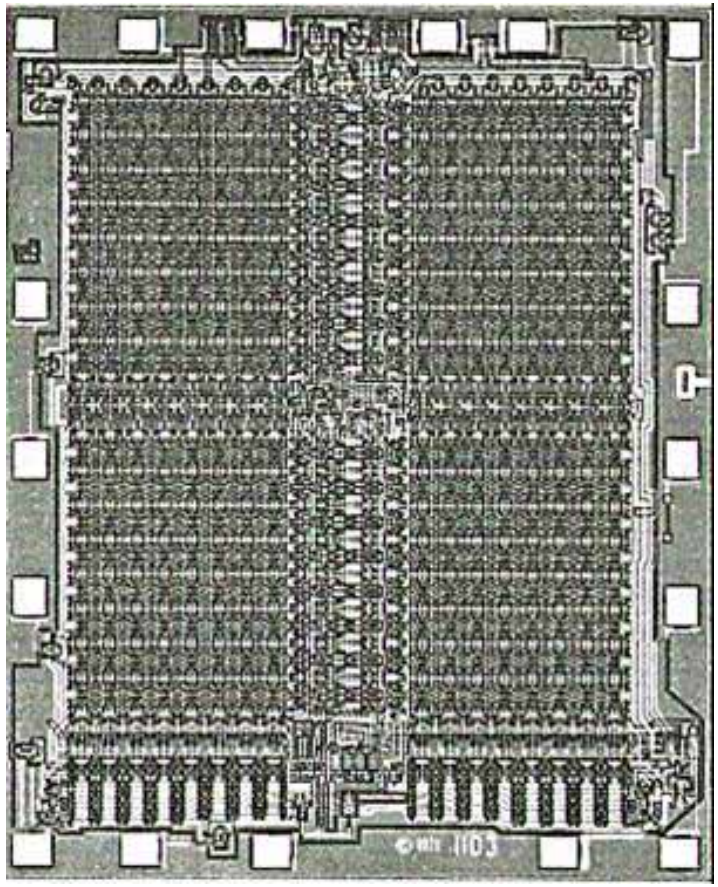
Top View



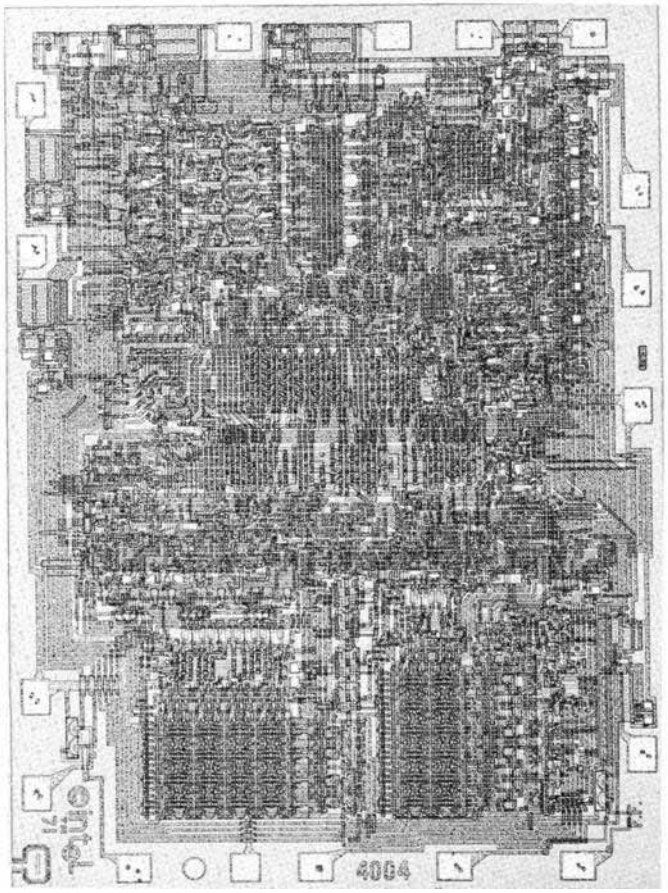


1970,71: 1st generation of LSIs

DRAM Intel 1103

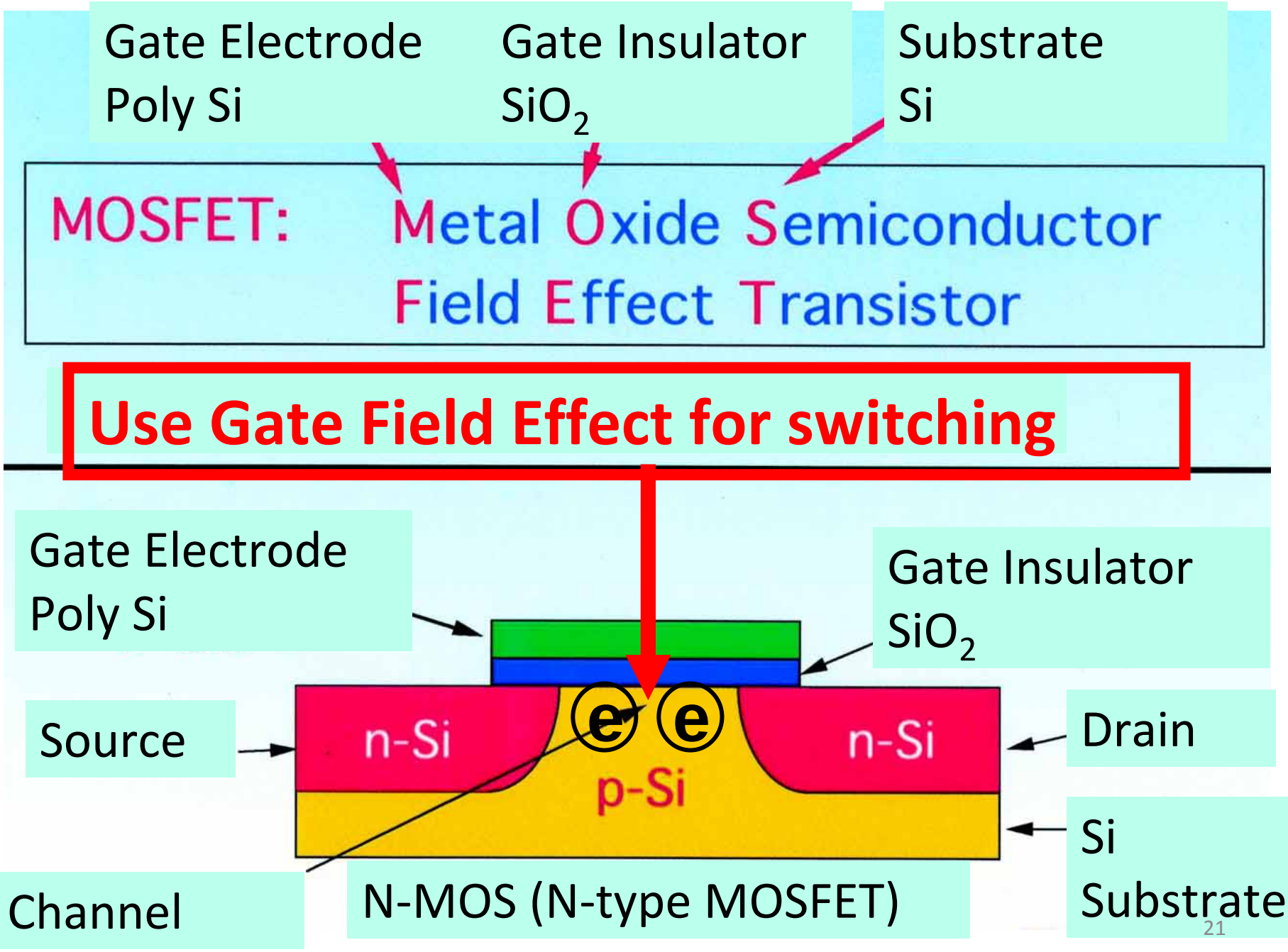


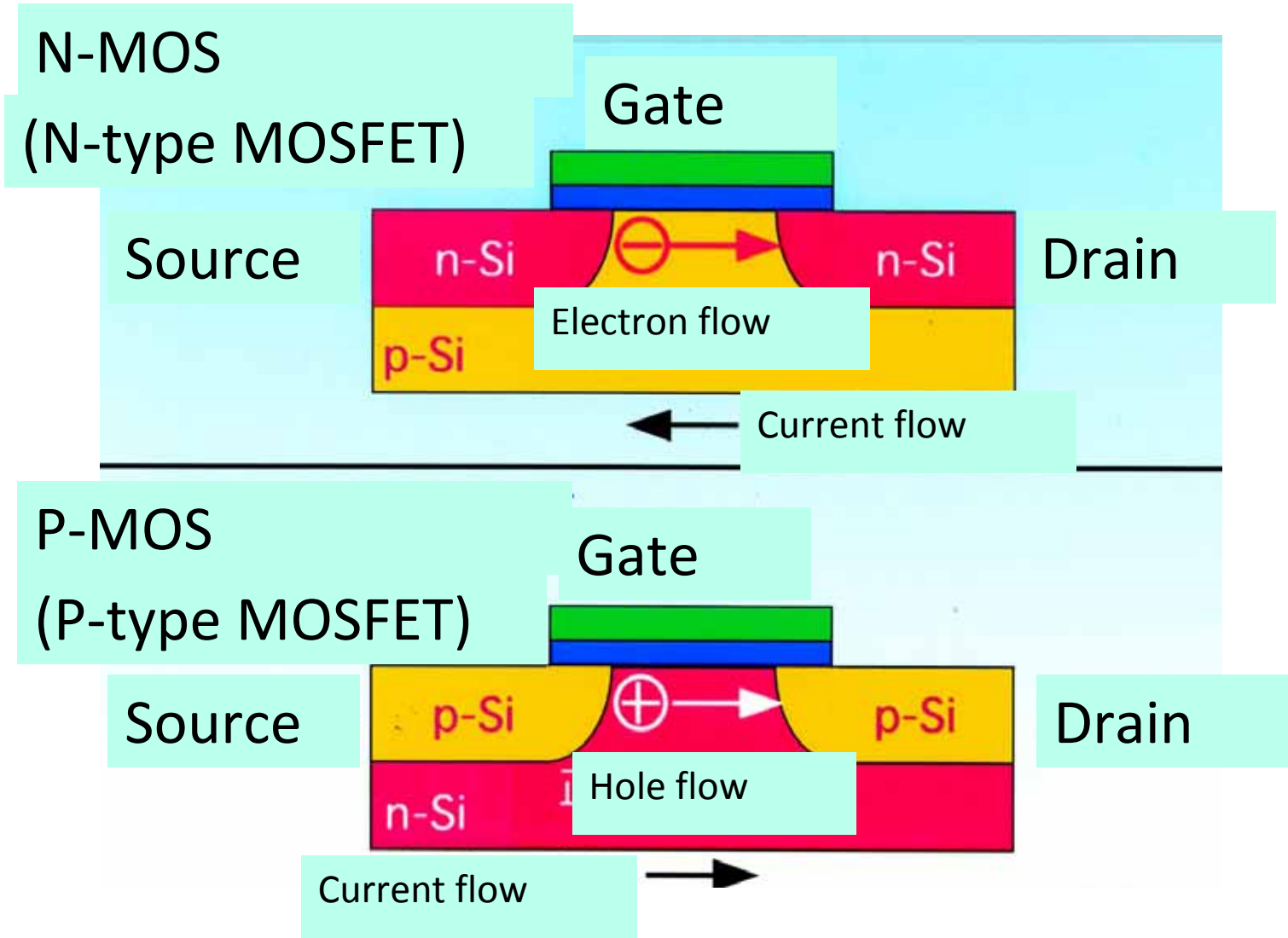
MPU Intel 4004



MOS LSI experienced continuous progress for many years

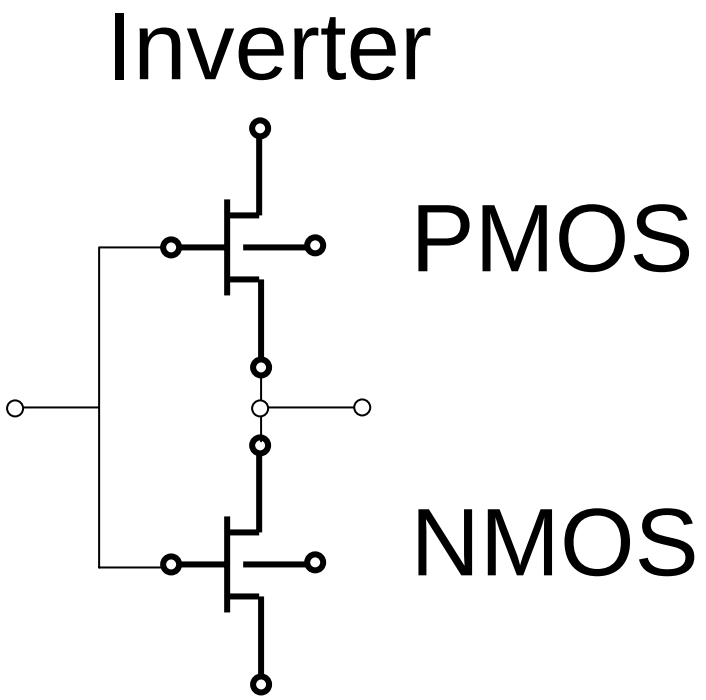
	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000


Gate Electrode
Poly Si
Gate Insulator
SiO2
Substrate
Si
MOSFET: Metal Oxide Semiconductor
Field Effect Transistor
Use Gate Field Effect for switching
Gate Electrode
Poly Si
Gate Insulator
SiO2
Source
n-Si
e
e
n-Si
Drain
p-Si
Si
Substrate
Channel
N-MOS (N-type MOSFET)


N-MOS
(N-type MOSFET)
Gate
Source
n-Si
n-Si
Drain
Electron flow
p-Si
Current flow
P-MOS
(P-type MOSFET)
Gate
Source
p-Si
p-Si
Drain
Hole flow
n-Si
Current flow

CMOS

Complimentary MOS



When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

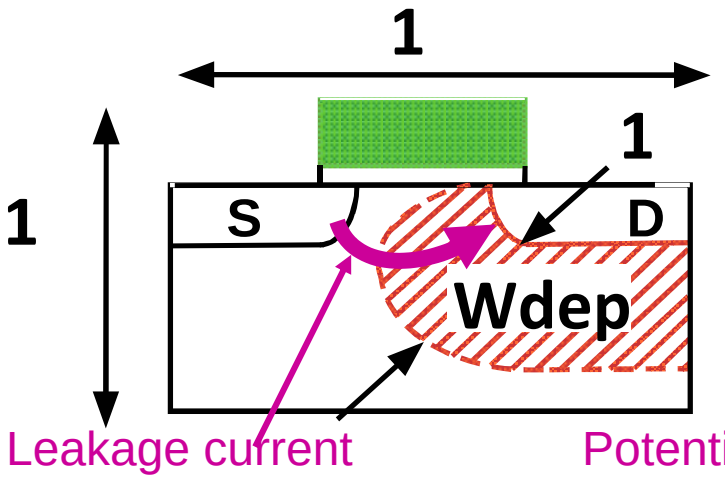
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

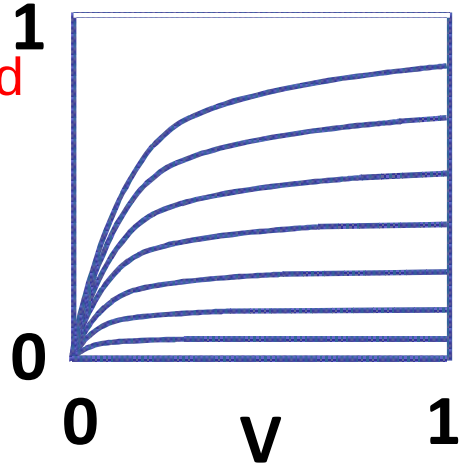
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

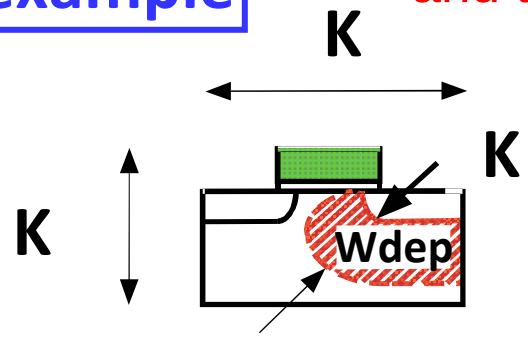
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

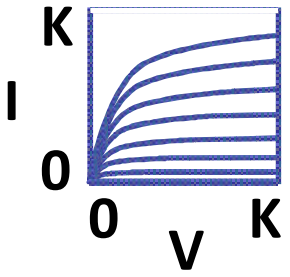
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$Wdep \propto \sqrt{V/Na}$$
$$: K$$



I : K

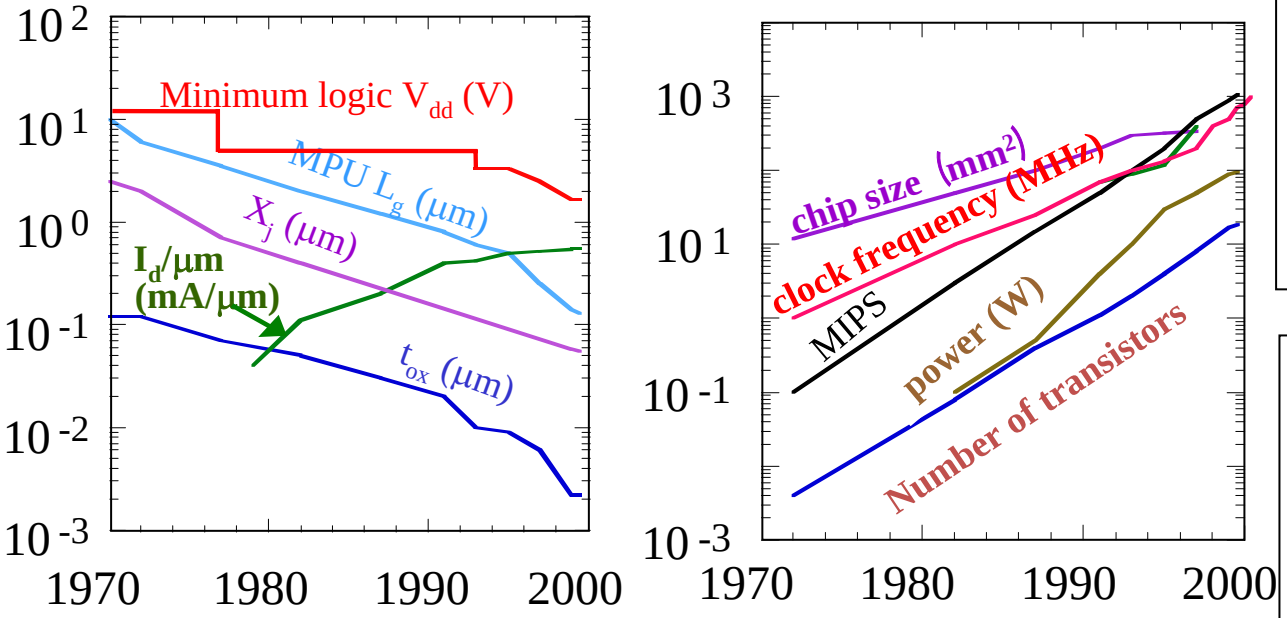
27

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area → $W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ → KK/K = K
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ → KK/K= K
Clock frequency	f	1/K	$f = 1/\tau$ = 1/K
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha>1$ for most cases**
Integration (# of Tr)	N	α/K^2	N → α/K^2 **= $1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2$ → $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **= 1, when $\alpha=1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7 P (Power)/Clock → 0.7^3 = 0.34 τ (Switching time) → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5 P (Power)/Clock → 0.5^3 = 0.125 τ (Switching time) → 0.5
Chip N (# of Tr) → $1/0.7^2$ = 2 f (Clock) → 1/0.7 = 1.4 P (Power) → 1	N (# of Tr) → $1/0.5^2$ = 4 f (Clock) → 1/0.5 = 2 P (Power) → 1

Actual past downscaling trend until year 2000



Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	1/K(10^{2})	10^{3}
t_{ox}	K(10^{-2})	10^{-2}						
V_{dd}	K(10^{-2})	10^{-1}	I_d/μm	1	10^{1}	P	α(10^{1})	10^{5}
						= fαNCV²		
A_{chip}	α	10^{1}	N	α/K²(10^{5})	10^{4}			

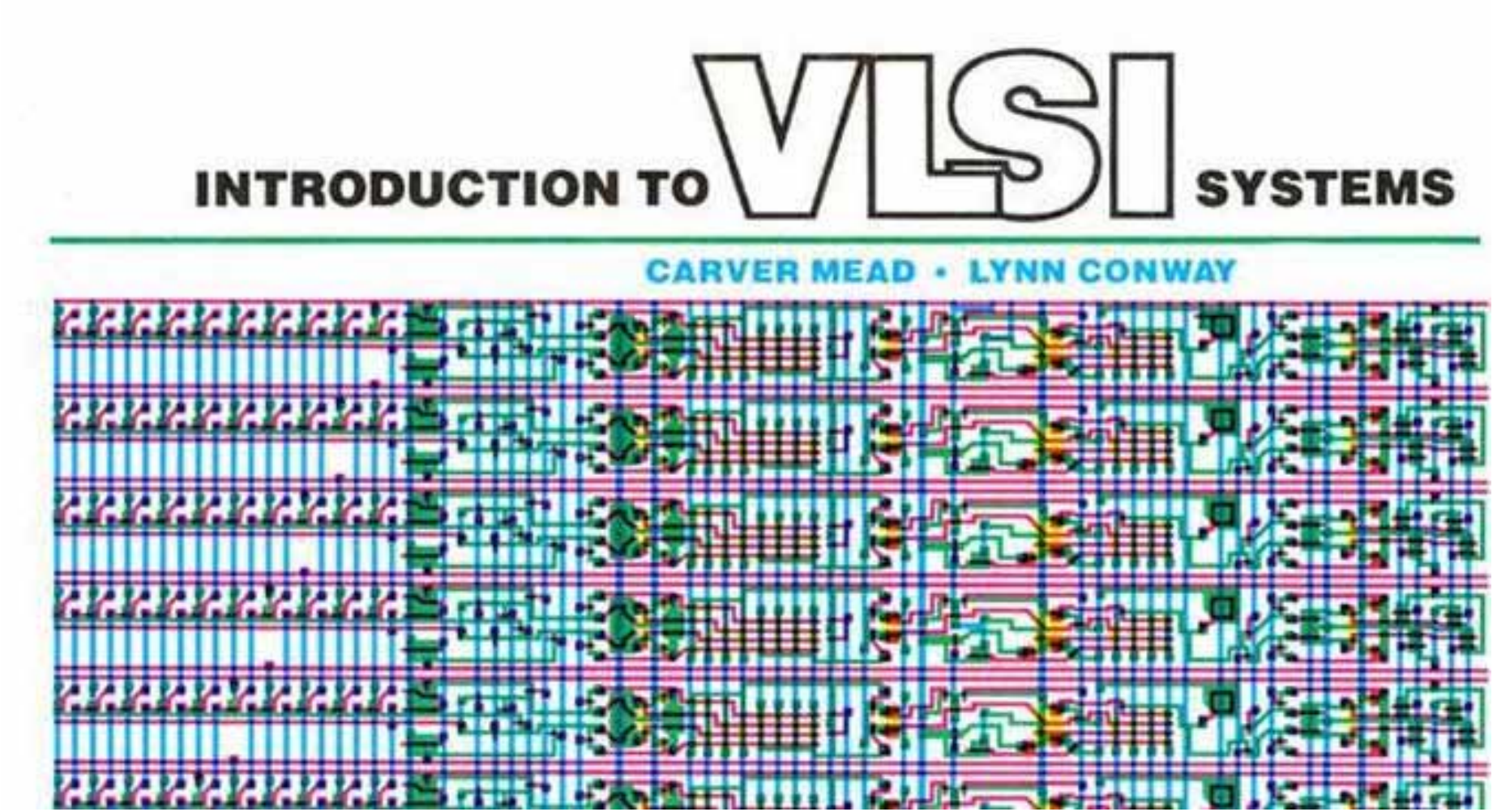
Vd scaling insufficient, α increased → N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

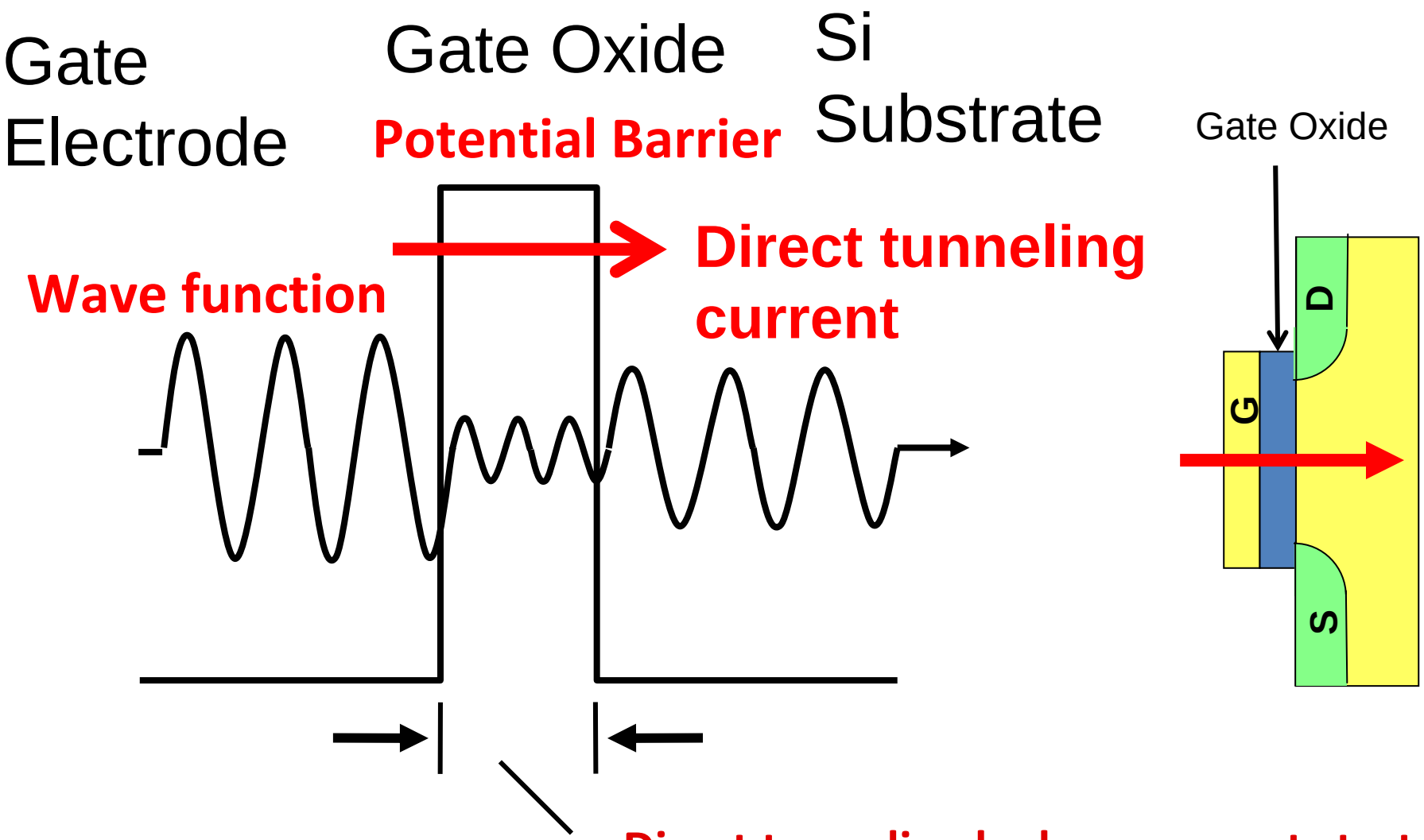


C. Mead L. Conway

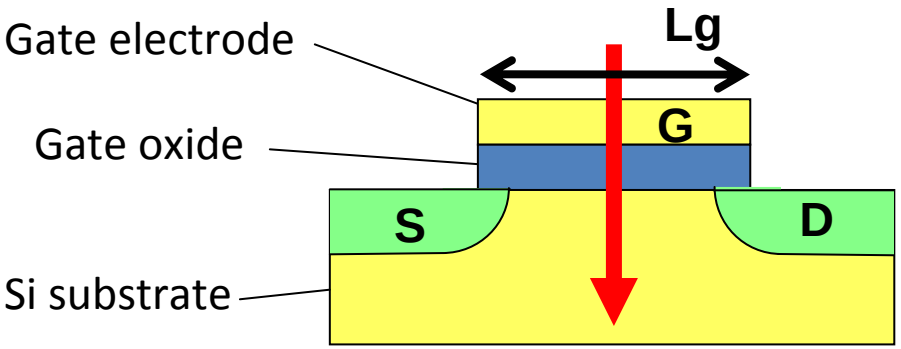
VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



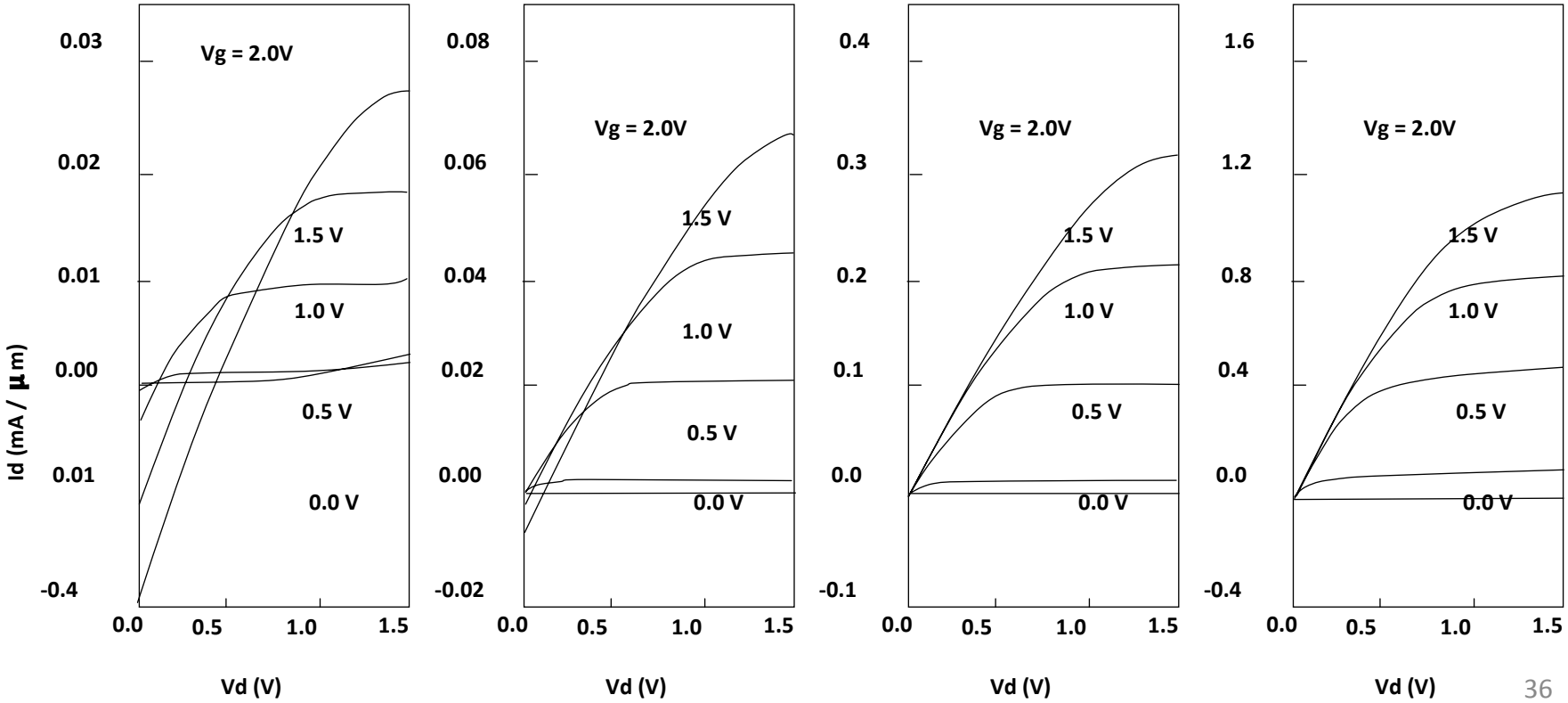
Direct tunneling leakage current start to flow when the thickness is 3 nm.

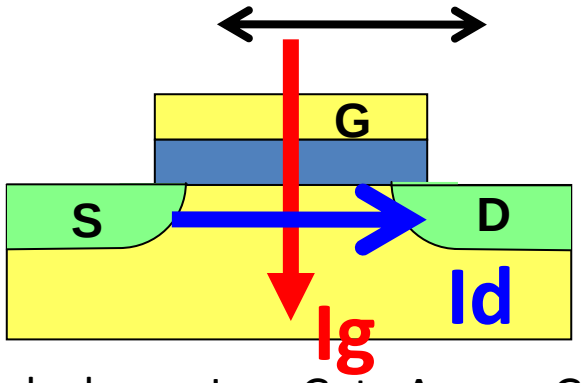


Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

Lg = 10 μm | Lg = 5 μm | Lg = 1.0 μm | Lg = 0.1μm



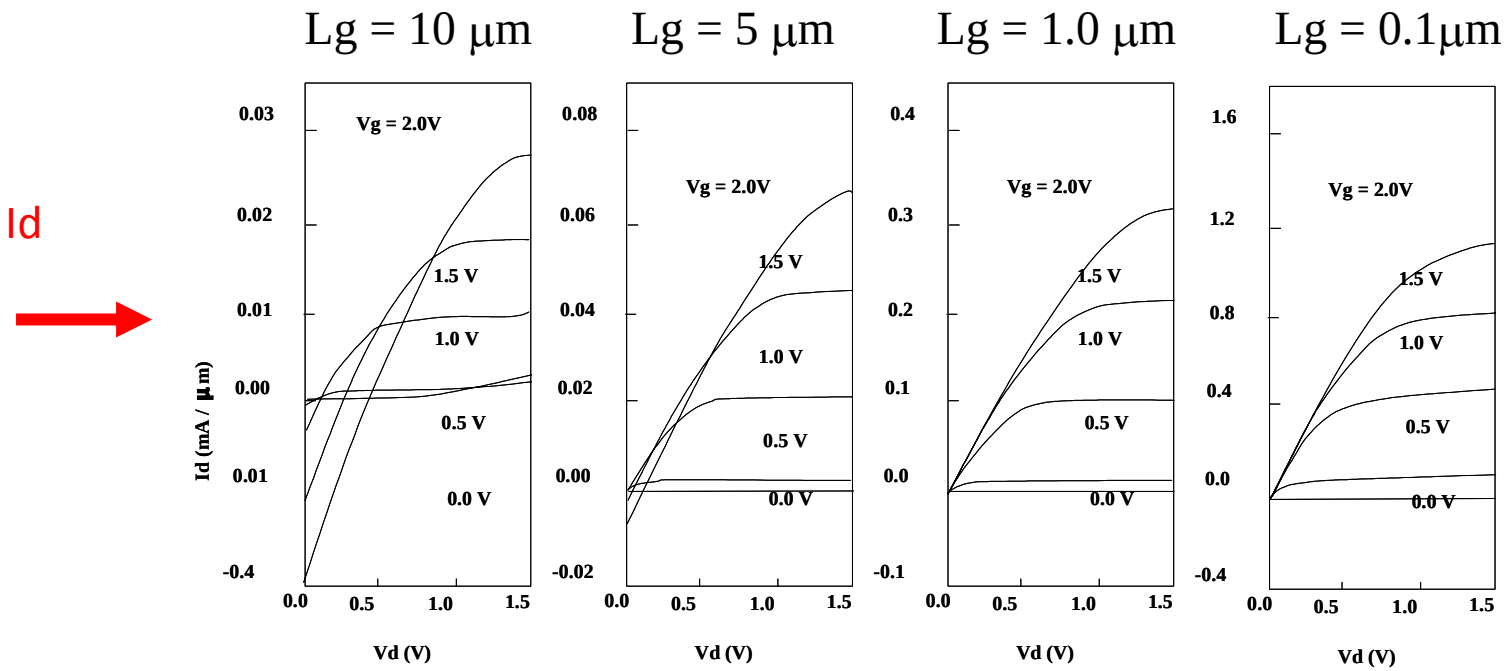


Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

Then, Ig → small, Id → large, Thus, Ig/Id → very small



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

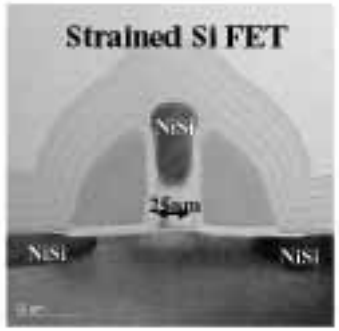
90nm node

Lg=50nm

65nm node

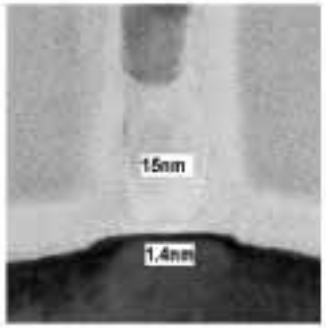
Lg=35nm

45nm node



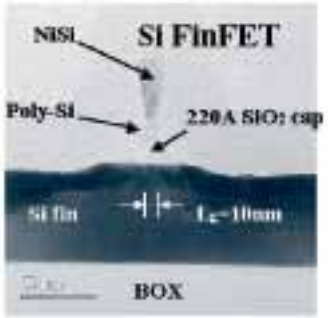
Lg=25nm

32nm node

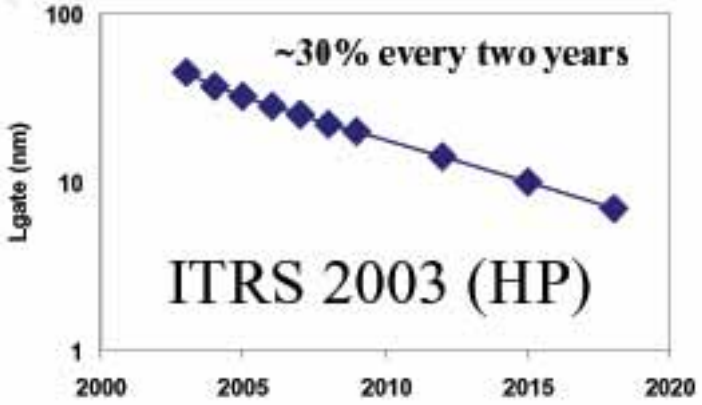


Lg=15nm

22nm node



Lg=10nm

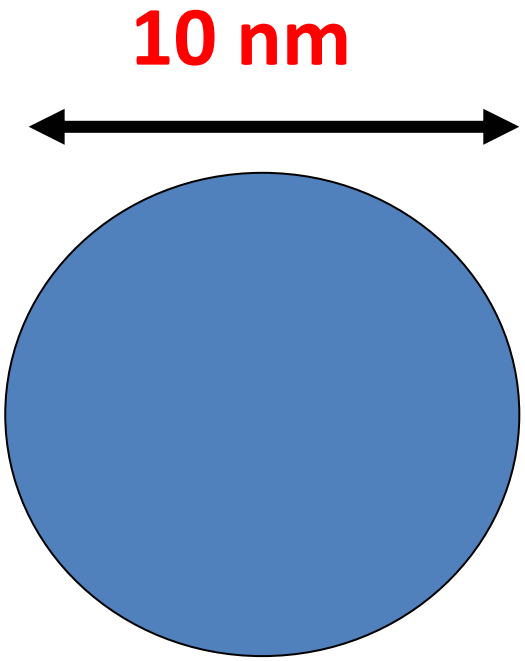


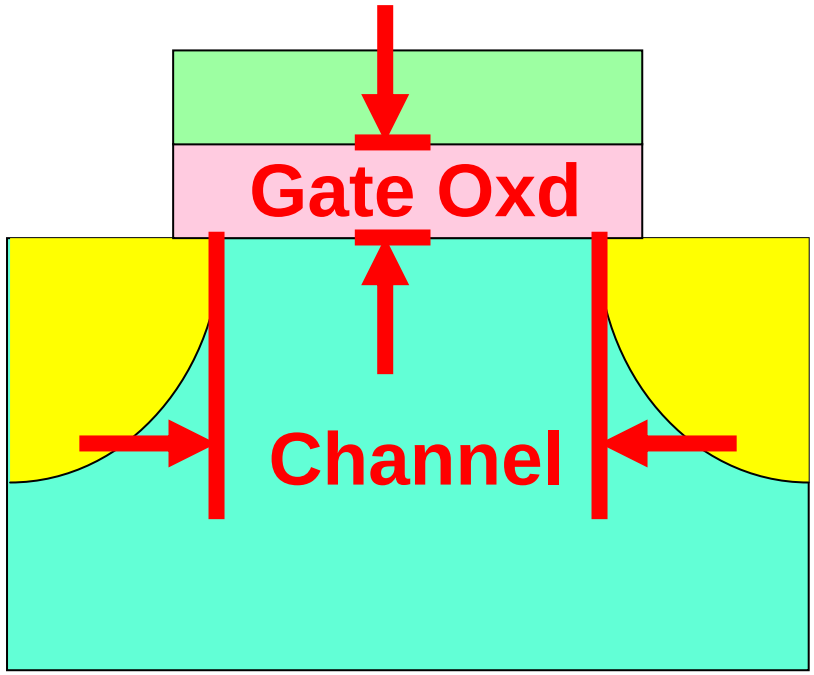
Qi Xinag, ECS 2004, AMD

Downsizing limit?

Channel length?

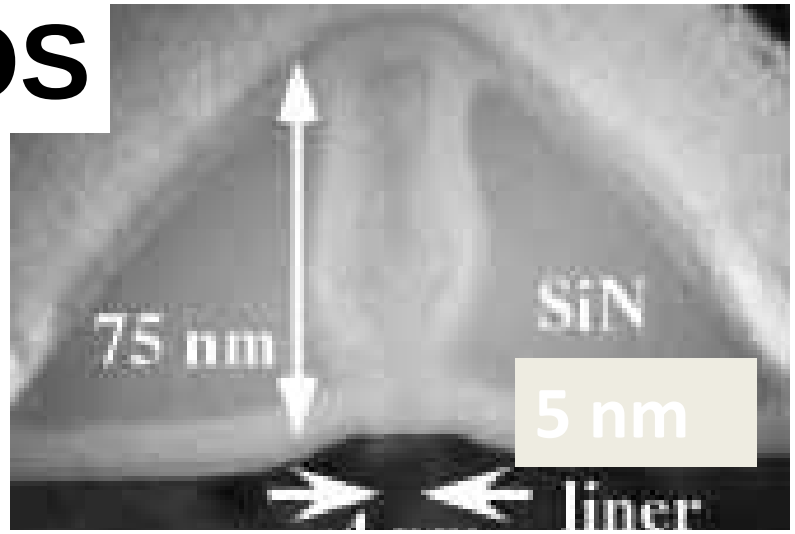
Electron wave length



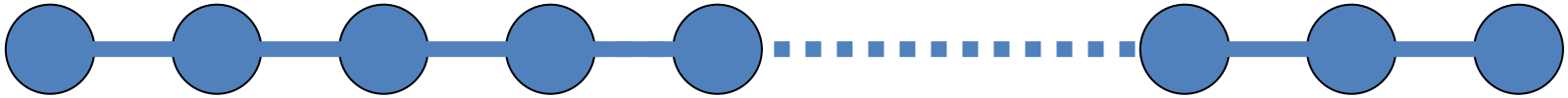


5 nm gate length CMOS

Is a Real Nano Device!!

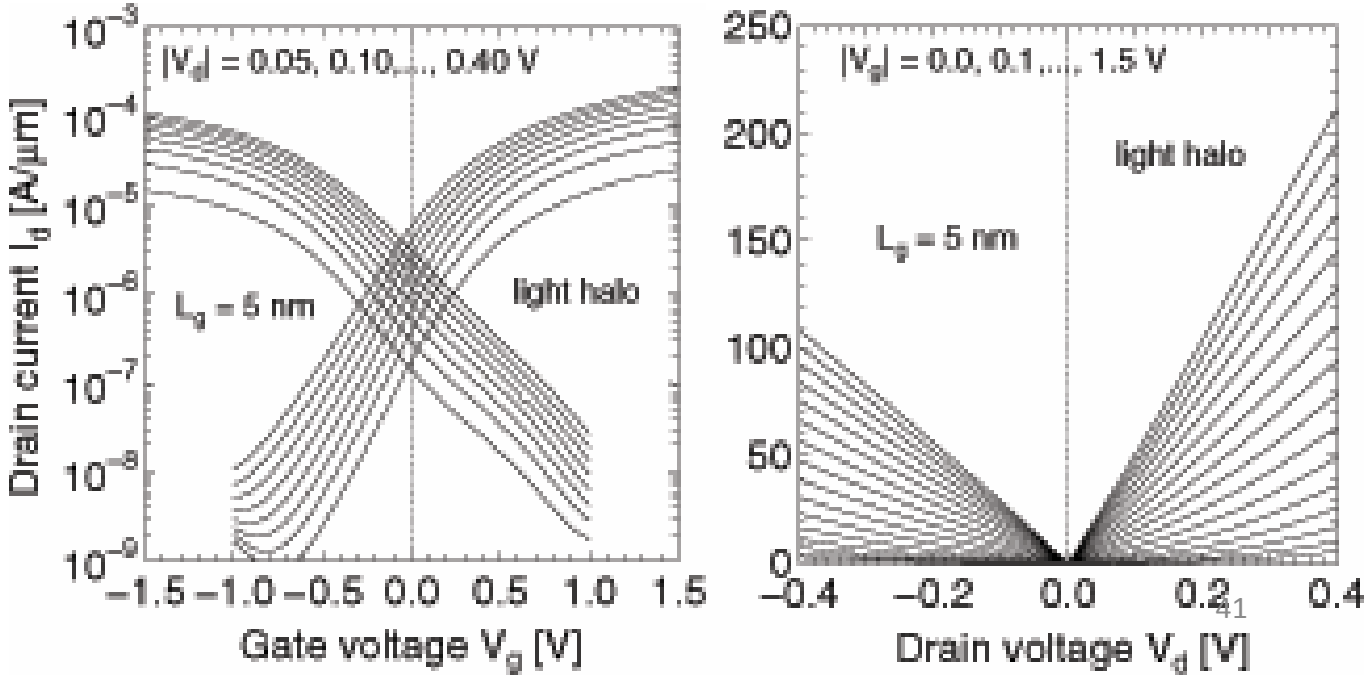


Length of 18 Si atoms



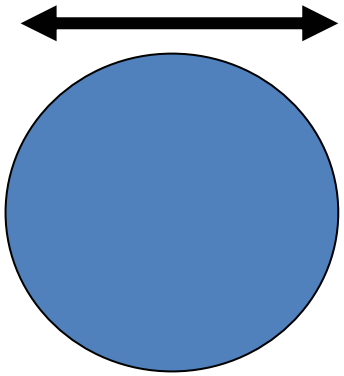
H. Wakabayashi
et.al, NEC

IEDM, 2003



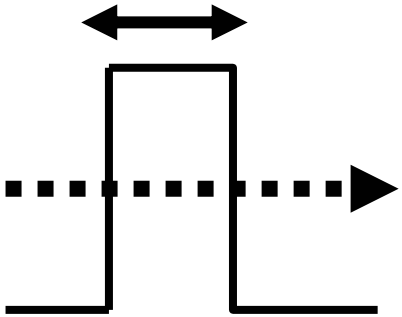
Electron wave length

10 nm



Tunneling distance

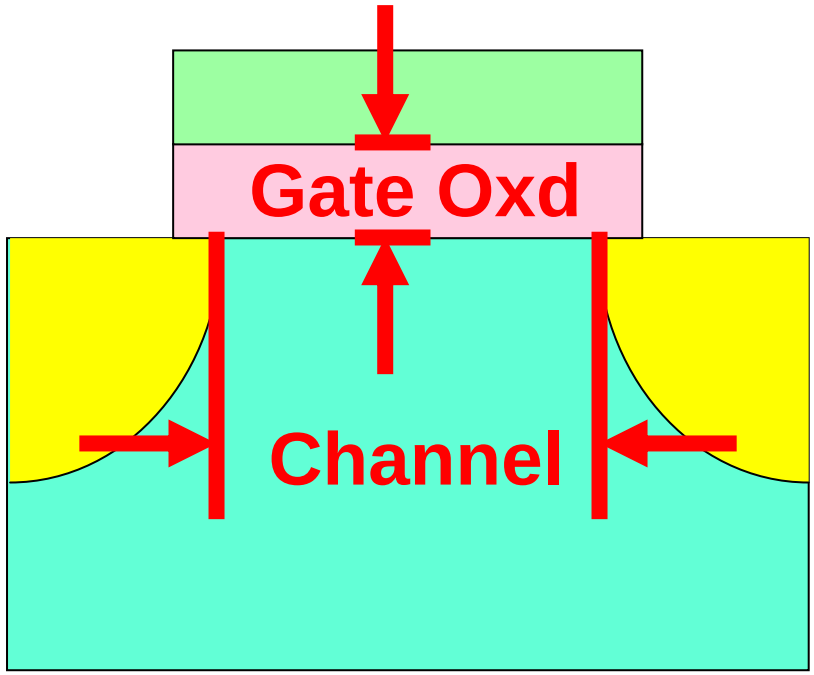
3 nm



Downsizing limit!

Channel length

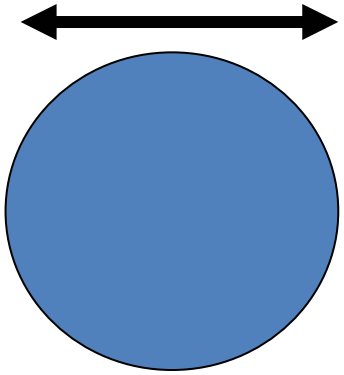
Gate oxide thickness



Prediction now!

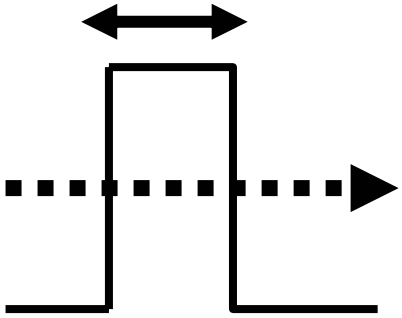
Electron wave length

10 nm



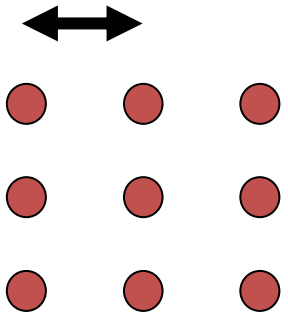
Tunneling distance

3 nm



Atom distance

0.3 nm

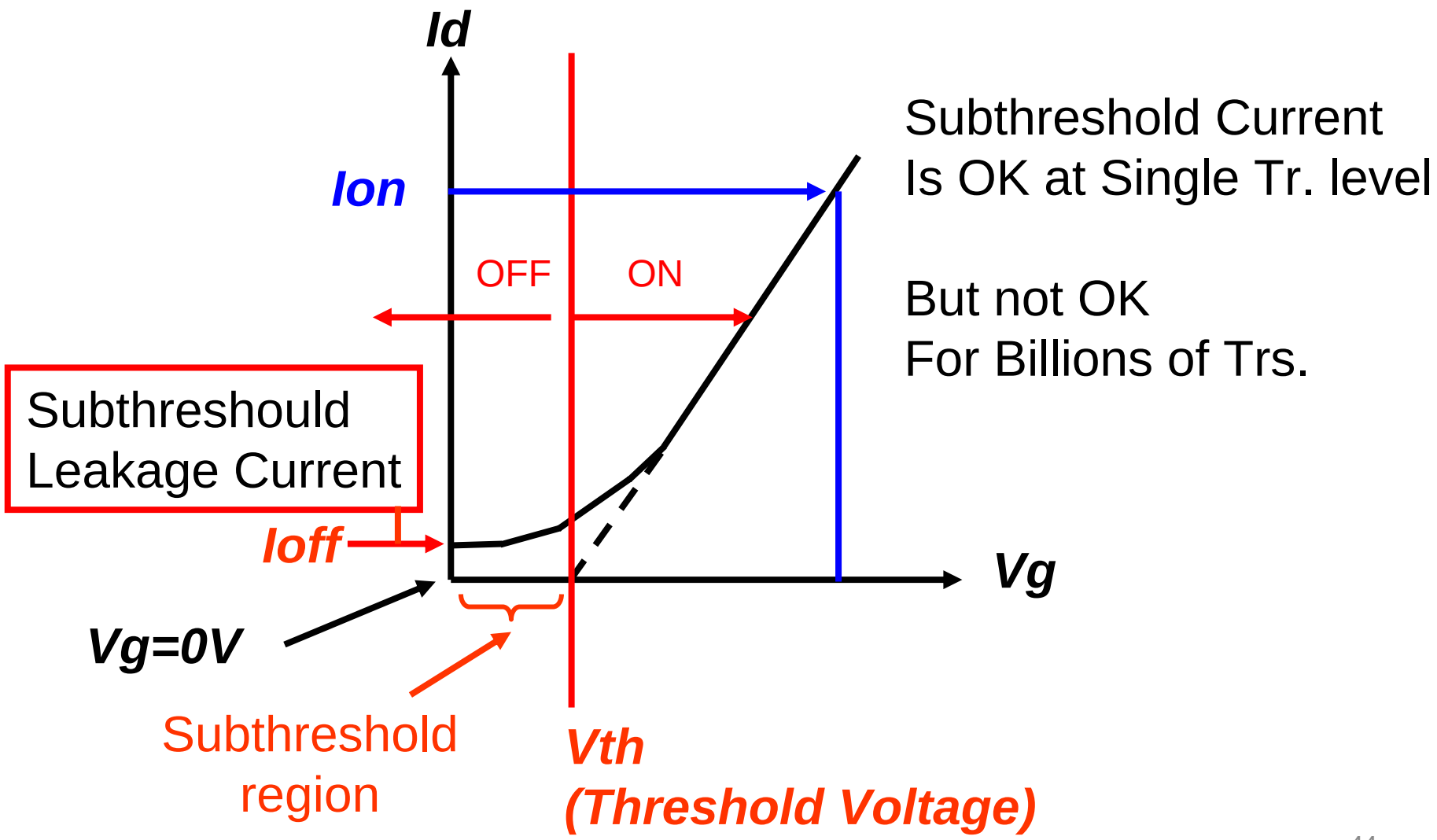


MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Subtheshold leakage current of MOSFET



Subthreshold Current
Is OK at Single Tr. level

But not OK
For Billions of Trs.

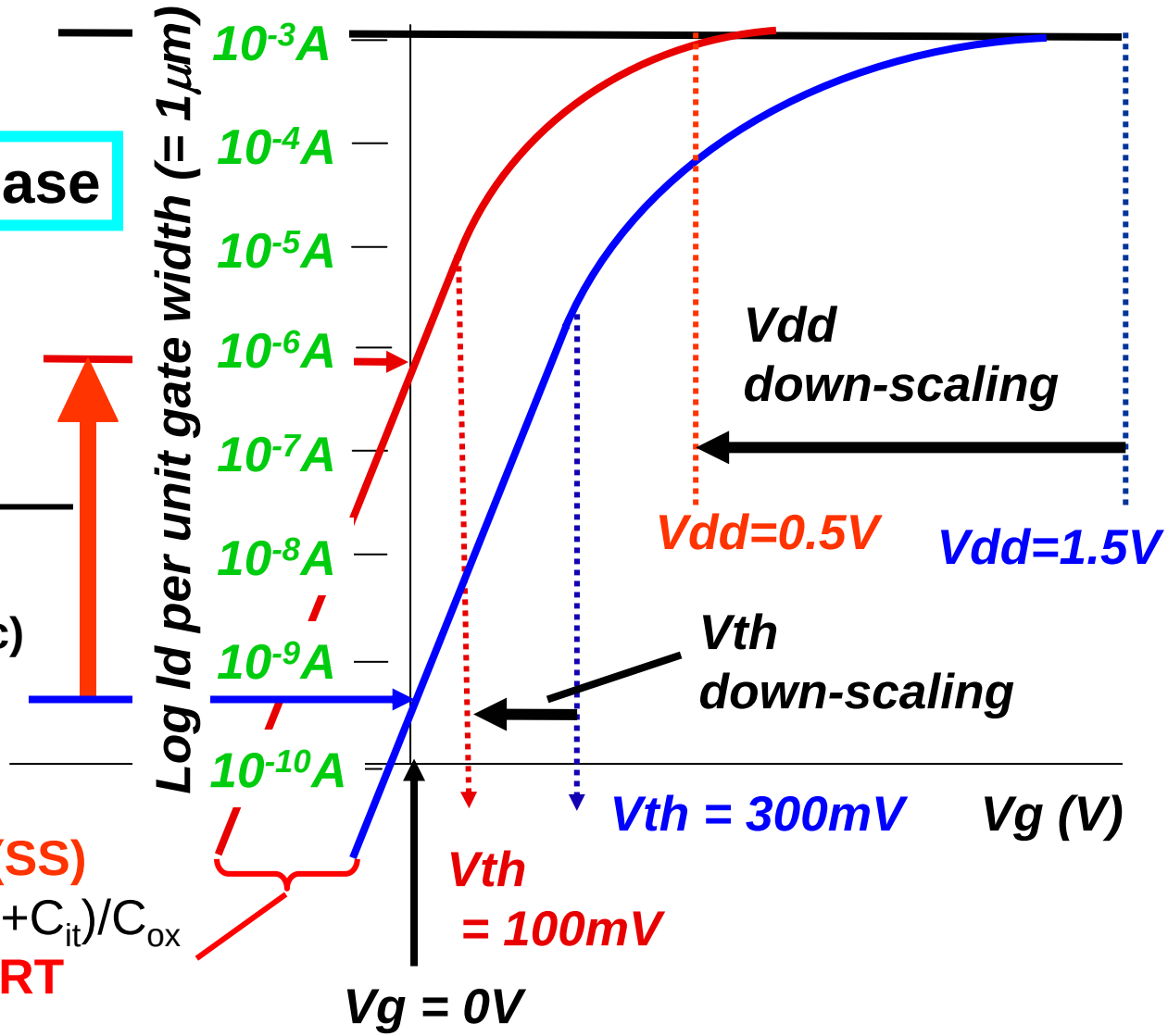
44

Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV
Ioff increases with 3.3 decades

(300 – 100)mV/(60mv/dec) = 3.3 dec



Subthreshold slope (SS)
= $(Ln10)(kT/q)(C_{ox}+C_D+C_{it})/C_{ox}$
> **~ 60 mV/decade at RT**

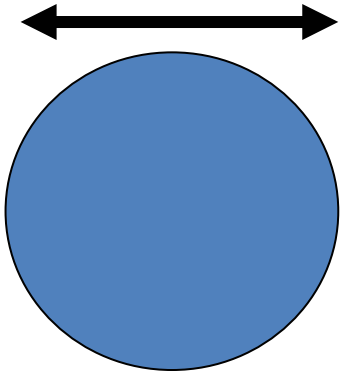
SS value:
Constant and does not become small with down-scaling

45

Prediction now!

Electron wave length

10 nm

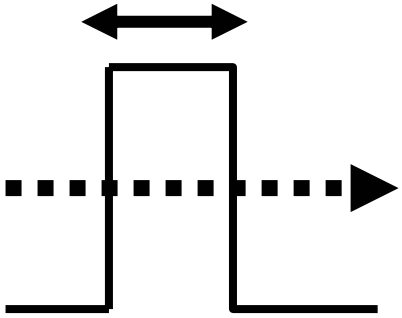


Practical limit for integration

Lg = 5 nm?

Tunneling distance

3 nm

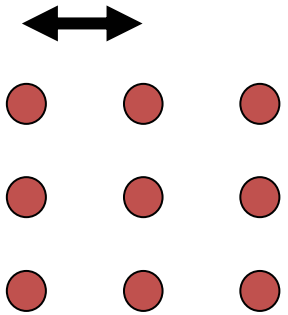


MOSFET operation

Lg = 2 ~ 1.5 nm?

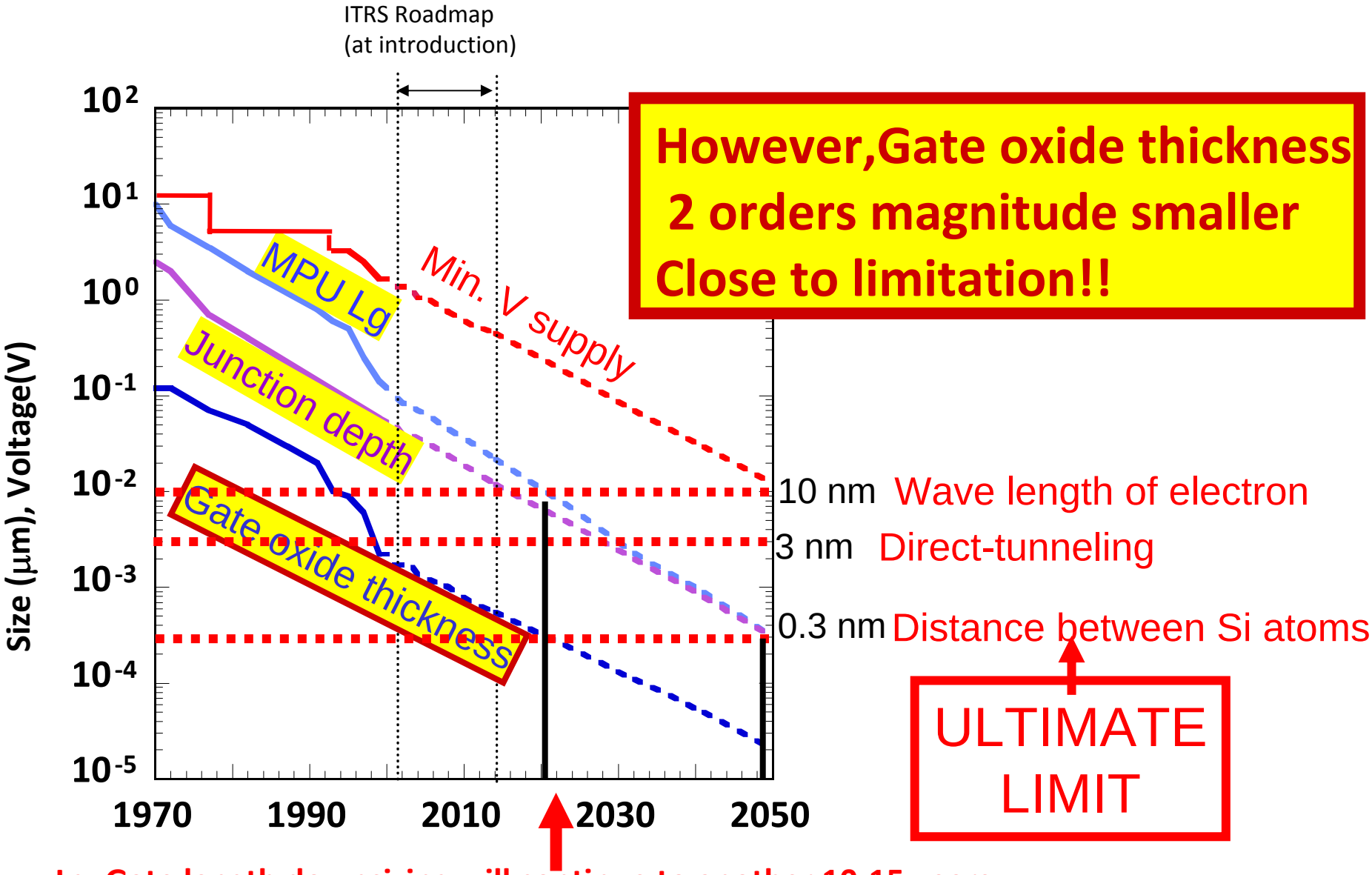
Atom distance

0.3 nm



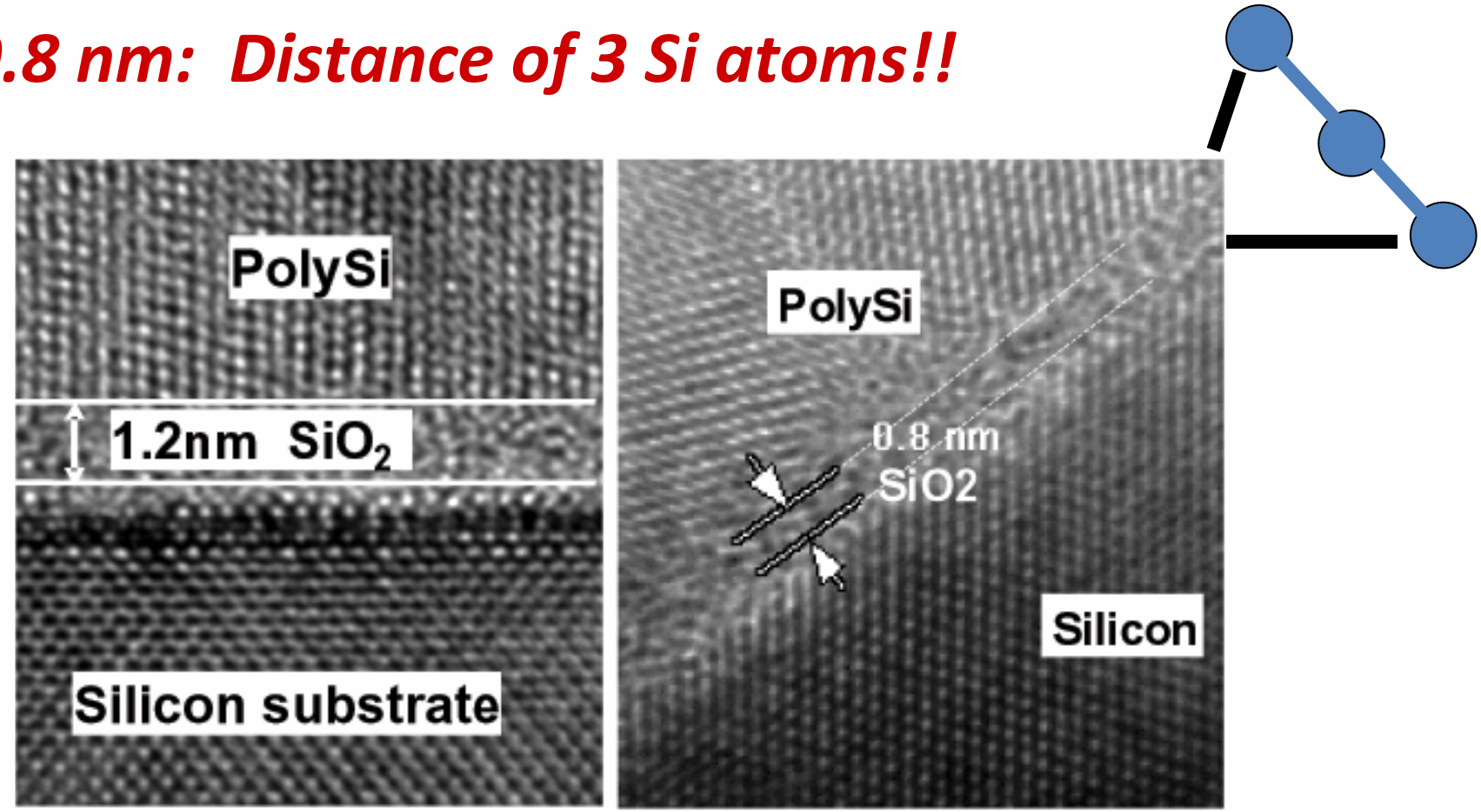
Below this, no one knows future!

Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

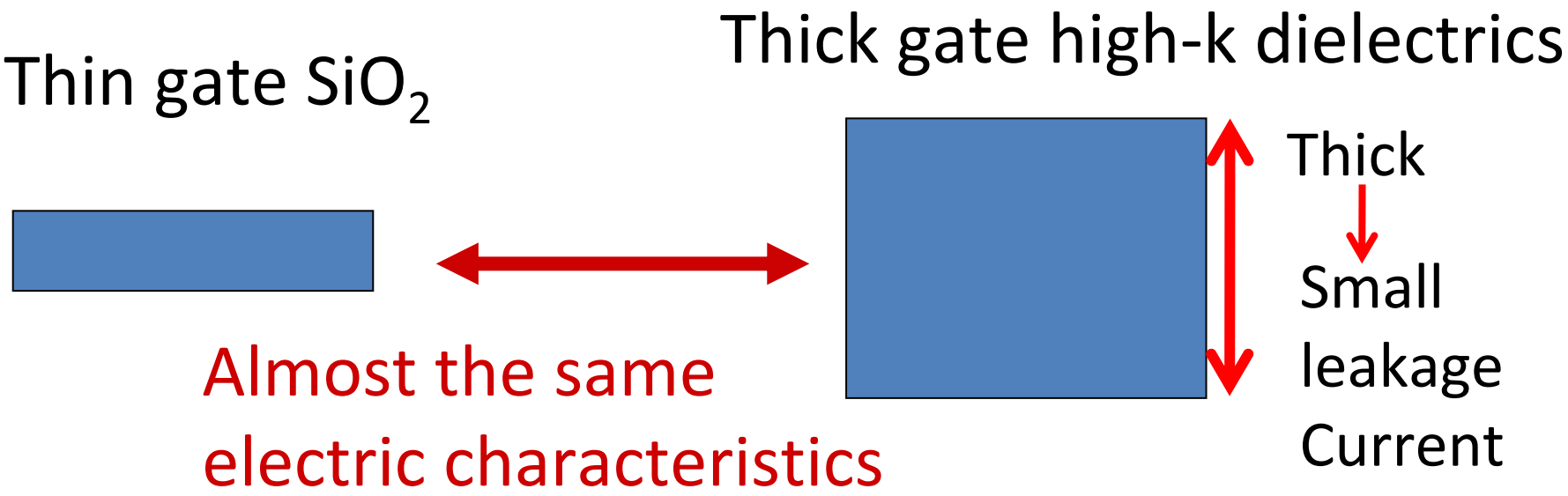
By Robert Chau, IWGI 2003

So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constant

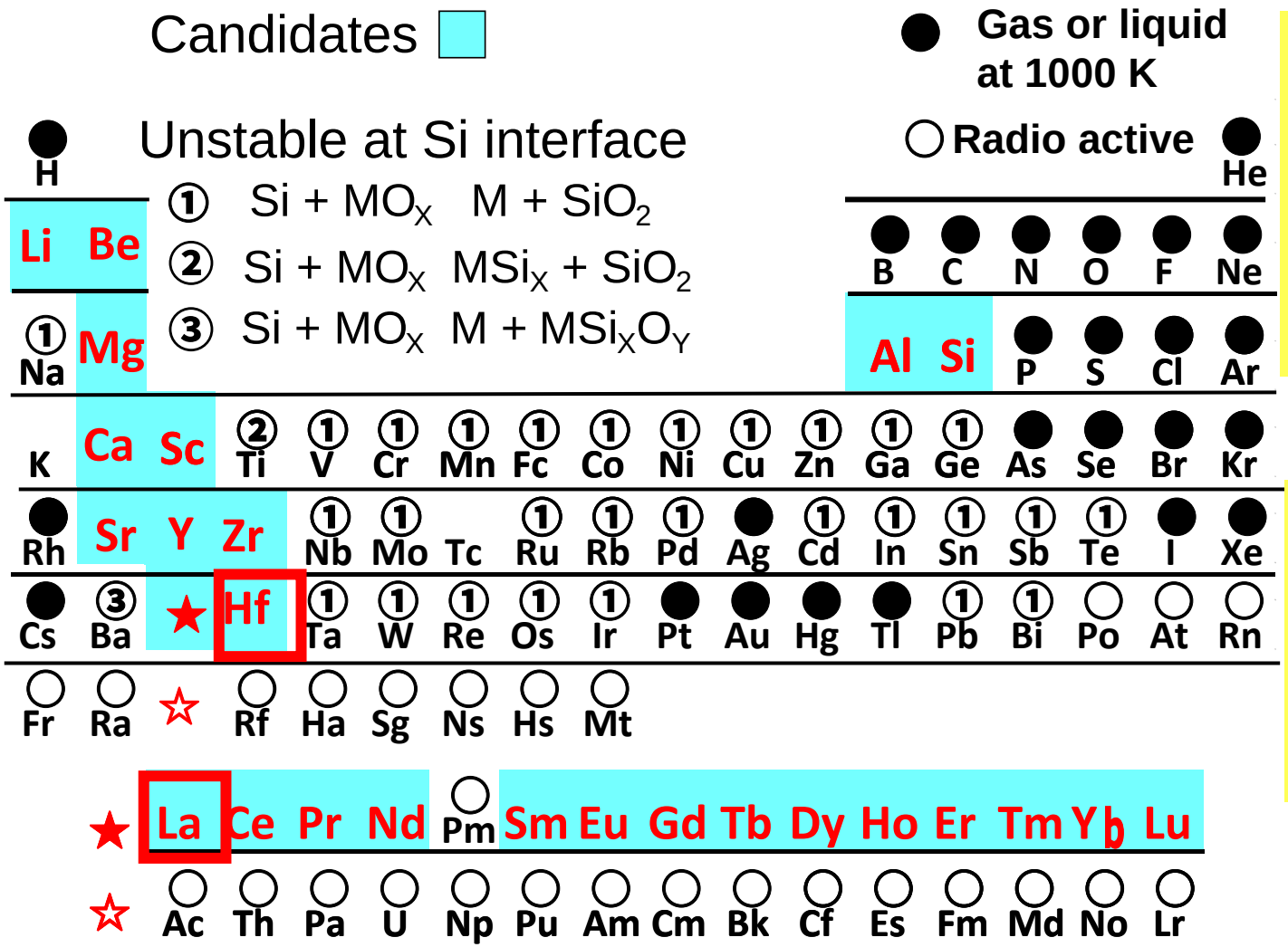
To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide

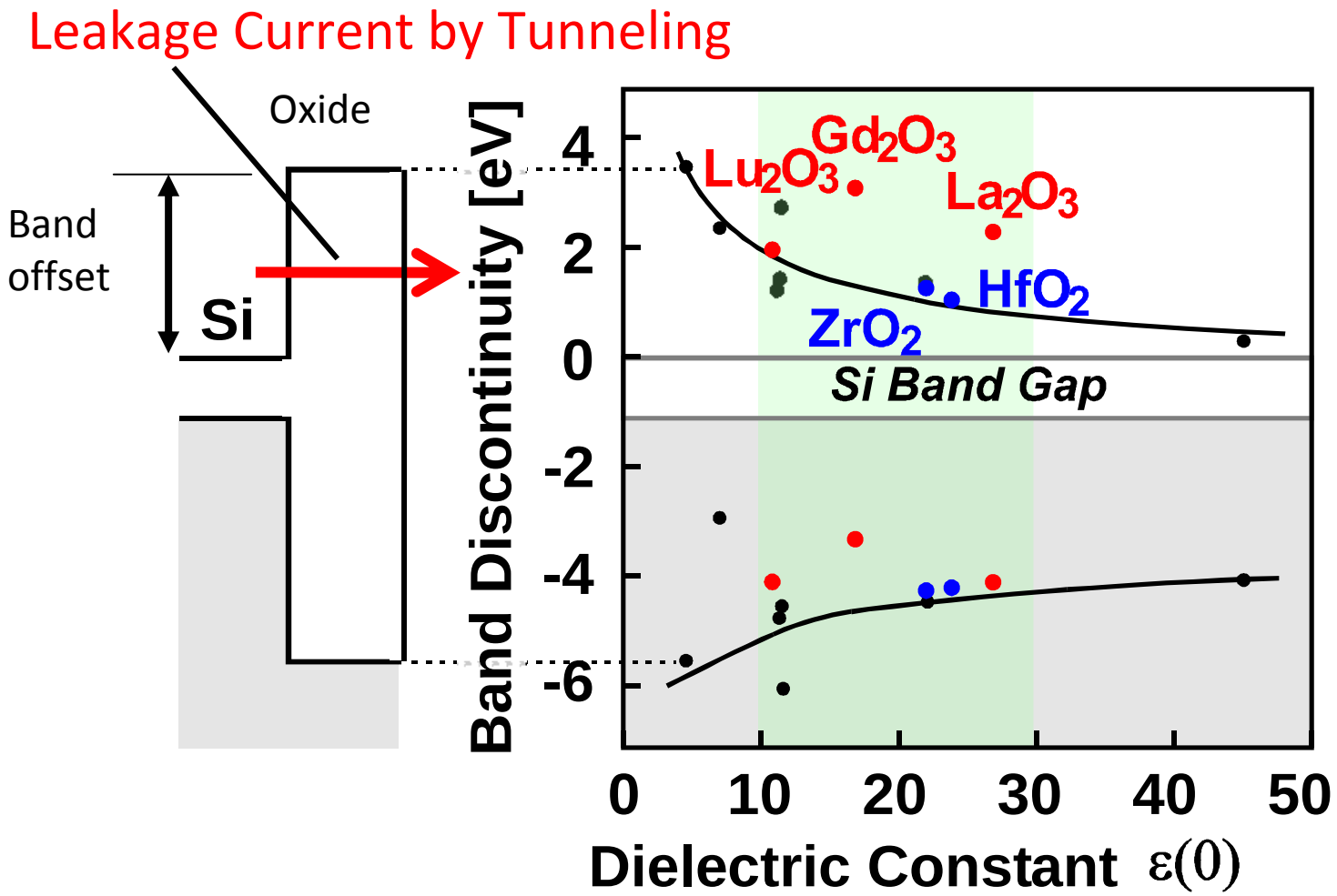


HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

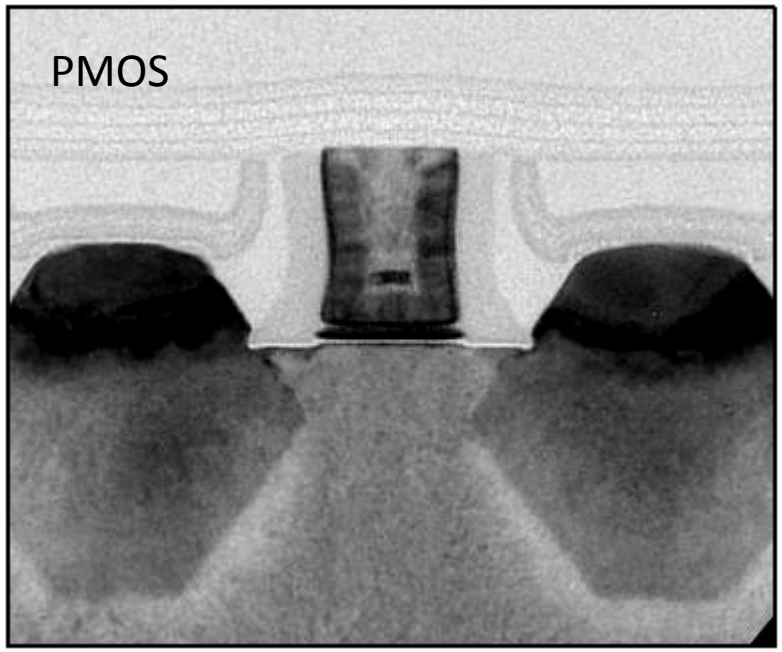
Conduction band offset vs. Dielectric Constant

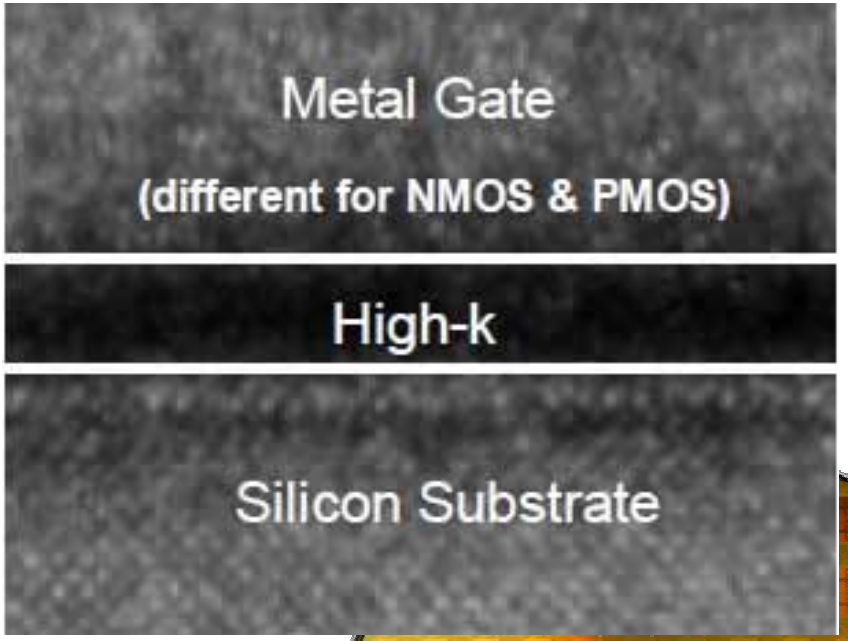


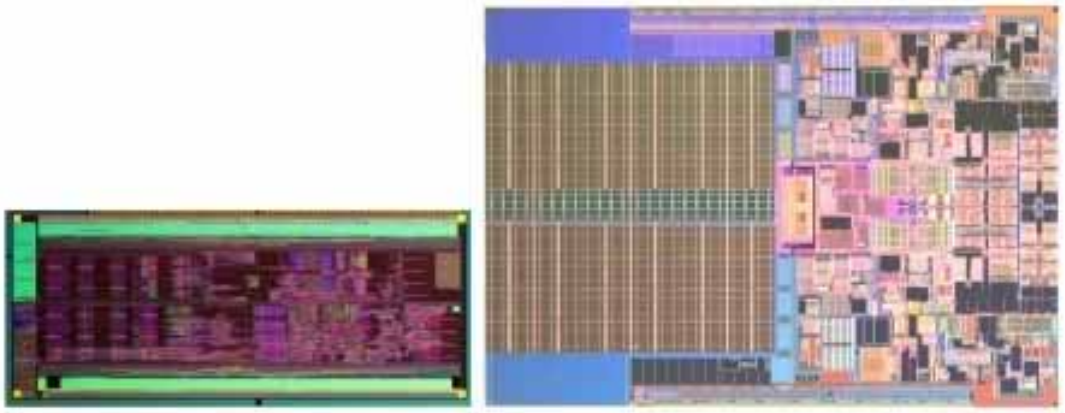
XPS measurement by Prof. T. Hattori, INFOS 2003

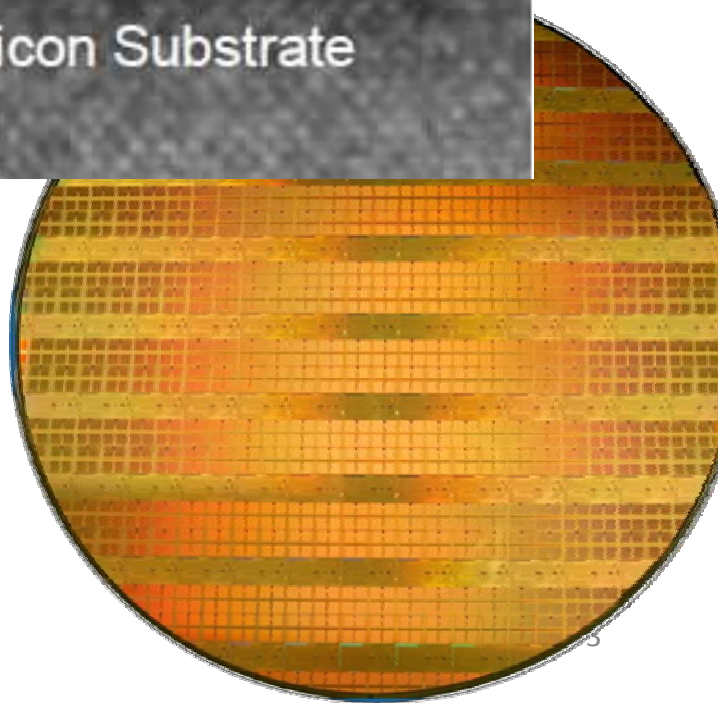
High-k gate insulator MOSFETs for Intel: EOT=1nm

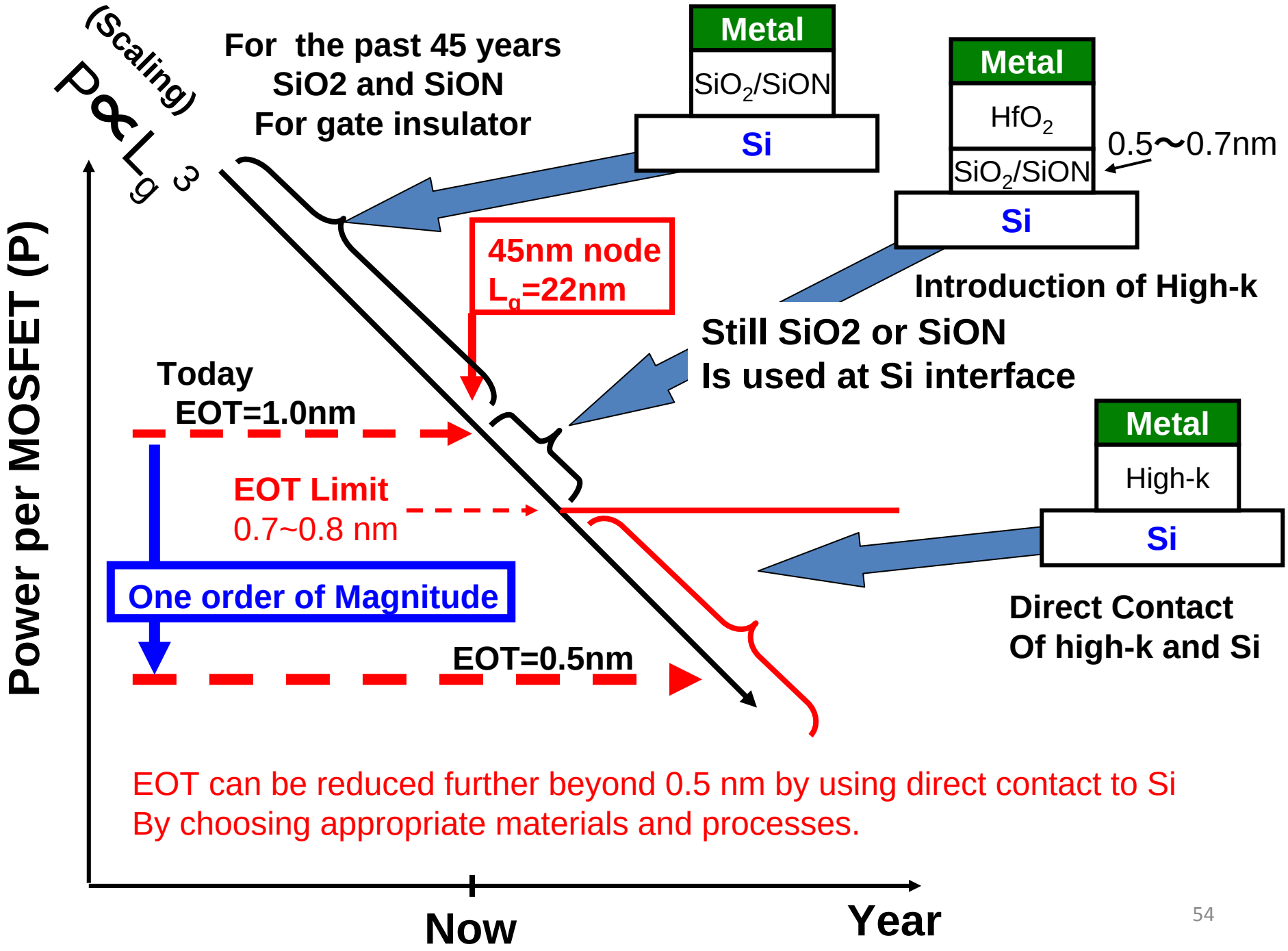
EOT: Equivalent Oxide Thickness





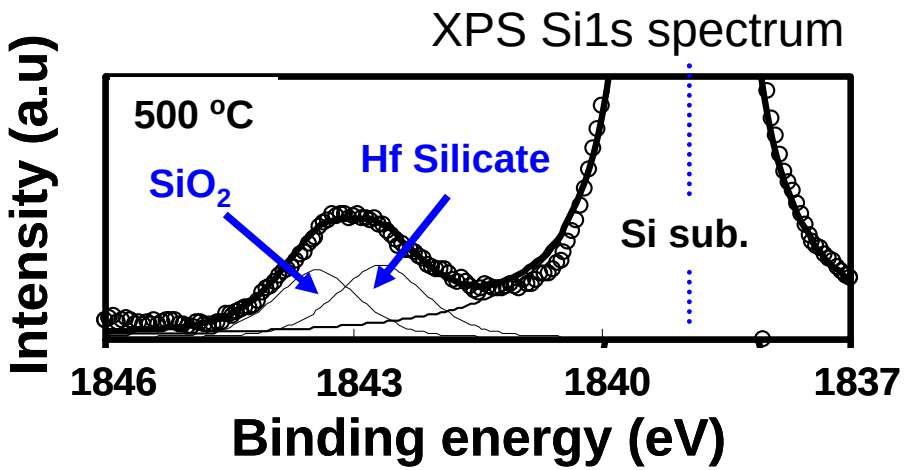


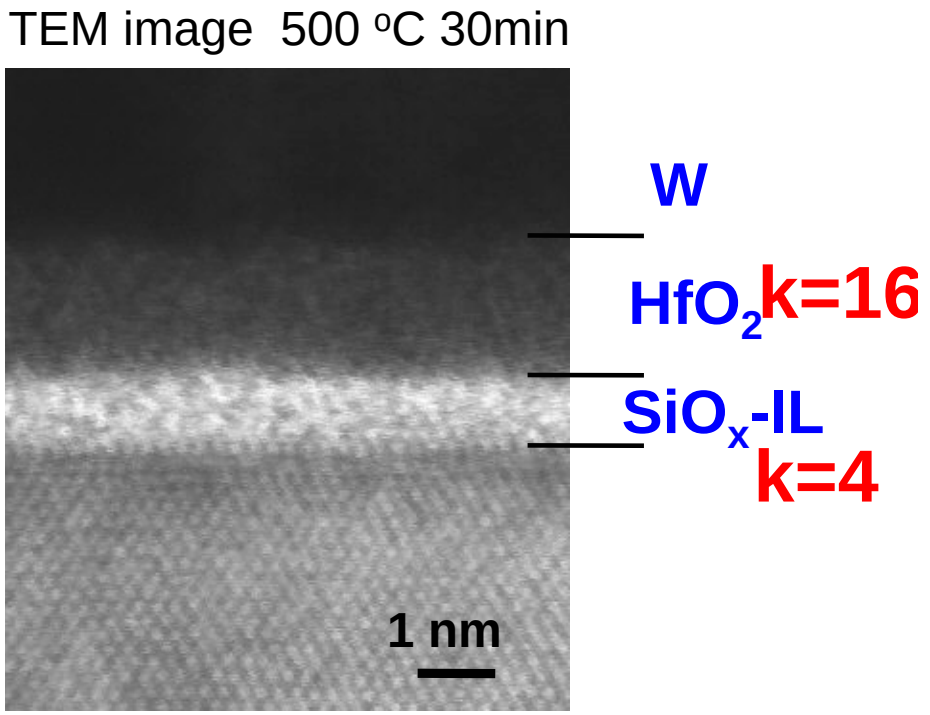




EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

SiO_x-IL growth at HfO_2/Si Interface





Phase separator

$$HfO_2 + Si + O_2 \rightarrow HfO_2 + Si + 2O^* \rightarrow HfO_2 + SiO_2$$

H. Shimizu, JJAP, 44, pp. 6131

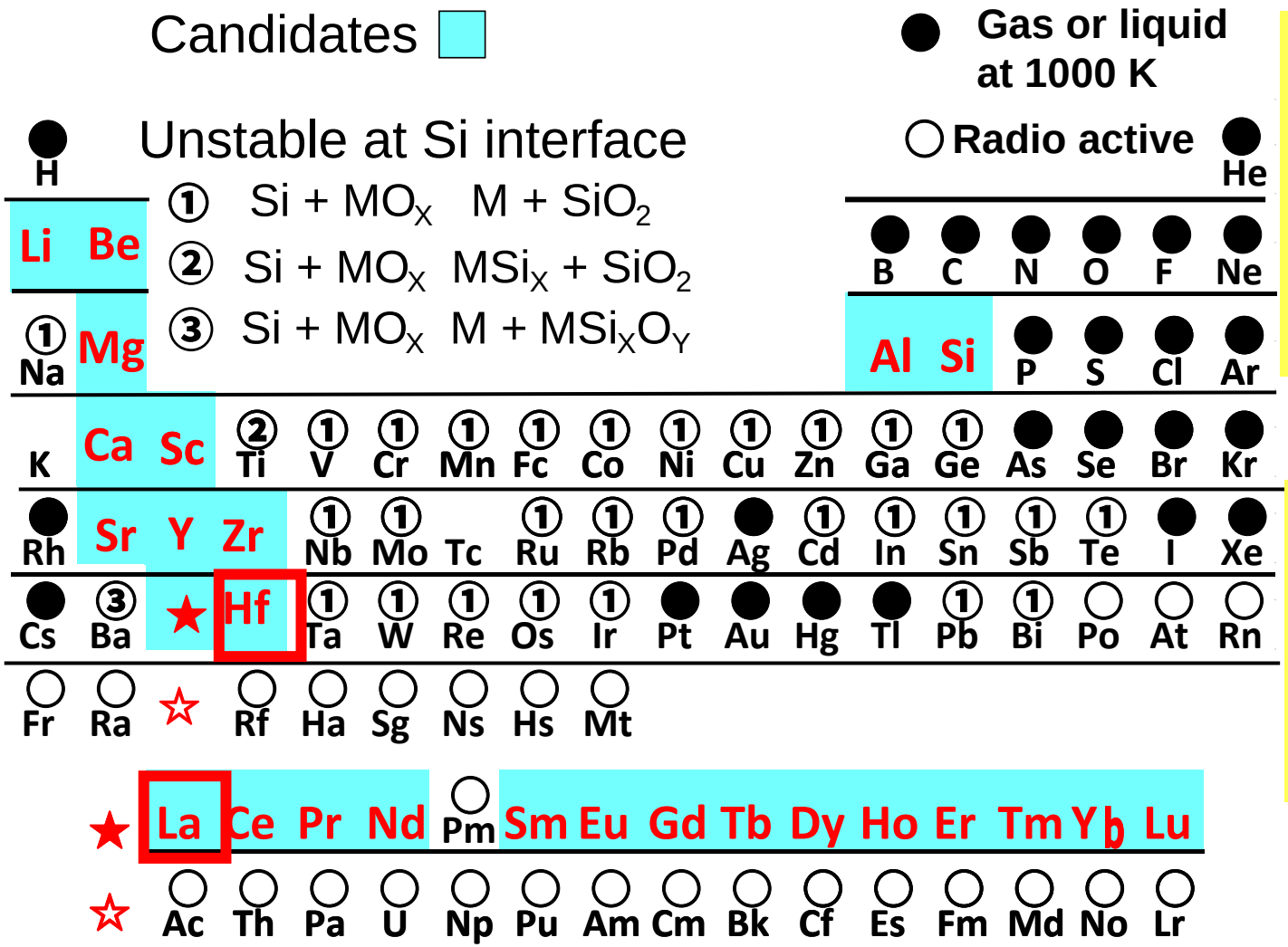
Oxygen supplied from W gate electrode

D.J.Lichtenwalner, Tans. ECS 11, 319

SiO_x-IL is formed after annealing

Oxygen control is required for optimizing the reaction

Choice of High-k elements for oxide



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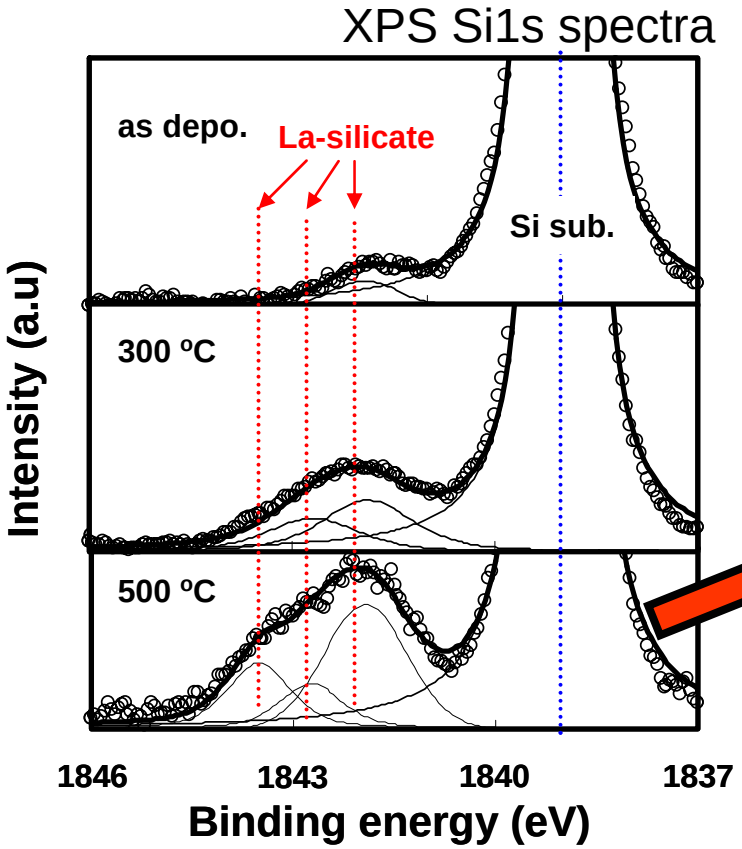
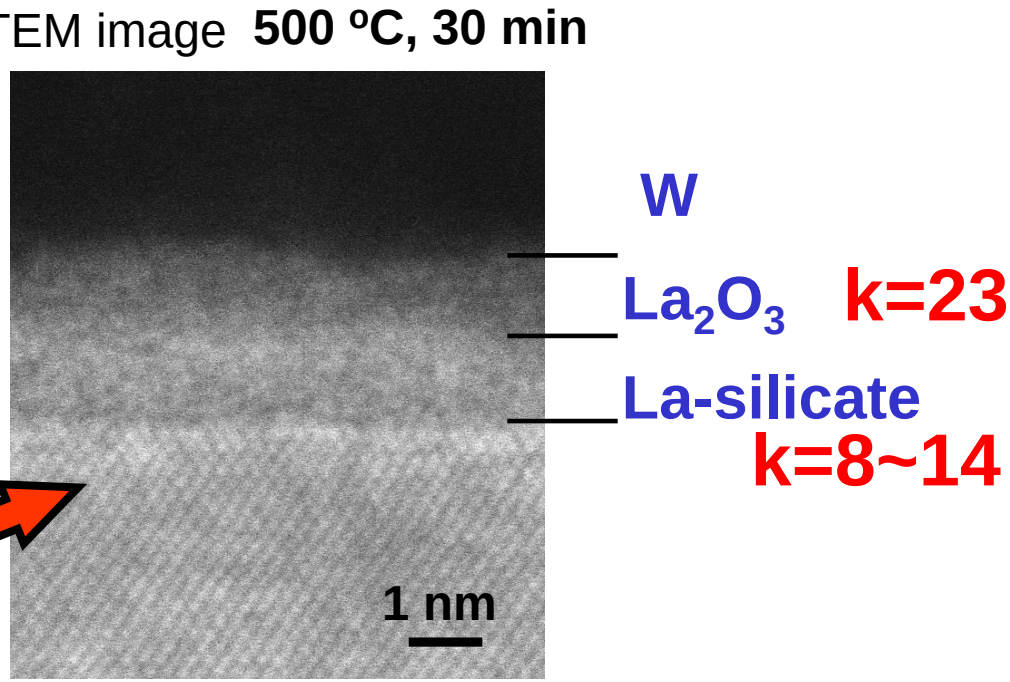
R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

La-Silicate Reaction at La_2O_3/Si

Direct contact high-k/Si is possible

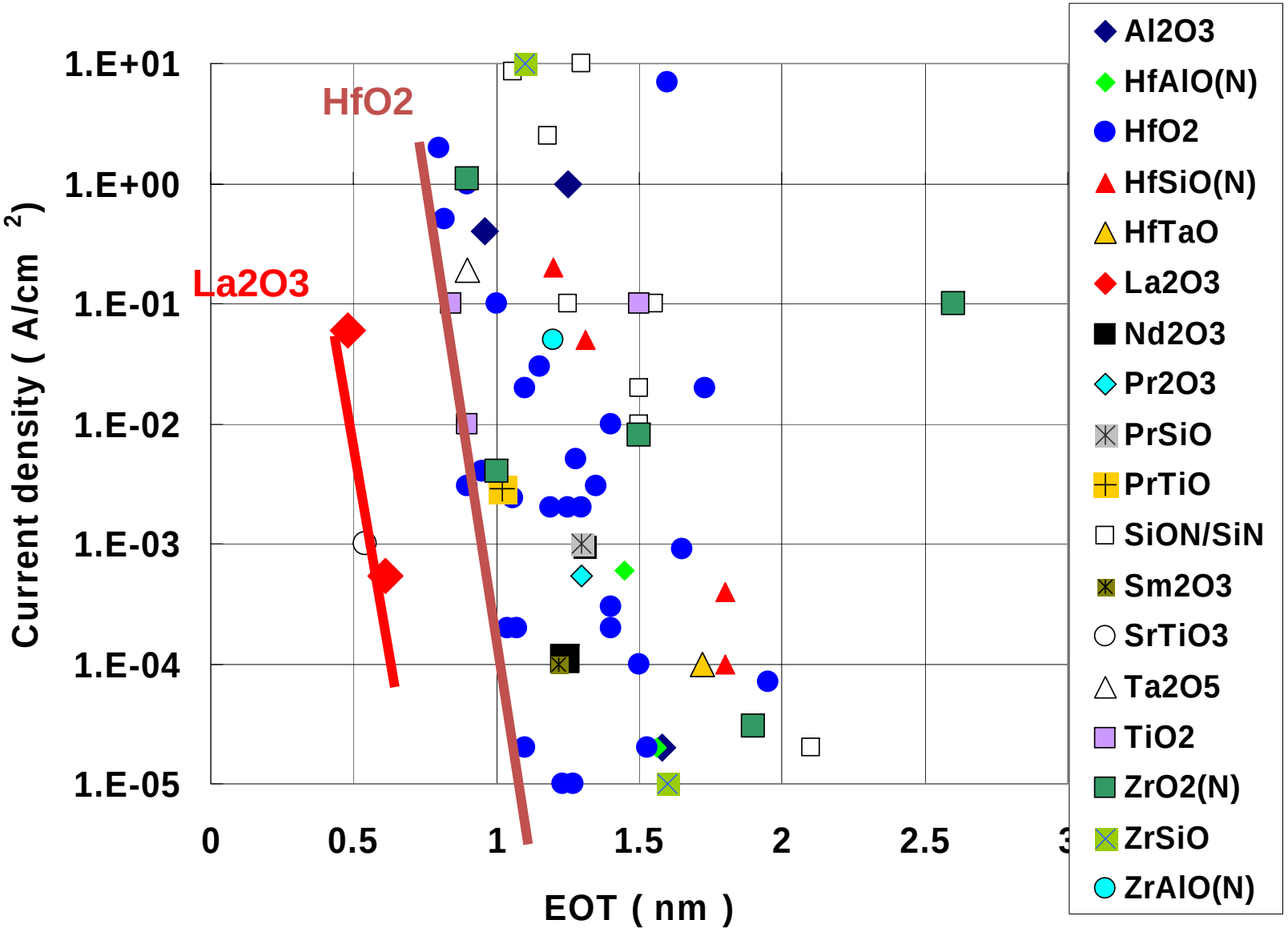




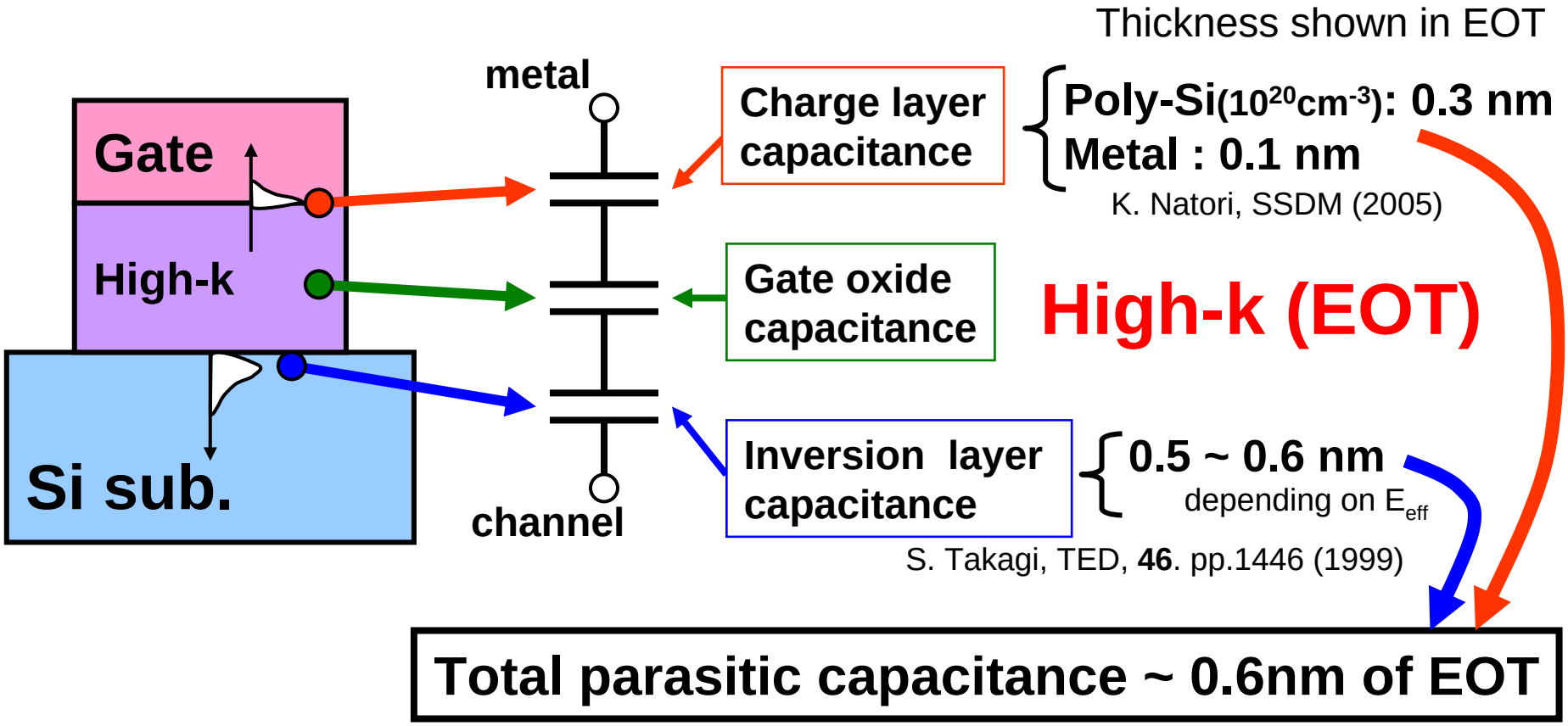
$La_2O_3 + Si + nO_2$
→ La_2SiO_5, $La_2Si_2O_7$,
$La_{9.33}Si_6O_{26}$, $La_{10}(SiO_4)_6O_3$, etc.

La_2O_3 can achieve direct contact of high-k/Si

Gate Leakage vs EOT, (Vg=|1|V)



Quantum Effect in Gate Stack

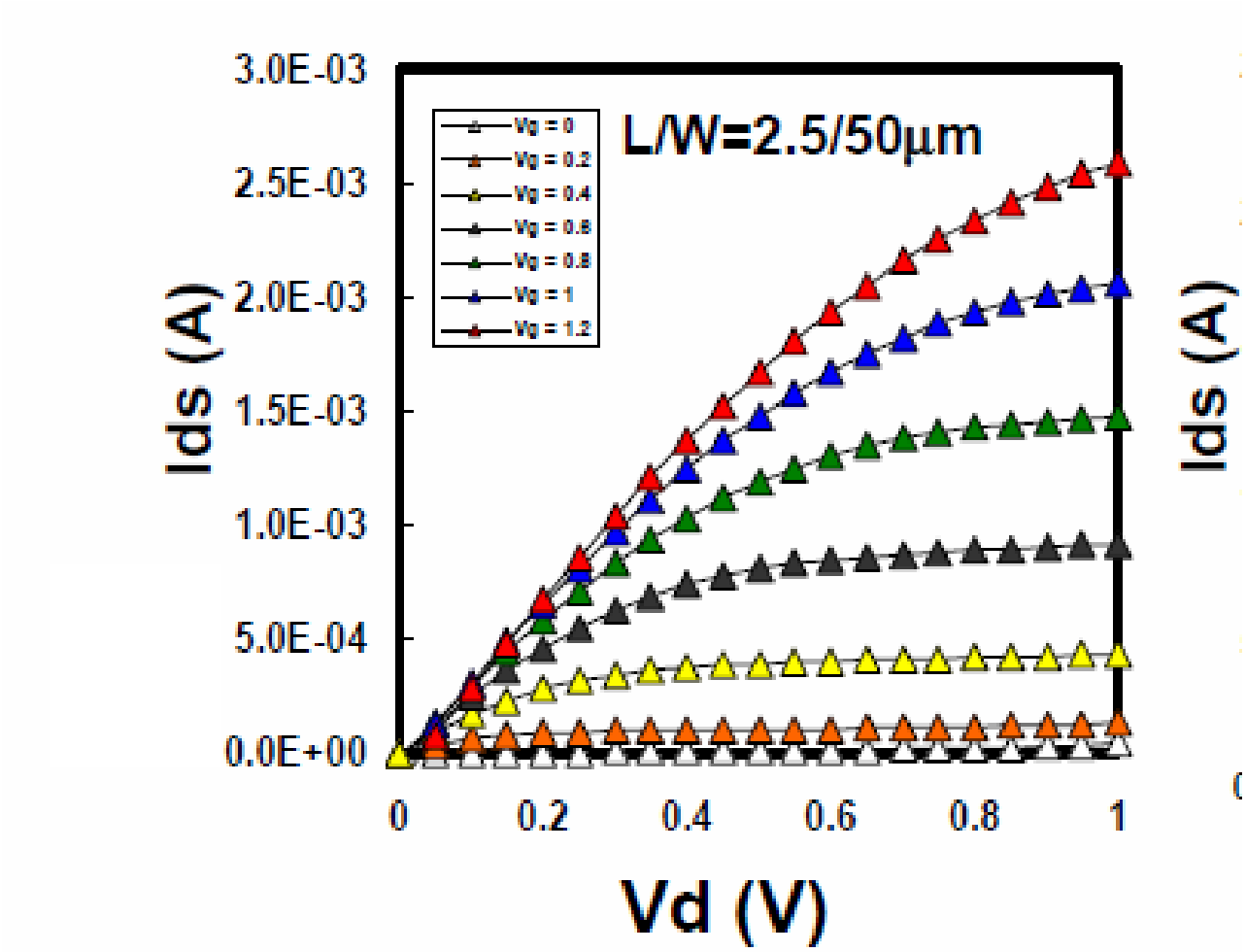


- **A question if the performance improvement can be obtained with EOT<0.5nm**
- **Is EOT<0.5nm achievable?**

EOT = 0.48 nm

Our results

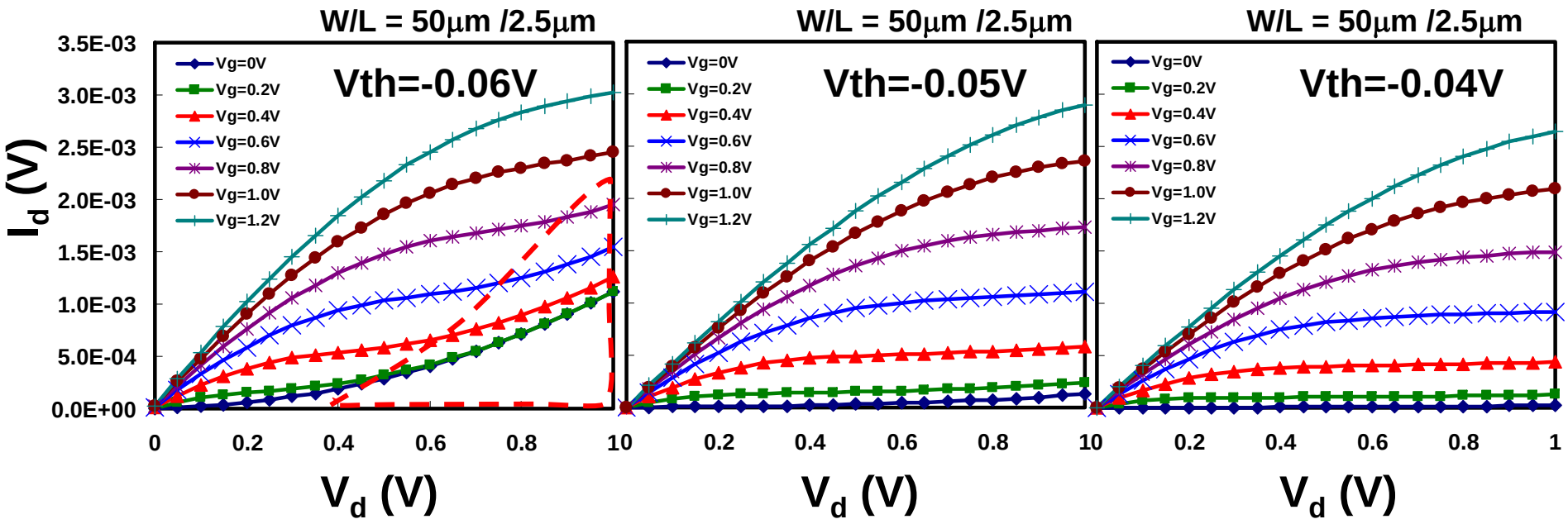
Transistor with La2O3 gate insulator



EOT=0.37nm

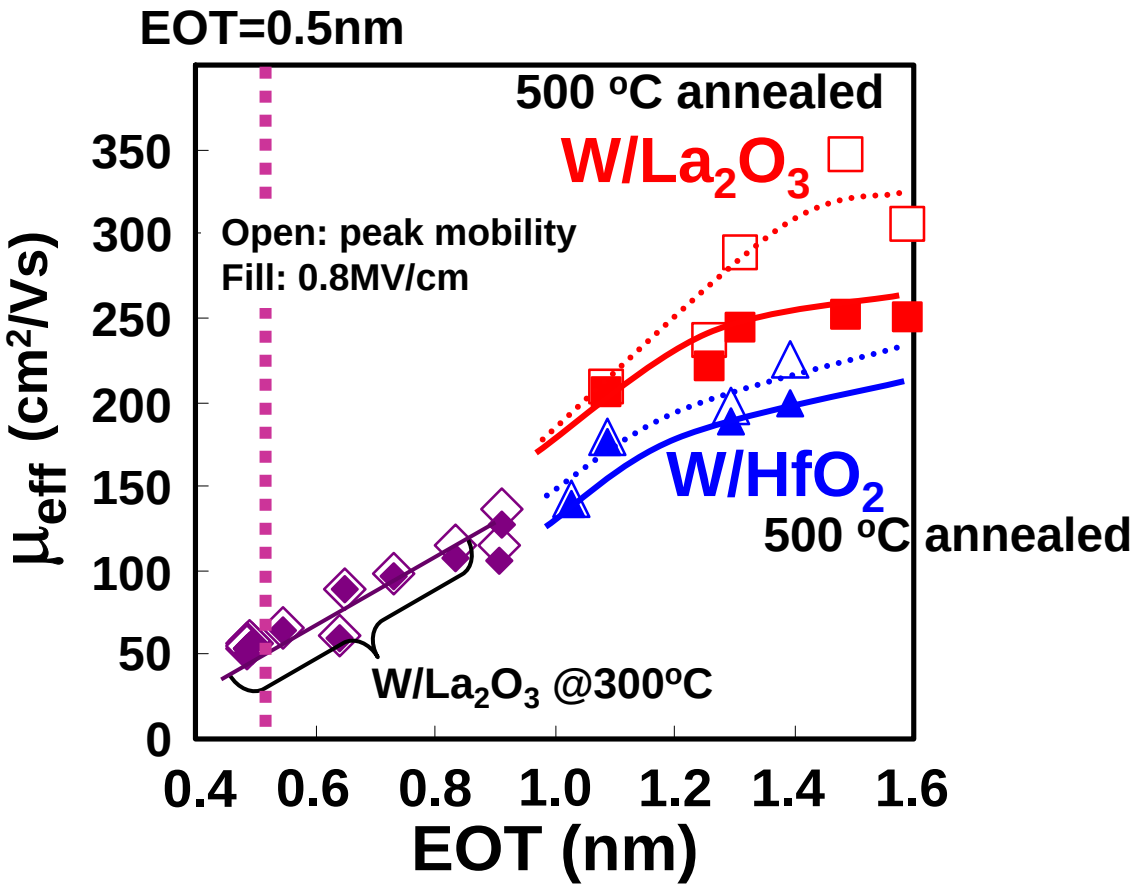
La2O3

EOT=0.37nm EOT=0.40nm EOT=0.48nm



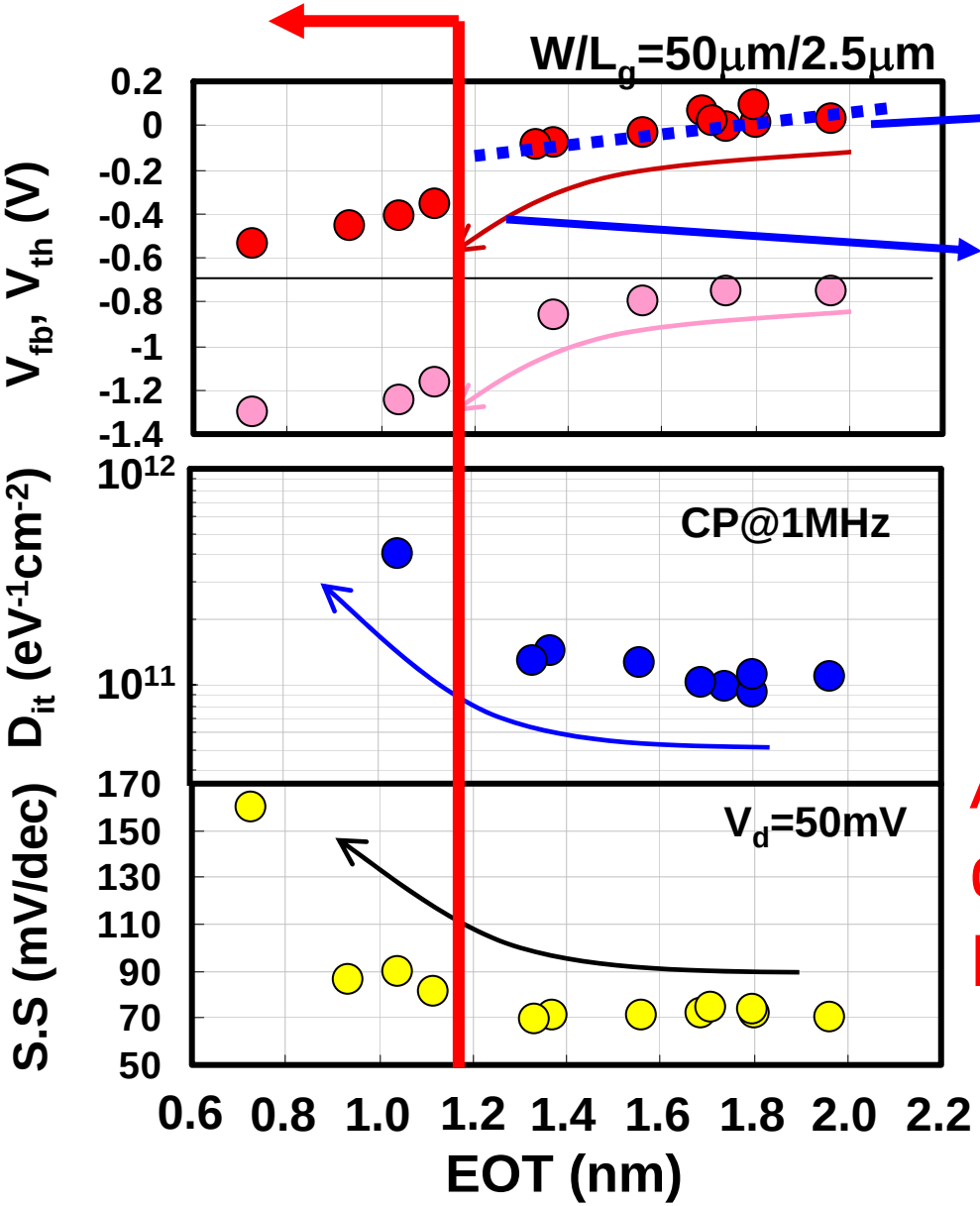
0.48 →0.37nm Increase of Id at 30%

μ_{eff} of W/La_2O_3 and W/HfO_2 nFET on EOT



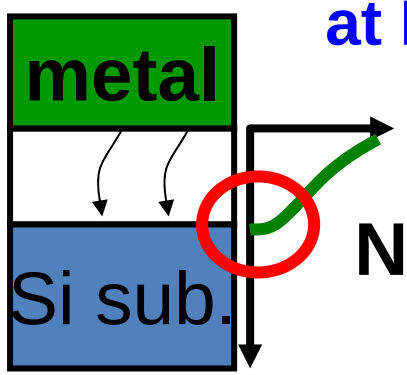
- W/La_2O_3 exhibits higher μ_{eff} than W/HfO_2
- μ_{eff} start degrades below EOT=1.4nm

FET characteristics of W/La_2O_3 on EOT



$N_{fix}=7x10^{12}$ cm^{-2}

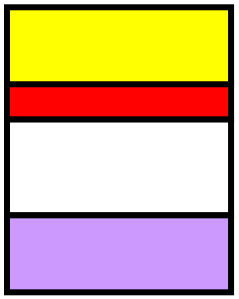
Aggressive N_{fix} generation at EOT<1.2nm



N_{fix} and D_{it}

All characteristics start to degrade or shift below EOT=1.4nm

Gate Metal Induced Defects Compensation

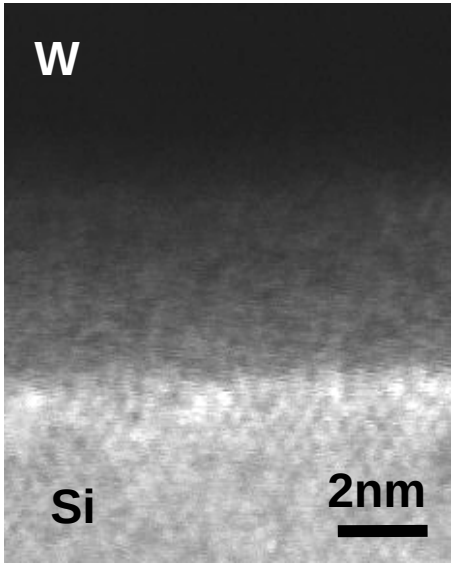


Metal Gate

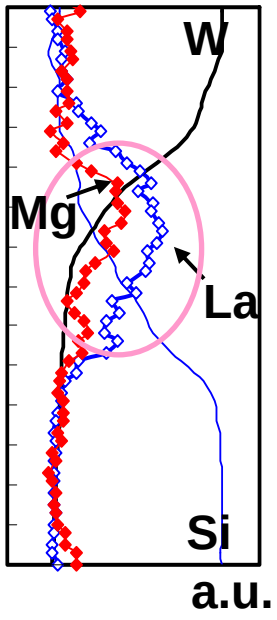
MgO

La2O3

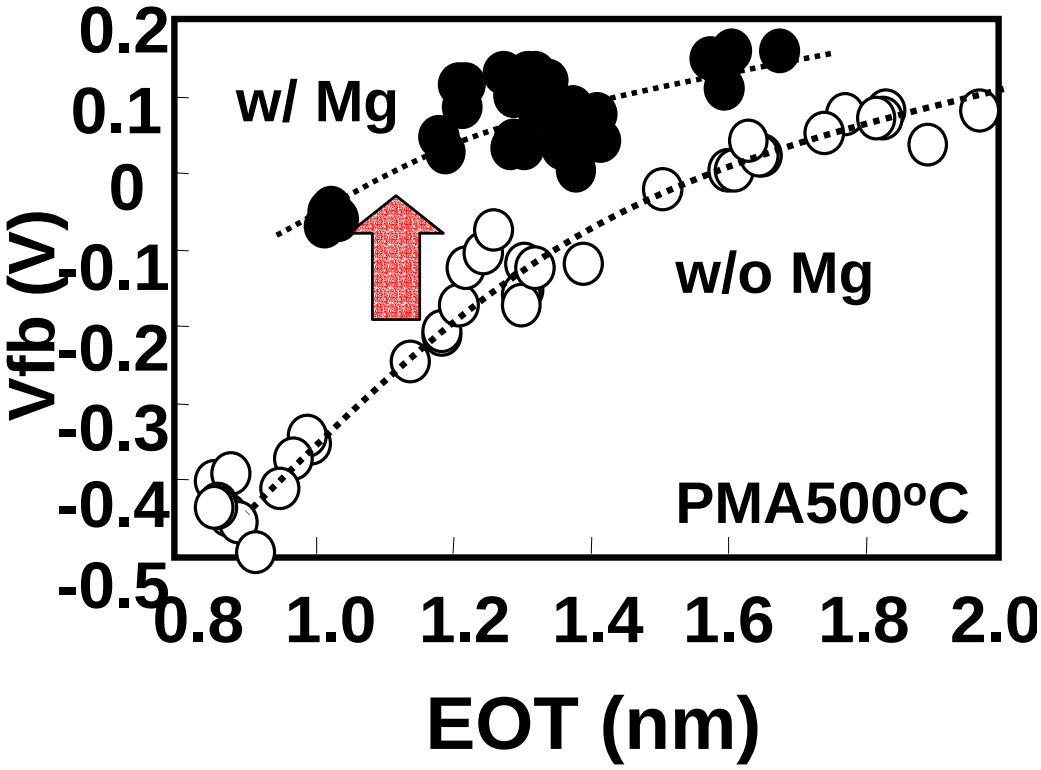
Si



TEM

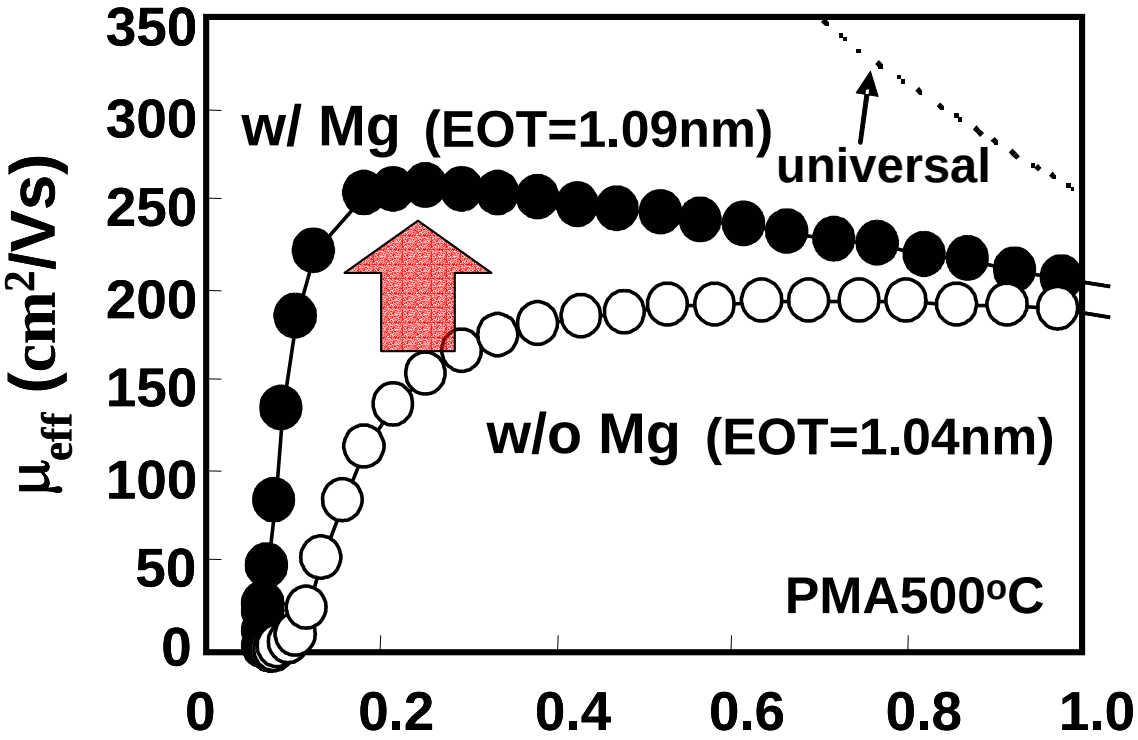


EDX



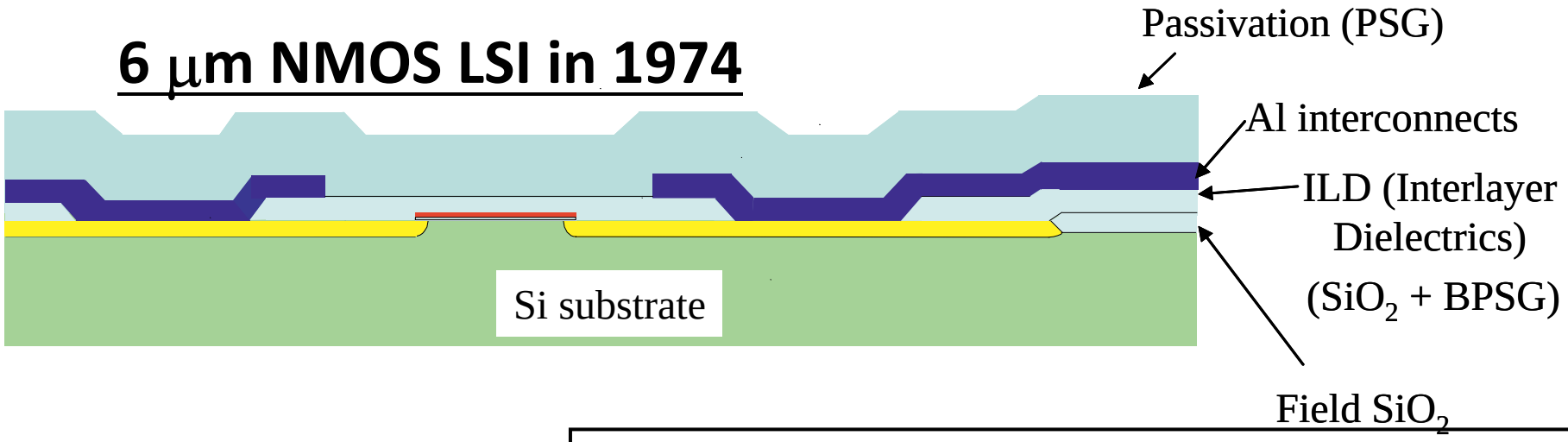
Suppression of aggressive shift in V_{fb}

Mobility Improvement with Mg Incorporation

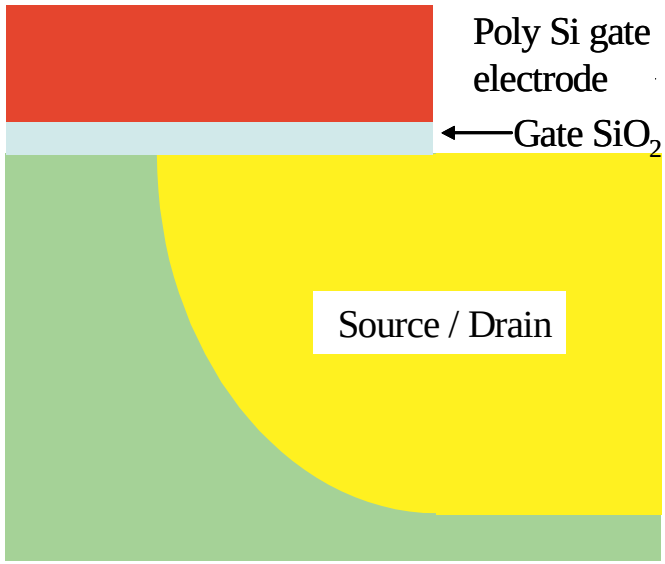


Recovery of μ_{eff} mainly at low E_{eff}

6 μm NMOS LSI in 1974



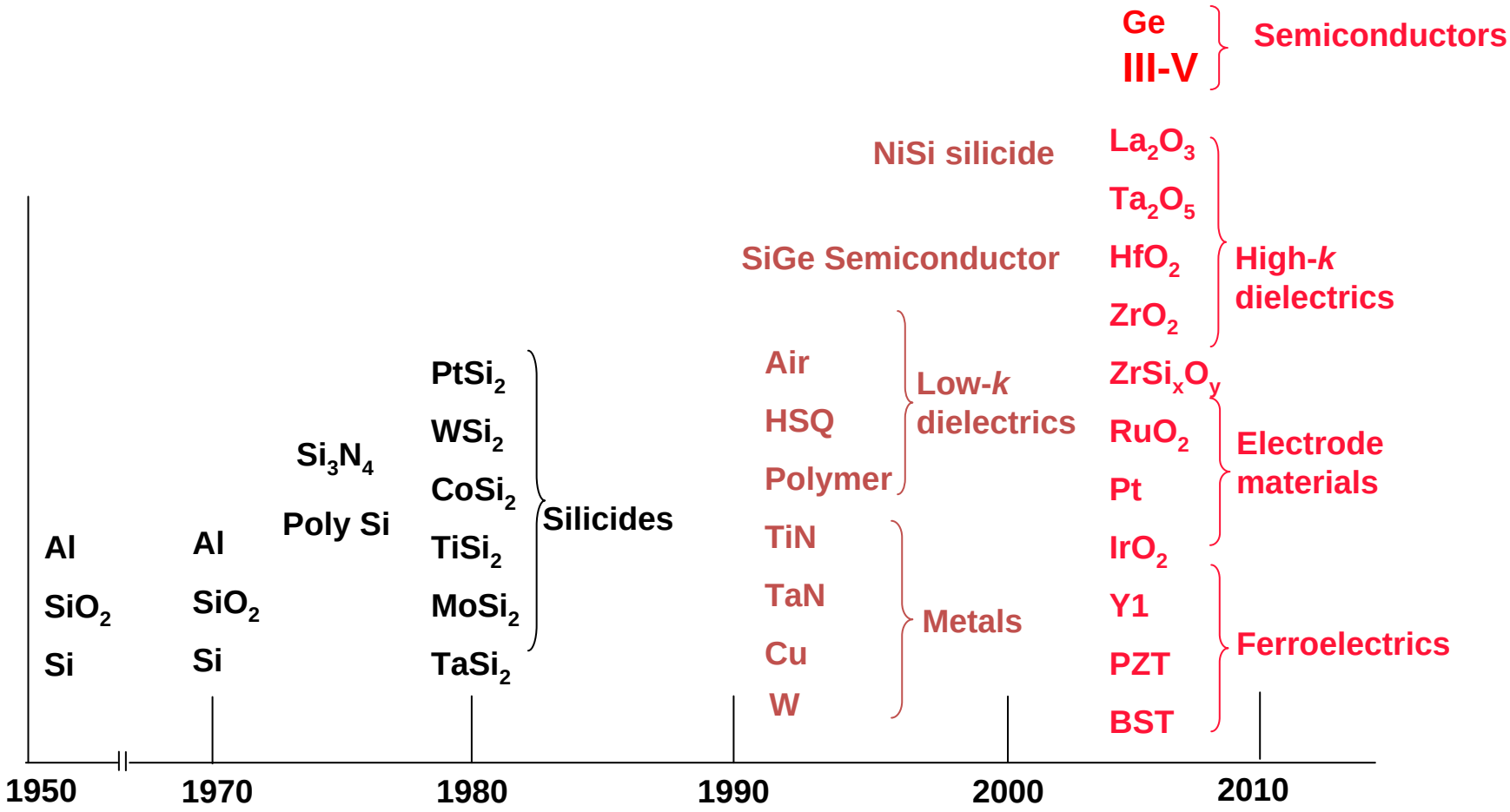
magnification



Layers	Materials	Atoms
1. Si substrate	1. Si	1. Si
2. Field oxide	2. SiO_2	2. O
3. Gate oxide	3. BPSG	3. P
4. Poly Si	4. Al	4. B
5. S/D	5. PSG	5. Al
6. Interlayer		(H, N, Cl)
7. Aluminum		
8. Passivation		

New materials

Just examples!
Many other candidates



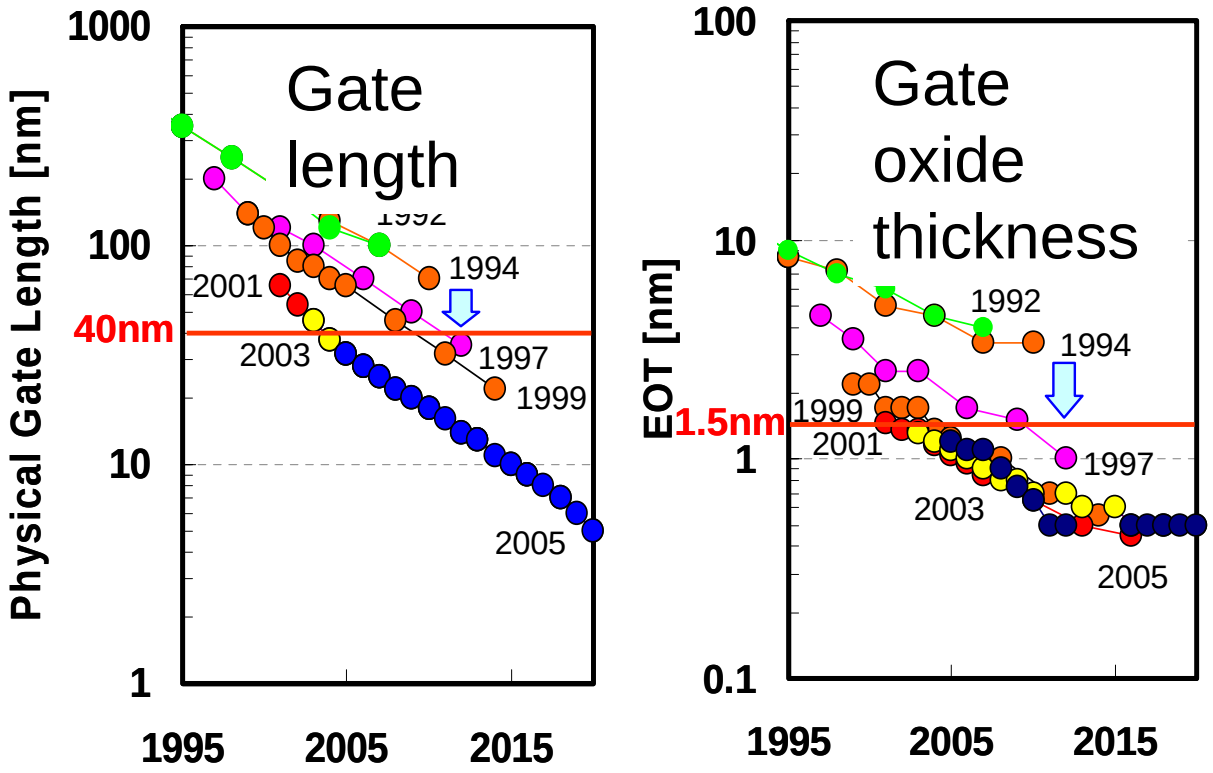
Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

What is a roadmap? What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors made by SIA (Semiconductor Industry Association with Collaboration with Japan, Europe, Korea and Taiwan)

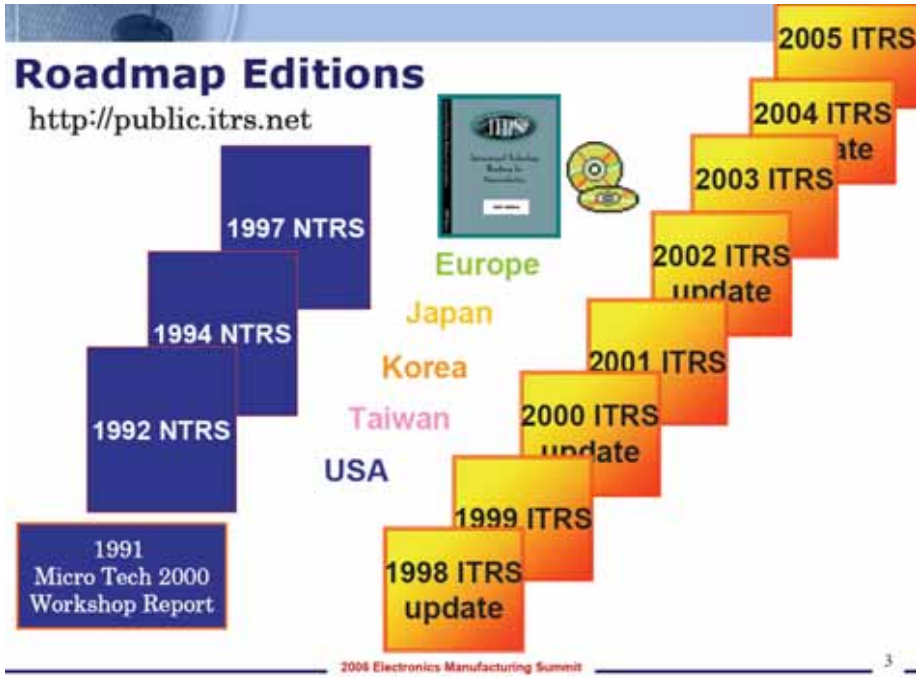


1992 -1997:NTRS (National Technology Roadmap)
1998 - : ITRS (International Technology Roadmap)

2008 ITRS update

2007 ITRS

2006 ITRS update



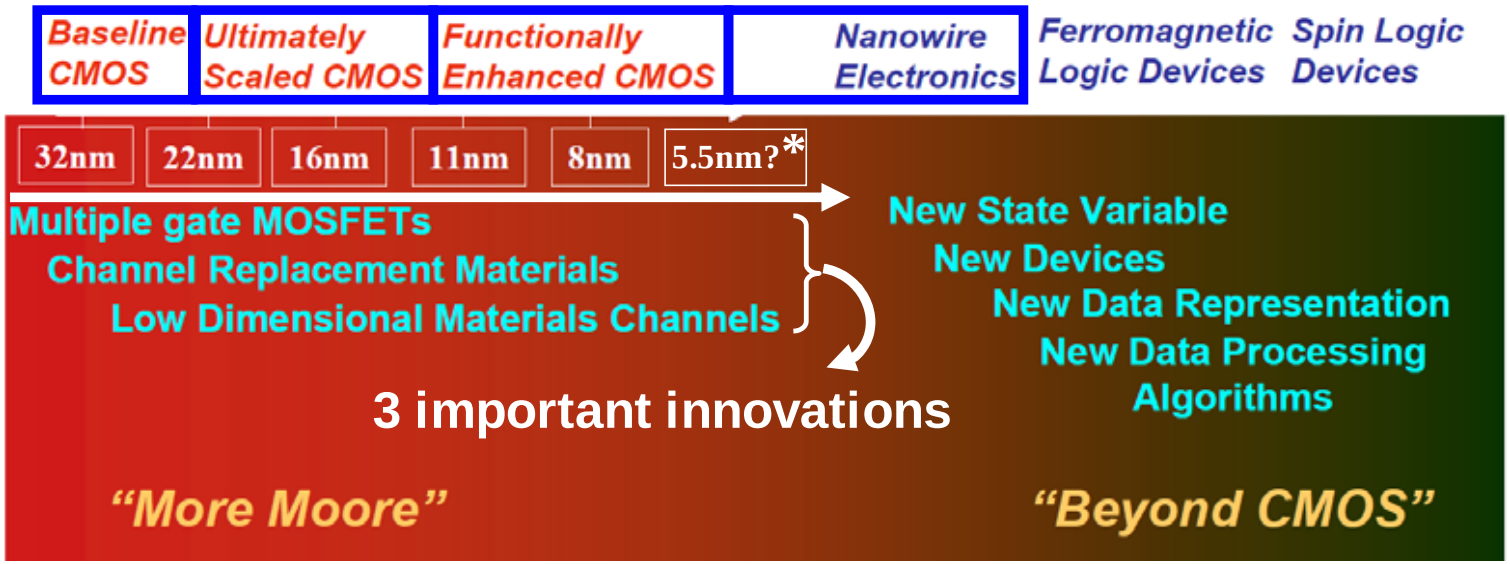
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



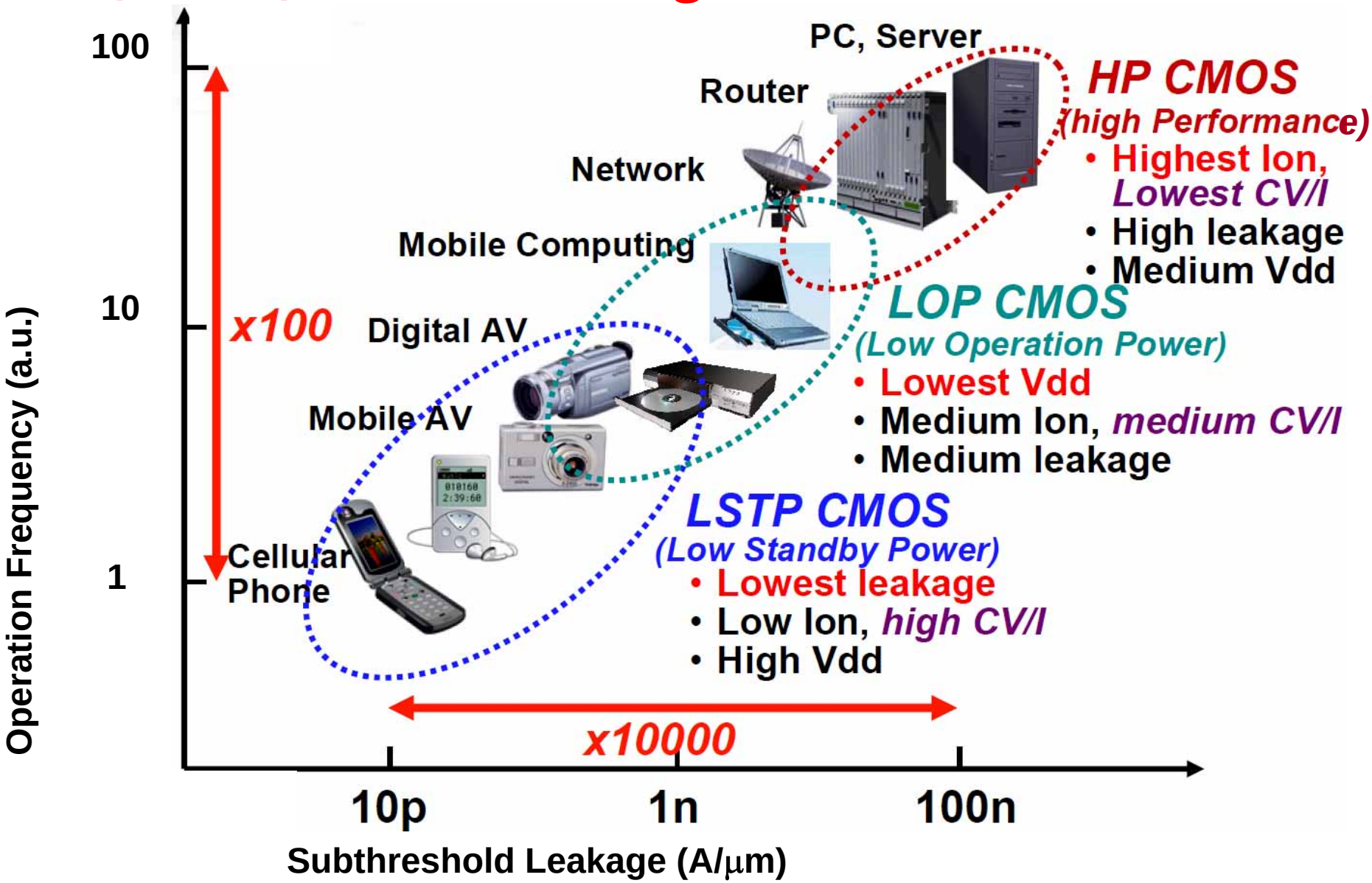
ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

***5.5nm? was added by Iwai**

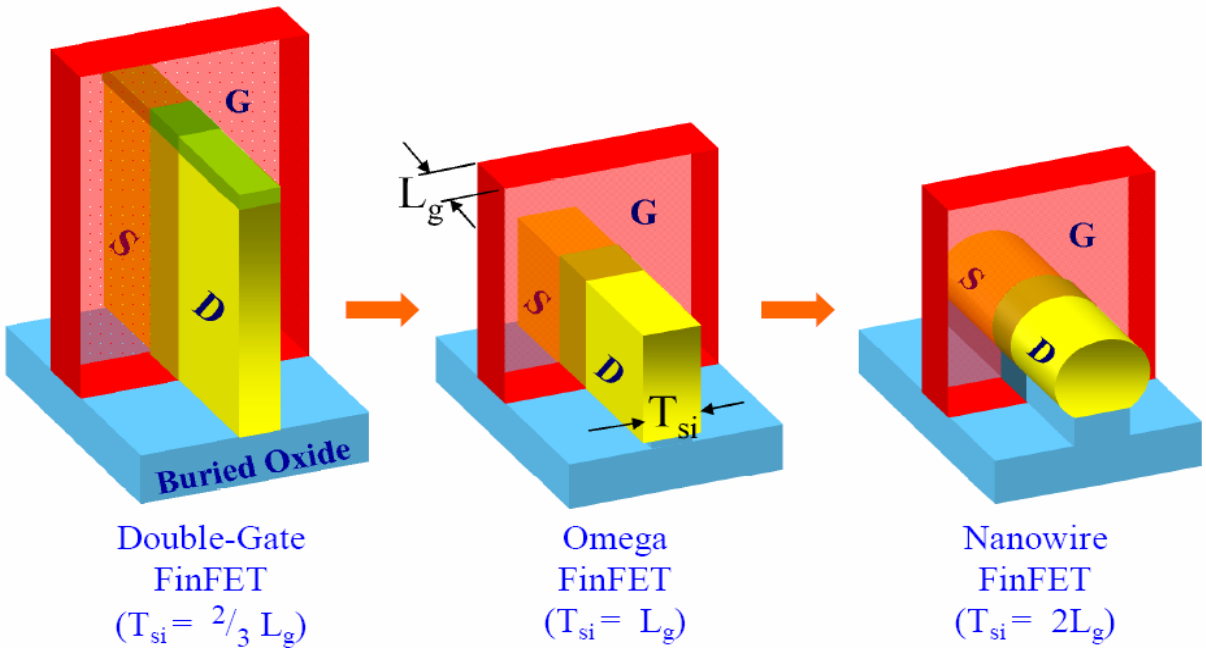
70

HP, LOP, LSTP for Logic CMOS



Source: 2007 ITRS Winter Public Conf.

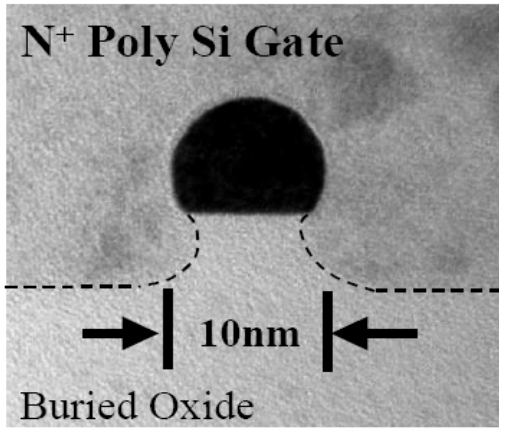
FinFET to Nanowire

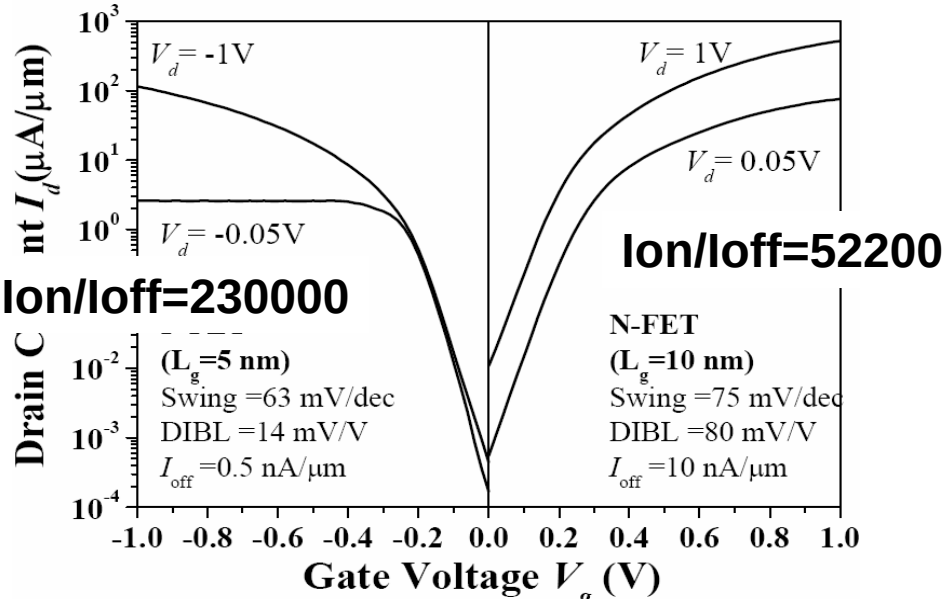


Double-Gate FinFET ($T_{si} = {}^{2}/_{3}\, L_g$)

Omega FinFET ($T_{si} = L_g$)

Nanowire FinFET ($T_{si} = 2L_g$)



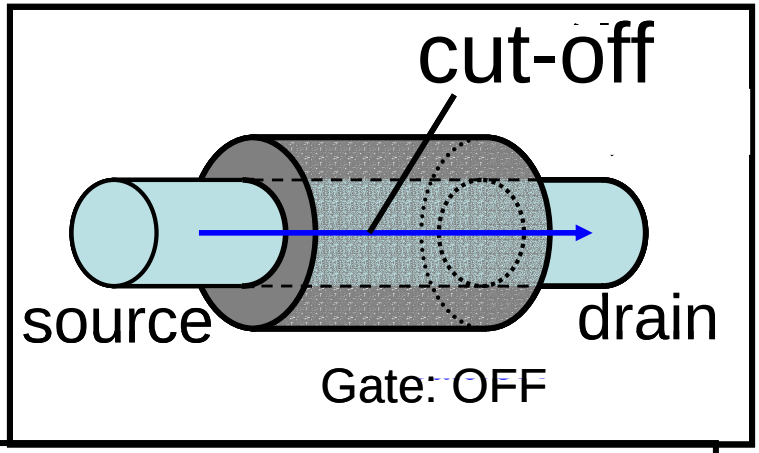


Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

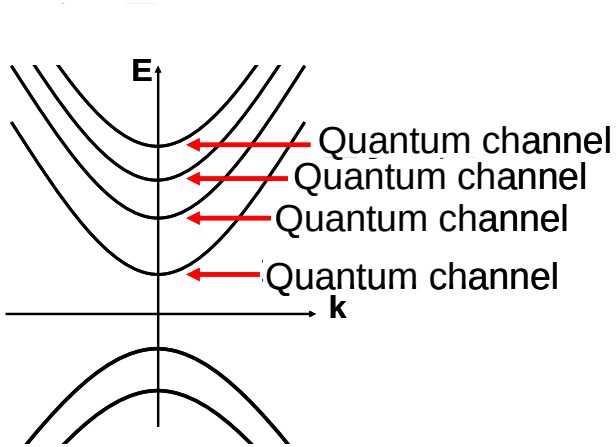
Si nanowire FET as a strong candidate after CMOS limitation

1. Compatibility with current CMOS process
2. Good controllability of I_{OFF}
3. High drive current

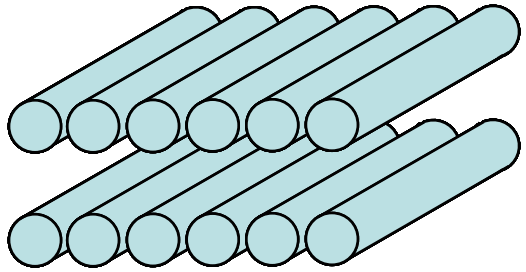


1D ballistic conduction

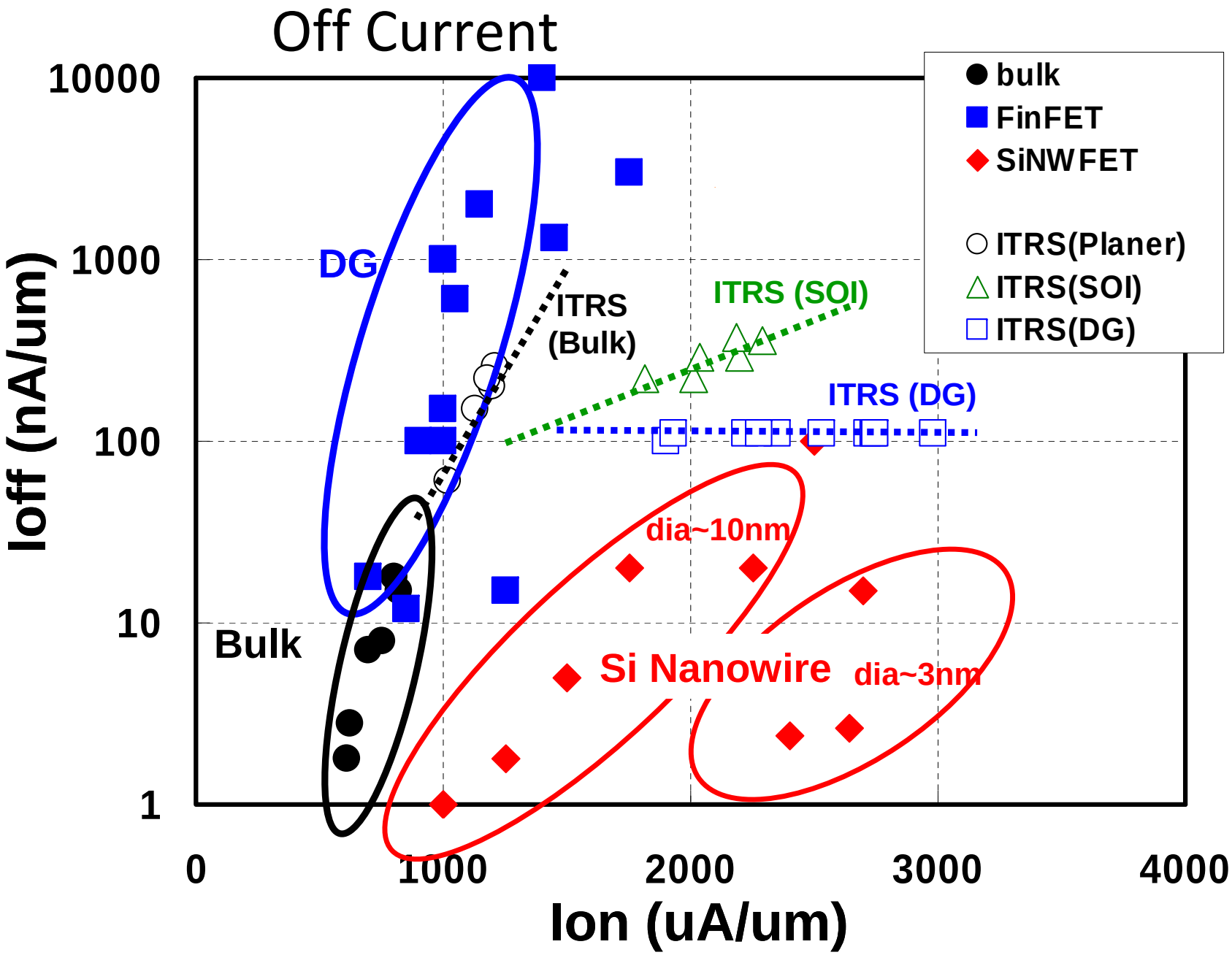
Multi quantum Channel



High integration of wires

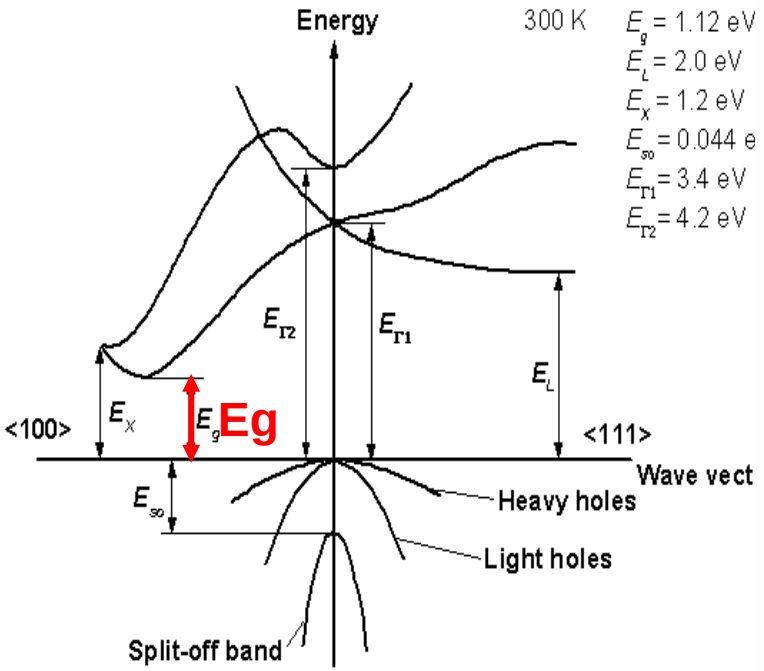


by the courtesy of Professor H. Iwai

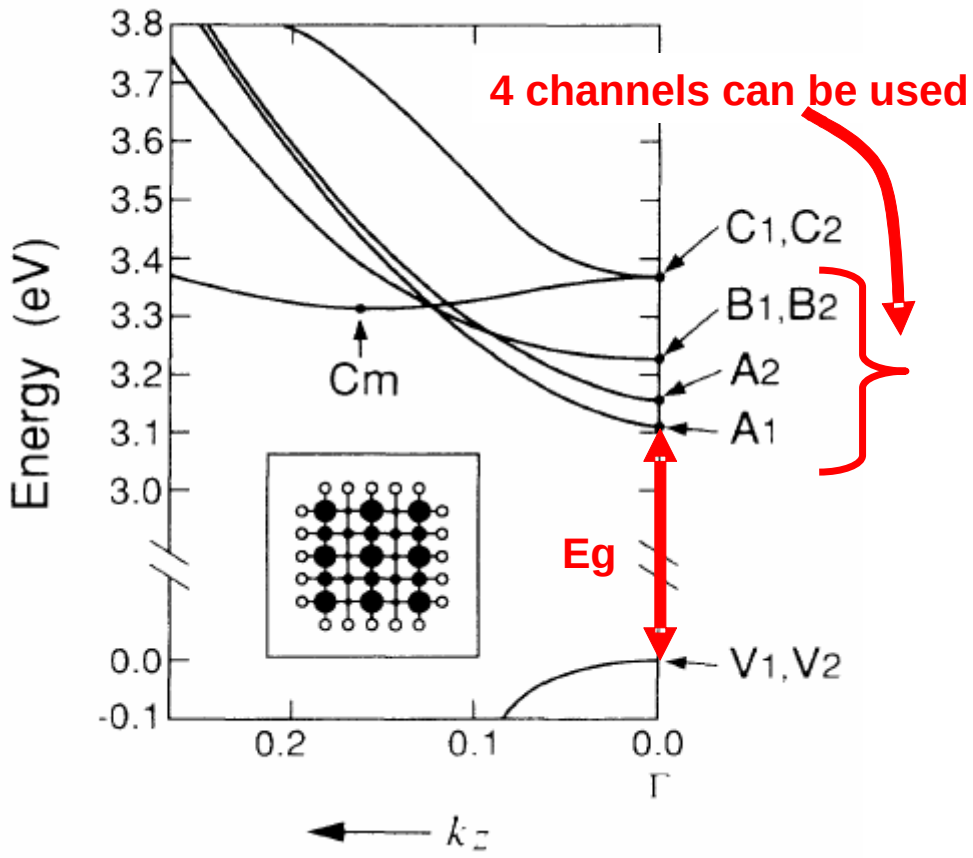

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



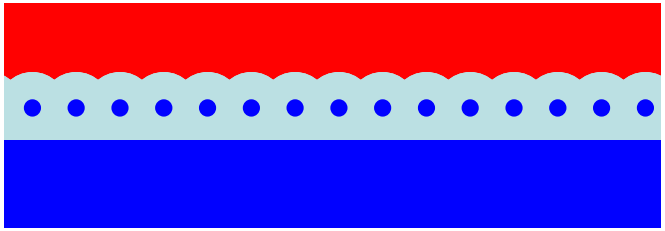
Energy band of Bulk Si



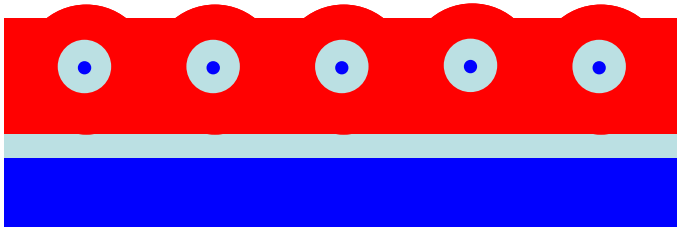
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

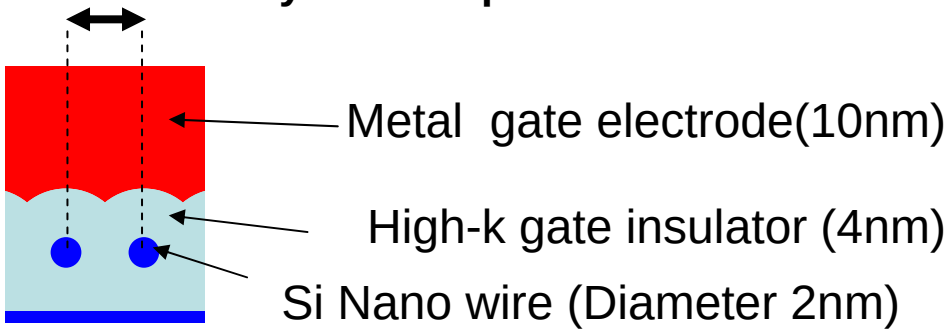
Front gate type MOS 165 wires /μm

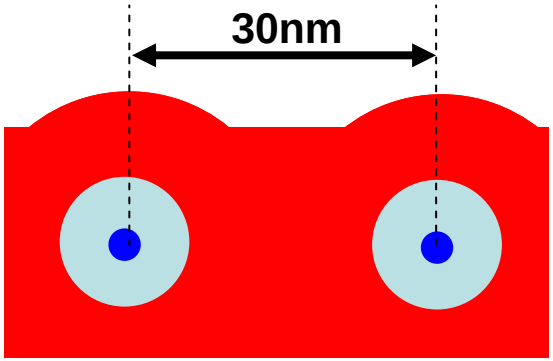


Surrounded gate type MOS 33 wires/μm

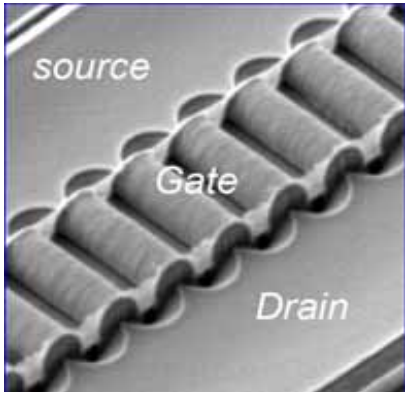


6nm pitch
By nano-imprint method



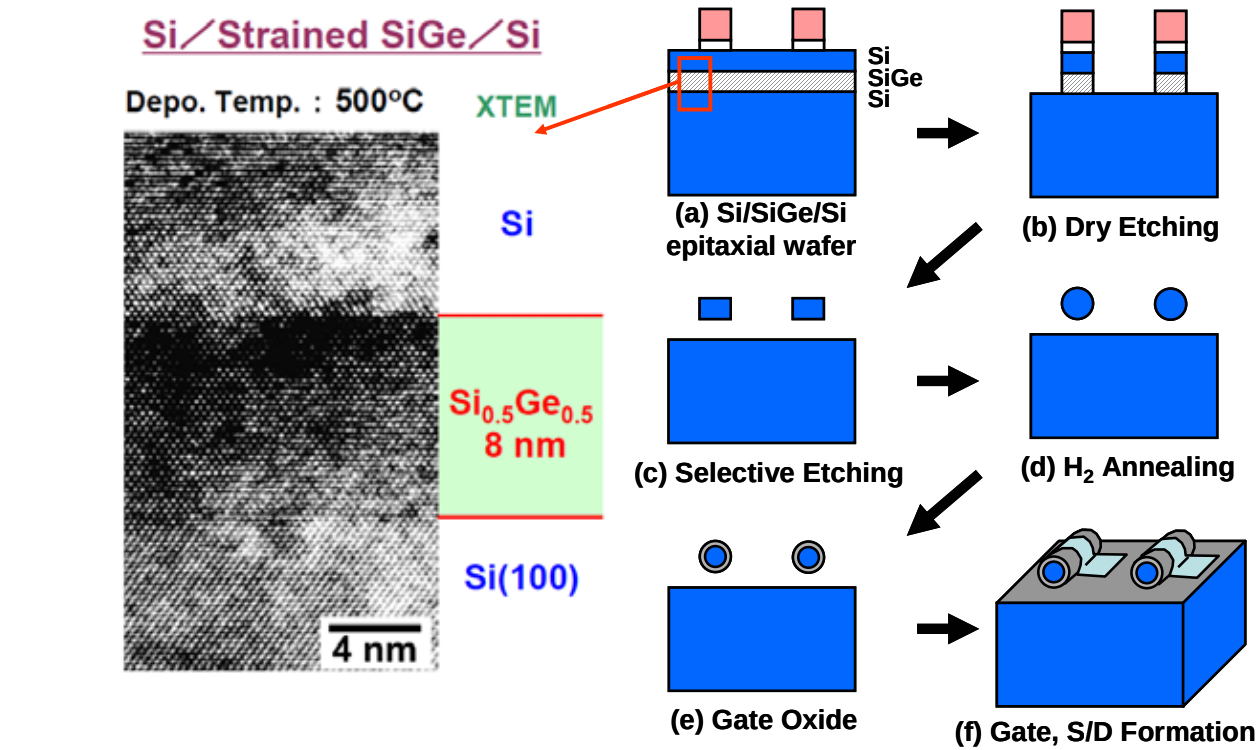


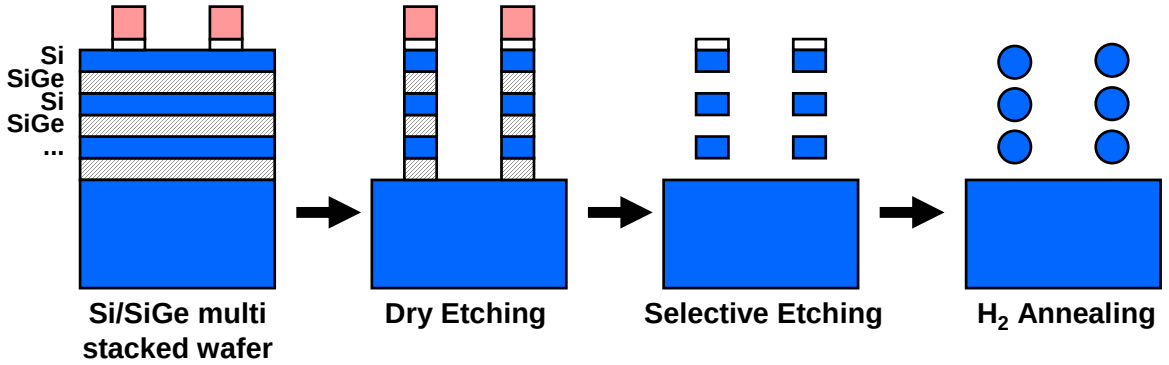
30nm pitch:
EUV lithograpy



Surrounded gate MOS

Increase the number of wires towards vertical dimension

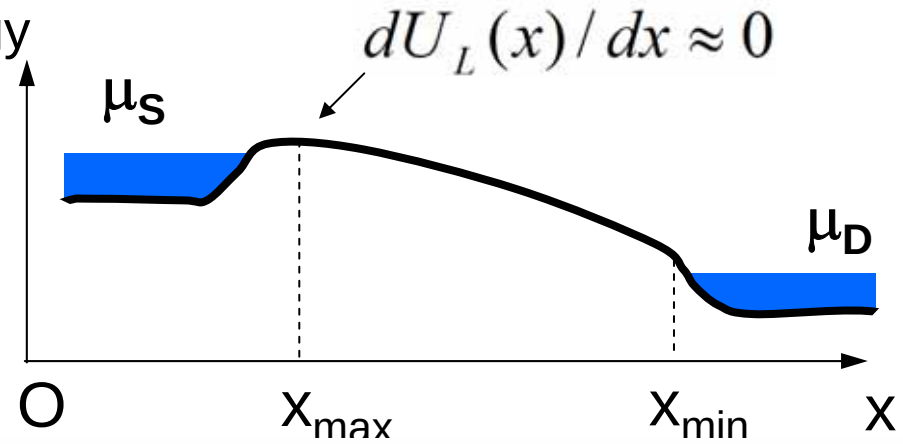




Theoretical model of SiNW FET

Landauer Formalism for Ballistic FET

Potential Energy

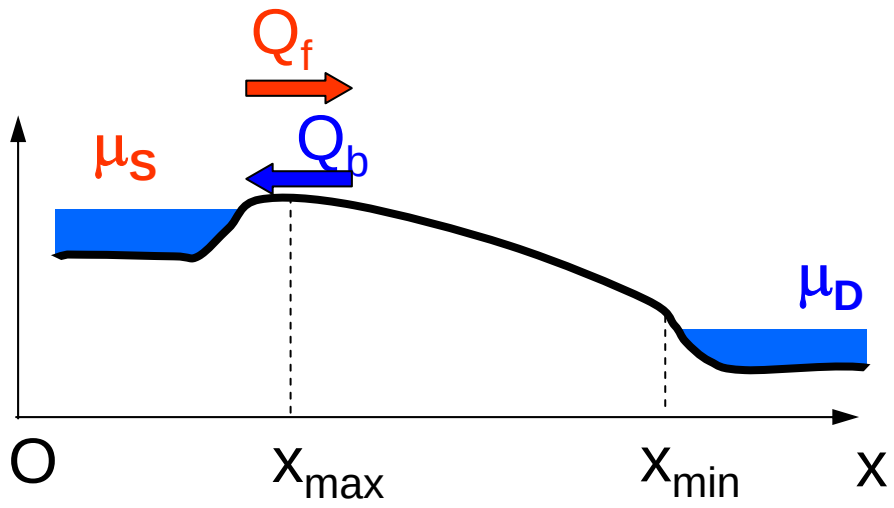


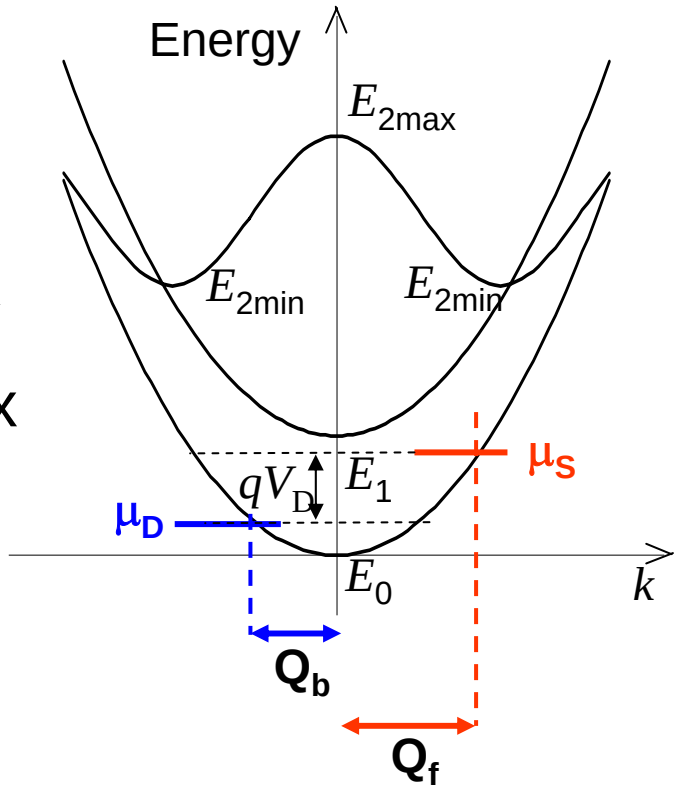
$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f(E,\mu_S) - f(E,\mu_D) \right] T_i(E)\, dE$$

From x_{max} to x_{min} $\quad T_i(E) \approx 1$

$$I_D = G_0 \left(\frac{k_B T}{q} \right) \sum_i g_i \ln \left\{ \frac{1+\exp\left[(\mu_S - E_{i0})/k_B T \right]}{1+\exp\left[(\mu_D - E_{i0})/k_B T \right]} \right\}$$

Carrier Density obtained from E-k Band

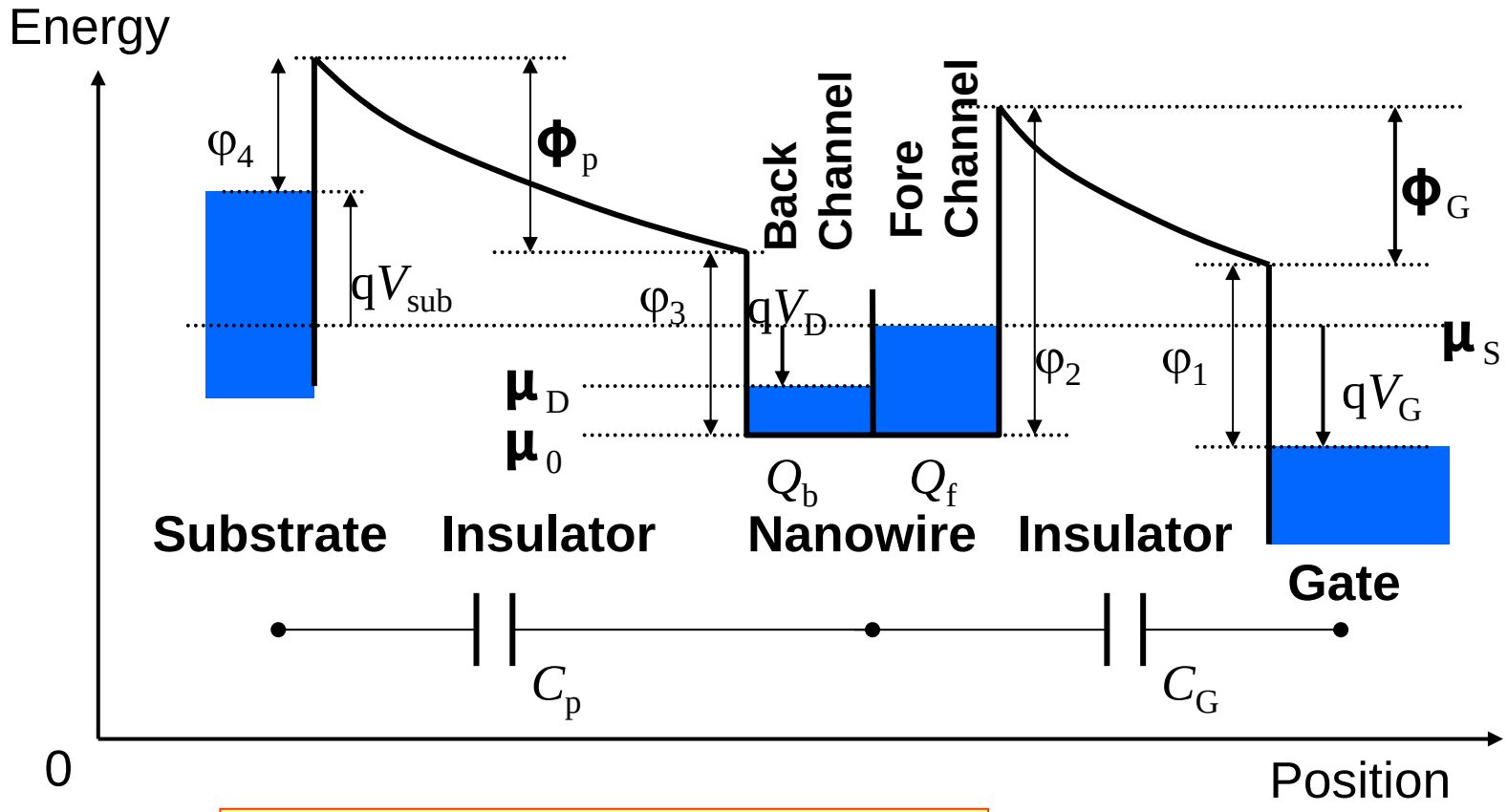




$$|Q| = |Q_f| + |Q_b|$$

$$= \frac{q}{\pi} \sum_i g_i \left[\int_{k_{i\min}}^{\infty} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_S}{k_B T}\right\}} + \int_{-\infty}^{k_{i\min}} \frac{dk}{1+\exp\left\{\frac{E_i(k)-\mu_D}{k_B T}\right\}} \right]$$

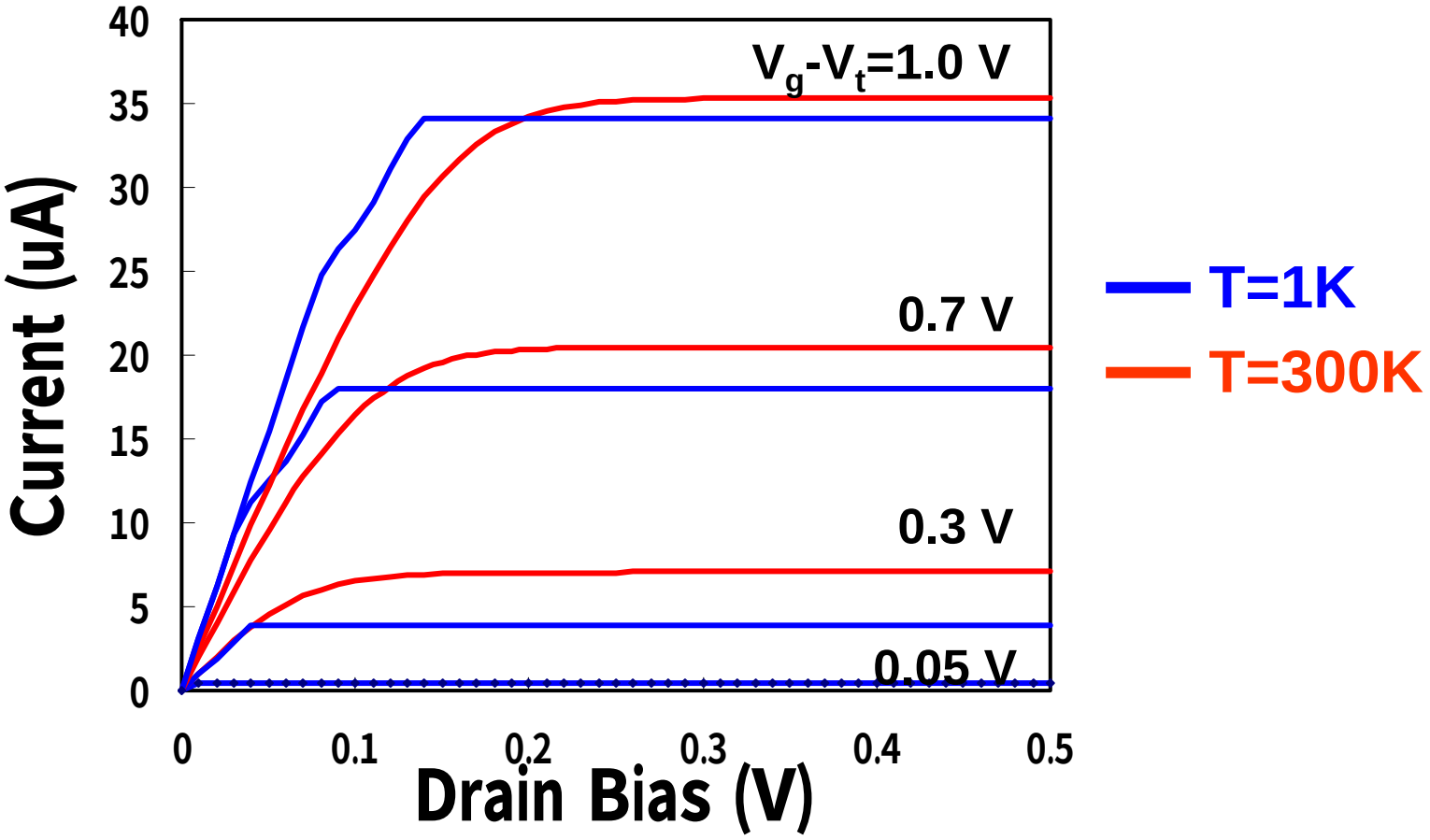
Carrier Density obtained from Band Diagram



$$\frac{|Q|}{C_G} = (V_G - V_t) - \alpha \frac{\mu_S - \mu_0}{q}$$

$$\alpha = 1 + \frac{C_P}{C_G}$$

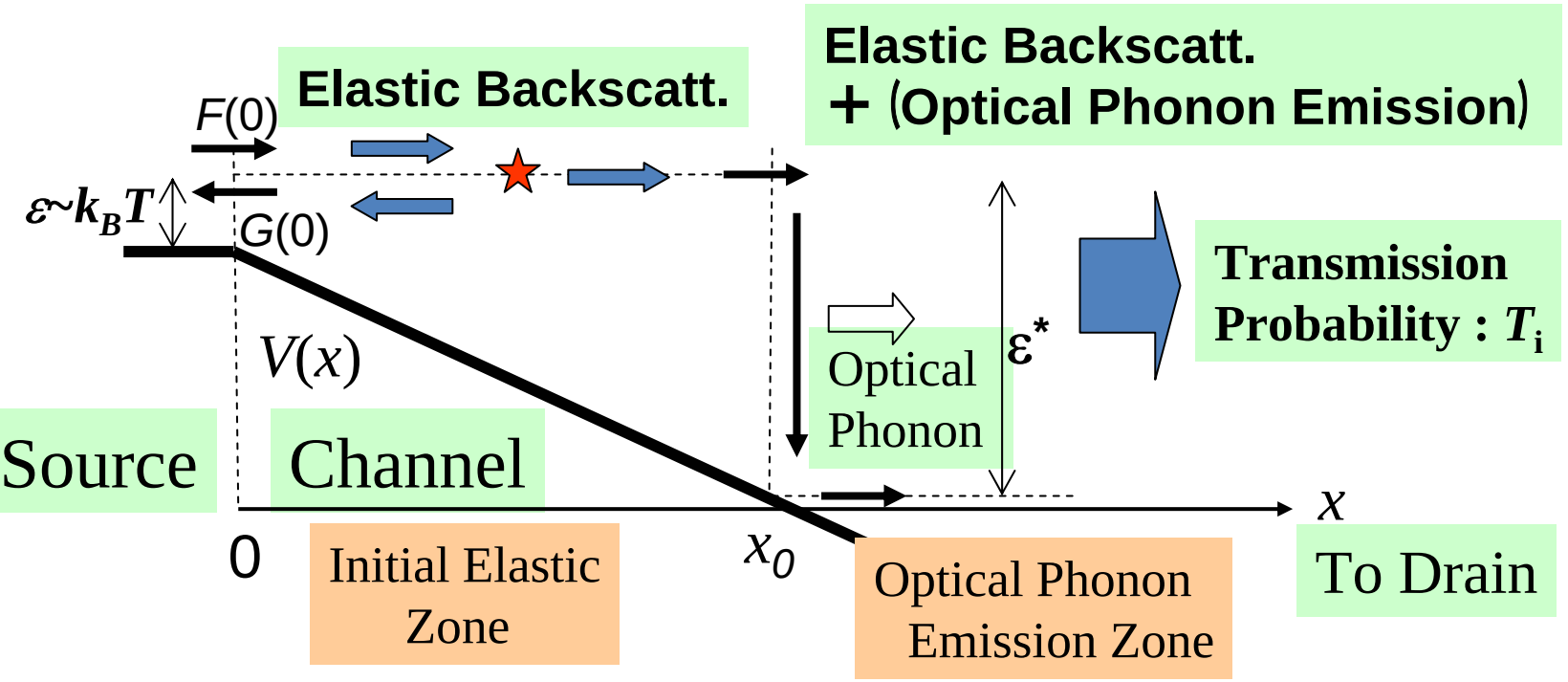
IV Characteristics of Ballistic SiNW FET



Small temperature dependency
35μA/wire for 4 quantum channels

Model of Carrier Scattering

Linear Potential Approx. ; Electric Field E



Transmission Probability to Drain

$$T(\varepsilon) = \left.\frac{F(0) - G(0)}{F(0)}\right)_{\text{Injection from Drain}=0}$$

Résumé of the Compact Model

$$I = \frac{q}{\pi\hbar}\sum_i g_i \int \left[f(\varepsilon,\mu_s) - f(\varepsilon,\mu_D) \right] T_i \, d\varepsilon$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left\{\dfrac{\sqrt{2r+t_{ox}}+\sqrt{t_{ox}}}{\sqrt{2r+t_{ox}}-\sqrt{t_{ox}}}\right\}}.$$

Planar Gate

$$(V_G - V_t) - \alpha\frac{\mu_S - \mu_0}{q} = \frac{\left|Q_f + Q_b\right|}{C_G}.$$

$$\mu_S - \mu_D = qV_D$$

$$C_G = \frac{2\pi\varepsilon_{ox}}{\ln\left(\dfrac{r+t_{ox}}{r}\right)}.$$

GAA

(Electrostatics requirement)

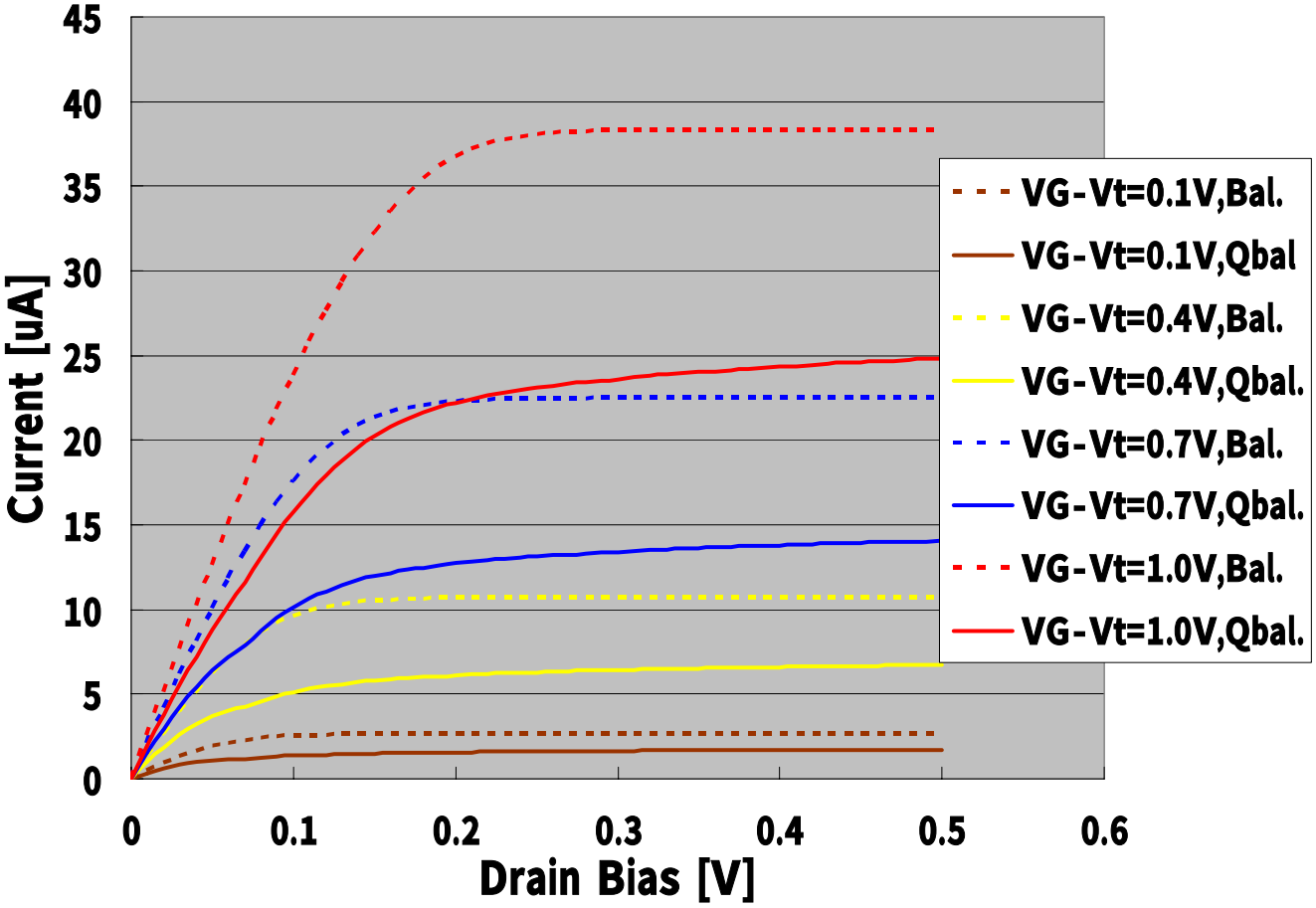
$$\left|Q_f + Q_b\right| = \frac{q}{\pi}\sum_i g_i \left[\int_{-\infty}^{\infty} \frac{dk}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \int_{-\infty}^{0} \left\{ \frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_S}{k_BT}\right\}} - \frac{1}{1+\exp\left\{\dfrac{\varepsilon_i(k)-\mu_D}{k_BT}\right\}} \right\} T_i(\varepsilon_i(k))dk \right]$$

$$T(\varepsilon) = \frac{\sqrt{2D_0}\,qE}{\left(\sqrt{B_0+D_0}+\sqrt{D_0}\right)qE + \sqrt{2mD_0}\,B_0 \ln\left(\dfrac{qEx_0+\varepsilon}{\varepsilon}\right)}$$

(Carrier distribution in Subbands)

Unknowns are I_D, $(\mu_S-\mu_0)$, $(\mu_D-\mu_0)$, および (Q_f+Q_b)

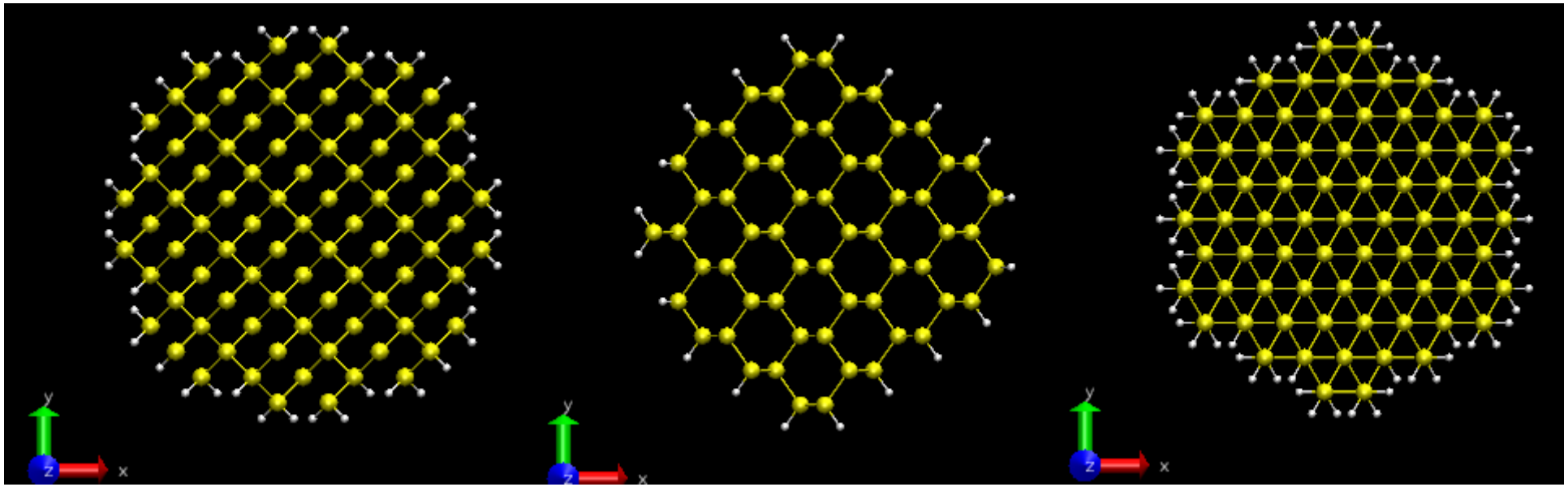
I-V_D Characteritics (RT)



- Electric current 20～25 μA
- No satruration at Large V_D

Cross section of Si NW

First principal calculation, TAPP

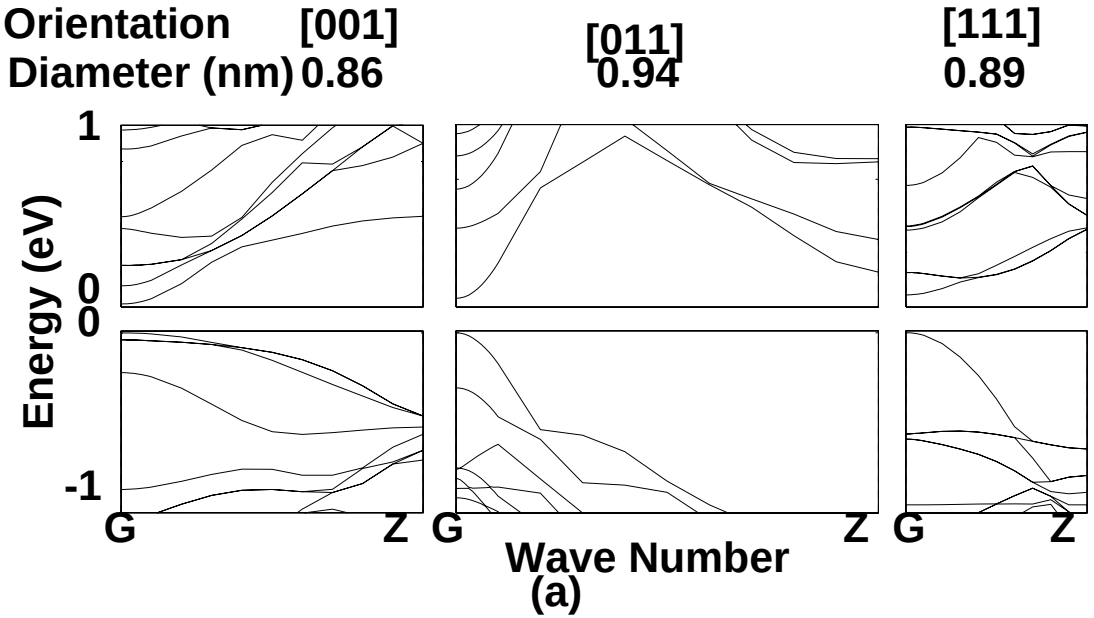


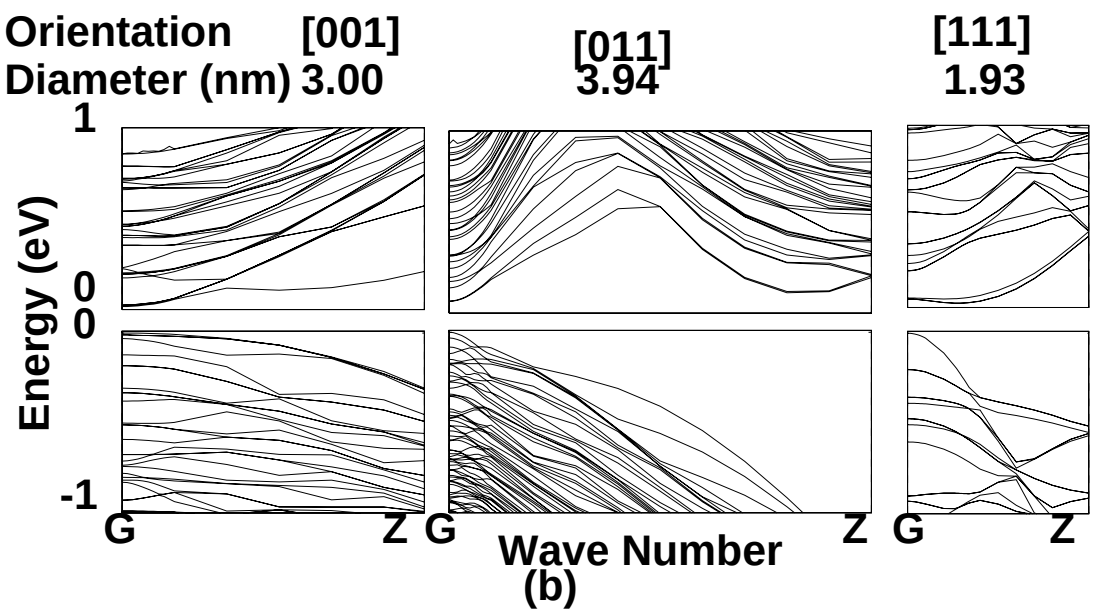
D=1.96nm
[001]

D=1.94nm
[011]

D=1.93nm
[111]

Si nanowire FET with 1D Transport

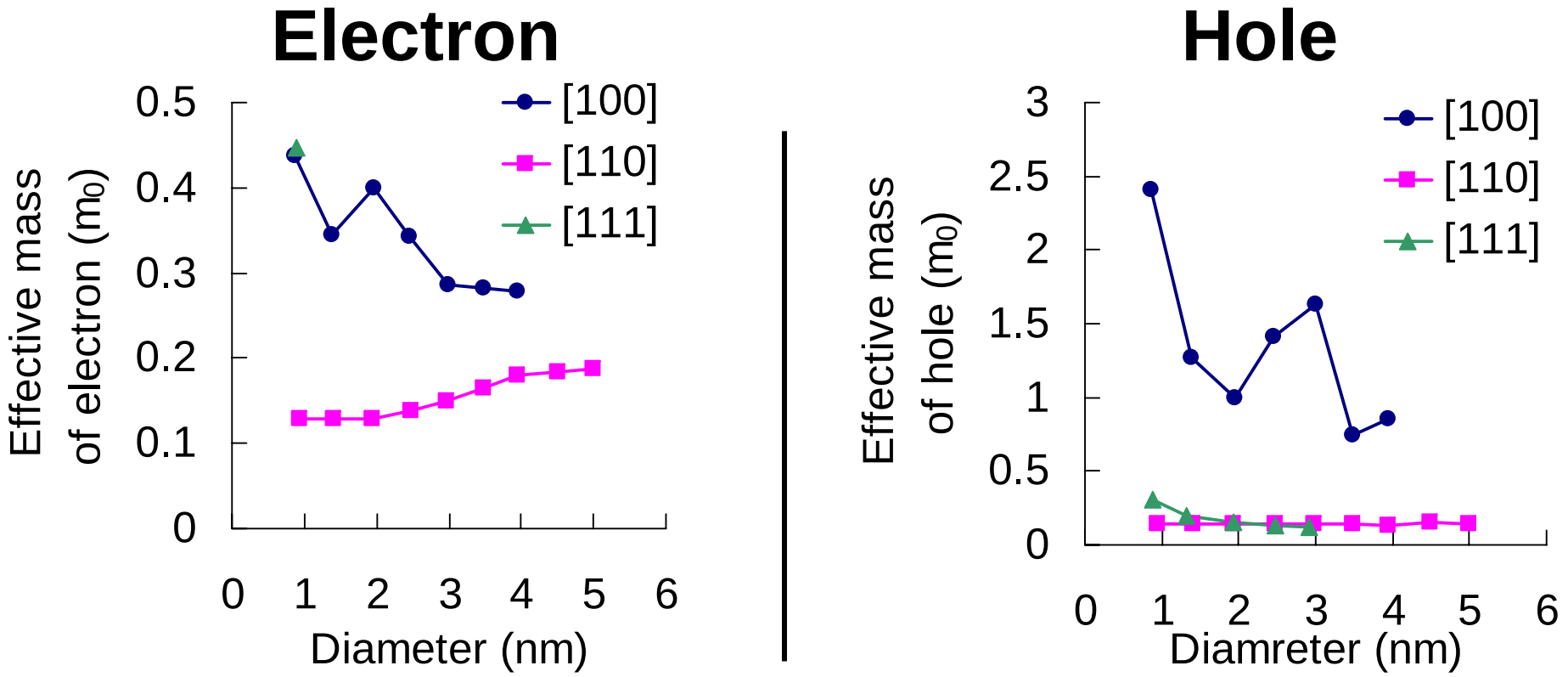




Small mass with [011]

Large number of quantum channels with [001]

Effective mass

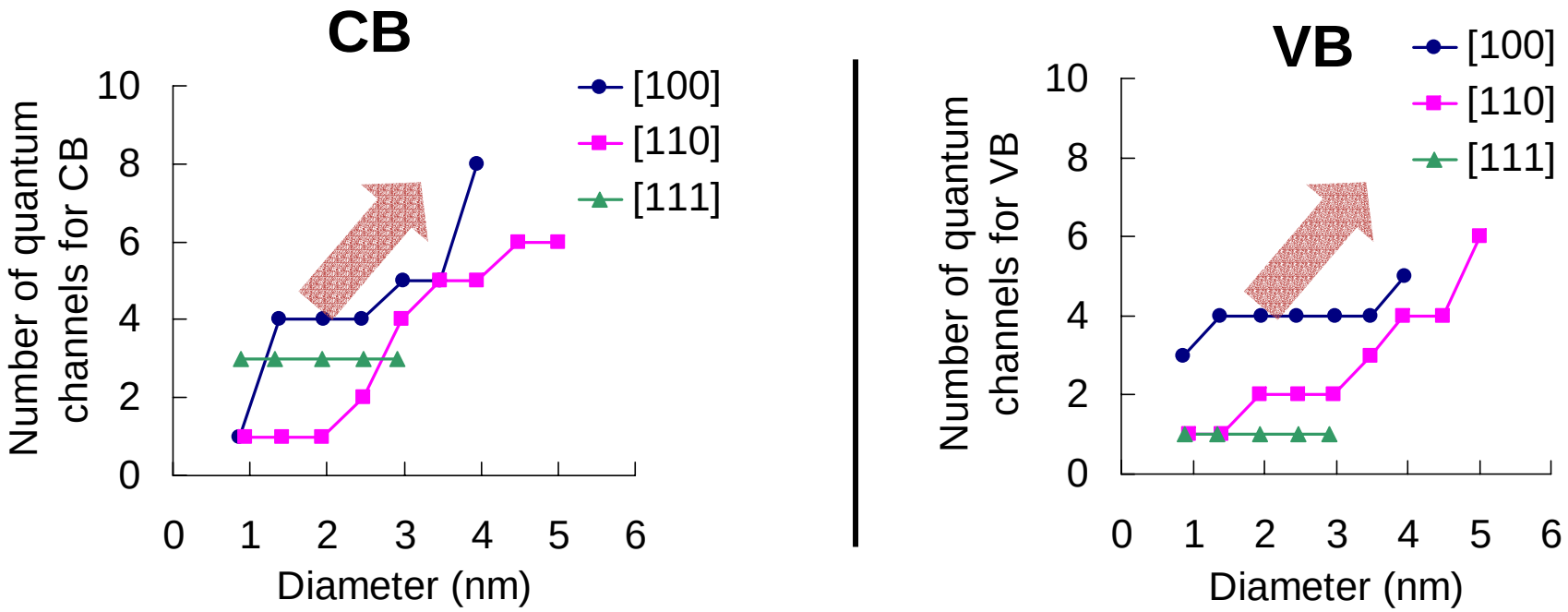


Lighter effective masses make conductance higher

Electron	**[100]**	**[111]**	**>**	**[110]**	**lighter**
Hole	**[100]**	**>>**	**[110]**	**[111]**	

Numbers of Quantum Channels

Quantum channels denote subband edges within 0.1 eV from CBM and VBM



Quantum channels increase in large wire

Quantum channel ➡ **Passage for transport**

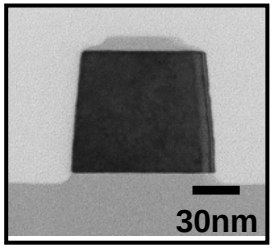
CB [110] [111] < [100] **more**

VB [111] < [110] < [100]

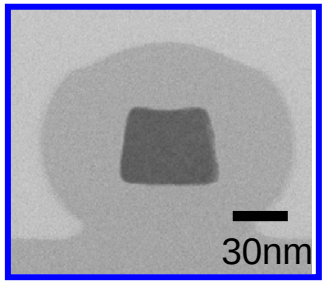
SiNW FET Fabrication

SiNW FET Fabrication

S/D & Fin Patterning

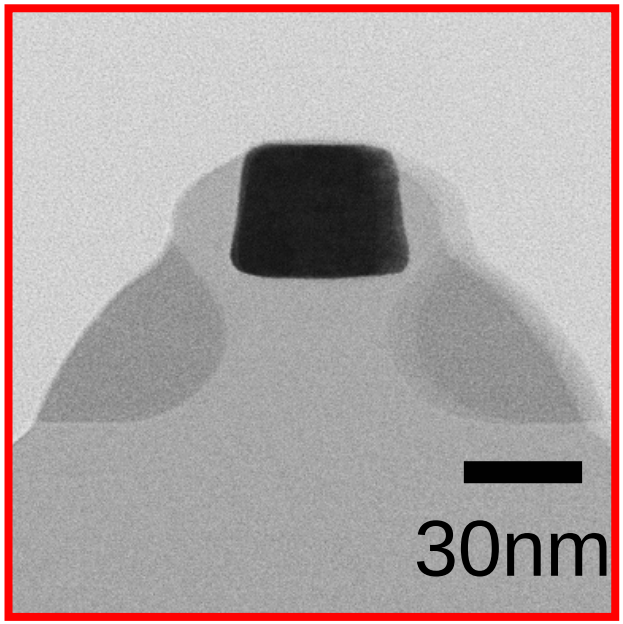


Sacrificial Oxidation



Oixde etch back

SiN sidewall support formation



Gate Oxidation & Poly-Si Deposition

Gate Lithography & RIE Etching

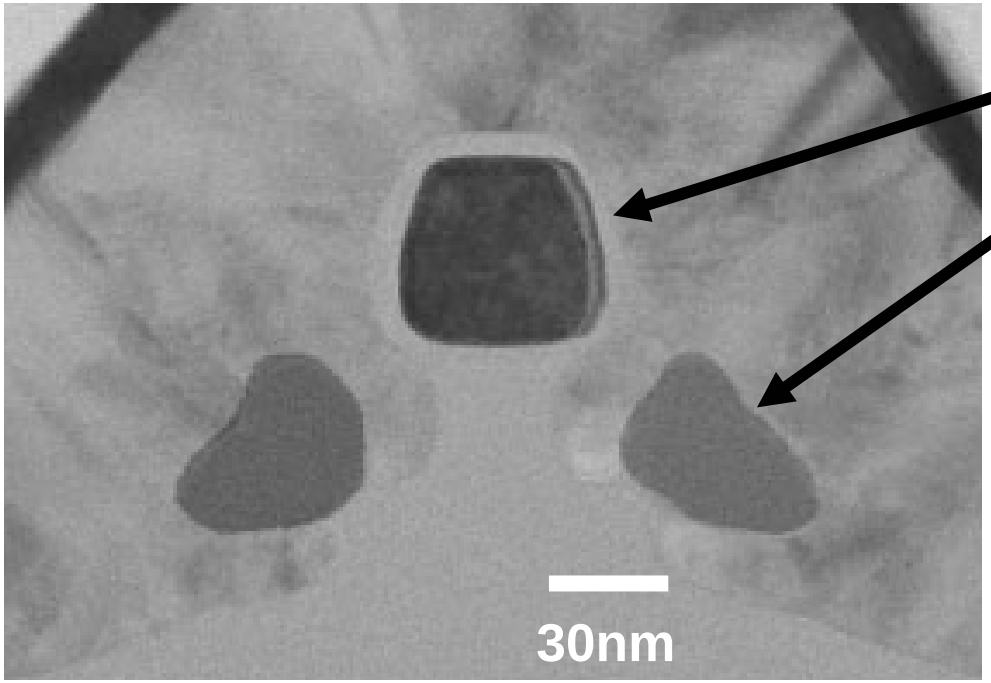
Gate Sidewall Formation

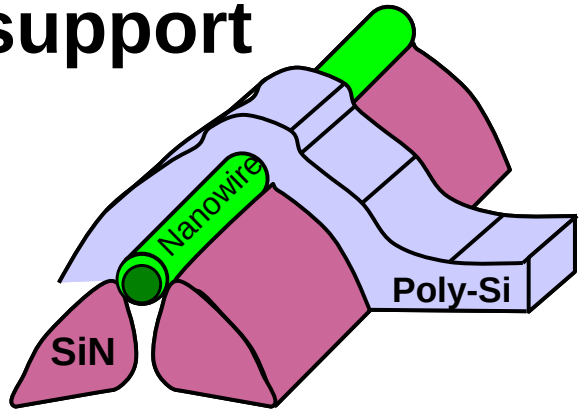
Ni SALISIDE Process (Ni 9nm / TiN 10nm)

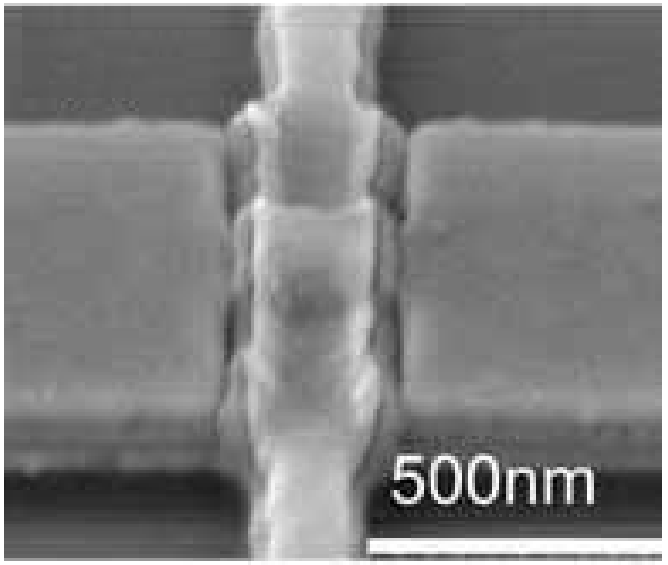
Backend

Standard recipe for gate stack formation

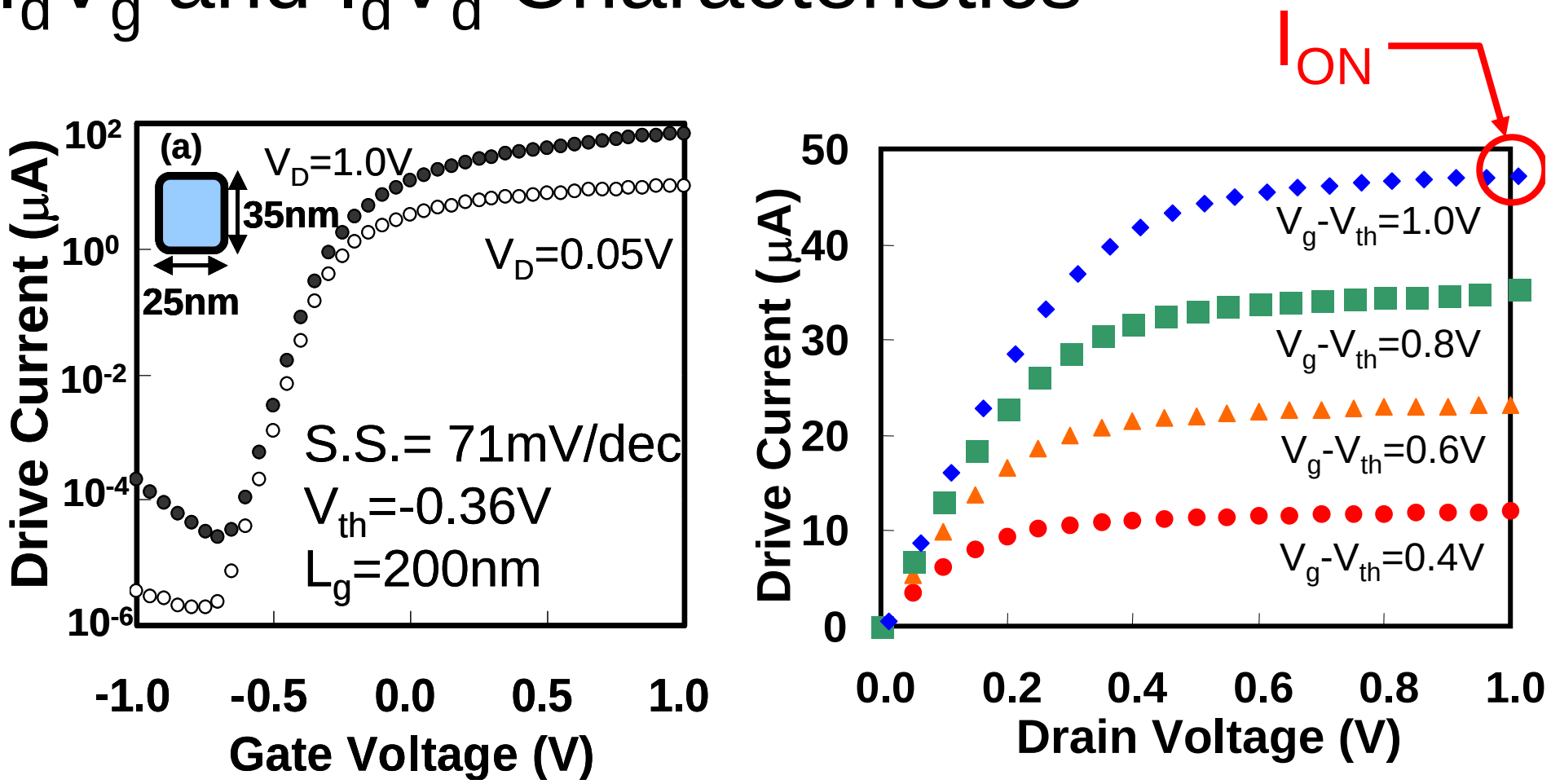
Fabricated SiNW FET





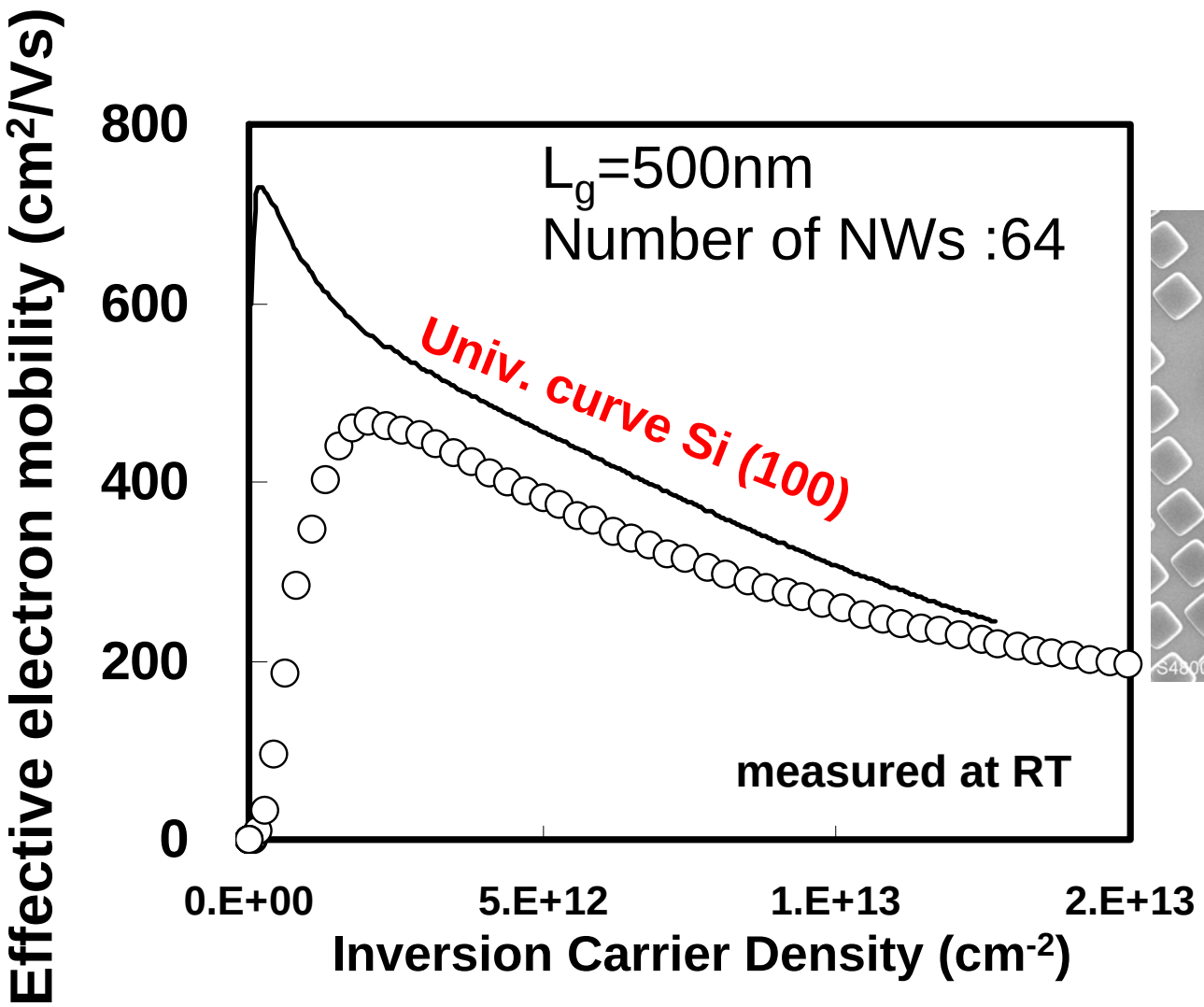


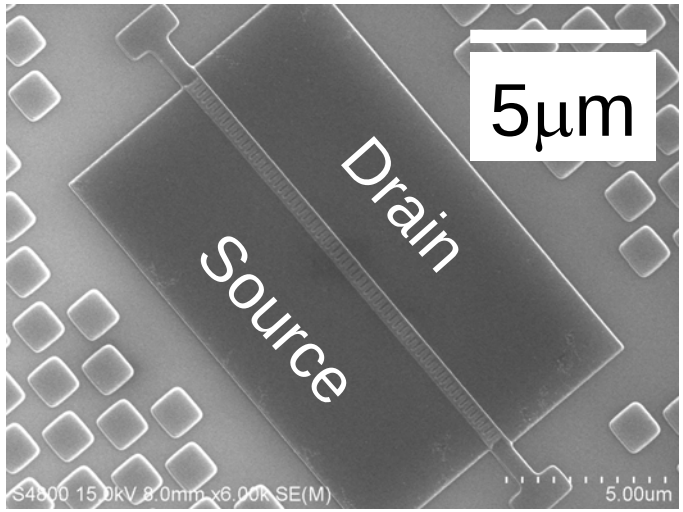
I_dV_g and I_dV_d Characteristics



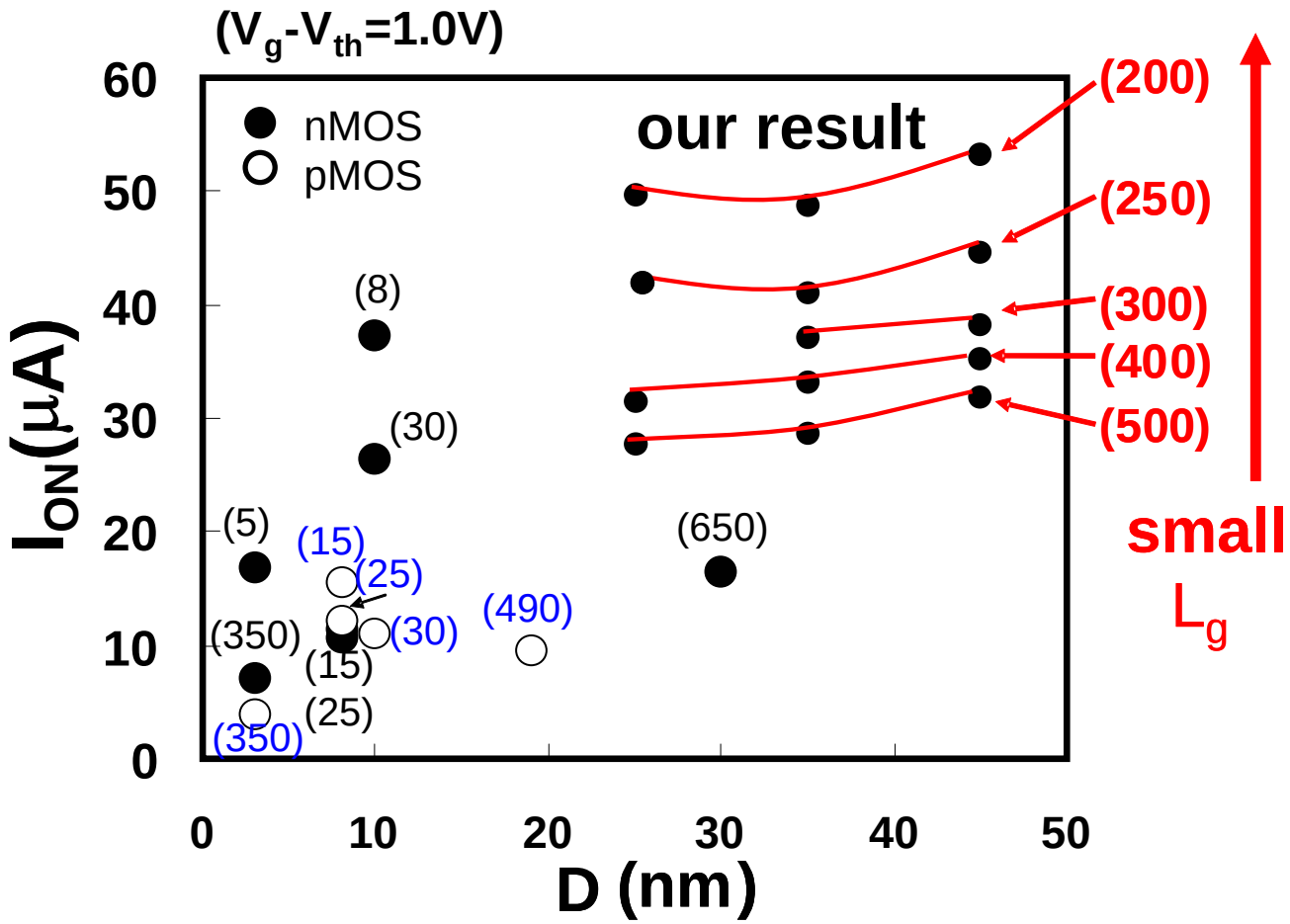
I_{on}/I_{off} ratio of ~10^7, high I_{on} of 49.6 μA/wire

Effective mobility extraction





Comparison of Si NW FET being already reported with Si NW FETs in this work



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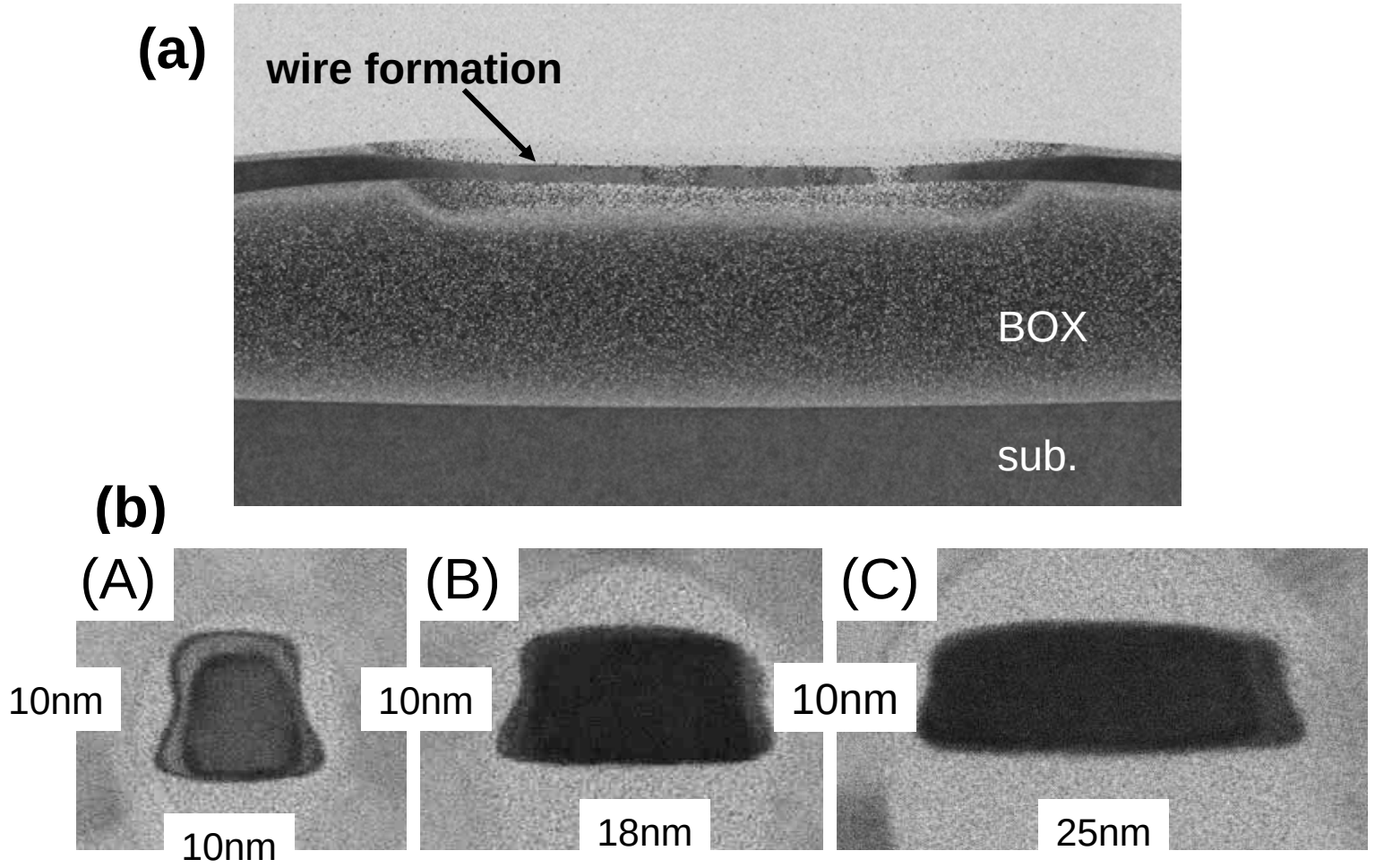
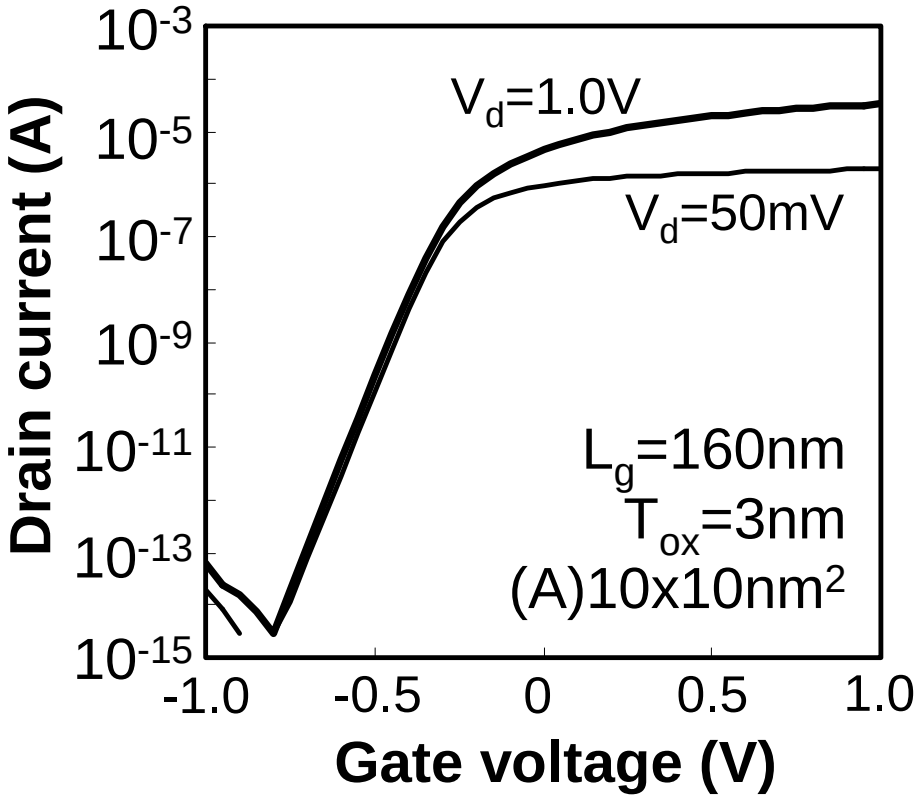
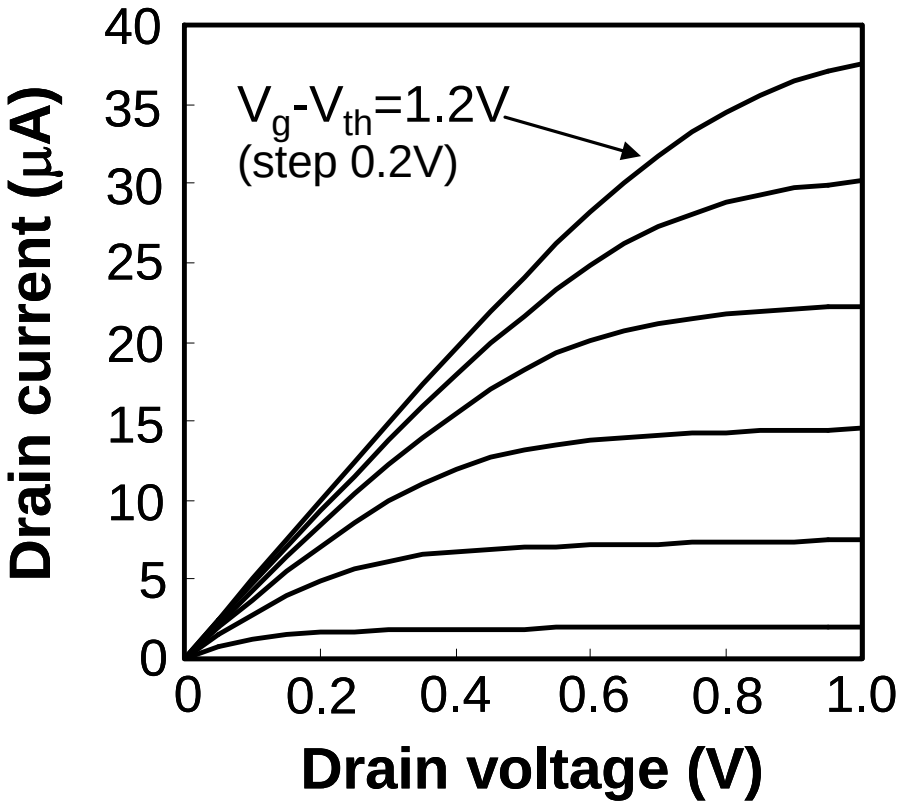
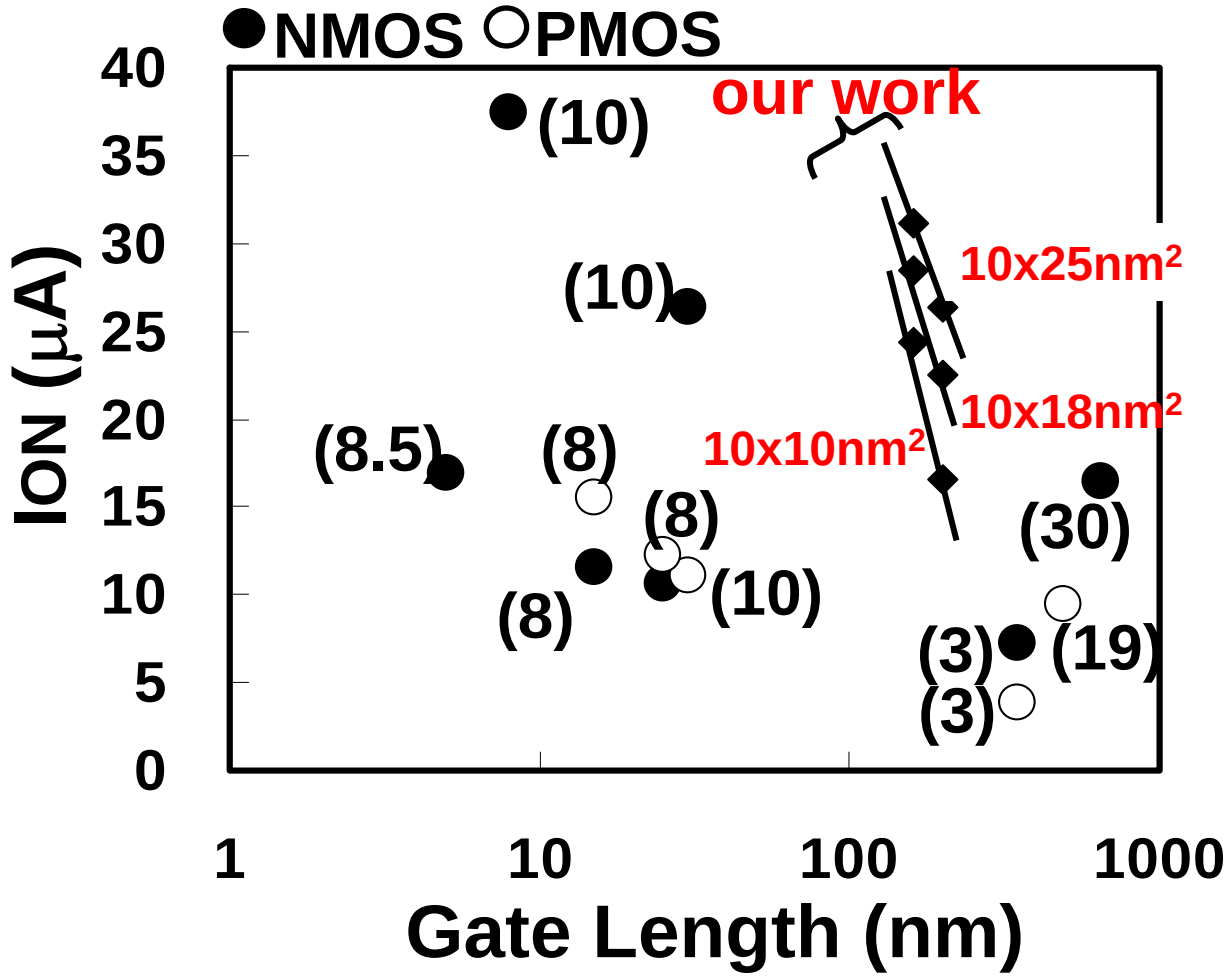

(a)
wire formation
BOX
sub.
(b)
(A)
10nm
10nm
(B)
10nm
18nm
(C)
10nm
25nm

Output characteristics of 10x10cm^2 SiNW FET



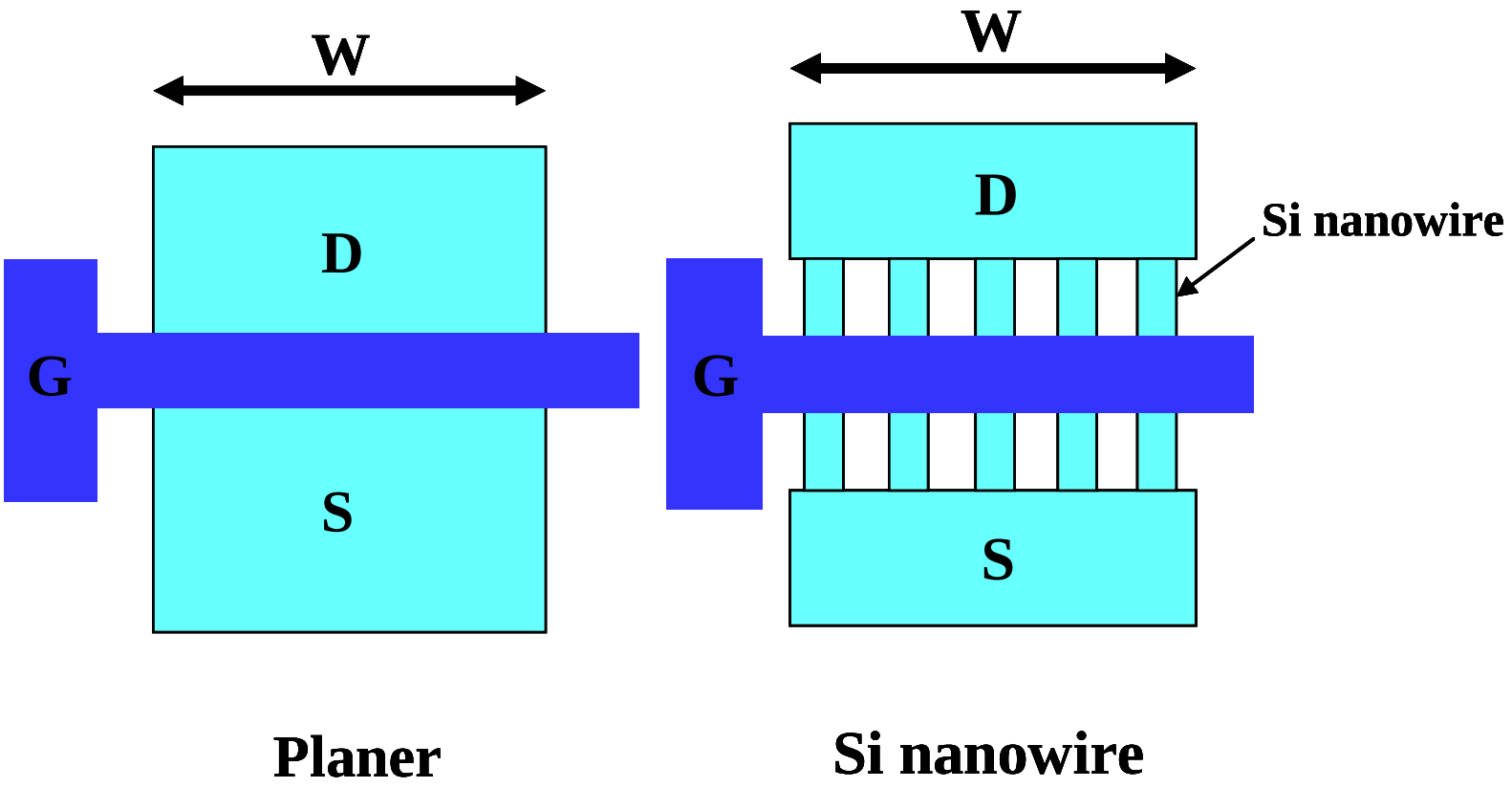


Obtained Ion with reported data

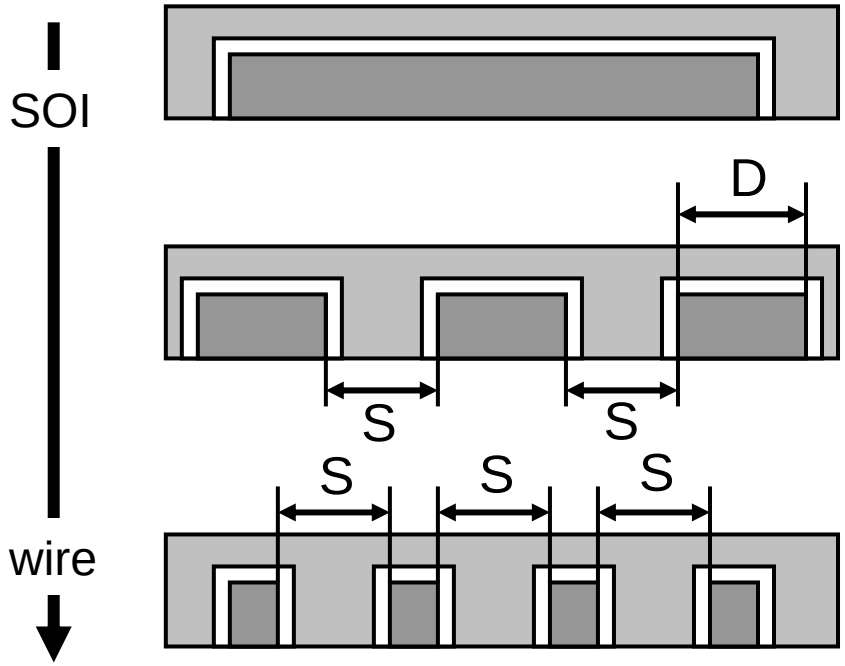


Even with large L_g, fairly nice I_{ON} have been achieved

Occupying area of Si bulk planar FET and Si NW FET.
Drive current should be compared with the same width, W



On current evaluation base on gate width



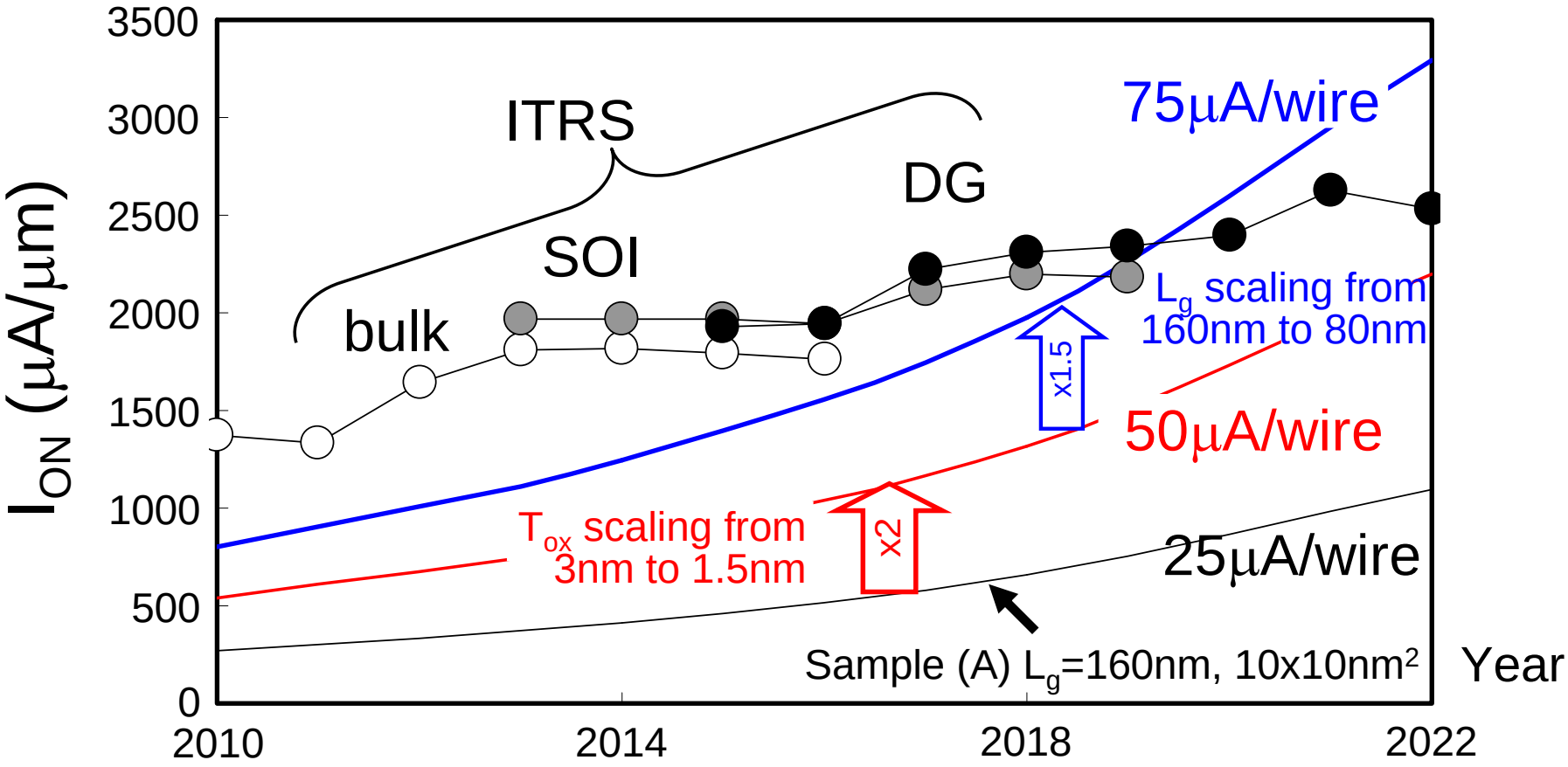
Year	half-pitch (nm), P
2010	45
2014	28
2018	18
2022	11

(based on ITRS2008update)

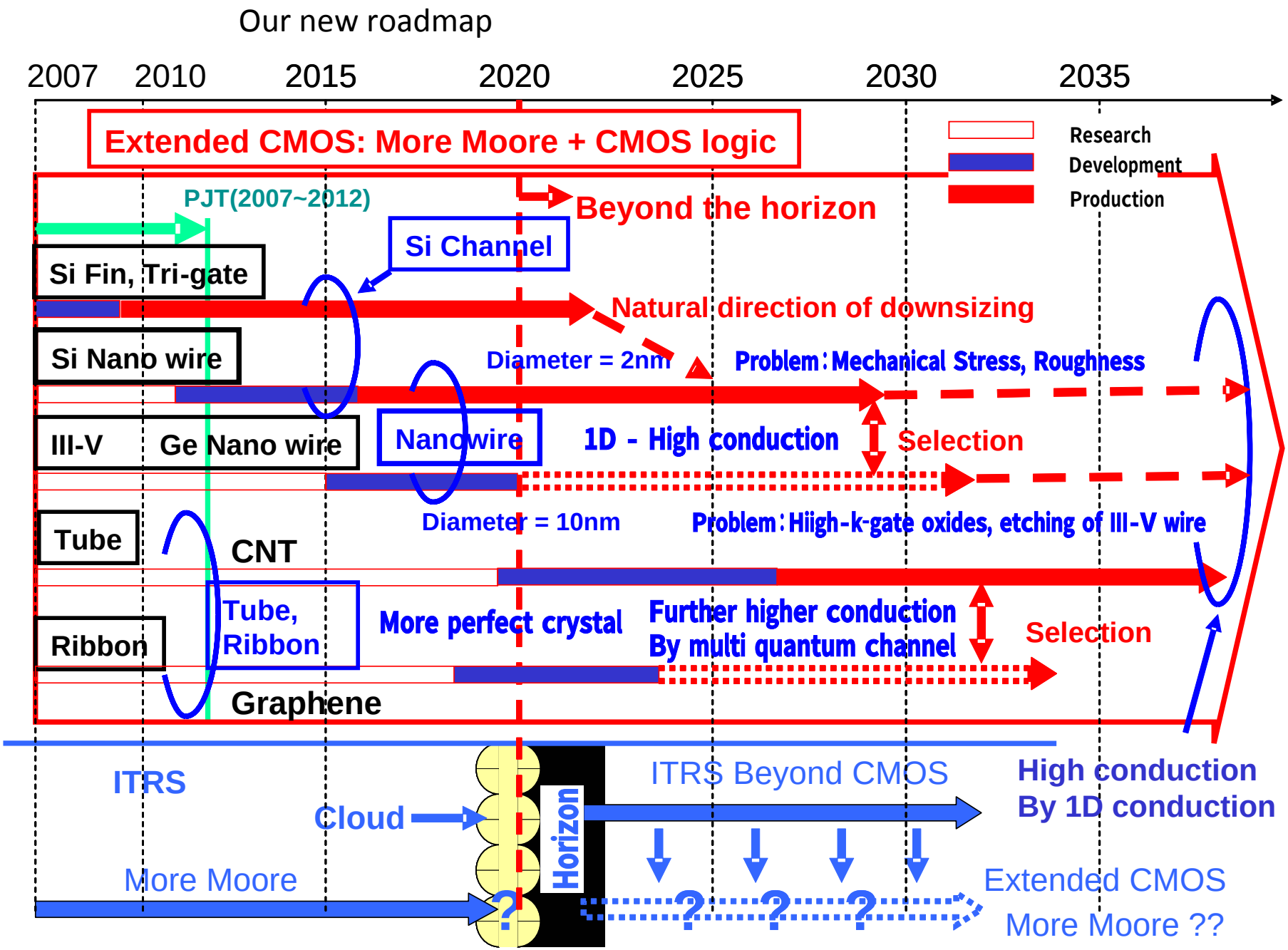
Numbers of wires are determined by the lithographic technology

$$\#N = \frac{1000(\text{nm})}{P} \quad \text{(at } D<P/2\text{)} \qquad \text{or} \qquad \frac{1000(\text{nm})}{D+P/2} \quad \text{(at } D>P/2\text{)}$$

Performance of SiNW FET in ITRS



With device scaling in T_{ox} and L_g, SiNW FET can exceed the required performance in ITRS


Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V
Ge Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Graphene
ITRS
Cloud
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
More Moore
?
?
?
?
Extended CMOS
More Moore ??

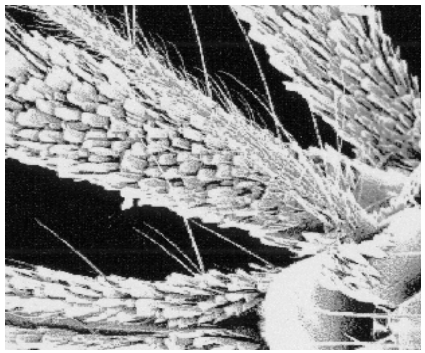
Brain

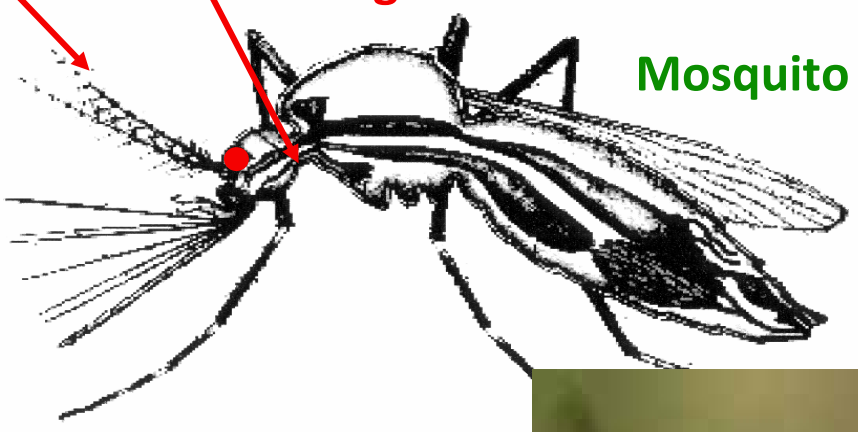
Ultra small volume
Small number of neuron cells
Extremely low power

Sensor

Infrared
Humidity
CO_2

Real time image processing
(Artificial) Intelligence
3D flight control





Mosquito

System and Algorism becomes more important!

But do not know how?

Dragonfly is further high performance

Thank you
for your attention!