Si Nanowire experiment

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Nanoelectronics Device Technology PJT
Study on Nano-wire FET 2.5 US$

Members

TIT: Iwai, Natori, Tsutsui, Kakushima, Parhat
Tsukuba Univ: Shiraishi, Oshiyama, Okada, Nomura
Waseda Univ: Yamada, Ohmori
- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

Source: 2008 ITRS Summer Public Conf.

* 5.5nm? was added by Iwai
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

- Reduction in $I_{off}$ ($I_{sd}$-leak)
  - Good control of $I_{sd}$-leak by surrounding gate

- Increase in $I_{on}$ ($I_{ds}$-sat)

Trade off

- Carrier scattering probability
  - Small
  - Large

- # of quantum channel
  - Small
  - Large

High Conduction (1D)

$G_0 = 77.8 \mu \text{S/wire}$

Multiple quantum channel (QC) used for conduction


Brief process flow of Si Nanowire FET

1. S/D&Fin Patterining (ArF Lithography and RIE Etching)
2. Sacrificial Oxidation & Oxide Removal (not completely released from BOX layer)
3. Nanowire Sidewall Formation (oxide support protector)
4. Gate Oxidation (5nm) & Poly-Si Deposition (75nm)
5. Gate Lithography & RIE Etching
6. Gate Sidewall Formation
7. Ni SALISIDE Process
(a) Fin structure formed on BOX layer. (b) XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

![Images showing the above descriptions]
(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.
(a) A cross sectional TEM image of Si NW FET in this work. Oxide support still remains thanks to nanowire sidewall (SiN). Semi-Around gate structure, nearby 300 degree of whose channel is surrounded by gate oxide and poly-Si electrode. Schematic illustration is shown in upper-right.
$D_W=25\text{nm}$ and $D_H=35\text{nm}$. Fairly nice $I_{on}/I_{off}$ ratio of $10^7$ with a low subthreshold slope of $71\text{mV/dec}$. has been obtained.
(a) Drain current dependence on Lg of different DW Si NW FETs per one nanowire

(b) Drain current dependence on Lg normalized by three surface width (left, right and top)
Comparison of Si NW FET being already reported with Si NW FETs in this work
Effective electron mobility of [110]-directed multi channel Si NW FET in this work. \((D_W=25\text{nm}, D_H=35\text{nm})\)
Occupying area of Si bulk planar FET and Si NW FET. Drive current should be compared with the same width, W.
Drive current comparison among NTRS 200nm phase, SOI planar FET in this work and estimated drive current of Si NW FET assumed that distance of Si NW FETs and the width of Si NW is equal.
Drive current estimation of multi-channel NWFET @ Lg=200nm, which is much larger than the physical gate length shown in ITRS 2007. Space between NW is half pitch in each technology node. The number of NW is calculated by a equation, 1000 / ( w+s ), where w is NW width 25nm and s is space. Blue rectangles are intended to be Si NWs.

<table>
<thead>
<tr>
<th>DRAM Half Pitch (nm)</th>
<th>Physical Gate Length (nm)</th>
<th>Schematic Illustration</th>
<th>Number of NW in 1µm</th>
<th>µA/µm (nanowire)</th>
</tr>
</thead>
<tbody>
<tr>
<td>45</td>
<td>18</td>
<td>![25 45 25 45 25 (nm)]</td>
<td>14</td>
<td>694</td>
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<tr>
<td>32</td>
<td>13</td>
<td>![25 32 25 32 25 (nm)]</td>
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<td>10</td>
<td>![25 25 25 (nm)]</td>
<td>20</td>
<td>992</td>
</tr>
</tbody>
</table>
DRAM half pitch in ITRS 2007 (left axis) and estimated drive current of Si NW FET ($L_g=200\text{nm}$, right axis) Blue line is drive current of SOI planar FET in this work
Conclusion

We have experimentally confirmed that Si nanowire FETs have superiority not only the suppression of off-leakage, but also on driving on-current.

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We have obtained the same conclusion for nanowire with 10 nm diameter.