G-COE Workshop on Nanoelectronics

Si Nanowire experiment

July 3, 2009,
at Dept. of Engineering, University of Cambridge
9. JJ Thomson Avenue, Cambridge CB3 0FA

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Tokyo Institute of Technology

METI (Ministry of Economy, Trade, and Industry)

NEDO (New Energy and Industrial Technology Development Organization)

Nanoelectronics Device Technology PJT

Study on Nano-wire FET 2.5 US$

Dec. 2007 – Mar. 2011

Members

TIT: Iwai, Natori, Tsutsui, Kakushima, Parhat

Tsukuba Univ: Shiraishi, Oshiyama, Okada, Nomura

Waseda Univ: Yamada, Ohmori

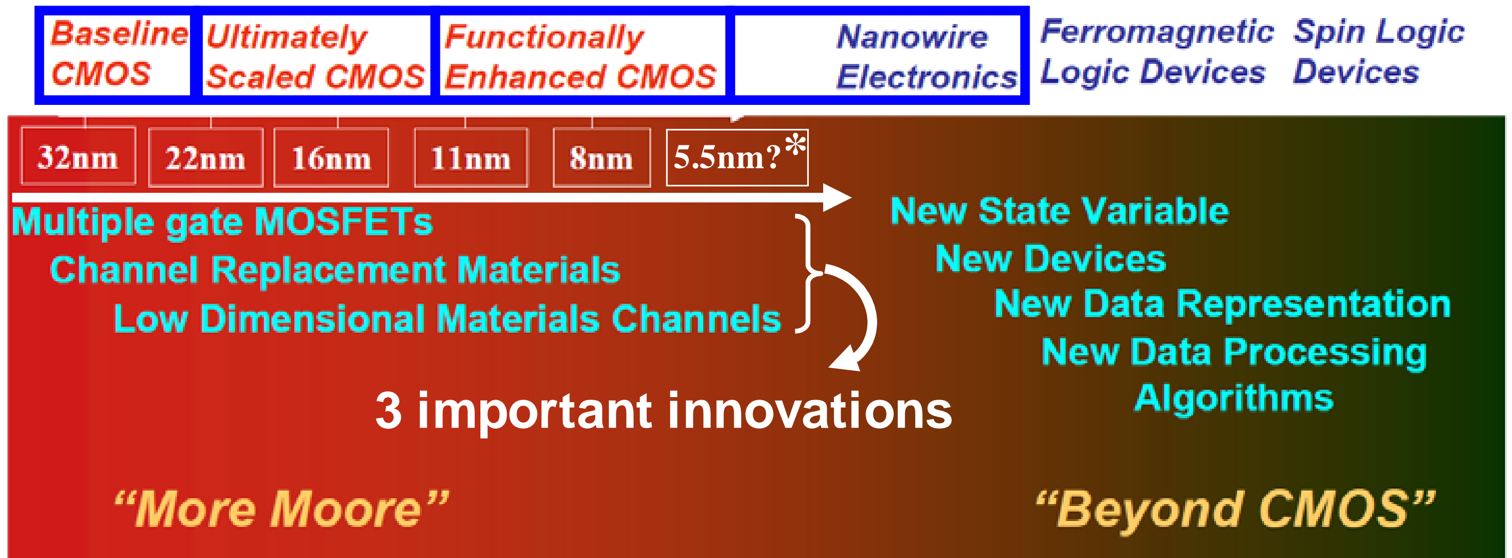
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



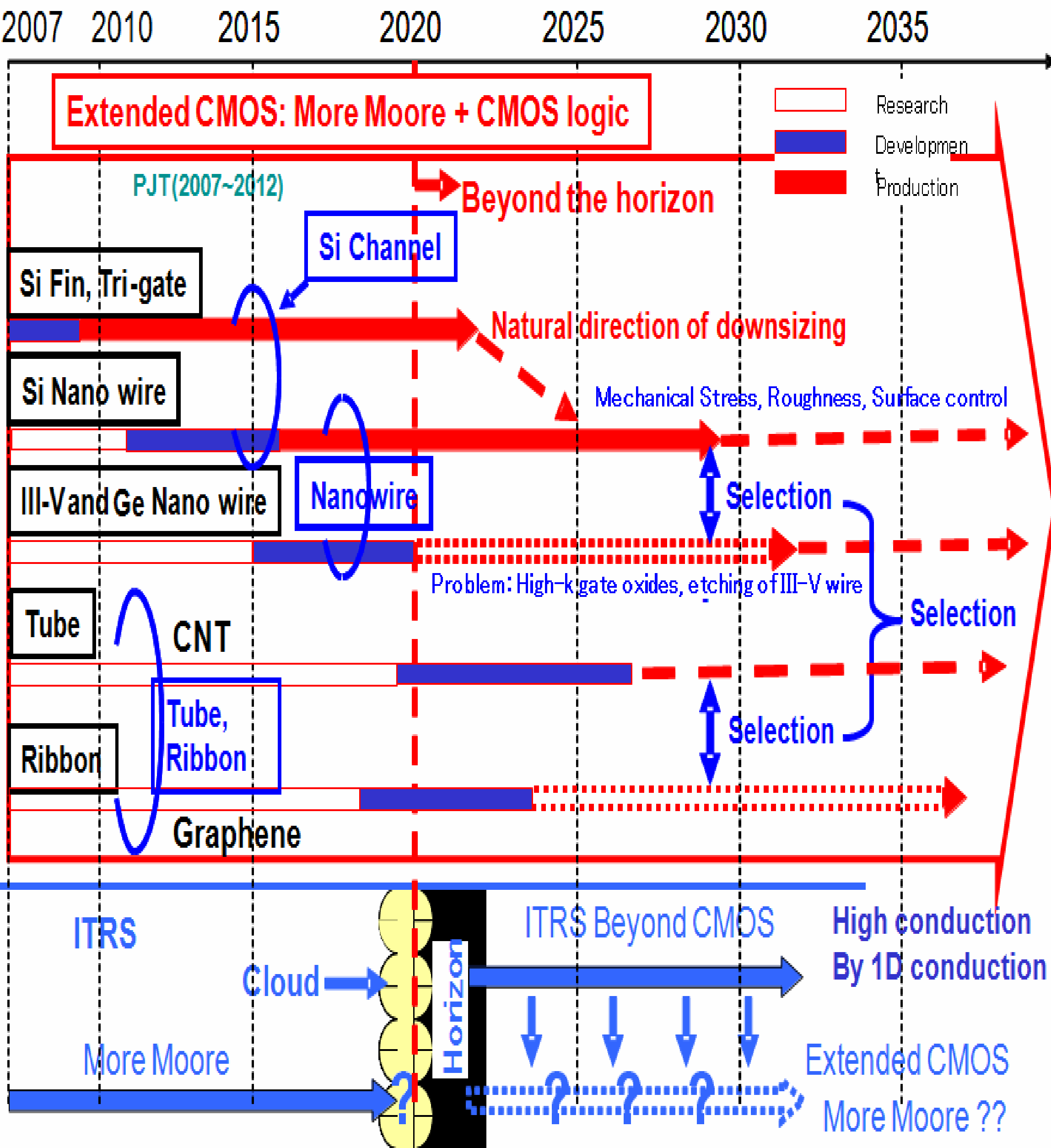
ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

*5.5nm? was added by Iwai

Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property
Source Drain contact
Optimization of wire diameter
Compact I-V model

III-V & Ge Nanowire

High-k gate insulator
Wire formation technique

CNT:

Growth and integration of CNT
Width and Chirality control
Chirality determines conduction types: metal or semiconductor

Graphene:

Graphene formation technique
Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap

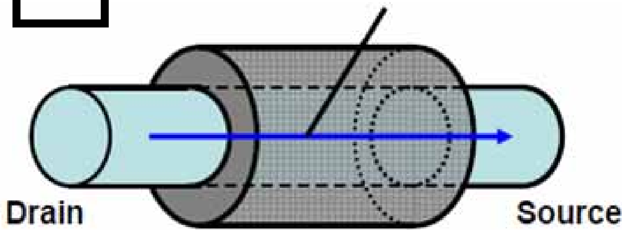
Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

Source: Y. Lee., T. Nagata., K. Kakushima., K. Shiraishi, and H. Iwai, IWDTF 2008, Tokyo, November, 2008

Reduction in Ioff (Isd-leak)

0



Good control of Isd-leak by surrounding gate

Trade off

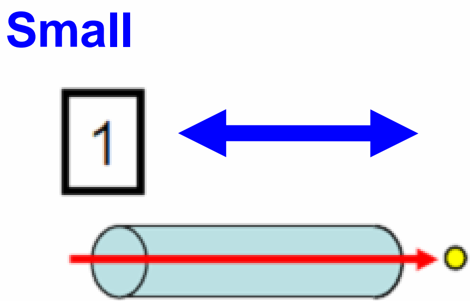
Carrier scattering probability

Small **Large**

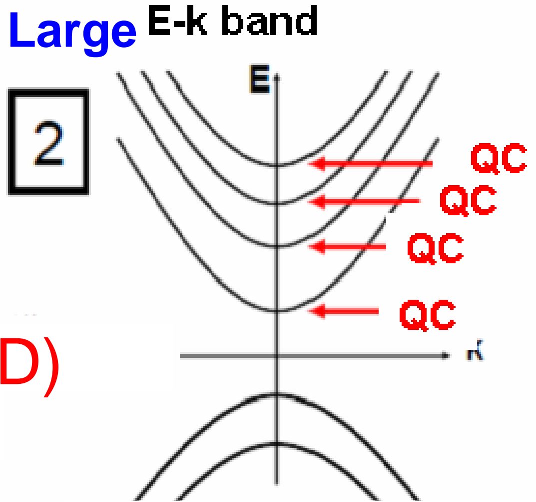
# of quantum channel

Small **Large**

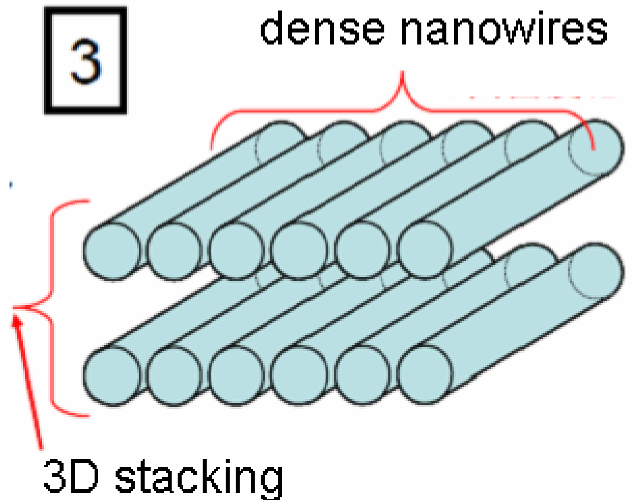
Increase in Ion (Id-sat)



High Conduction (1D)
Go=77.8μS/wire



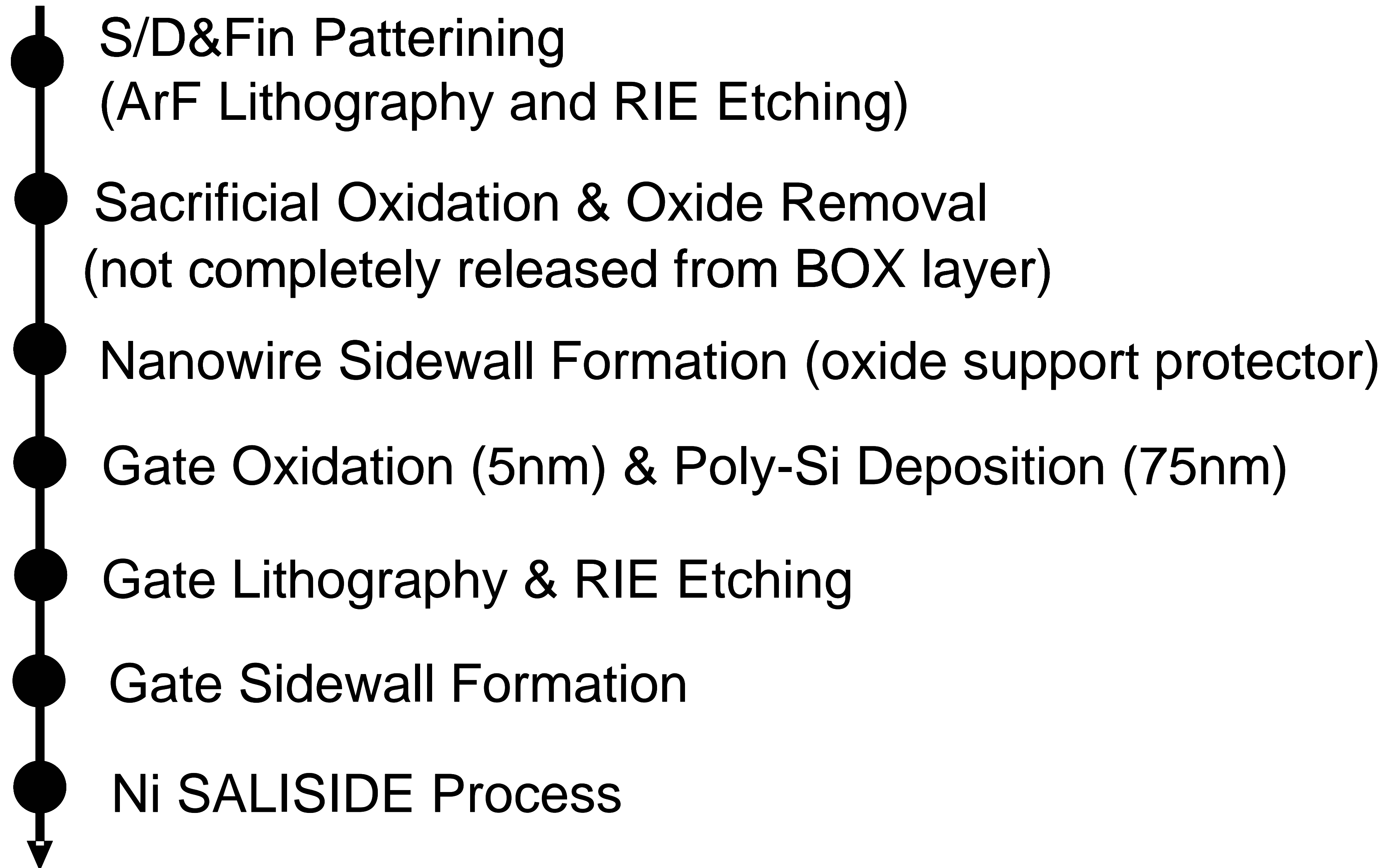
Multiple quantum channel (QC) used for conduction



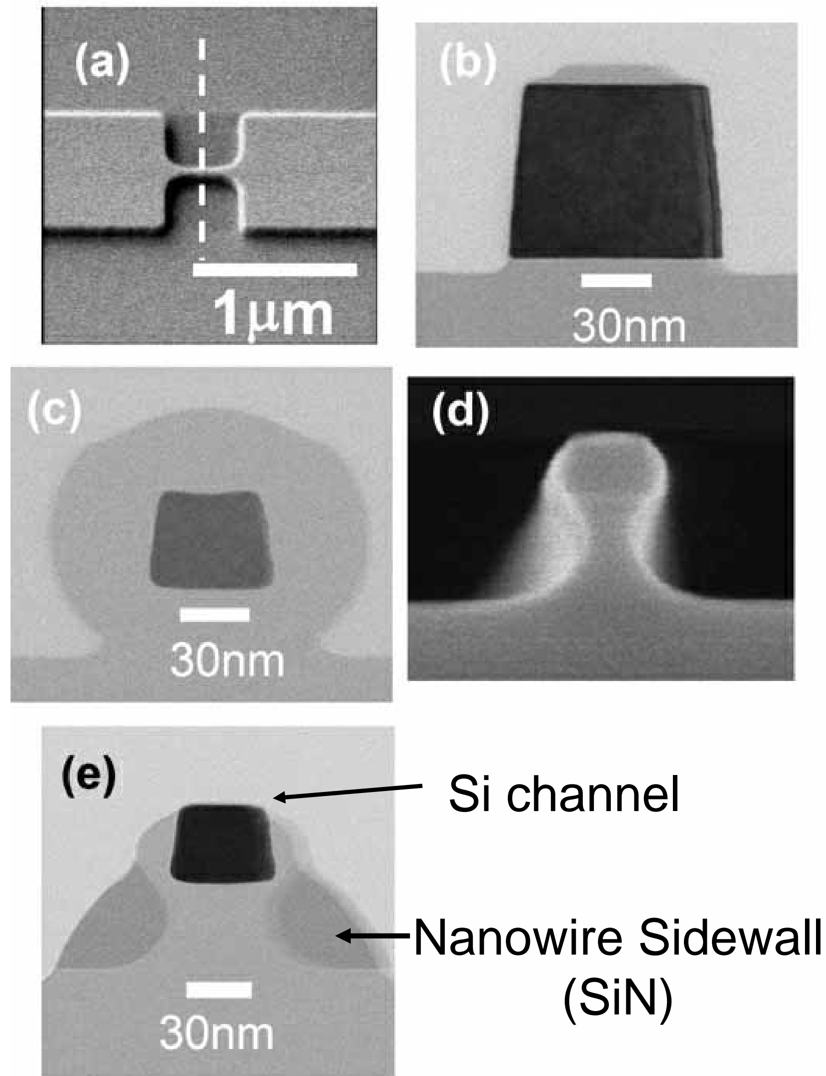
High-density lateral and vertical integration

Source: T. Ohno, K. Shiraishi, and T. Ogawa, Phys. Rev. Lett. ,1992

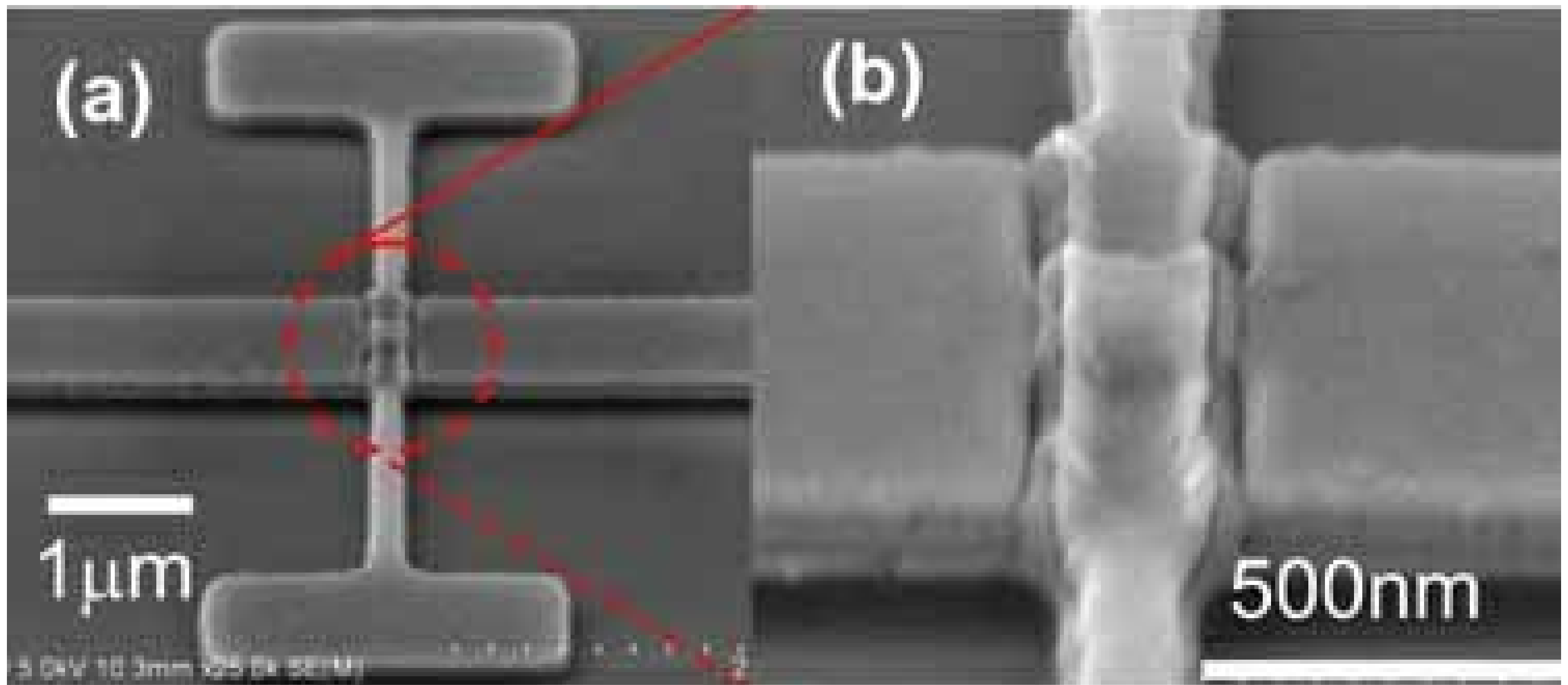
Brief process flow of Si Nanowire FET



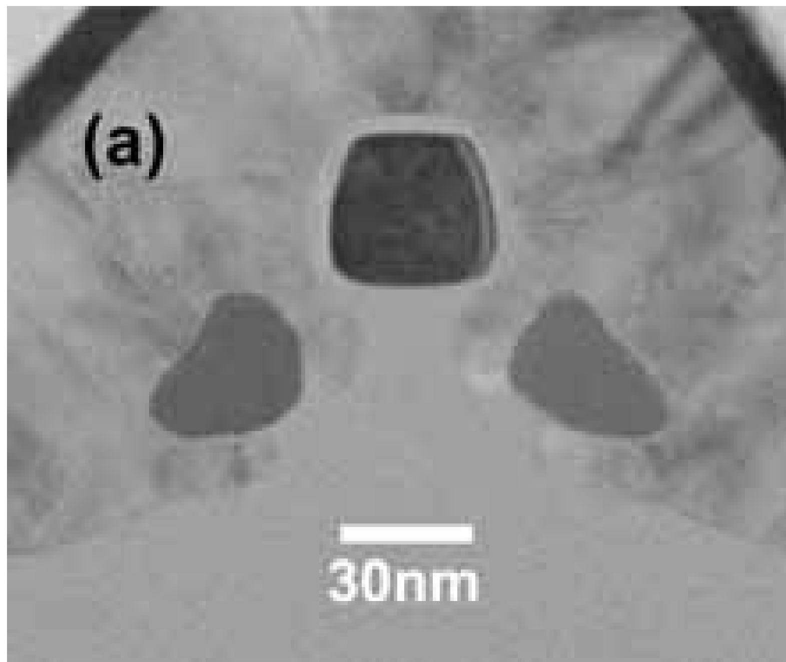
(a) Fin structure formed on BOX layer. (b)XTEM image of fin shown in (a) (c) XTEM image after sacrificial oxidation (d) Cross sectional SEM image after partial removal of sacrificial oxide (e) XTEM after nanowire sidewall formation

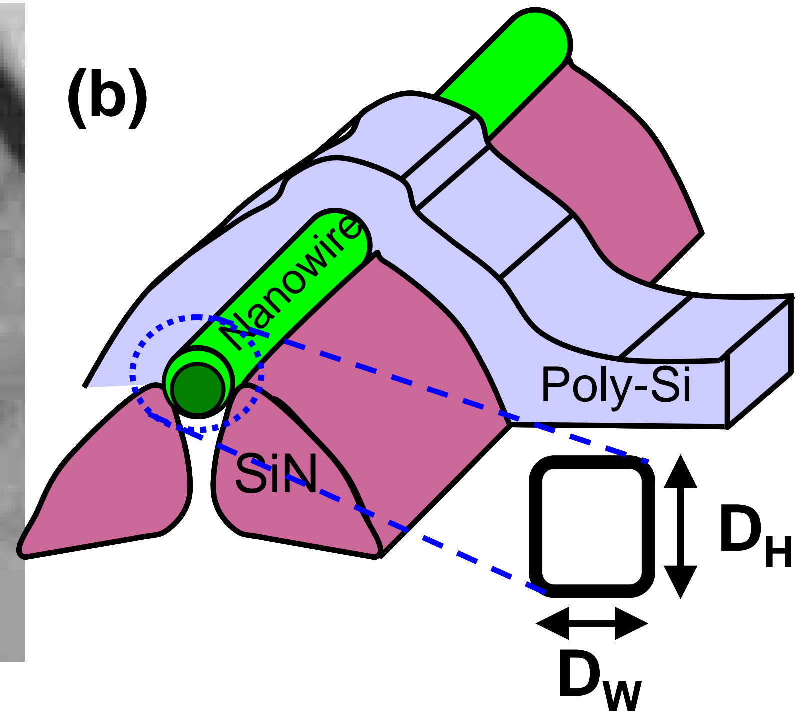


(a) SEM image of Si NW FET (Lg = 200nm)
(b) high magnification observation of gate and its sidewall.

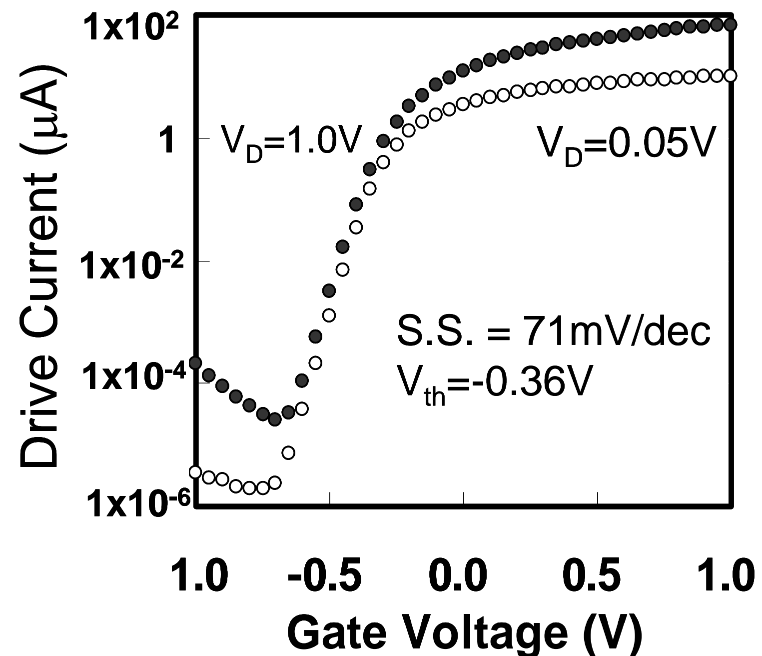


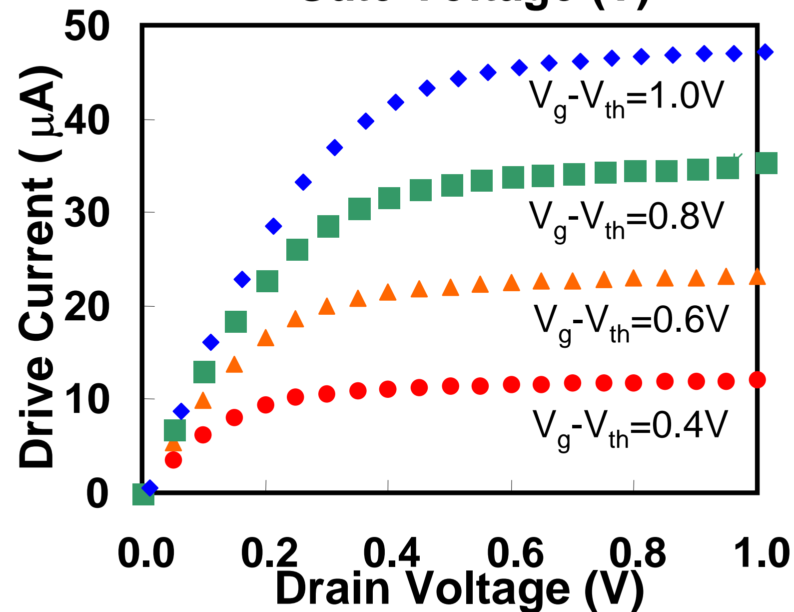
(a) A cross sectional TEM image of Si NW FET in this work. Oxide support still remains thanks to nanowire sidewall (SiN). Semi-Around gate structure, nearby 300 degree of whose channel is surrounded by gate oxide and poly-Si electrode. Schematic illustration is shown in upper-right.





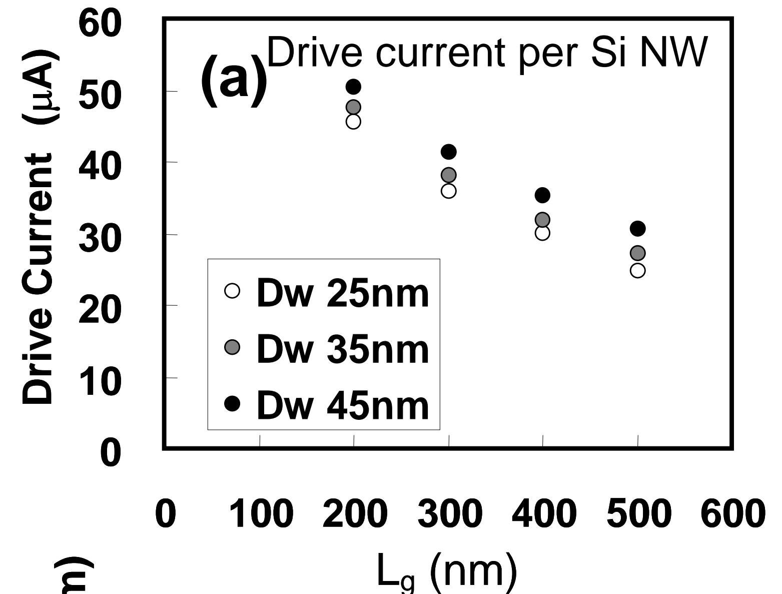
D_W=25nm and D_H=35nm.
Fairly nice I_{on}/I_{off} ratio of 10^7 with a low subthrshold slope of 71mV/dec. has been obtained.

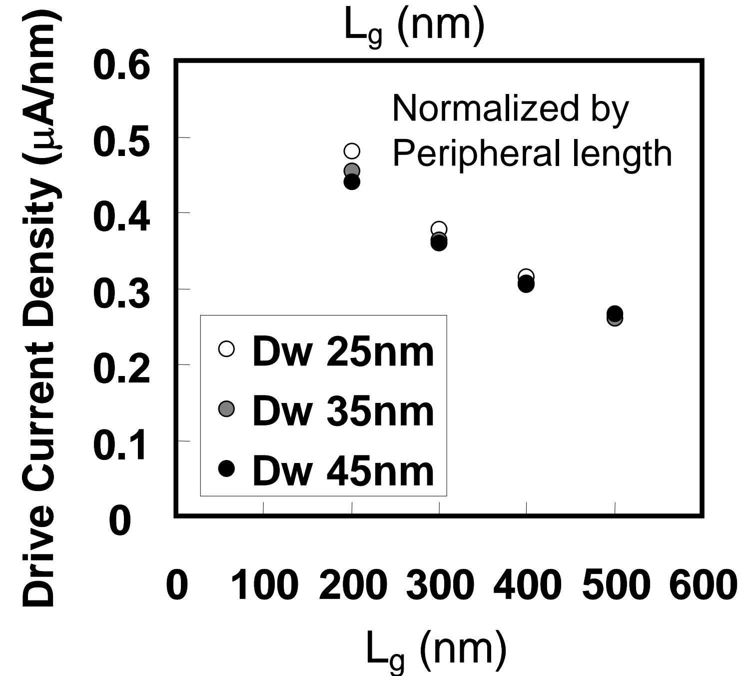




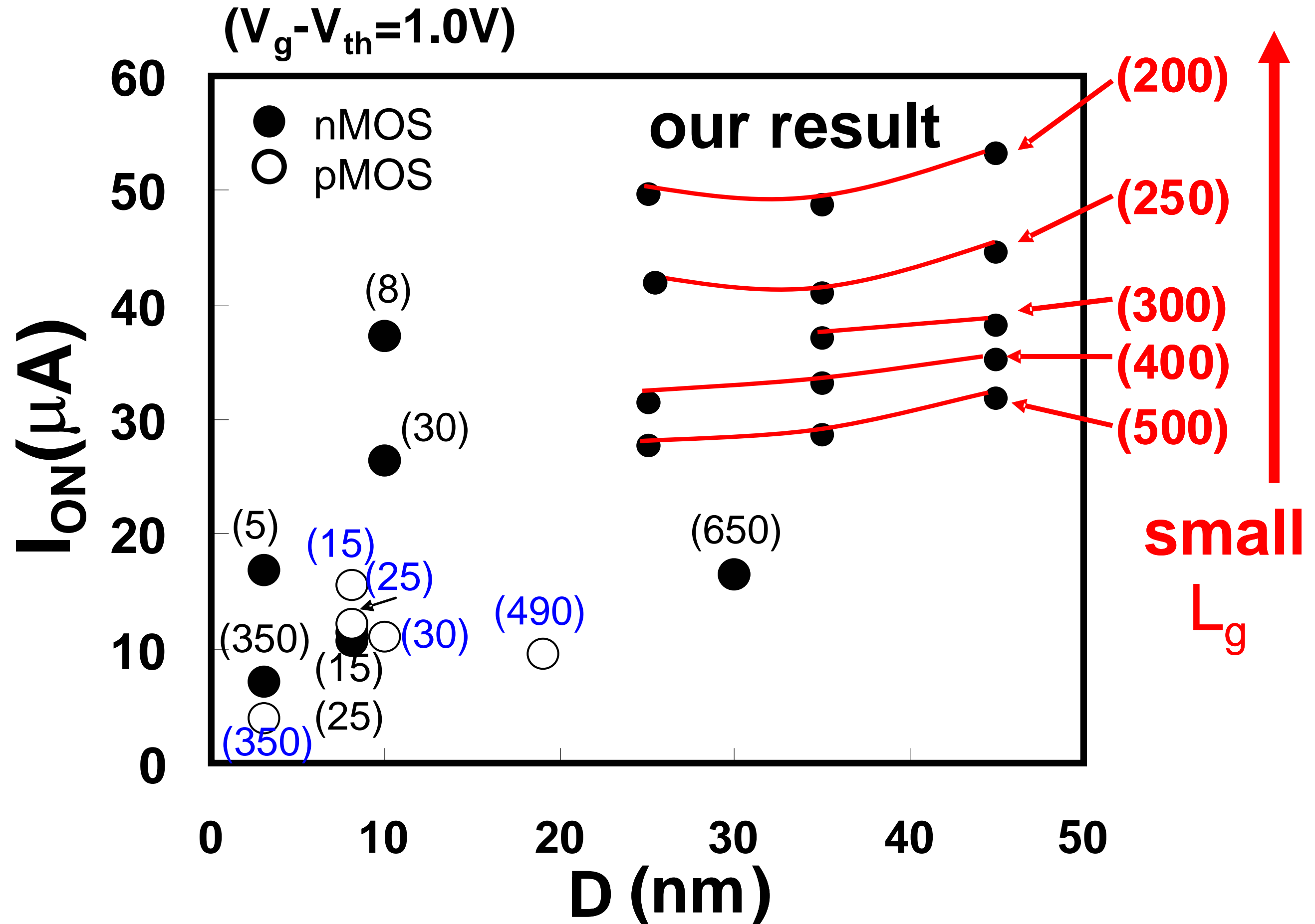
(a) Drain current dependence on Lg of different DW Si NW FETs per one nanowire

(b) Drain current dependence on Lg normalized by three surface width (left, right and top)

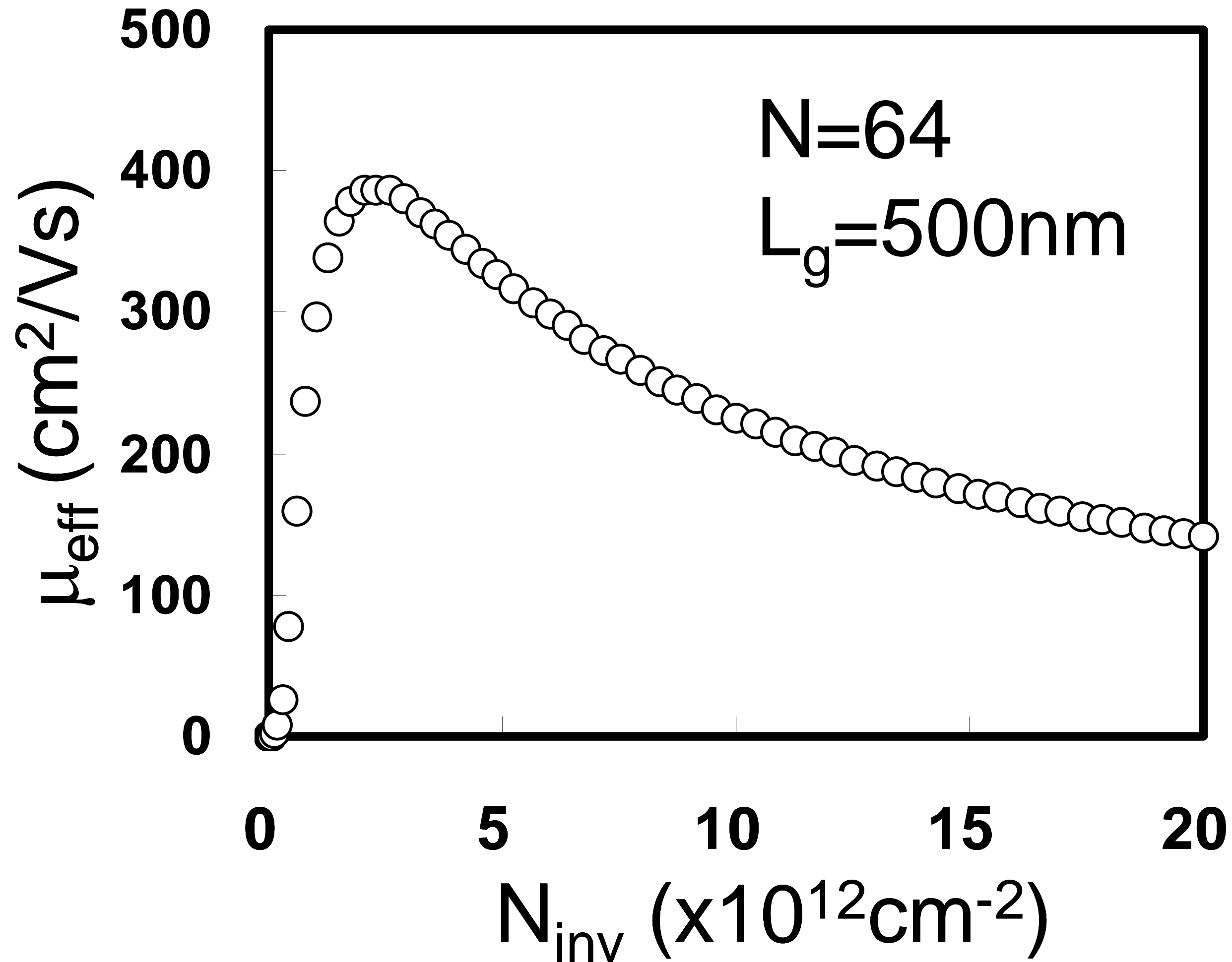




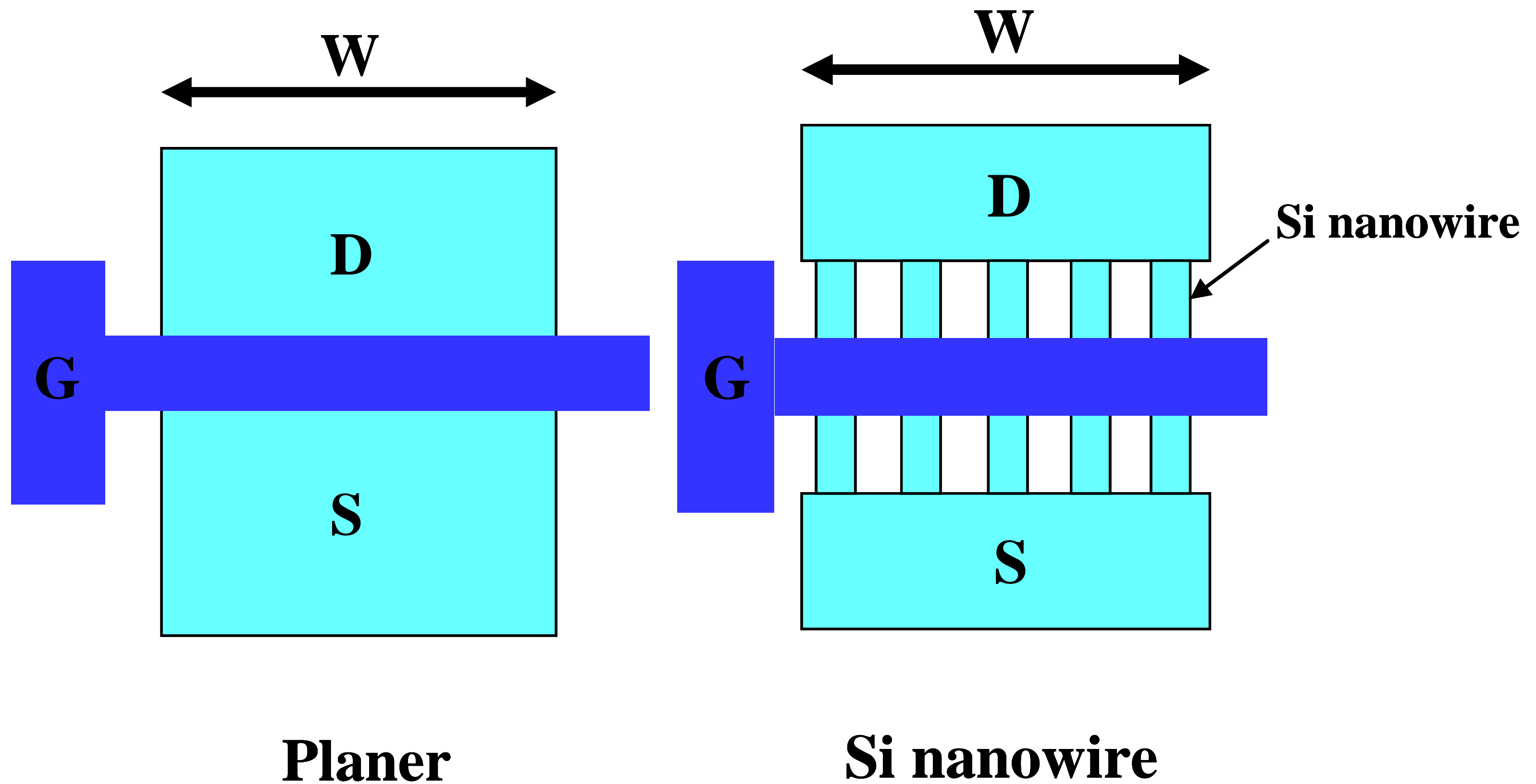
Comparison of Si NW FET being already reported with Si NW FETs in this work



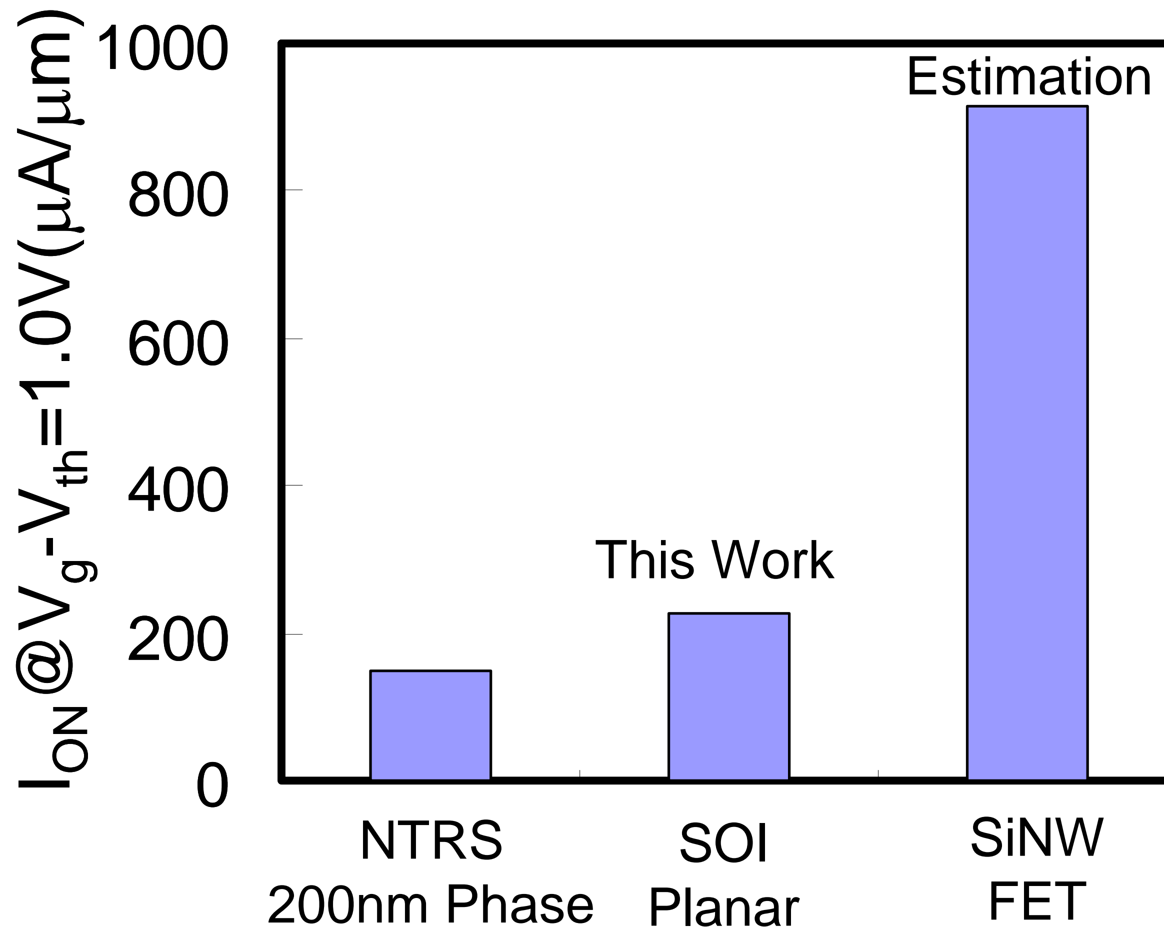
Effective electron mobility of [110]-directed multi channel Si NW FET in this work. (D_W=25nm, D_H=35nm)



Occupying area of Si bulk planar FET and Si NW FET.
Drive current should be compared with the same width, W



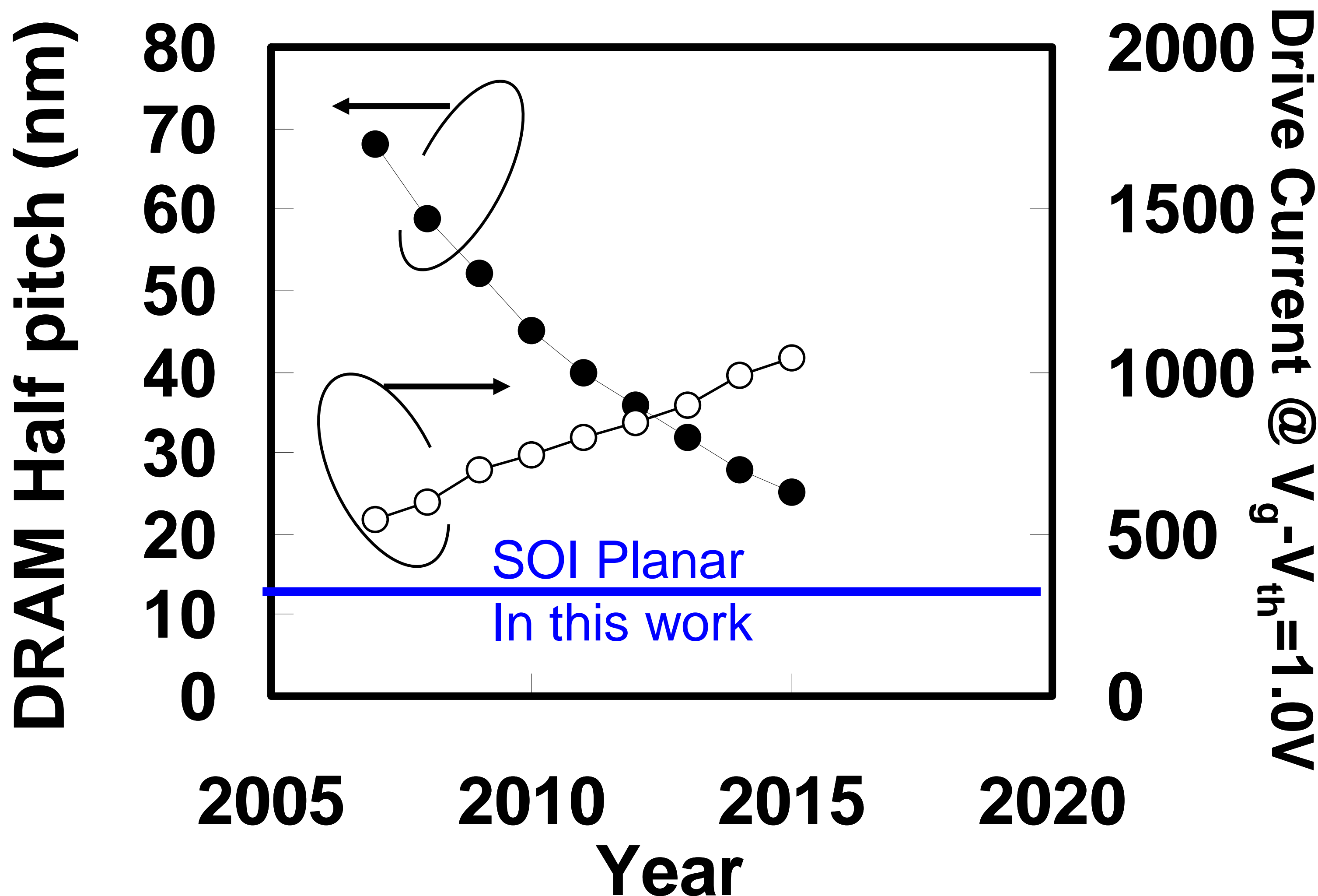
Drive current comparison among NTRS 200nm phase, SOI planar FET in this work and estimated drive current of Si NW FET assumed that distance of Si NW FETs and the width of Si NW is equal



Drive current estimation of multi-channel NWFET @ Lg=200nm, which is much larger than the physical gate length shown in ITRS 2007. Space between NW is half pitch in each technology node. The number of NW is calculated by a equation, 1000 / (w+s), where w is NW width 25nm and s is space. Blue rectangles are intended to be Si NWs

DRAM Half Pitch (nm)	**Physical Gate Length(nm)**	Schematic Illustration	**Number of NW in 1μm**	μA/μm (nanowire)
45	18	25 ←45→ 25 ←45→ 25 (nm)	14	694
32	13	25 ←32→ 25 ←32→ 25 (nm)	17	843
25	10	25 ←25→ 25 ←25→ 25 (nm)	20	992

DRAM half pitch in ITRS 2007 (left axis) and estimated drive current of Si NW FET (L_g=200nm, right axis) Blue line is drive current of SOI planar FET in this work



Conclusion

We have experimentally confirmed
that Si nanowire FETs have superiority
not only the suppression of off-leakage,
but also on driving on-current.

This is published at ESSDERC 2009

We have obtained the same conclusion
for nanowire with 10 nm diamenter