Past and Future of Integrated Circuits Technology

June 3, 2009

@WIMNACT, Himalaya Hotel
Kathmandu, Nepal

Hiroshi Iwai,
Tokyo Institute of Technology
Founded in 1881, Promoted to Univ. 1929
<table>
<thead>
<tr>
<th>Category</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Income</td>
<td>371M $</td>
</tr>
<tr>
<td>Sponsored Research</td>
<td>100M $</td>
</tr>
<tr>
<td>Employee (incl. Faculty)</td>
<td>1770</td>
</tr>
<tr>
<td>Faculty</td>
<td>729</td>
</tr>
<tr>
<td>Graduate student</td>
<td>4903</td>
</tr>
</tbody>
</table>

Year 2003
Total 982
(As of May. 1, 2005)
Tokyo Institute of Technology

Interdisciplinary Graduate School of Science and Engineering

Dept. of Electronics and Physics

5 other schools

4 Laboratories

Frontier Research Center

GCEO (Global Center of Excellence) for Photonics Nanodevice Integration Engineering

5000 Undergraduate students

5000 Graduate Students

2 major campuses

Ookayama, Tokyo

Suzukakedai, Yokohama

10 other dept.

Consists of about 10 professor who have big projects

Consists of 5 EE Related departments

Innovation Research Initiatives (革新的的研究集団）
Welcome to Iwai Lab.

岩井研究室 ~Iwai Lab.~

ご挨拶

・最近の研究テーマ

SIデバイスの重要性

近年のSIデバイスの重要性をランダムに選択します。

微細化限界打破の手法

新素材 high-k/metal ゲートスタック構造

異種材料の導入による新しい展開の可能性

新プロセス プラスマドーピング技術、メタルS/D

技術的なプレースリューが期待できる新しいプロセス

新構造 SiNanowire トランジスタ

超高速、高密度、機能化デバイスの実現

EMアシナジング技術 GeMOSFET、CNTデバイス

SIデバイス S2価段回路への融合

High-k/metalゲートスタック

直接トランジスタ流は低く実効容量率は大きく！

次世代ゲート絶縁体材料として

La2O3に注目

岩井研究室で検討してきた材料

SiO2 Gate Large leakage

Gate

High-k

Gate

Small leakage

Large capacitance

Gate

High-k

Gate

Small leakage

Large capacitance

材料の選択

ゲート材料の選択

高k材料の選択

XPS measurement by Prof. T. Hattoi, INFOS 2003

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

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Dielectric Constant (DC)

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SiO2

Dielectric Constant (DC)

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Dielectric Constant (DC)

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Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)

0 10 20 30 40 50

SiO2

Dielectric Constant (DC)
• There were many inventions in the 20\textsuperscript{th} century: Airplane, Nuclear Power generation, Computer, Space aircraft, etc
• However, everything has to be controlled by electronics
• Electronics
  Most important invention in the 20\textsuperscript{th} century
• What is Electronics: To use electrons, Electronic Circuits
Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias

Same mechanism as that of transistor
4 wives of Lee De Forest

1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress
First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device

Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption
History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor: 
   Ge Semiconductor, Bardeen, Brattin  
   → Nobel Prize

1948, 1st Junction Bipolar Transistor, 
   Ge Semiconductor, Schokley  
   → Nobel Prize

1958, 1st Integrated Circuits, 
   Ge Semiconductor, J.Kilby  → Nobel Prize

1959, 1st Planar Integrated Circuits, 
   R.Noice

1960, 1st MOS Transistor, Kahng, 
   Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass
J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928
Capacitor structure with notch

**Negative bias**

- Gate Electrode
- Gate Insulator
- Semiconductor
- Electron

No current

**Positive bias**

- Electric field

Current flows
Surface Potential (Negative direction)

0 bias for gate

Positive bias for gate

Electron flow

Source Channel Drain

Gate electrode
Gate Oxid

S G D

1V
N-Si

0V
N^+ -Si

N-Si

P-Si
However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!
Very bad interface property between the semiconductor and gate insulator.

Drain Current was several orders of magnitude smaller than expected.

Even Shockley!
However, they found amplification phenomenon when investigating Ge surface when putting needles. This is the 1st Transistor:

Not Field Effect Transistor, 
But Bipolar Transistor (another mechanism)

**1947: 1st transistor**

J. Bardeen  
W. Bratten,

Bipolar using Ge  
W. Shockley
1958: 1st Integrated Circuit

Connect 2 bipolar transistors in the Same substrate by bonding wire.
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Si
Source

Drain

Al Gate

Si

Si/SiO₂ Interface is extraordinarily good
1970,71: 1st generation of LSIs

DRAM   Intel 1103

MPU     Intel 4004
MOS LSI experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Decade</th>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s</td>
<td>IC (Integrated Circuits)</td>
<td>~ 10</td>
</tr>
<tr>
<td>1970s</td>
<td>LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s</td>
<td>VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s</td>
<td>ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s</td>
<td>?LSI (? Large Scale IC)</td>
<td>~1,000,000,000</td>
</tr>
</tbody>
</table>
MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching

N-MOS (N-type MOSFET)
N-MOS
(N-type MOSFET)

N-type MOSFET

Source

Drain

Electron flow

Current flow

P-MOS
(P-type MOSFET)

P-type MOSFET

Source

Drain

Hole flow

Current flow
n-MOSFET

OFF

Gate

Source 0 V

Drain 1 V

Electrons

n-MOSFET

ON

Gate

Source 1 V

Drain 1 V

Electron flow

High Potential Region
n-MOSFET

- Positive gate bias
- Drain current increases with positive voltage
- Threshold voltage
- OFF state: 0V, 0A
- ON state: positive voltage, positive current

p-MOSFET

- Negative gate bias
- Drain current decreases with negative voltage
- Threshold voltage
- OFF state: negative voltage, 0A
- ON state: 0V, positive current
CMOS

Complimentary MOS

Inverter

PMOS

NMOS

When NMOS is ON, PMOS is OFF
When PMOS is ON, NMOS is OFF
CMOS: Low Power: No DC current from Power supply to the ground

\[ V_D \]

1 cycle

\[ P = \frac{1}{2} CV_D^2 \]

Clock frequency \( f \)

\[ P = \frac{1}{2} fCV_D^2 \]
2 input NAND Circuit

AND
Input 1 1 1 0 0
Input 2 1 0 1 0
Output 1 0 0 0

NAND = NOT \cdot AND
Input 1 1 1 0 0
Input 2 1 0 1 0
Output 0 1 1 1
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:
There is no computer in banks, and
world economical activities immediately stop.

Cellarer phone dose not exists
Downsizing of the components has been the driving force for circuit evolution.

<table>
<thead>
<tr>
<th>Year</th>
<th>Vacuum Tube</th>
<th>Transistor</th>
<th>IC</th>
<th>LSI</th>
<th>ULSI</th>
</tr>
</thead>
<tbody>
<tr>
<td>1900</td>
<td>10 cm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1950</td>
<td>cm</td>
<td>10 cm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1960</td>
<td>mm</td>
<td>10 µm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1970</td>
<td>100 nm</td>
<td>10⁻⁷m</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td>10⁻⁻³m</td>
<td>10⁻⁻⁵m</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. **Reduce Capacitance**
   - Reduce switching time of MOSFETs
   - Increase clock frequency
     - Increase circuit operation speed

2. **Increase number of Transistors**
   - Parallel processing
     - Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

Thus, downsizing of Si devices is the most important and critical issue.
Scaling Method: by R. Dennard in 1974

$W_{dep}$: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed Otherwise, large leakage between S and D

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

$X, Y, Z: K$, $V: K$, $Na: 1/K$

By the scaling, $W_{dep}$ is suppressed in proportion, and thus, leakage can be suppressed.

$W_{dep} \propto \sqrt{V/Na}$

K=0.7 for example

Good scaled I-V characteristics
<table>
<thead>
<tr>
<th>Geometry &amp; Supply voltage</th>
<th>L&lt;sub&gt;G&lt;/sub&gt;, W&lt;sub&gt;G&lt;/sub&gt;</th>
<th>K</th>
<th>Scaling K : K=0.7 for example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drive current in saturation</td>
<td>I&lt;sub&gt;d&lt;/sub&gt;</td>
<td>K</td>
<td>I&lt;sub&gt;d&lt;/sub&gt; = v&lt;sub&gt;sat&lt;/sub&gt;W&lt;sub&gt;G&lt;/sub&gt;C&lt;sub&gt;o&lt;/sub&gt; (V&lt;sub&gt;G&lt;/sub&gt;-V&lt;sub&gt;th&lt;/sub&gt;) C&lt;sub&gt;o&lt;/sub&gt; : gate C per unit area</td>
</tr>
<tr>
<td>I&lt;sub&gt;d&lt;/sub&gt; per unit W&lt;sub&gt;G&lt;/sub&gt;</td>
<td>I&lt;sub&gt;d&lt;/sub&gt;/µm</td>
<td>1</td>
<td>I&lt;sub&gt;d&lt;/sub&gt; per unit W&lt;sub&gt;G&lt;/sub&gt; = I&lt;sub&gt;d&lt;/sub&gt;/W&lt;sub&gt;G&lt;/sub&gt; = 1</td>
</tr>
<tr>
<td>Gate capacitance</td>
<td>C&lt;sub&gt;g&lt;/sub&gt;</td>
<td>K</td>
<td>C&lt;sub&gt;g&lt;/sub&gt; = ε&lt;sub&gt;o&lt;/sub&gt;ε&lt;sub&gt;ox&lt;/sub&gt;L&lt;sub&gt;G&lt;/sub&gt;W&lt;sub&gt;G&lt;/sub&gt;/t&lt;sub&gt;ox&lt;/sub&gt; KK/K = K</td>
</tr>
<tr>
<td>Switching speed</td>
<td>τ</td>
<td>K</td>
<td>τ = C&lt;sub&gt;g&lt;/sub&gt;V&lt;sub&gt;dd&lt;/sub&gt;/I&lt;sub&gt;d&lt;/sub&gt; KK/K = K</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>f</td>
<td>1/K</td>
<td>f = 1/τ = 1/K</td>
</tr>
<tr>
<td>Chip area</td>
<td>A&lt;sub&gt;chip&lt;/sub&gt;</td>
<td>α</td>
<td>α: Scaling factor In the past, α&gt;1 for most cases</td>
</tr>
<tr>
<td>Integration (# of Tr)</td>
<td>N</td>
<td>α/K&lt;sup&gt;2&lt;/sup&gt;</td>
<td>N → α/K&lt;sup&gt;2&lt;/sup&gt; = 1/K&lt;sup&gt;2&lt;/sup&gt;, when α=1</td>
</tr>
<tr>
<td>Power per chip</td>
<td>P</td>
<td>α</td>
<td>fNCV&lt;sup&gt;2&lt;/sup&gt;/2 → K&lt;sup&gt;-1&lt;/sup&gt;(αK&lt;sup&gt;-2&lt;/sup&gt;)K (K&lt;sup&gt;1&lt;/sup&gt;)&lt;sup&gt;2&lt;/sup&gt; = α = 1, when α=1</td>
</tr>
</tbody>
</table>

Downscaling merit: Beautiful!
<table>
<thead>
<tr>
<th>k= 0.7 and α =1</th>
<th>k= 0.7² =0.5 and α =1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Single MOFET</strong></td>
<td><strong>Chip</strong></td>
</tr>
<tr>
<td>Vdd → 0.7</td>
<td>N (# of Tr) → 1/0.7² = 2</td>
</tr>
<tr>
<td>Lg → 0.7</td>
<td>f (Clock) → 1/0.7 = 1.4</td>
</tr>
<tr>
<td>Id → 0.7</td>
<td>P (Power) → 1</td>
</tr>
<tr>
<td>Cg → 0.7</td>
<td>τ (Switching time) → 0.7</td>
</tr>
<tr>
<td>P (Power)/Clock → 0.7³ = 0.34</td>
<td>N (# of Tr) → 1/0.5² = 4</td>
</tr>
<tr>
<td></td>
<td>f (Clock) → 1/0.5 = 2</td>
</tr>
</tbody>
</table>

Vdd → 0.5
Lg → 0.5
Id → 0.5
Cg → 0.5
P (Power)/Clock → 0.5³ = 0.125
τ (Switching time) → 0.5

N (# of Tr) → 1/0.7² = 2
f (Clock) → 1/0.7 = 1.4
P (Power) → 1
Actual past downscaling trend until year 2000


Change in 30 years

<table>
<thead>
<tr>
<th></th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
<th>Ideal scaling</th>
<th>Real Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_g$, $t_{ox}$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$K$</td>
<td>$10^{-2}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
</tr>
<tr>
<td>$V_{dd}$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td>$I_d$</td>
<td>$K(10^{-2})$</td>
<td>$10^{-1}$</td>
<td>$10^1$</td>
</tr>
<tr>
<td>$A_{chip}$</td>
<td>$\alpha$</td>
<td>$10^1$</td>
<td>$I_d/\mu m$</td>
<td>1</td>
<td>$10^1$</td>
<td>$10^1$</td>
</tr>
<tr>
<td></td>
<td>$N$</td>
<td>$\alpha/K^2(10^5)$</td>
<td>$P$</td>
<td>$\alpha(10^1)$</td>
<td>$10^5$</td>
<td>$f NCV^2$</td>
</tr>
</tbody>
</table>

Vd scaling insufficient, $\alpha$ increased $\rightarrow$ N, Id, f, P increased significantly

Past 30 years scaling
Merit: N, f increase
Demerit: P increase

V_{dd} scaling insufficient
Additional significant increase in $I_d$, f, P

$= f NCV^2$
Many people wanted to say about the limit. Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1µm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5µm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25µm:</td>
<td>Direct-tunneling of gate SiO₂</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1µm:</td>
<td>‘0.1µm brick wall’(various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing. VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit \(^{10}\) of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Gate Electrode  Gate Oxide  Potential Barrier  Si Substrate

Wave function  Direct tunneling current

Direct tunneling leakage current starts to flow when the thickness is 3 nm.
Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide

Lg = 10 µm  Lg = 5 µm  Lg = 1.0 µm  Lg = 0.1 µm

Id (mA/µm) vs. Vd (V)

Vg = 2.0V

Gate electrode
Gate oxide
Si substrate

G
S
D

43
Gate leakage: \( I_{g} \propto \text{Gate Area} \propto \text{Gate length (Lg)} \)

Drain current: \( I_{d} \propto 1/\text{Gate length (Lg)} \)

\( L_{g} \to \text{small}, \)

Then, \( I_{g} \to \text{small}, I_{d} \to \text{large}, \) Thus, \( I_{g}/I_{d} \to \text{very small} \)
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

- **90nm node**: Lg=50nm
- **65nm node**: Lg=35nm
- **45nm node**: Lg=25nm
- **32nm node**: Lg=15nm
- **22nm node**: Lg=10nm

Graph showing Lg gate (nm) vs. years with a trend line indicating approximately 30% improvement every two years.

*Qi Xinag, ECS 2004, AMD*
Downsizing limit?

Channel length?

Electron wave length

10 nm

Gate Oxd

Channel
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Electron wave length
10 nm

Tunneling distance
3 nm

Downsizing limit!
Channel length
Gate oxide thickness
Prediction now!

Electron wave length 
10 nm

Tunneling distance 
3 nm

Atom distance 
0.3 nm

MOSFET operation 
$Lg = 2 \sim 1.5 \text{ nm}$?

Below this, no one knows future!
Subthreshold leakage current of MOSFET

Subthreshold Current Is OK at Single Tr. level
But not OK For Billions of Trs.

Subthreshold Leakage Current

$V_{g} = 0\text{V}$

Subthreshold region

$V_{th}$
(Threshold Voltage)
Vth cannot be decreased anymore

significant Ioff increase

Vth: 300mV → 100mV
Ioff increases with 3.3 decades

(300 – 100)mV/(60mV/dec) = 3.3 dec

Subthreshold slope (SS)
= (Ln10)(kT/q)(Cox+C_D+Cit)/Cox
> ~ 60 mV/decade at RT

SS value:
Constant and does not become small with down-scaling

Log scale Id plot

\[ V_{dd} = 0.5V \]
\[ V_{dd} = 1.5V \]

Vth down-scaling

Vth = 300mV
Vg (V)

Vth = 100mV

Ion

Ioff

Log Id per unit gate width (= 1µm)

10^{-10}A
10^{-9}A
10^{-8}A
10^{-7}A
10^{-6}A
10^{-5}A
10^{-4}A
10^{-3}A
Prediction now!

Electron wavelength

10 nm

Tunneling distance

3 nm

Atom distance

0.3 nm

Practical limit for integration

Lg = 5 nm?

MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this, no one knows future!
However, Gate oxide thickness 2 orders magnitude smaller Close to limitation!!

Lg: Gate length downsizing will continue to another 10-15 years
0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! To use high-k dielectrics

Thin gate SiO₂

Almost the same electric characteristics

Thick gate high-k dielectrics

K: Dielectric Constant

However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO₂!
Choice of High-k elements for oxide

Candidates

Unstable at Si interface

- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

Gas or liquid at 1000 K

Radio active

He

B C N O F Ne

Al Si P S Cl Ar

K Ca Sc Ti V Cr Mn Fc Co Ni Cu Zn Ga Ge As Se Br Kr

Sr Y Zr Nb Mo Tc Ru Rb Pd Ag Cd In Sn Sb Te I Xe

Cs Ba Hf Ta W Re Os Ir Pt Au Hg Ti Pb Bi Po At Rn

Fr Ra Rf La Ce Pr Nd Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

Ac Th Pa U Np Pu Am Cm Bk Cf Es Fm Md No Lr

Unstable at Si interface

Si + MOₓ M + SiO₂
Si + MOₓ MSiₓ + SiO₂
Si + MOₓ M + MSiₓOᵧ

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in 1) band-offset, 2) dielectric constant 3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Conduction band offset vs. Dielectric Constant

Leakage Current by Tunneling

XPS measurement by Prof. T. Hattori, INFOS 2003
High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness
For the past 45 years, SiO₂ and SiON have been used as gate insulators. Today, EOT=1.0nm.

The EOT limit is 0.7~0.8 nm. One order of magnitude reduction is possible.

EOT can be reduced further beyond 0.5 nm by using direct contact to Si and choosing appropriate materials and processes.
Choice of High-k elements for oxide

<table>
<thead>
<tr>
<th>Candidates</th>
<th>Gas or liquid at 1000 K</th>
<th>Radio active</th>
<th>He</th>
</tr>
</thead>
<tbody>
<tr>
<td>Na, Mg</td>
<td>B, C, N, O, F, Ne</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ca, Sc</td>
<td>Al, Si, P, S, Cl, Ar</td>
<td></td>
<td></td>
</tr>
<tr>
<td>K, Ca, Sc</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sr, Y, Zr</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cs, Ba, Hf</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fr, Ra, Rf, Ha, Sg, Ng, Hs, Mt</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Unstable at Si interface

- Si + MO\textsubscript{X} \rightarrow M + SiO\textsubscript{2}
- Si + MO\textsubscript{X} \rightarrow MSi\textsubscript{X} + SiO\textsubscript{2}
- Si + MO\textsubscript{X} \rightarrow M + MSi\textsubscript{X}O\textsubscript{Y}

H\textsubscript{2}O\textsubscript{2} based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset, 2) dielectric constant 3) thermal stability

La\textsubscript{2}O\textsubscript{3} based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Gate Leakage vs EOT, (Vg=|1|V)

[Diagram showing gate leakage vs EOT for various materials such as Al2O3, HfO2, HfAlO(N), HfSiO(N), HfTaO, La2O3, Nd2O3, Pr2O3, PrSiO, PrTiO, SiON/SiN, Sm2O3, SrTiO3, Ta2O5, TiO2, ZrO2(N), ZrSiO, ZrAlO(N).]
EOT = 0.48 nm

Transistor with La2O3 gate insulator

Our results
EOT=0.37nm
La2O3

EOT=0.37nm  EOT=0.40nm  EOT=0.48nm

W/L = 50µm / 2.5µm  W/L = 50µm / 2.5µm  W/L = 50µm / 2.5µm

Vth=-0.06V  Vth=-0.05V  Vth=-0.04V

0.48 → 0.37nm Increase of Id at 30%
New material research will give us many future possibilities and the most important for Nano-CMOS!

Not only for high-k!
6 µm NMOS LSI in 1974

Layers
1. Si substrate
2. Field oxide
3. Gate oxide
4. Poly Si
5. S/D
6. Interlayer
7. Aluminum
8. Passivation

Materials
1. Si
2. SiO₂
3. BPSG
4. Al
5. PSG

Atoms
1. Si
2. O
3. P
4. B
5. Al
(H, N, Cl)
New materials

Y. Nishi, Si Nano Workshop, 2006,
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Just examples!
Many other candidates

Semiconductors

III-V

Ge

High-k dielectrics

La$_2$O$_3$
Ta$_2$O$_5$
HfO$_2$
ZrO$_2$
ZrSi$_x$O$_y$
RuO$_2$
Pt
IrO$_2$
Y1
PZT
BST

Electrode materials

Ferroelectrics

PtSi$_2$
WSi$_2$
CoSi$_2$
TiSi$_2$
MoSi$_2$
TaSi$_2$

Silicides

NiSi silicide

SiGe Semiconductor

Low-k dielectrics

Air
HSQ
Polymer

TiN
TaN
Cu
W

Metals

W

Low-$k$ dielectrics

Al
SiO$_2$
Poly Si

High-$k$ dielectrics

Si$_3$N$_4$
Si

Semiconductors

Ge

III-V

Al
SiO$_2$
Si

Just examples!
Many other candidates

New materials

NiSi silicide

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III-V

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SiO$_2$
Poly Si

Low-$k$ dielectrics

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HSQ
Polymer

TiN
TaN
Cu
W

Metals

W

Low-$k$ dielectrics

Al
SiO$_2$
Poly Si
Now: After 45 Years from the 1st single MOSFETs

32 Gb and 16Gb NAND, SAMSUNG
NAND flash trend

<table>
<thead>
<tr>
<th>Capacity</th>
<th>Node</th>
<th>1st Fabrication</th>
<th>Production</th>
</tr>
</thead>
<tbody>
<tr>
<td>512Mbit</td>
<td>120nm</td>
<td>2000</td>
<td>2001</td>
</tr>
<tr>
<td>1Gbit</td>
<td>100nm</td>
<td>2001</td>
<td>2002</td>
</tr>
<tr>
<td>2Gbit</td>
<td>90nm</td>
<td>2002</td>
<td>2003</td>
</tr>
<tr>
<td>4Gbit</td>
<td>70nm</td>
<td>2003</td>
<td>2004</td>
</tr>
<tr>
<td>8Gbit</td>
<td>60nm</td>
<td>2004</td>
<td>2005</td>
</tr>
<tr>
<td>16Gbit</td>
<td>50nm</td>
<td>2005</td>
<td>2006</td>
</tr>
<tr>
<td>32Gbit</td>
<td>40nm</td>
<td>2006</td>
<td>2008</td>
</tr>
</tbody>
</table>

Even Tbit would be possible in future!
Already 32 Gbit:
  larger than that of world population
  comparable for the numbers of neurons
  in human brain

256Gbit: larger than those of # of stars in galaxies
More Moore and More than Moore

Moore’s Law & More

More than Moore: Diversification
- Analog/RF
- Passives
- HV Power
- Sensors
- Actuators
- Biochips

Combining SoC and SiP: Higher Value Systems

Information Processing

Non-digital content System-in-package (SiP)

Beyond CMOS

ITRS 2005 Edition


Question what is the other side of the cloud?
FinFET to Nanowire

Channel conductance is well controlled by Gate even at L=5nm

F.-L. Yang, VLSI2004
- There will be still 4~6 cycles (or technology generations) left until we reach 11~5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

- Even after reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

- Two candidates have emerged for R & D
  1. Nanowire/tube MOSFETs
  2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.

Source: 2008 ITRS Summer Public Conf.

*I.5nm? was added by Iwai*
Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

- Reduction in $I_{off}$ ($I_{sd-leak}$)
  - Good control of $I_{sd-leak}$ by surrounding gate

- Increase in $I_{on}$ ($I_{d-sat}$)

- Trade off
  - Carrier scattering probability
    - Small
    - Large
  - # of quantum channel
    - Small
    - Large
  - High Conduction (1D)
    - $G_0=77.8 \mu S/wire$

- Multiple quantum channel (QC) used for conduction

- High-density lateral and vertical integration


Selection of MOSFET structure for high conduction: Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage
M1. Use 1D ballistic conduction
M2. Increase number of quantum channel
M3. Increase the number of wire or tube per area 3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.
1D conduction per one quantum channel:
\[ G = \frac{2e^2}{h} = 77.8 \mu S/wire \text{ or tube} \]
regardless of gate length and channel material

That is 77.8 \( \mu \text{A/wire} \) at 1V supply

This an extremely high value
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire

4 channels can be used
Maximum number of wires per 1 µm

- Front gate type MOS: 165 wires/µm
- Surrounded gate type MOS: 33 wires/µm

**Surrounded gate MOS**
- Metal gate electrode (10nm)
- High-k gate insulator (4nm)
- Si Nano wire (Diameter 2nm)

**30nm pitch**
- EUV lithography

**6nm pitch**
- By nano-imprint method

**Source** & **Drain**
Increase the number of wires towards vertical dimension
Our new roadmap

Extended CMOS: More Moore + CMOS logic

Beyond the horizon

Natural direction of downsizing

Selection

Diameter = 2nm

Si Channel

Si Fin, Tri-gate

Si Nano wire

III-V Ge Nano wire

Tube

CNT

Tube, Ribbon

Graphene

ITRS

High conduction

By 1D conduction

ITRS Beyond CMOS

Extended CMOS

More Moore

More Moore

Beyond the horizon

Extended CMOS: More Moore + CMOS logic

PJT (2007~2012)

Extended CMOS: More Moore + CMOS logic

Natural direction of downsizing

Selection

Diameter = 2nm

Si Channel

Si Fin, Tri-gate

Si Nano wire

III-V Ge Nano wire

Tube

CNT

Tube, Ribbon

Graphene

ITRS

High conduction

By 1D conduction

ITRS Beyond CMOS

Extended CMOS

More Moore

More Moore
Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues

Si Nanowire
- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire
- High-k gate insulator
- Wire formation technique

CNT:
- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:
- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap
Miniaturization of Interconnects on PCB (Printed Circuit Board)
Brain

Sensor
Infrared
Humidity
CO₂

Ultra small volume
Small number of neuron cells
Extremely low power

Real time image processing
(Artificial) Intelligence
3D flight control

System and
Algorism becomes
more important!

But do not know how?

Dragonfly is further high performance
Thank you for your attention!