

Past and Future of Integrated Circuits Technology

June 3, 2009

**@WIMNACT, Himalaya Hotel
Kathmandu, Nepal**

**Hiroshi Iwai,
Tokyo Institute of Technology**

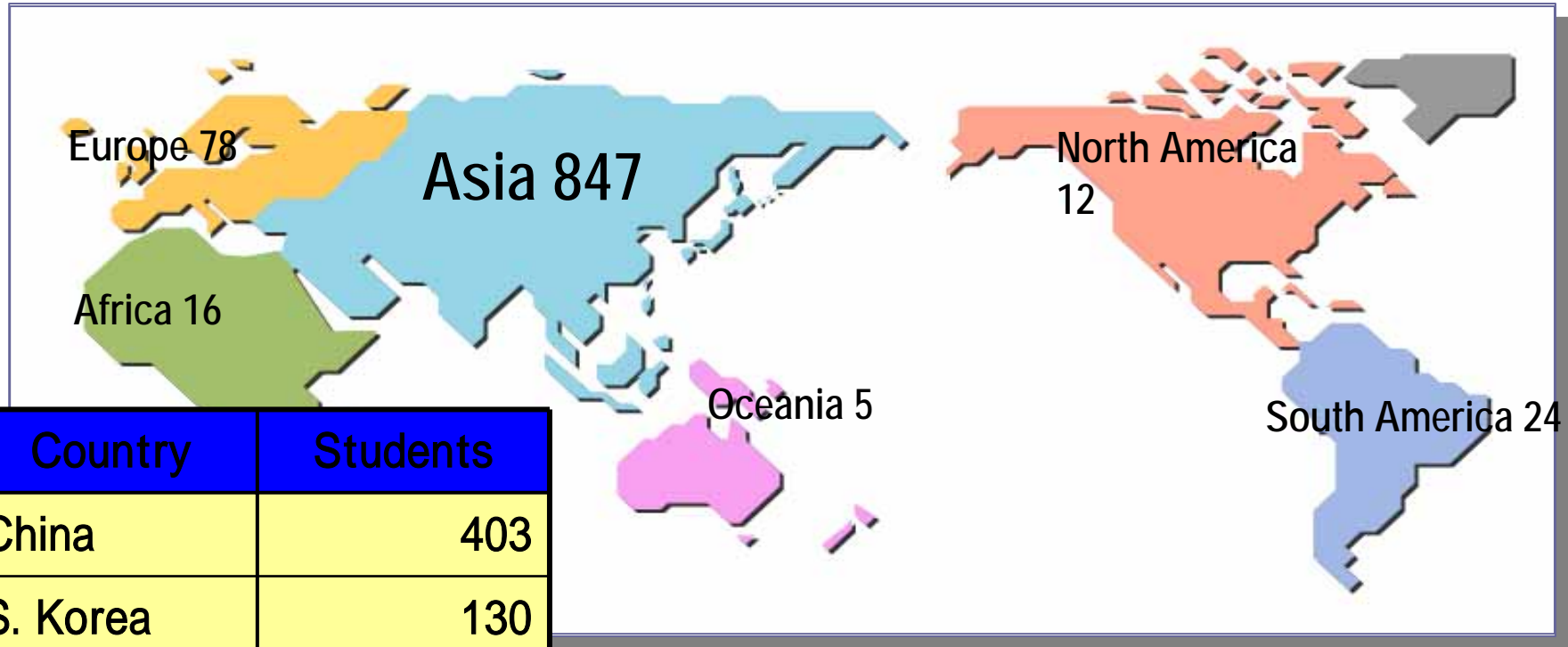


Founded in 1881, Promoted to Univ. 1929

Income	371M \$
Sponsored Research	100M \$
Employee(incl. Faculty)	1770
Faculty	729
Graduate student	4903

Year 2003

International Students



Country	Students
China	403
S. Korea	130
Indonesia	64
Thailand	55
Vietnam	60
Malaysia	28

Total 982
(As of May. 1, 2005)

Tokyo Institute of Technology
東京工業大学

2 major campuses
Ookayama, Tokyo
Suzukakedai, Yokohama

5000 Under graduate students
5000 Graduate Students

**Interdisciplinary Graduate School of
Science and Engineering**
大学院総合理工学研究科

**Dept. of Electronics
and Physics**
物理電子System創造専攻

5 other schools

10 other dept.

4 Laboratories

Frontier Research Center
先端創造共同研究中心

Consists of about 10 professor who
have big projects

**GCEO (Global Center of Excellence)
for Photonics Nanodevice Integration Engineering**

8 Other CEO

Consists of 5 EE
Related departments

Innovation Research Initiatives (革新的研究集団)

岩井研メンバー

(2009年04月1日現在)



教授
岩井洋



准教授(共同研究)
筒井一生



客員教授
服部健雄



特任教授
名取研二



連携教授
杉井信之



連携教授
西山彰



助教
Parhat Ahmet



助教
角嶋邦之

博士 研究員



ミノウハラ

博士 課程



D3
佐々木雄一朗



D3
ヘンドリアンシャー・サウディン



D3
下村浩



D3
宋在烈



D3
館喜一



D2
川那子高暢



D2
佐藤創志



D2
富田隆治



D1
Maimaitirexiati
Maimaiti



D1
Abudukelimu
Abudureheman



D1
幸田みゆき



筒井研 D3
小林勇介

修士 課程



M2
新井英朗



M2
李映勳



M2
中山寛人



M2
船水清永



M2
細田亘



M2
又野克哉



M1
タリス・ハサンサテ



M1
Mokhammad
Sholihul Hadi



M1
小柳友常



M1
小澤健児



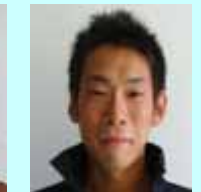
M1
神田高志



M1
澤田剛伸



M1
茂森直
登



M1
向井弘
樹



筒井研 M2
横田知之



筒井研 M2
星野憲文



筒井研 M2
横手義智

学部



B4
来山大祐

スタッフ



松本昭子



辛川美琴



西澤 正子

岩井研究室 ~Iwai Lab.~

● ご挨拶



Welcome to Iwai Lab.

総合理工学研究科 物理電子システム創造専攻 岩井研究室

当研究室では、シリコンをベースとした集積回路のデバイス技術、特に素子超微細化や集積回路限界の探査、研究や、新材料や三次元トランジスタ構造のシリコン集積回路への導入を行っています。さらにエマージング技術としてゲルマニウムやCNT(カーボンナノチューブ)デバイスの検討などを行っています。

LSI (Large scale Integrated Circuit, 大規模集積回路)の最初の製品とみなされるIntelの1k bit DRAMが製造されてから30年近くになりますが、この間にLSIは実に長足の発展を遂げ、高度な計算を行い動作や情報を制御する中枢部品としてありとあらゆる機器に用いられるようになってきました。

最近のMobile Telephone, Mobile PC, ひいてはインターネットの爆発的な普及も軽量、小型、低消費電力で極めてきたことによるものです。

今後更にこの文明飛躍的な発展を遂げて、近い将来人間の知性、感性の機能を代行する機器が出現することが大いに期待されます。

これはこれからの高齢化社会で予想される労働人口不足、老人介護人口不足などの状況のもとで、各人が平等にある程度以上の生活レベルを教授できるように行く行くは超えなければならぬハードルであると考えますが、何れにせよこれを実現するためには現状のものから何れも性能の高い機器の実現が必要であると考えられており、まずはハードとしてのLSIの発展が今後何十年かにわたって継続していくことが必要条件のひとつとも考えられています。

さて、LSIの発展はトランジスタを中心としたLSI中の素子の縮小化によってなされてきましたが、トランジスタの縮小化の限界がどこにあるかが重要な疑問としてクローズアップされてきます。この流れが今後も続くとする2005年頃にはゲート長が30nmとなり、更に今世紀の半ばにはゲート長はシリコン結晶中の原子の間隔である0.0003 μm(即ち3 Å)となる計算となります。この寸法辺りが原子を用いてトランジスタを形成する限りにおいて究極的な限界と考えられますが、このようなゲート長のトランジスタが動作するかどうかは甚だ疑問であると思われるため、経済的要因からはもう少し大きいところとも言われています。

研究テーマとしてはCMOS LSIの素子微細化の限界を見据えて、今後のLSIがハード、ソフトの両面から継続して発展していくためにはどう技術を開発していくべきかを考えつつ、まずは微細シリコントランジスタ微細の特性研究、微細化限界とその打破(高誘電体ゲート絶縁膜などの新材料の導入、構造の改良等)の研究などから手を染めていきたいと考えています。またその後のポストスケール時代に対応した、エマージング技術として、ゲルマニウムやシリコンナノワイヤートランジスタ、CNT(カーボンナノチューブ)デバイスの研究を行っていくと思っています。また、成果をできるだけ広く産業界に使っていただき、社会に貢献すること目指しており、産学連携と国際協力を研究の基本としています。

国際連携先: グルノーブル工科大学, LETI(フランス), 台湾交通大学 他多数

産学連携: SELETE, 東芝, 日立, アルパック, アルパックファイ, UJT

● 最近の研究テーマ

Siデバイスの重要性

現代社会: 生産、金融、運輸、医療、行政などの社会機構
インターネット、i-mode、Bluetooth、携帯電話、カーナビ、ゲーム、自動車、航空機、製造装置などの全ての機器、CD、DVDなどの機器

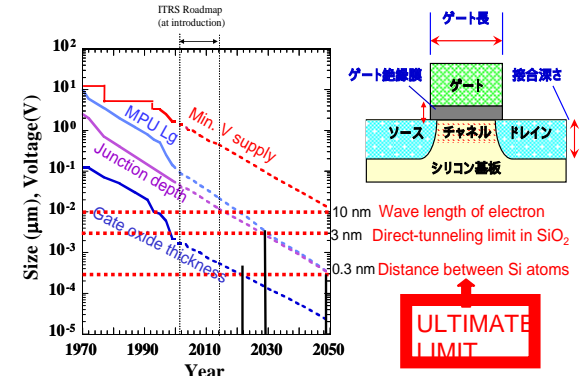
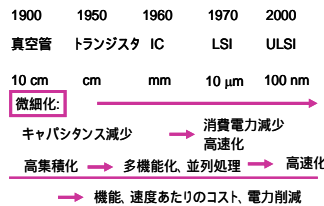
Si集積回路による管理・制御無くしてこれらは有り得ない

近年のSiデバイスの驚異的な発展

数千万個 - 数億個のトランジスタ集積
MPUのクロック周波数 3GHz
SiGeハイボララの f_t 300GHz以上

微細化の重要性

素子の微細化 (100年間で100万分の1に!)



微細化限界打破の手法

新材料 high-k/metal ゲートスタック構造

異種新材料の導入による新しい展開の可能性

新プロセス プラズマドーピング技術、メタルS/D

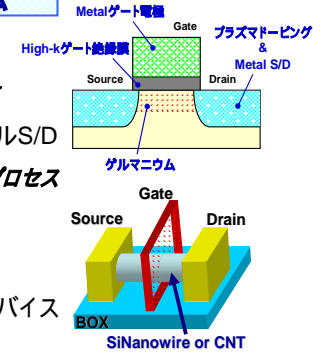
技術的なブレイクスルーが期待できる新しいプロセス

新構造 SiNanowireトランジスタ

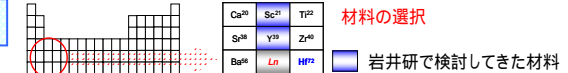
超高速、高密度、機能化デバイスの実現

エマージング技術 GeMOSFET、CNTデバイス

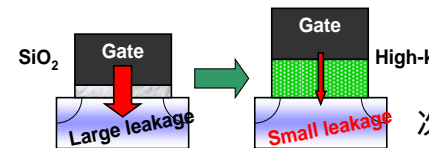
Siデバイス・Si集積回路との融合



High-k/metalゲートスタック



直接トンネル電流は低く、実効ゲート容量は大きく!



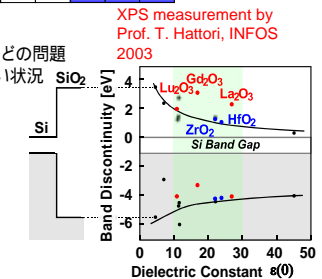
誘電率(κ)の高い材料: ZrO₂, HfO₂, La₂O₃

HfO₂が主流であるが、界面層成長、相分離などの問題があり、EOT<1nm以下の薄膜化は中々難しい状況

次世代ゲート絶縁膜材料として

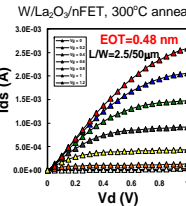
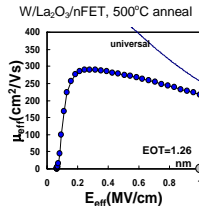
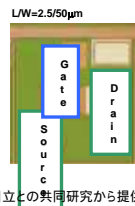
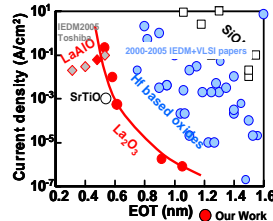
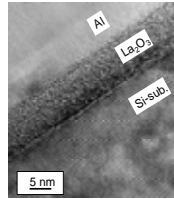
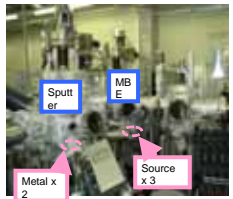
La₂O₃に注目

$$C_{ox} = \frac{\epsilon_d \epsilon_0}{t_{ox}} = \frac{\epsilon_{SiO_2} \epsilon_0}{EOT} \Rightarrow t_{ox} = \frac{\epsilon_d}{\epsilon_{SiO_2}} EOT$$



La₂O₃

EOT=0.5 nmでもリーク電流の抑制が可能である



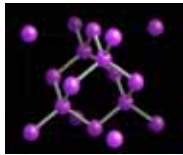
日立との共同研究から提供

高い移動度が得られ
実験値を使うことなく計算により物質の状態がわかる

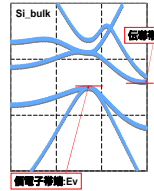
低EOTを実現

第一原理計算

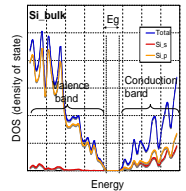
実験結果を裏付ける理論計算



Single crystal (Cubic structure)



バンドの構造が求まる

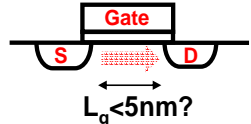


各bandを構成する電子の軌道がわかる

GeMOSFET

高移動度チャネル材料の必要性

ゲート長縮小の限界ソース/ドレイン間の漏れ電流増加



$$I_{ds} = \frac{W}{L} \mu_{eff} C_{ox} \frac{1}{2} (V_g - V_{th})^2$$

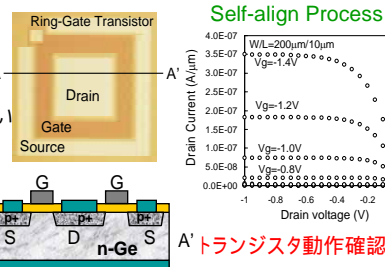
	μ_n [cm ² /Vs]	μ_p [cm ² /Vs]
Si	1400	450
Ge	3900	1900
GaAs	8500	400
InP	4600	650

Geトランジスタのゲート絶縁膜 W/La₂O₃/Ge p-MOSFET

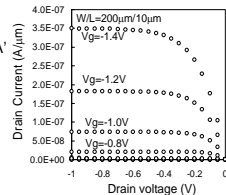
GeO₂は

- 高温熱処理で分解
- 水溶性(ウェットプロセス不可能)
- 比誘電率が低い
- 良好なトランジスタ特性が得られない

high-kをGeトランジスタのゲート絶縁膜として使おう!

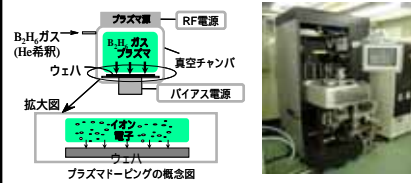


Self-align Process



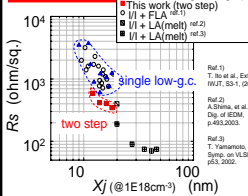
Plasma Doping

プラズマドーピング法の概念

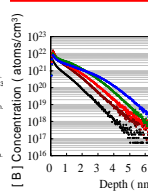


世界最小の接合深さを実現

Rs-Xj plots



as-doped B Profile



Metal Source/Drain

Source/Drain領域のスケーリング

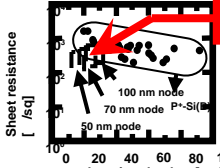
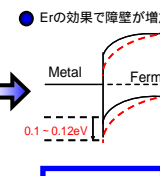
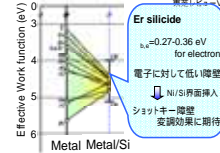
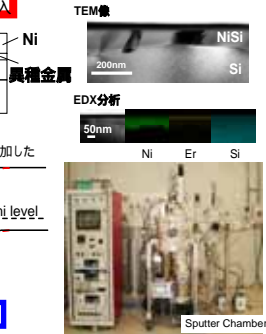


Fig.1 Sheet resistance vs. junction depth.

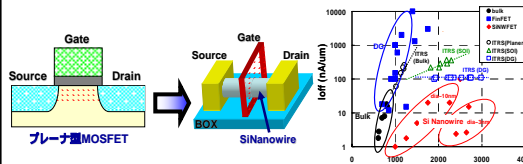


- 利点
 - 浅い接合形成が容易
 - ソース/ドレイン低抵抗
 - 短チャネル効果耐性が高い
- 課題
 - ショットキー障壁による駆動電流の劣化

Schottky障壁の制御が必要

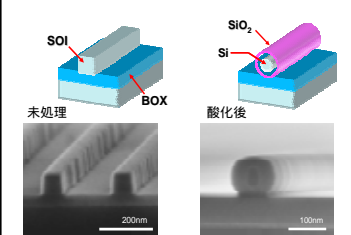


SiNanowireトランジスタ



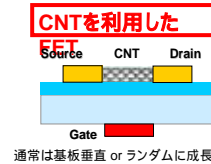
Nanowire型トランジスタ (1次元量子効果デバイス) → 短チャネル効果抑制 低電圧で高い駆動電流を実現

- Volume Inversion 反転電子密度の増加
- 1次元伝導の発現 量子化コンダクタンス
- エネルギーバンド構造 間接遷移型から直接遷移型 Egの増加



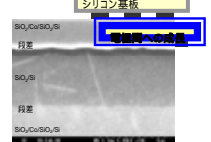
ワイヤ径の最適化、界面の制御 SiナノワイヤFETの作製

CNTデバイス

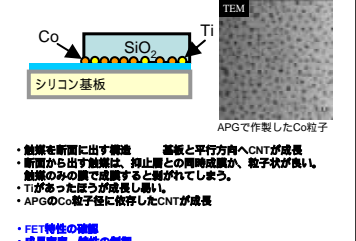


FETを利用した CNTデバイス

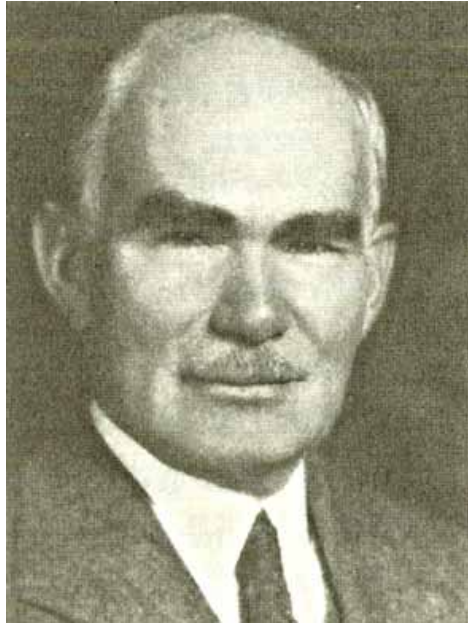
- なぜカーボンナノチューブなのか
 - 無散乱輸送: 高速動作
 - 高い電流駆動能力 高速動作
 - 電子と正孔で全く同じ移動度 n-chとp-chで同じ特性 CMOSに有利



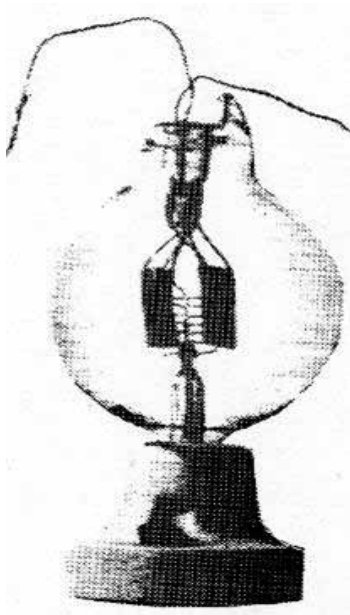
通常は基板垂直に成長するが、CVD法で成長させたCNTを利用するには基板水平方向に成長させる必要がある



- There were many inventions in the 20th century:
Airplane, Nuclear Power generation, Computer,
Space aircraft, etc
- However, everything has to be controlled by
electronics
- Electronics
Most important invention in the 20th century
- What is Electronics: To use electrons,
Electronic Circuits

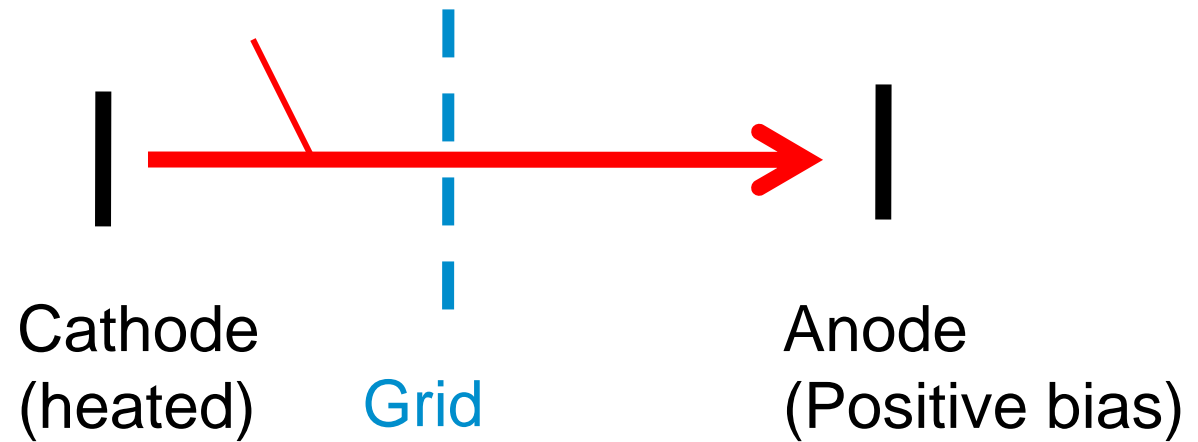


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

4 wives of Lee De Forest

1906 Lucille Sheardown

1907 Nora Blatch

1912 Mary Mayo, singer

1930 Marie Mosquini, silent film actress



Mary

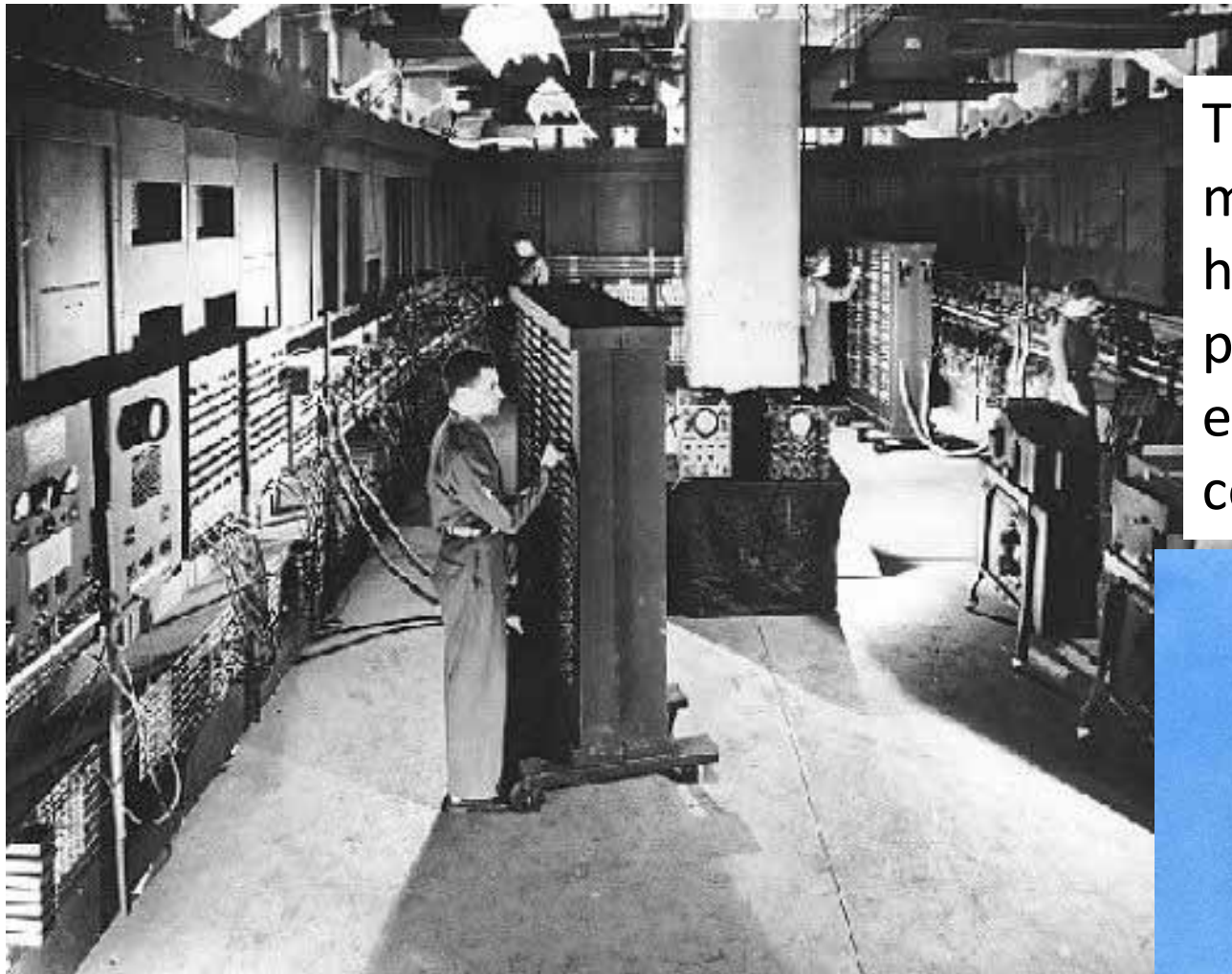


Marie



First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC
made of semiconductor
has much higher
performance with
extremely low power
consumption



History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor:

Ge Semiconductor, Bardeen, Brattin

→ Nobel Prize

1948, 1st Junction Bipolar Transistor,

Ge Semiconductor, Schokley

→ Nobel Prize

1958, 1st Integrated Circuits,

Ge Semiconductor, J.Kilby → Nobel Prize

1959, 1st Planar Integrated Circuits,

R.Noice

1960, 1st MOS Transistor, Kahng,

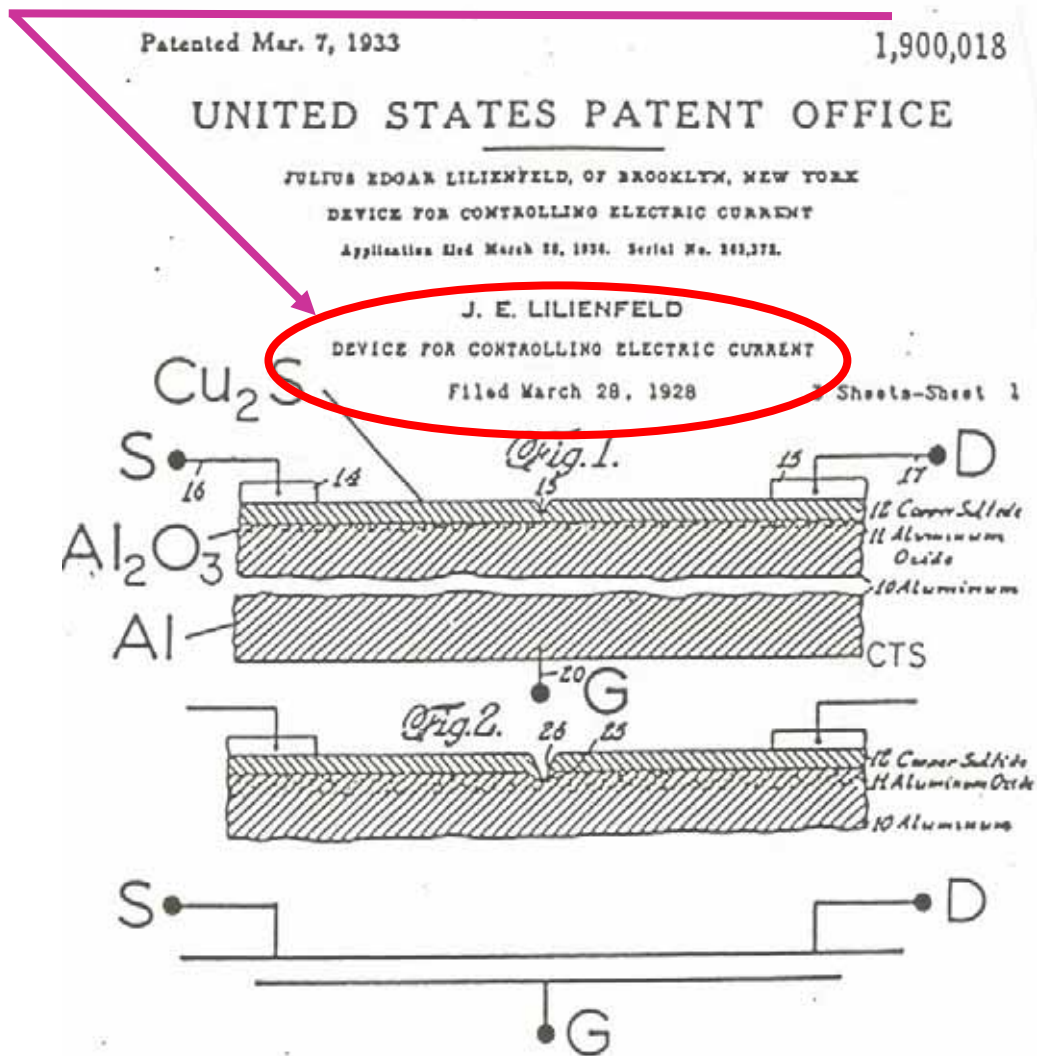
Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

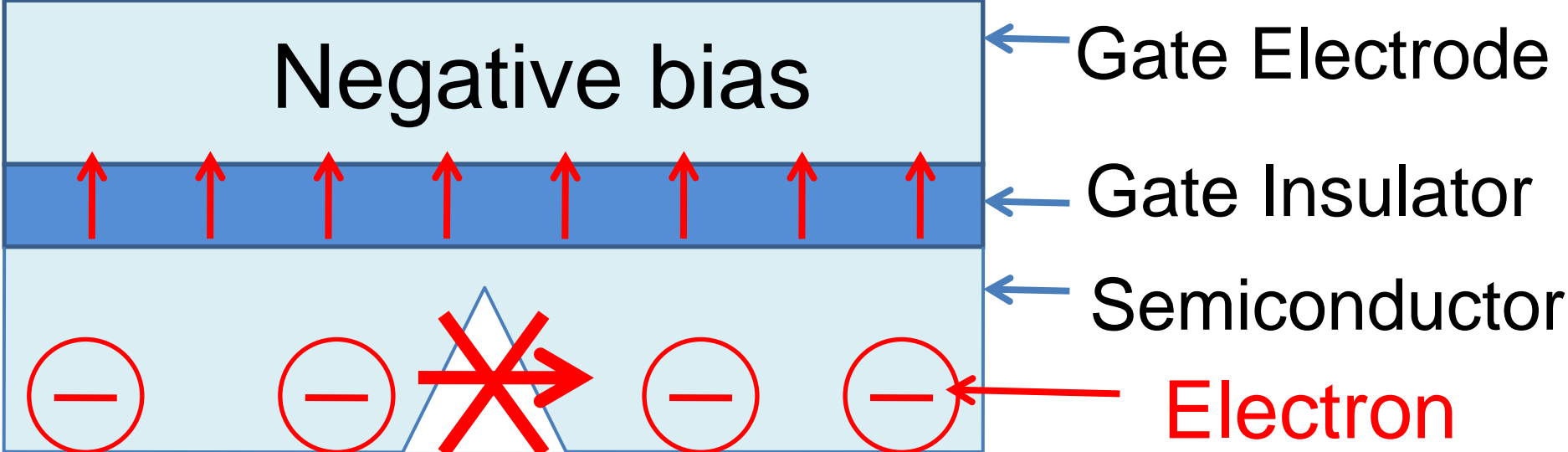
Filed March 28, 1928



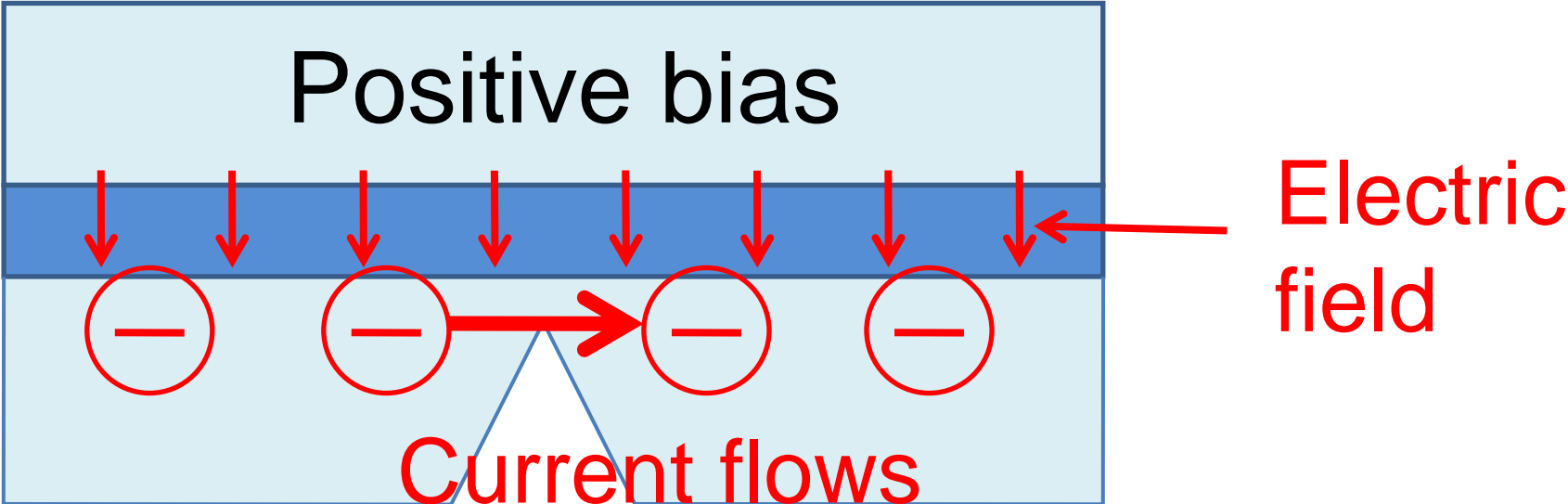
J.E.LILIENFELD

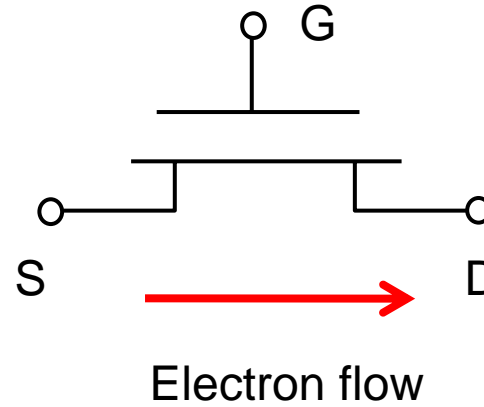
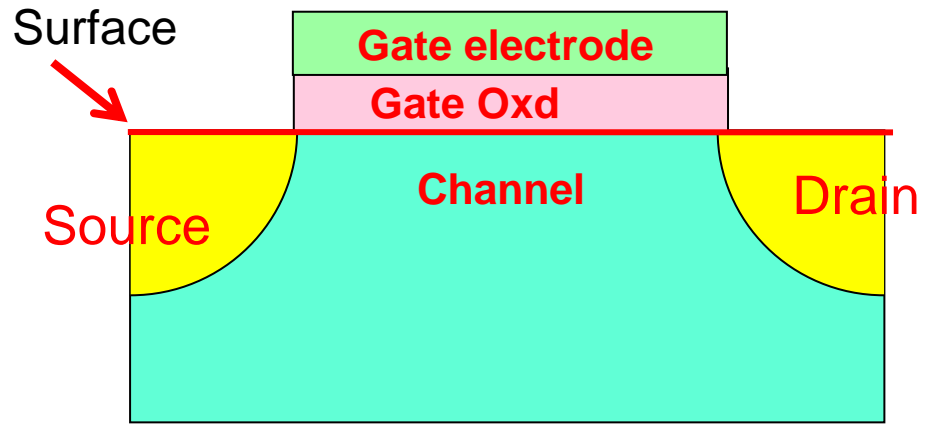


Capacitor structure with notch



No current

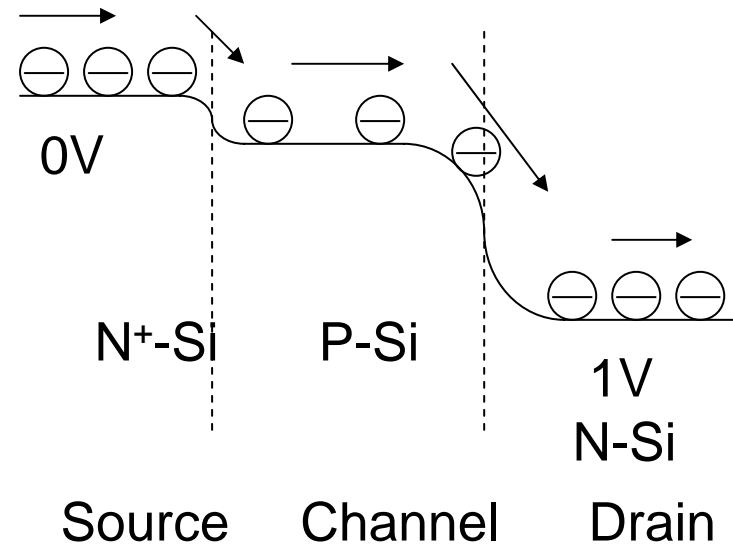
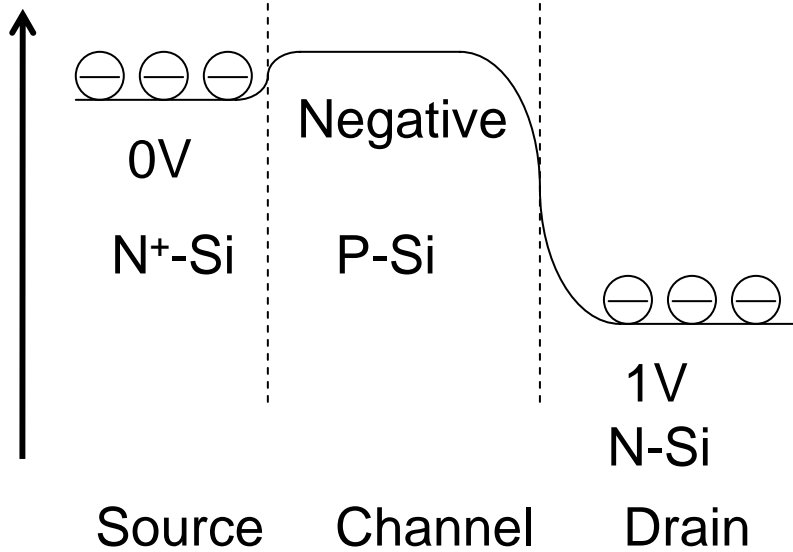




0 bias for gate

Positive bias for gate

Surface Potential (Negative direction)

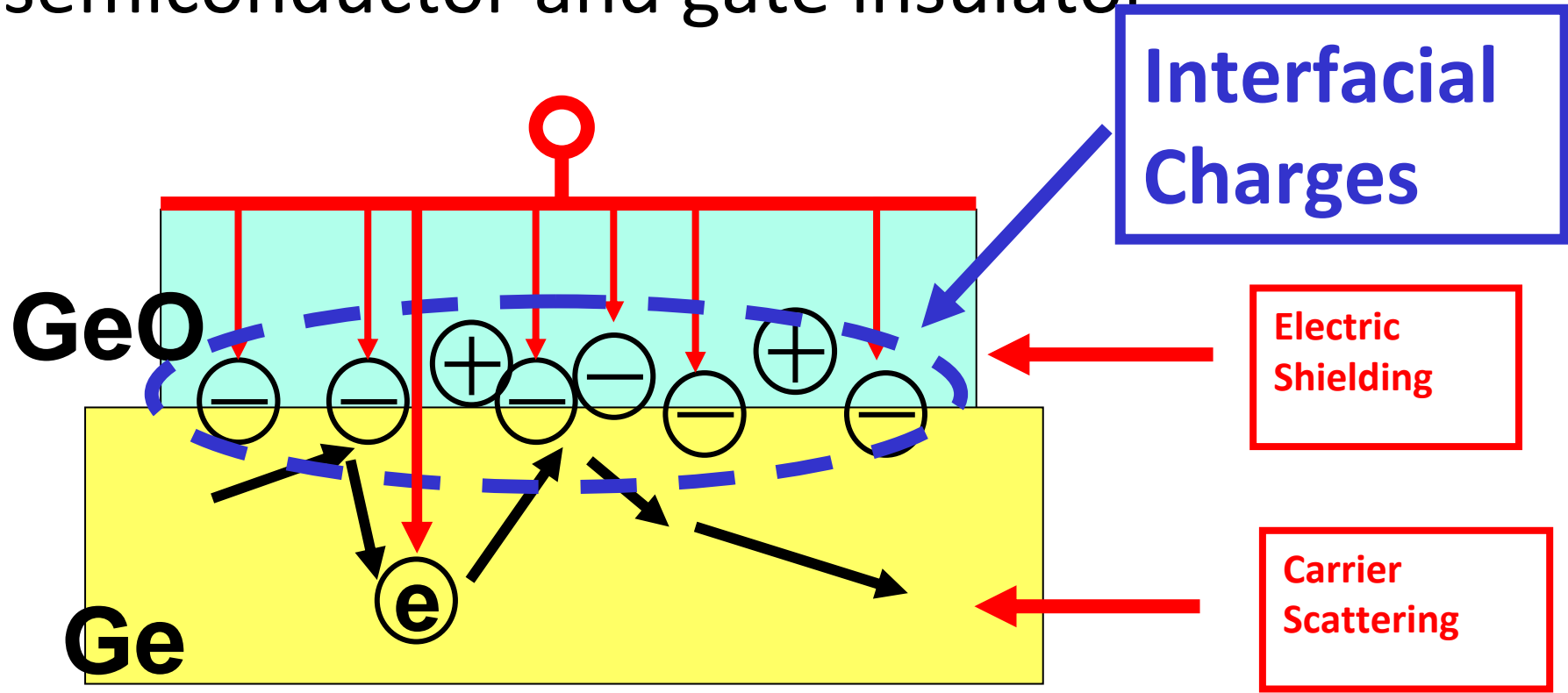


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Drain Current was several orders of magnitude smaller than expected

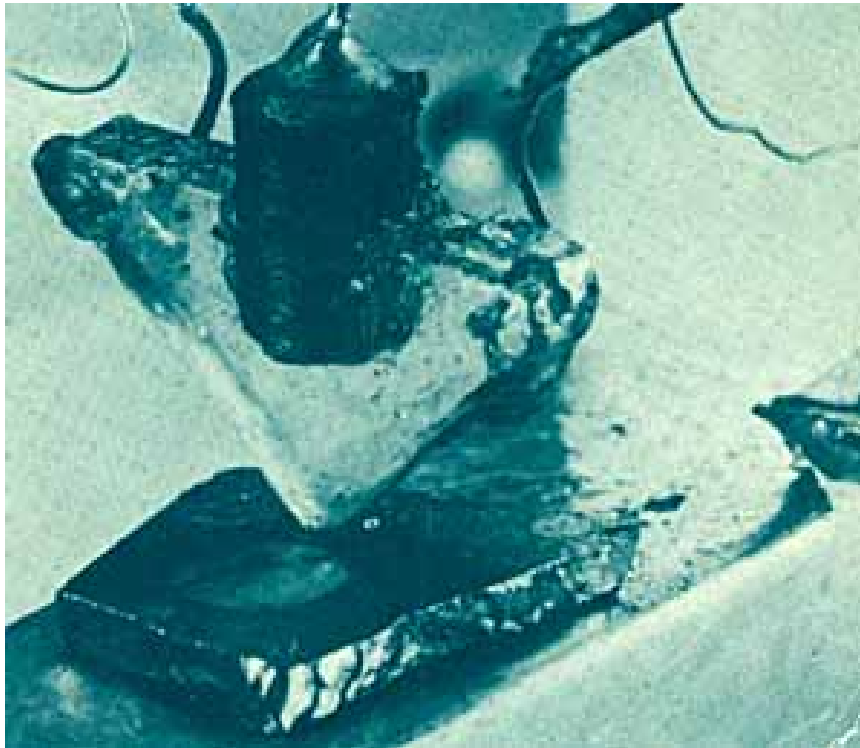
Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.

This is the 1st Transistor:

**Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)**

1947: 1st transistor



Bipolar using Ge

J. Bardeen

W. Bratten,

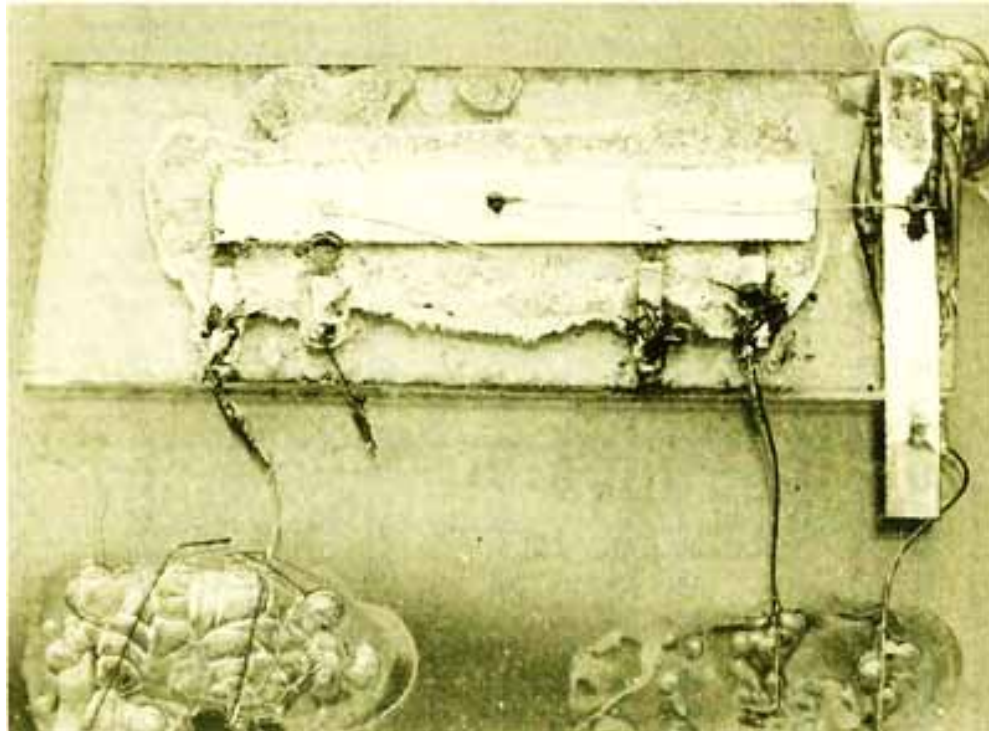


W. Shockley

1958: 1st Integrated Circuit

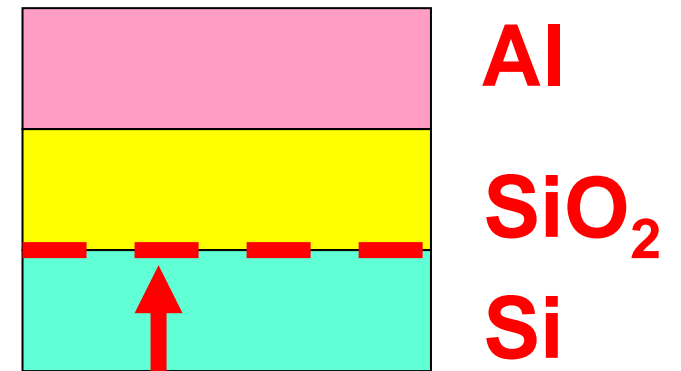
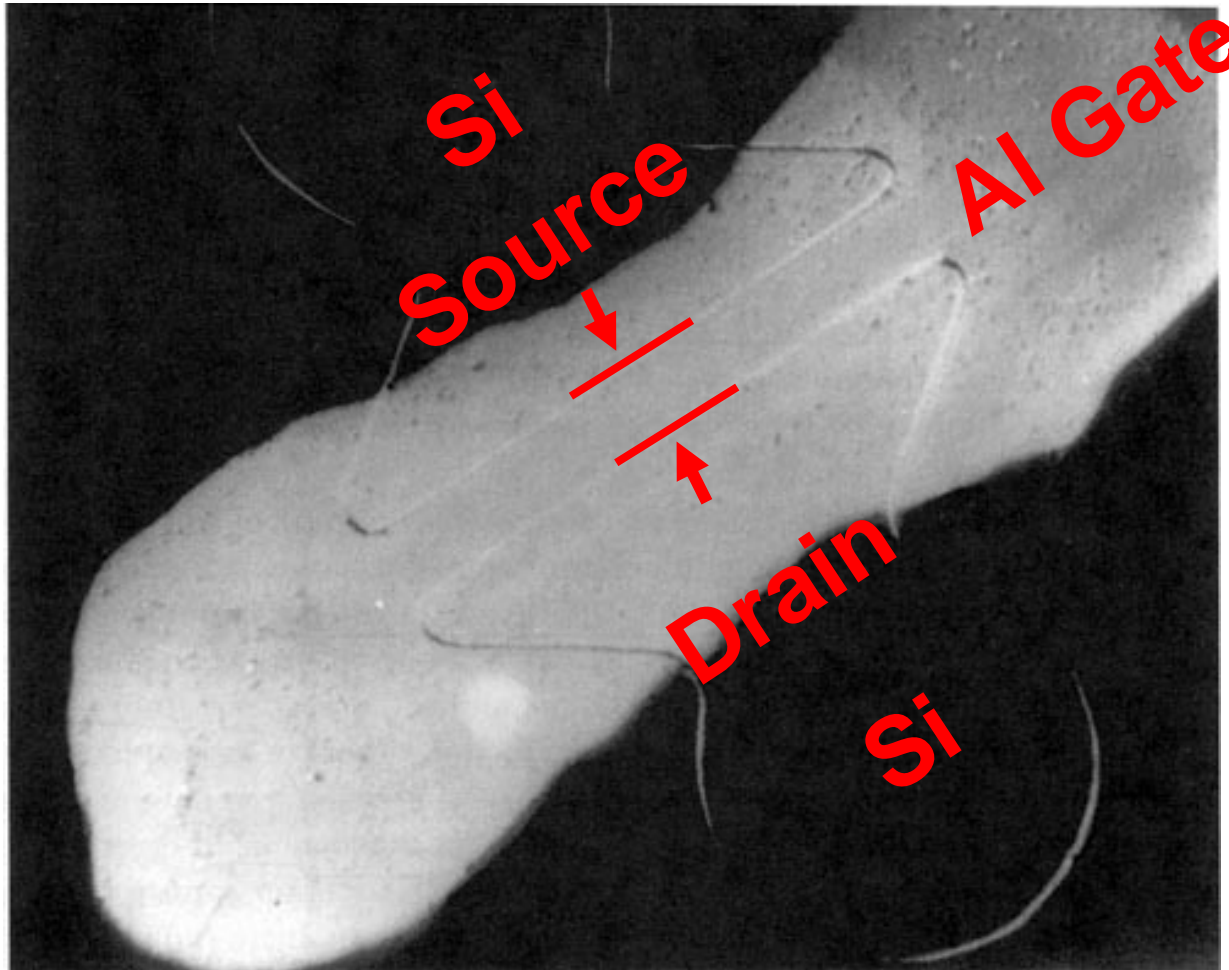
Jack S. Kilby

Connect 2 bipolar transistors in the Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

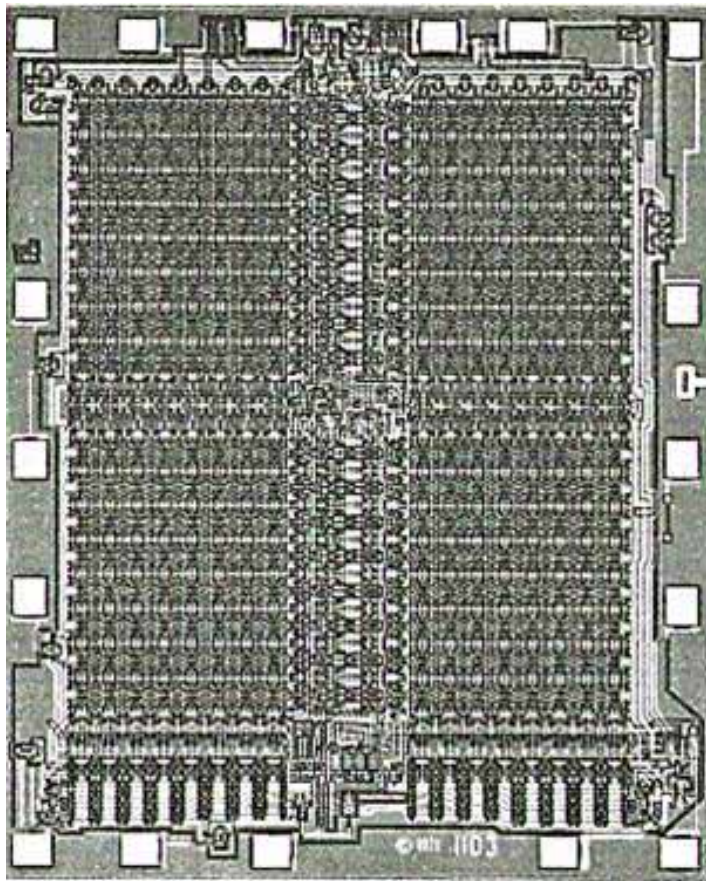
Top View



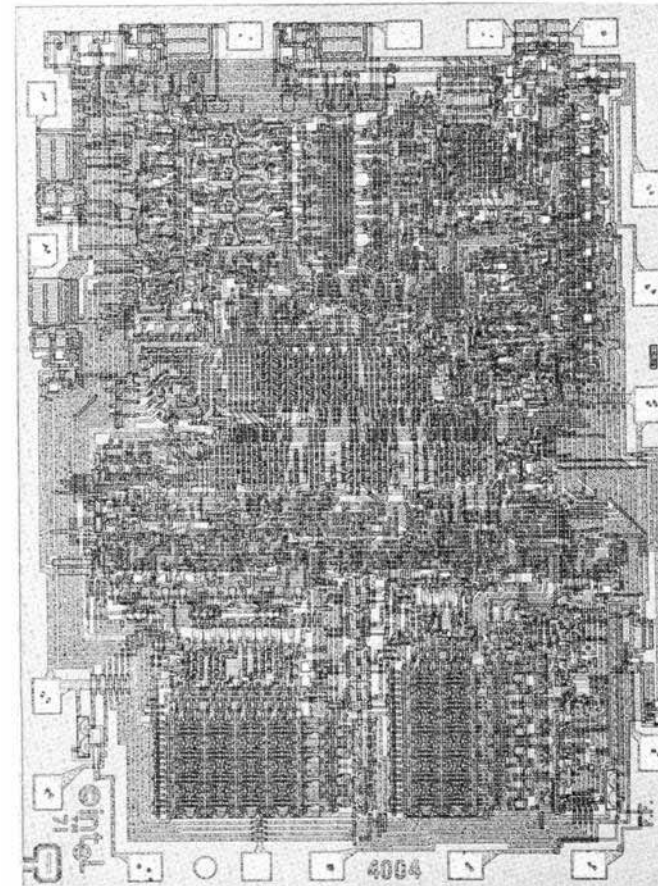
Si/SiO₂ Interface is
extraordinarily good

1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

Gate Electrode
Poly Si

Gate Insulator
SiO₂

Substrate
Si

MOSFET: Metal Oxide Semiconductor
Field Effect Transistor

Use Gate Field Effect for switching

Gate Electrode
Poly Si

Gate Insulator
SiO₂

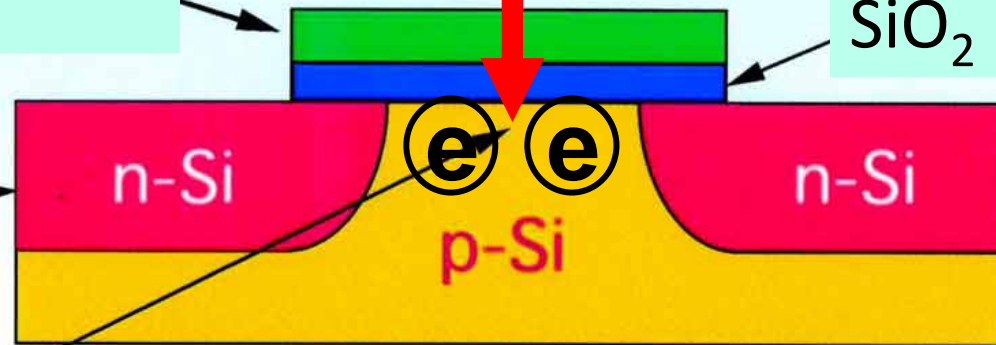
Source

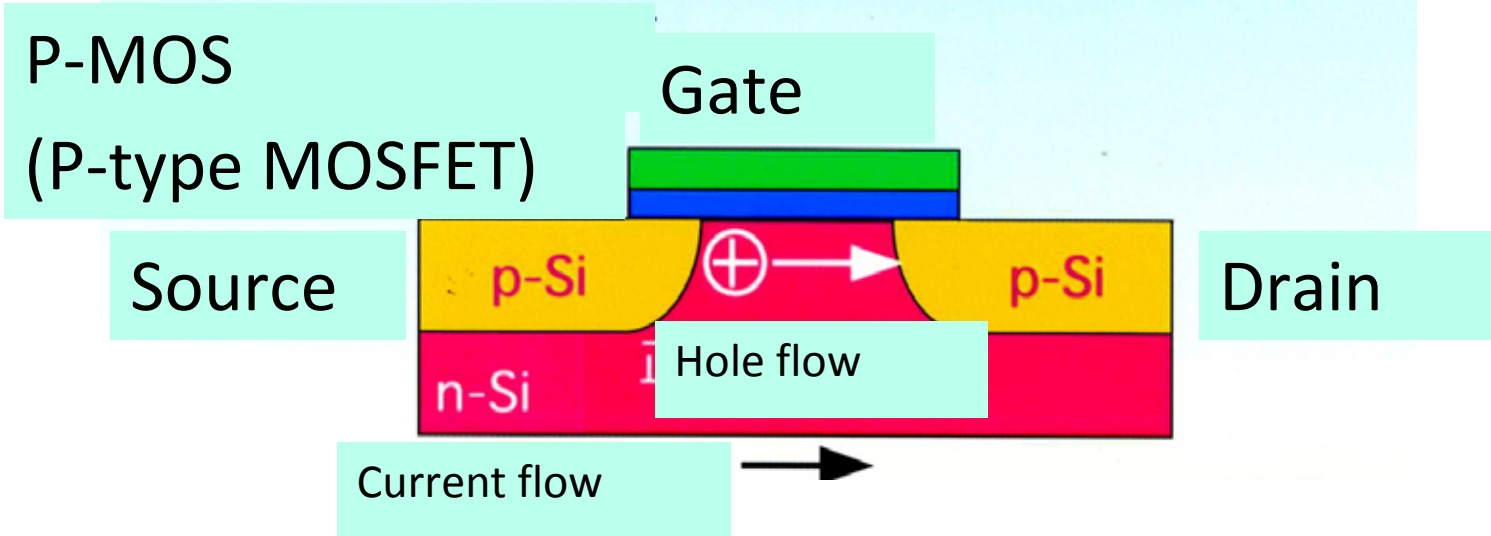
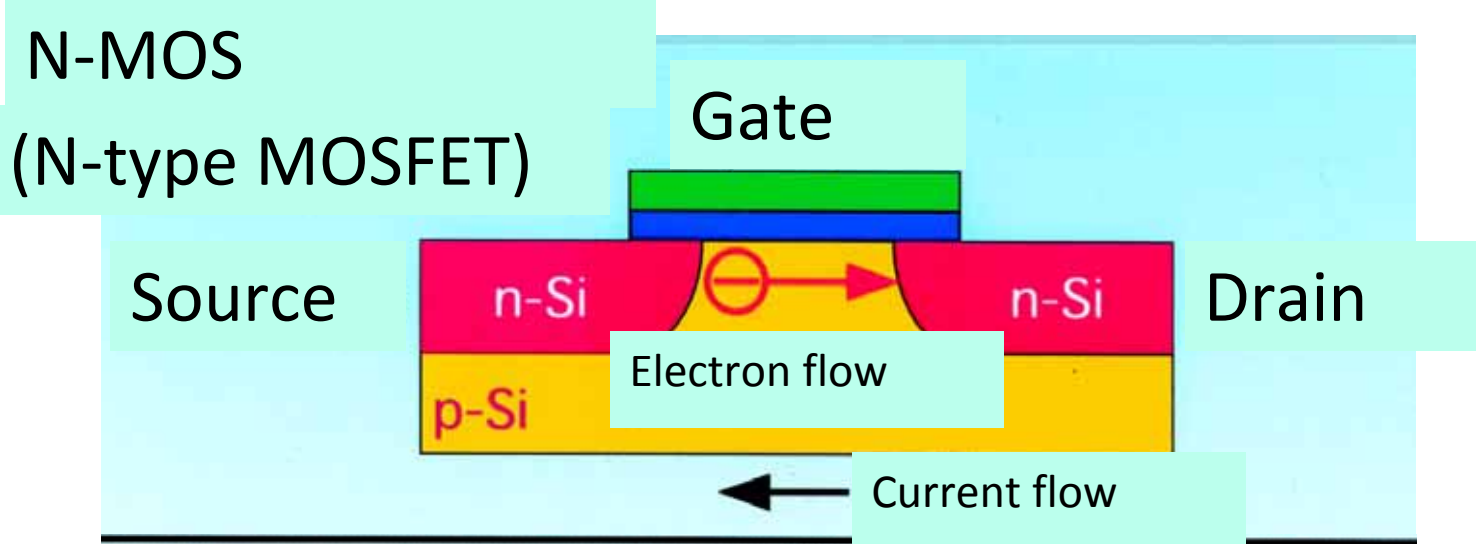
Drain

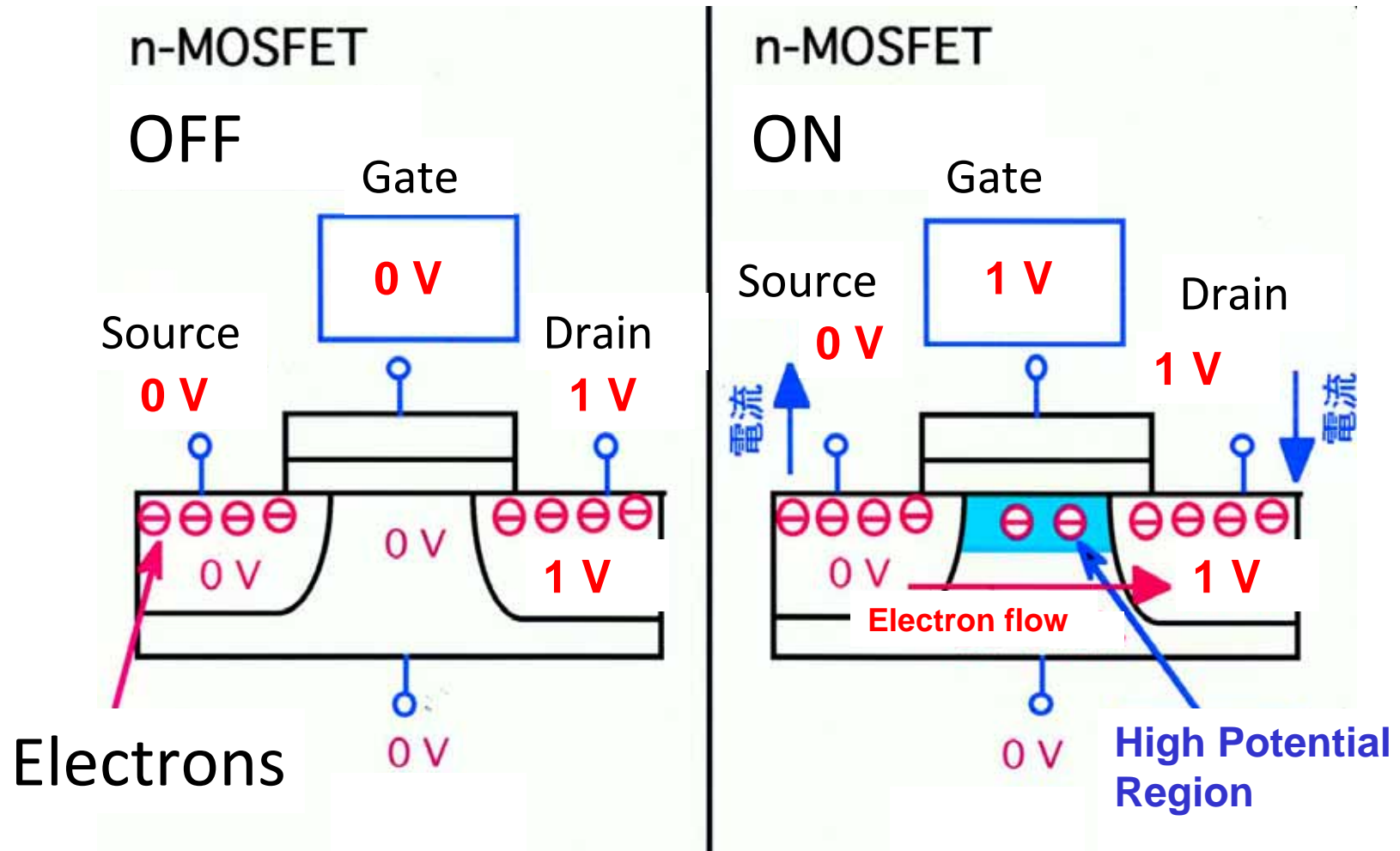
Channel

N-MOS (N-type MOSFET)

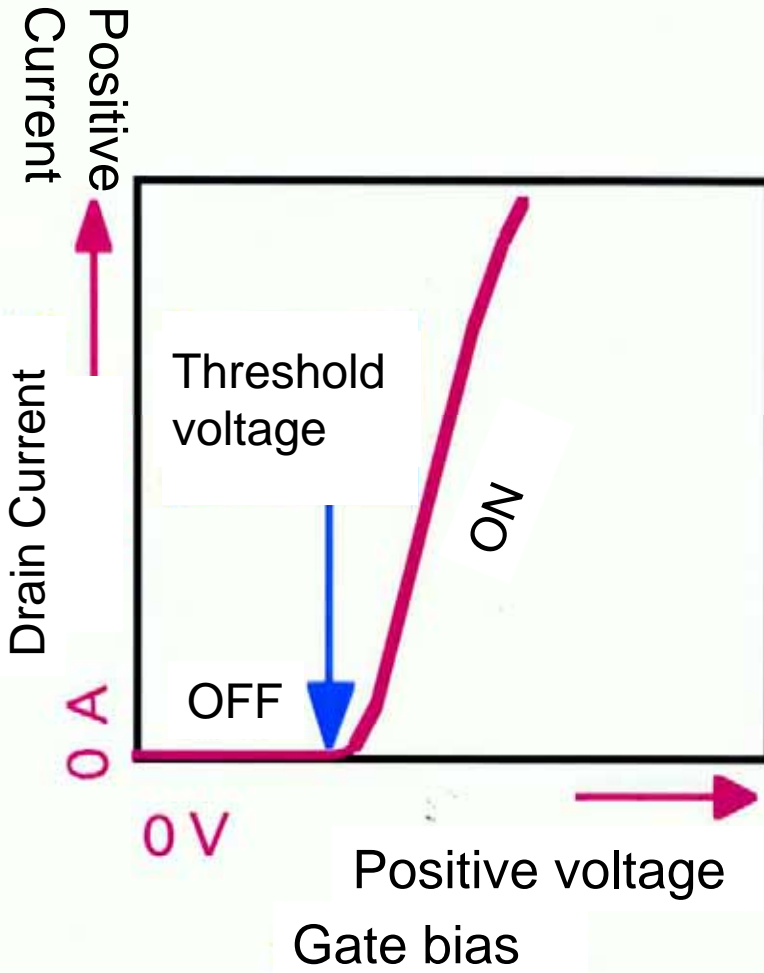
Si
Substrate



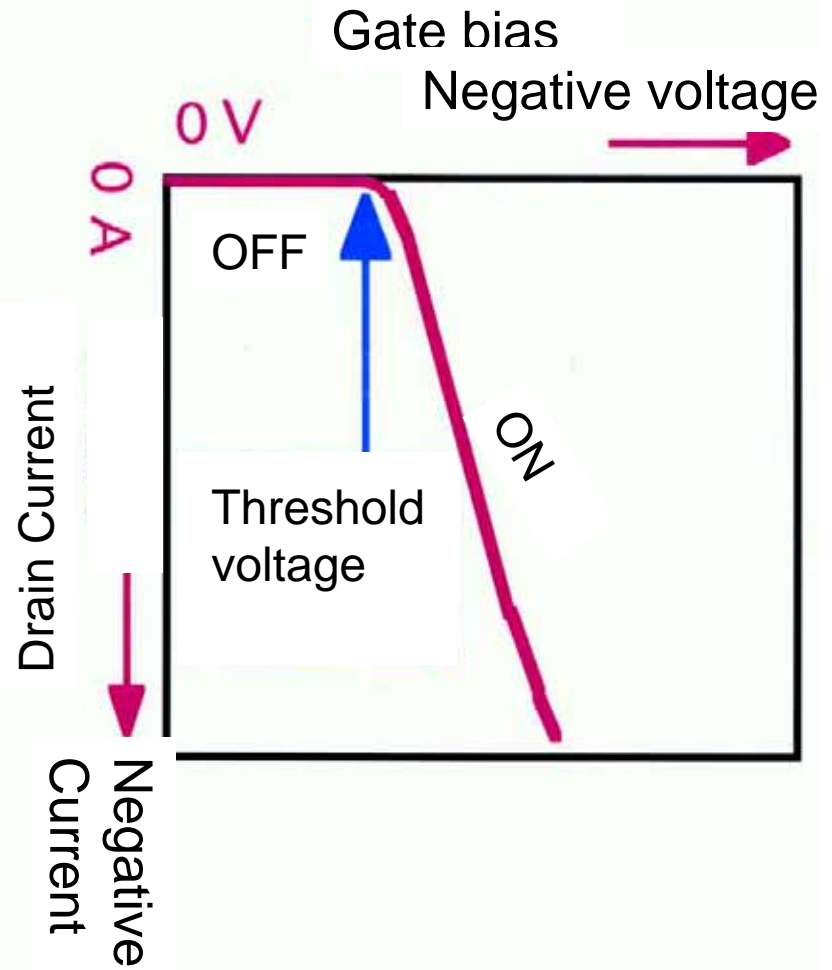




n-MOSFET

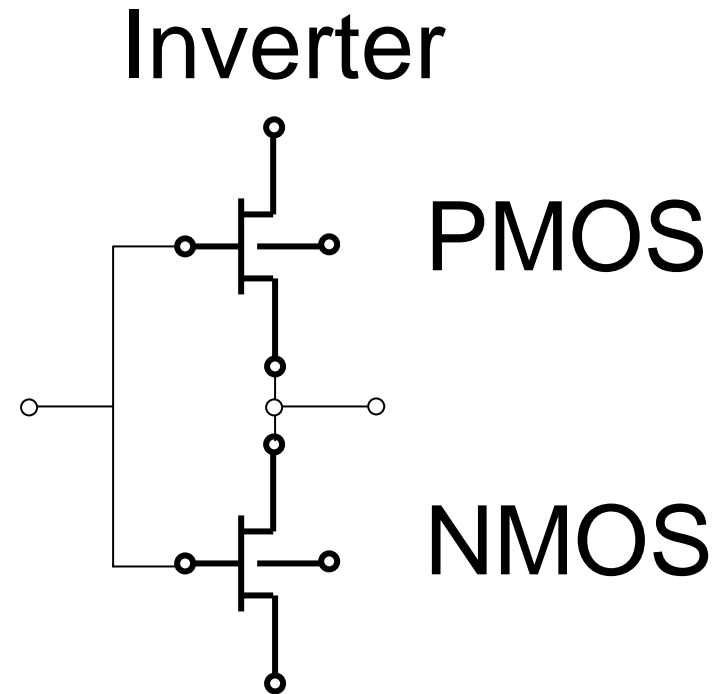


p-MOSFET



CMOS

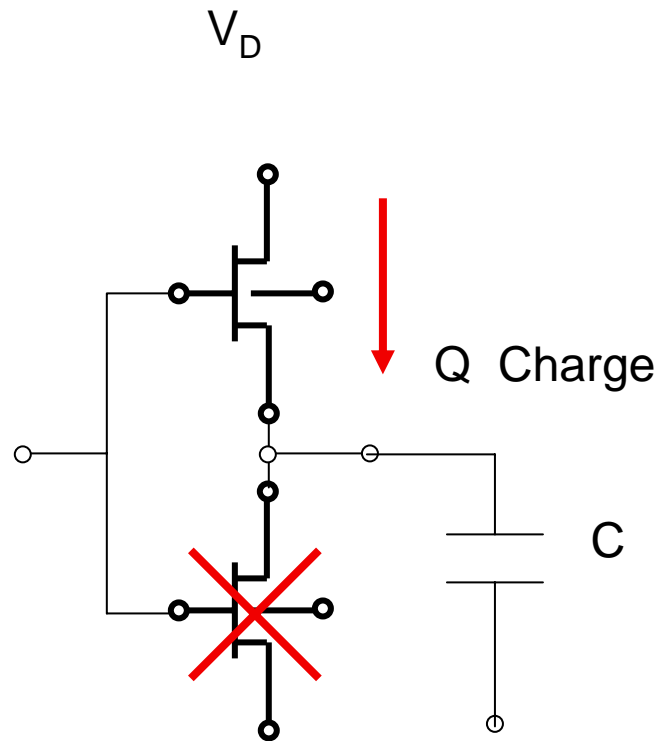
Complimentary MOS



When NMOS is ON, PMOS is OFF

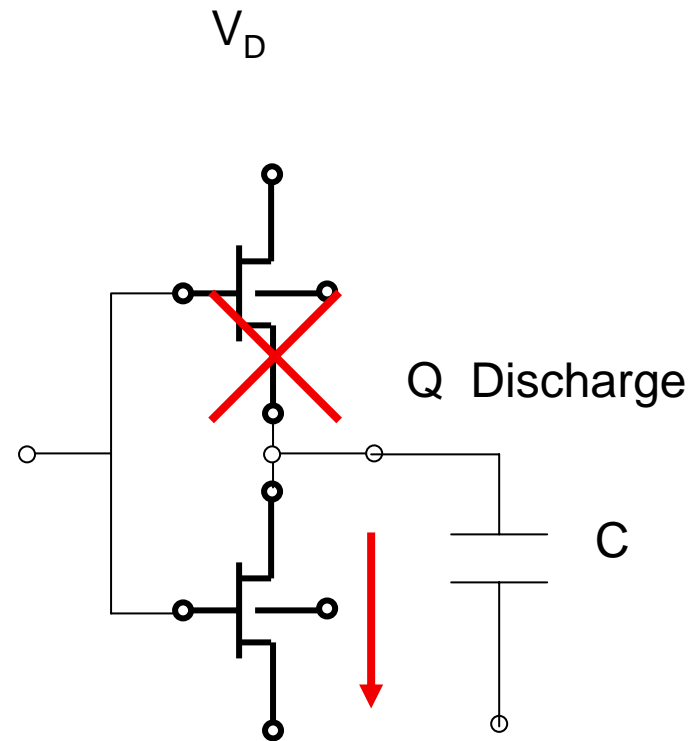
When PMOS is ON, NMOS is OFF

CMOS: Low Power: No DC current from Power supply to the ground



1 cycle

$$P = \frac{1}{2} CV_D^2$$



Clock frequency f

$$P = \frac{1}{2} fCV_D^2$$

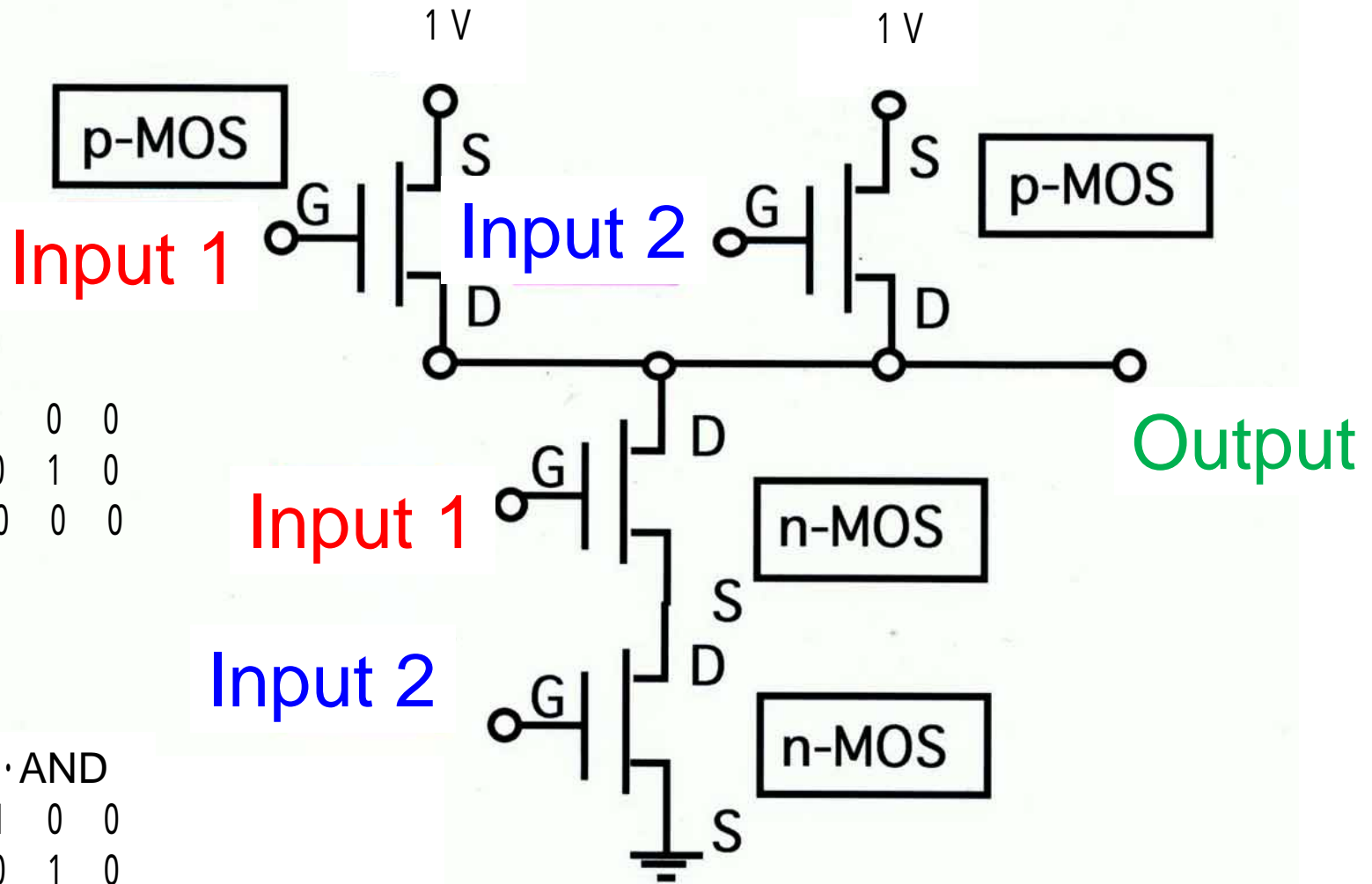
2 input NAND Circuit

AND

Input 1	1	1	0	0
Input 2	1	0	1	0
Output	1	0	0	0

NAND = NOT · AND

Input 1	1	1	0	0
Input 2	1	0	1	0
Output	0	1	1	1



Needless to say, but....

CMOS Technology:

Indispensable for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication,
transportation, medical care, education,
entertainment, etc.

Without CMOS:

There is no computer in banks, and
world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution



1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μ m	100 nm
10^{-1} m	10^{-2} m	10^{-3} m	10^{-5} m	10^{-7} m

In 100 years, the size reduced by one million times. There have been many devices from stone age. **We have never experienced such a tremendous reduction of devices in human history.**

Downsizing

1. Reduce Capacitance

→ Reduce switching time of MOSFETs

→ Increase clock frequency

→ Increase circuit operation speed

2. Increase number of Transistors

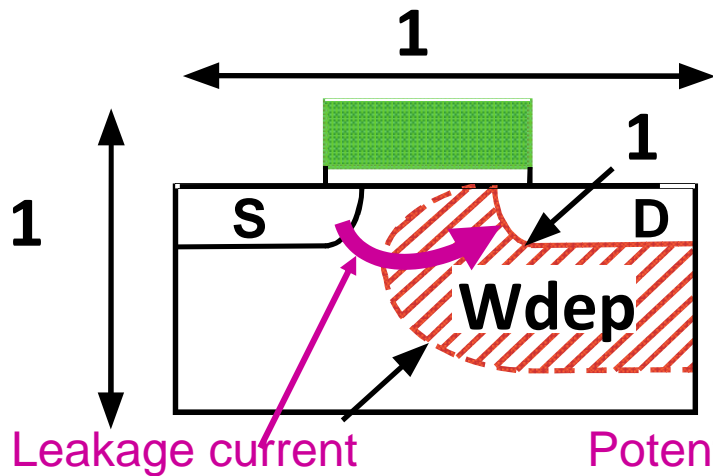
→ Parallel processing

→ Increase circuit operation speed

Downsizing contribute to the performance increase in double ways

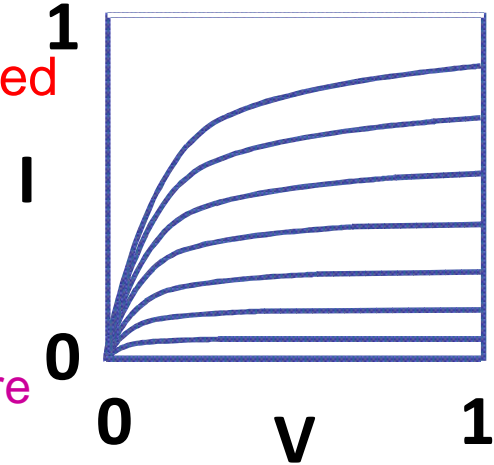
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage
between S and D



Leakage current

Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

**K=0.7
for
example**

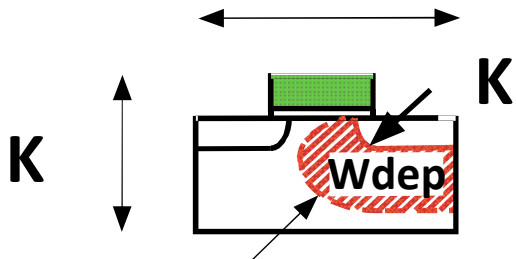


X , Y , Z : K, V : K, Na : 1/K

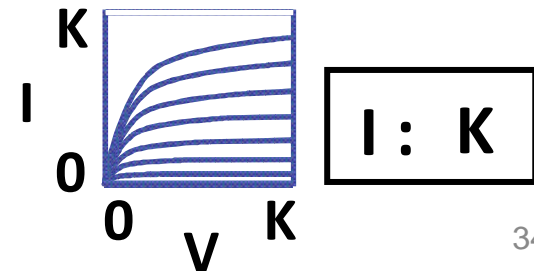
By the scaling, Wdep is suppressed in proportion,
and thus, leakage can be suppressed.

K

→ Good scaled I-V characteristics



**Wdep ∝ √(V/Na)
: K**



I : K

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	Scaling K : K=0.7 for example
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o : gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1} (V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d / \mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \epsilon_o \epsilon_{ox} L_g W_g / t_{ox} \rightarrow KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d \rightarrow KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor \rightarrow In the past, $\alpha > 1$ for most cases
Integration (# of Tr)	N	α/K^2	$N \rightarrow \alpha/K^2 = 1/K^2$, when $\alpha=1$
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha = 1$, when $\alpha=1$

$k = 0.7$ and $\alpha = 1$

Single MOFET

$V_{dd} \rightarrow 0.7$

$L_g \rightarrow 0.7$

$I_d \rightarrow 0.7$

$C_g \rightarrow 0.7$

P (Power)/Clock

$\rightarrow 0.7^3 = 0.34$

τ (Switching time) $\rightarrow 0.7$

$k = 0.7^2 = 0.5$ and $\alpha = 1$

$V_{dd} \rightarrow 0.5$

$L_g \rightarrow 0.5$

$I_d \rightarrow 0.5$

$C_g \rightarrow 0.5$

P (Power)/Clock

$\rightarrow 0.5^3 = 0.125$

τ (Switching time) $\rightarrow 0.5$

Chip

N (# of Tr) $\rightarrow 1/0.7^2 = 2$

f (Clock) $\rightarrow 1/0.7 = 1.4$

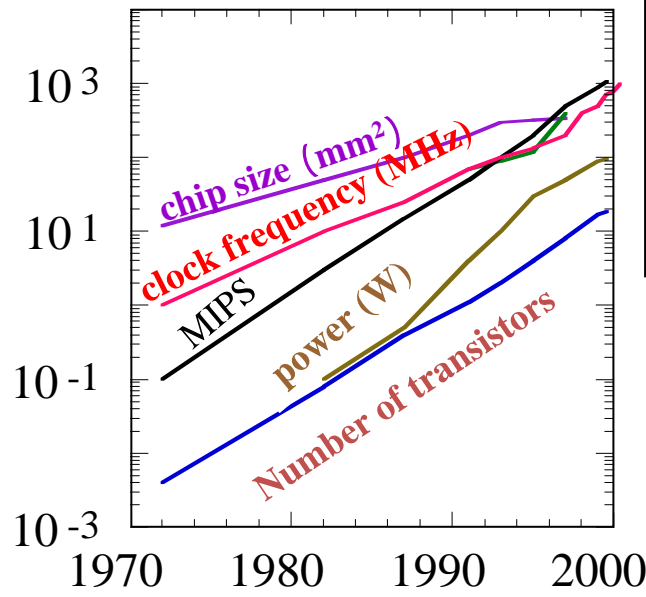
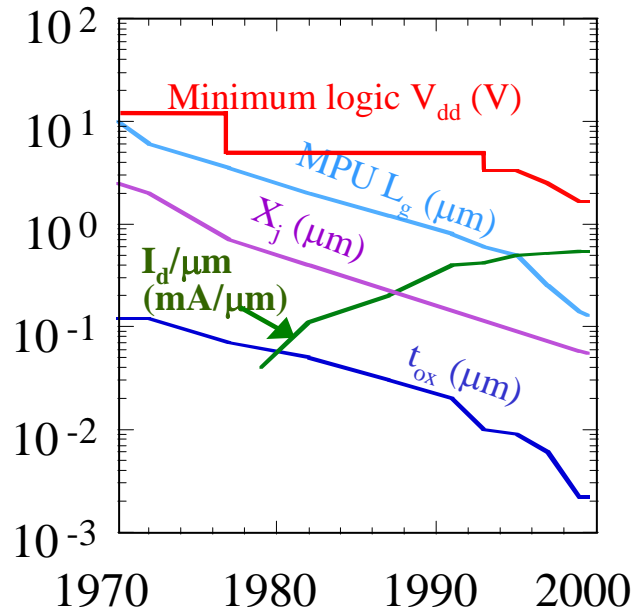
P (Power) $\rightarrow 1$

N (# of Tr) $\rightarrow 1/0.5^2 = 4$

f (Clock) $\rightarrow 1/0.5 = 2$

P (Power) $\rightarrow 1$

Actual past downscaling trend until year 2000



Past 30 years scaling
 Merit: N, f increase
 Demerit: P increase

V_{dd} scaling insufficient
 ↓
 Additional significant increase in I_d, f, P

Source: Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	$1/K(10^2)$	10^3
t_{ox}	K(10^{-2})	10^{-2}	$I_d/\mu m$	1	10^1	P	$\alpha(10^1)$	10^5
V_{dd}	K(10^{-2})	10^{-1}	N	$\alpha/K^2(10^5)$	10^4	= $f\alpha NCV^2$		
A_{chip}	α	10^1						

V_d scaling insufficient, α increased → N, I_d, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1 μ m:	SCE
Early 1980's	0.5 μ m:	S/D resistance
Early 1980's	0.25 μ m:	Direct-tunneling of gate SiO ₂
Late 1980's	0.1 μ m:	'0.1 μ m brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micrometer would be the limit because of direct-tunneling current through the very thin-gate oxide.

INTRODUCTION TO **VLSI** SYSTEMS

CARVER MEAD • LYNN CONWAY





C. Mead

L. Conway

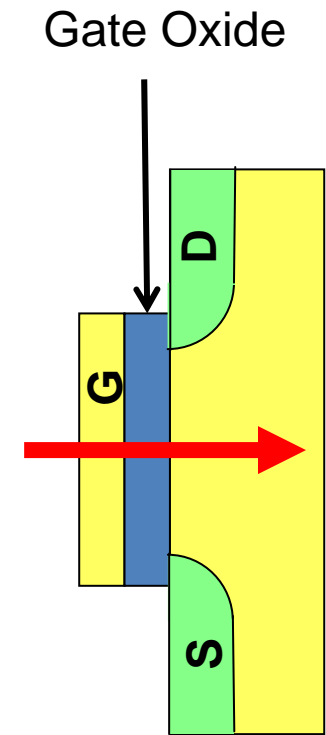
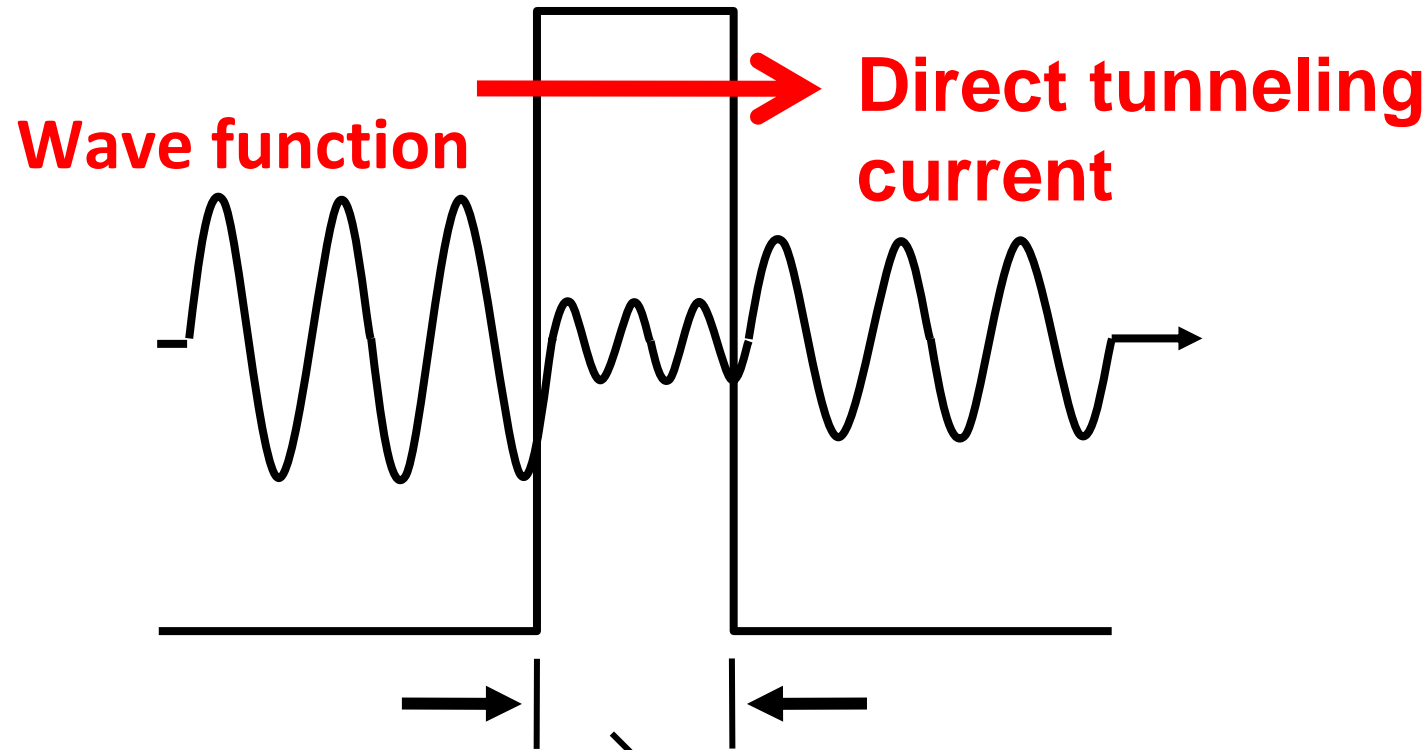
VLSI textbook

Finally, there appears to be a fundamental limit ¹⁰ of approximately quarter micron channel length, where certain physical effects such as the **tunneling through the gate oxide begin to make the devices of smaller dimension unworkable.**

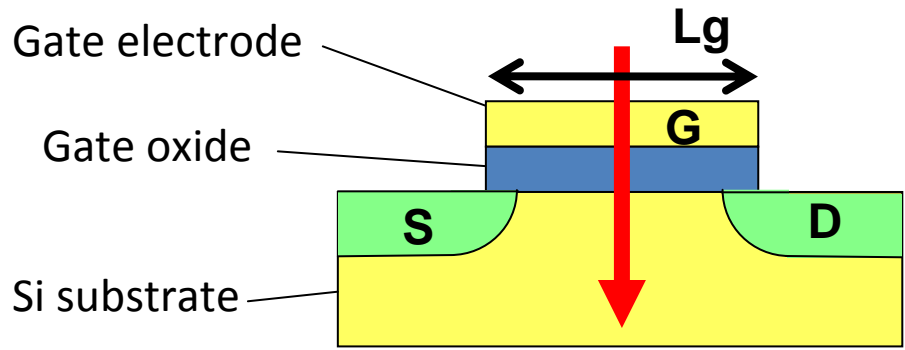
Direct-tunneling effect

Gate Electrode Gate Oxide Si Substrate

Potential Barrier

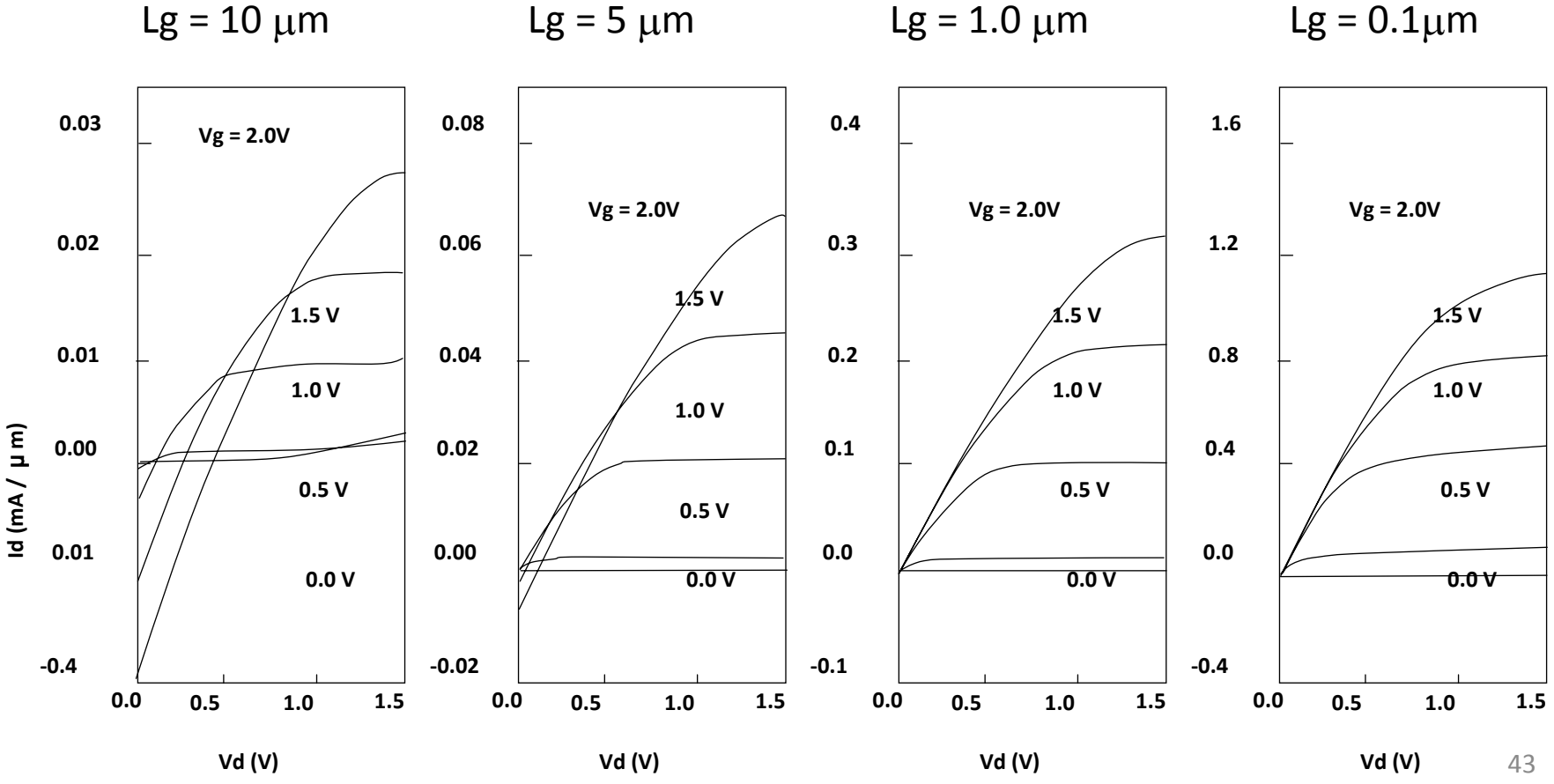


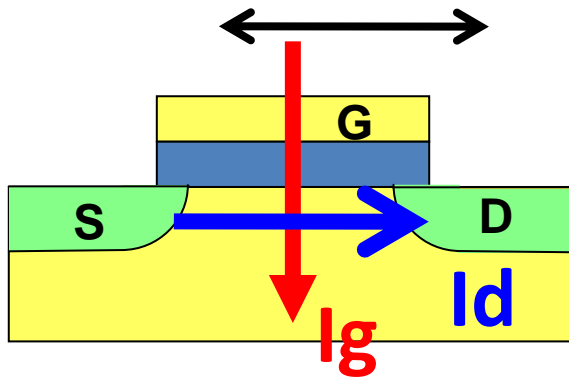
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide



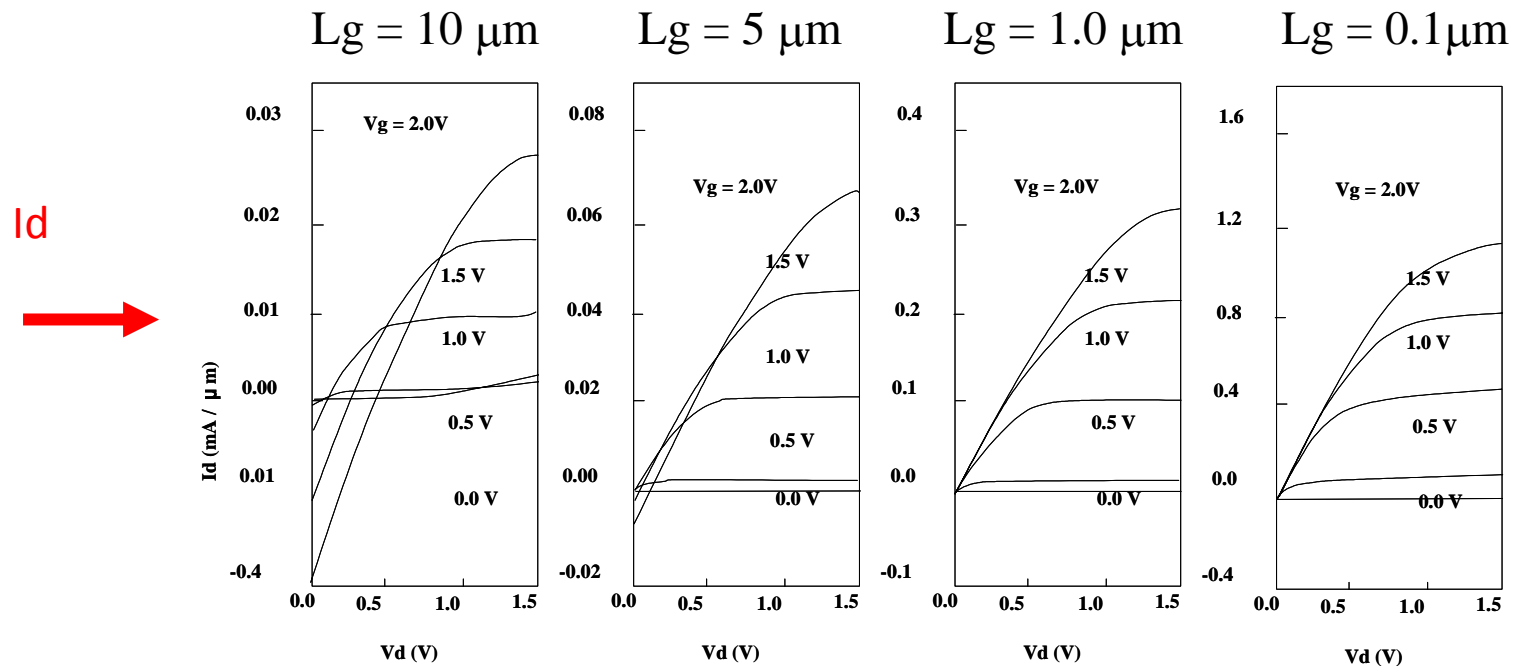


Gate leakage: $I_g \propto \text{Gate Area} \propto \text{Gate length (L}_g)$

Drain current: $I_d \propto 1/\text{Gate length (L}_g)$

$L_g \rightarrow$ small,

Then, $I_g \rightarrow$ small, $I_d \rightarrow$ large, Thus, $I_g/I_d \rightarrow$ very small



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

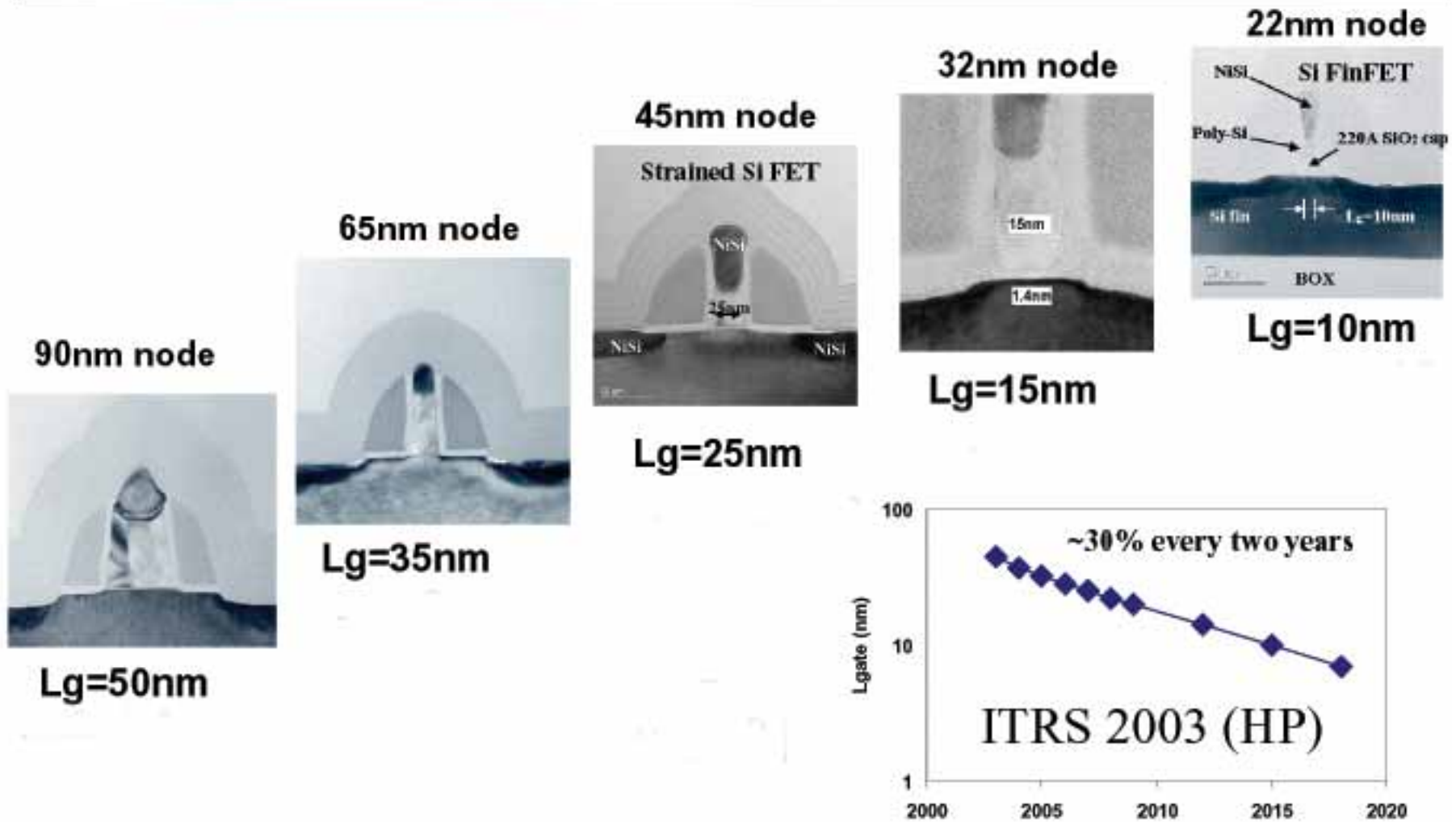
There would be a solution!

Think, Think, and Think!

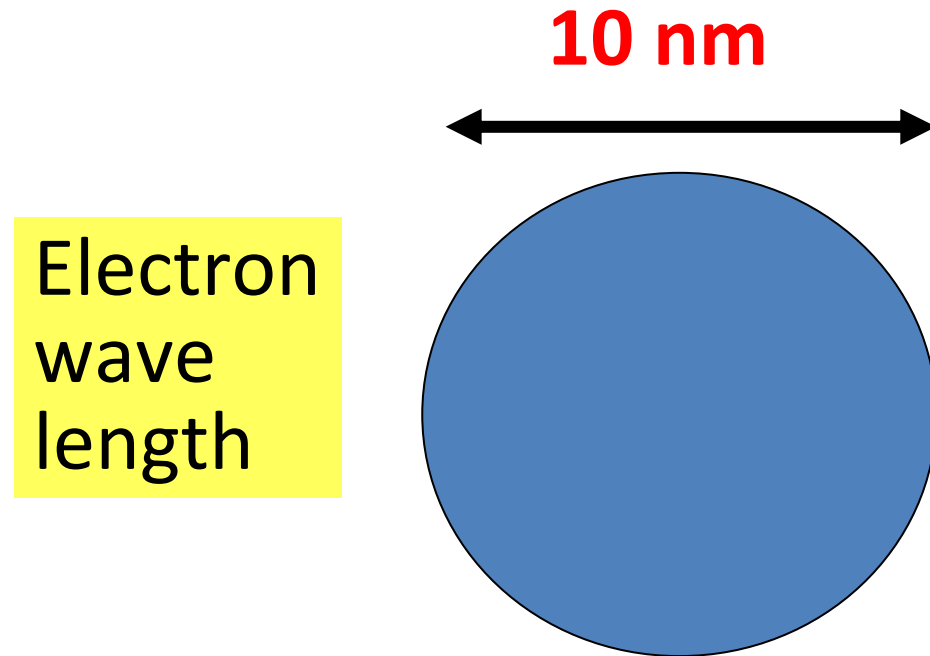
Or, Wait the time!

Some one will think for you

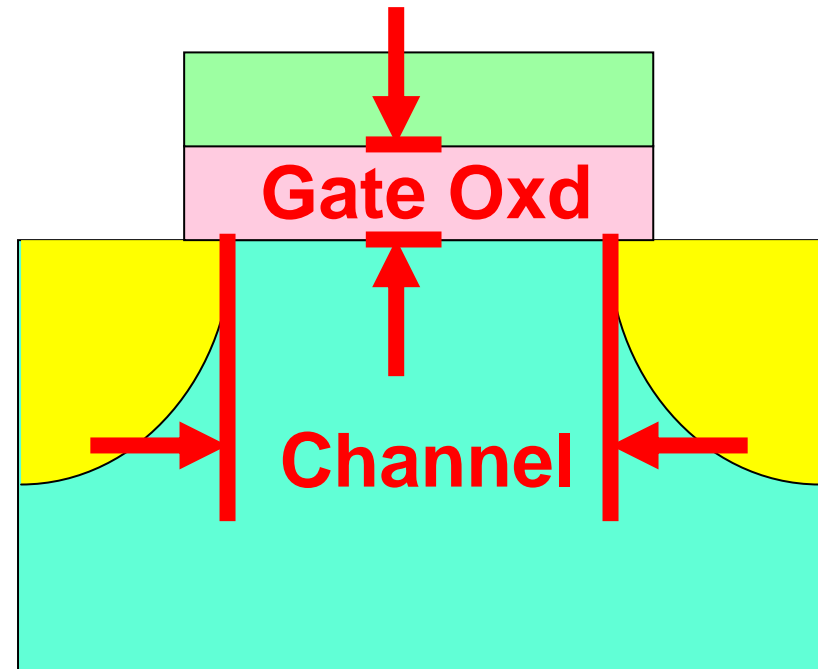
Transistor Scaling Continues



Downsizing limit?

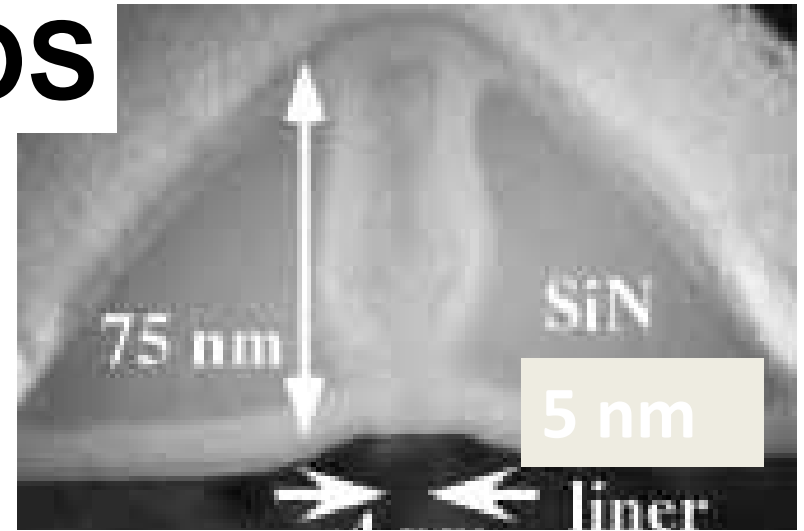


Channel length?

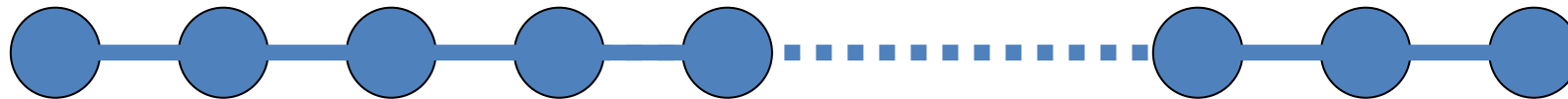


5 nm gate length CMOS

Is a Real Nano Device!!

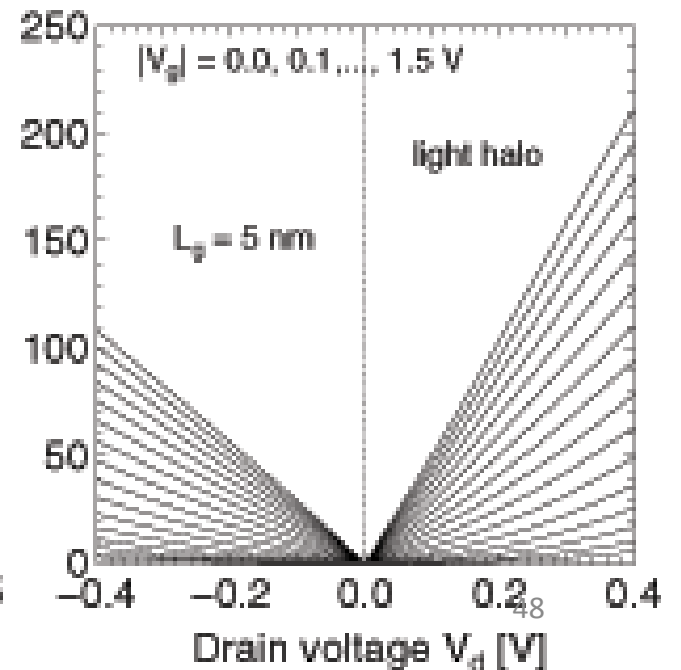
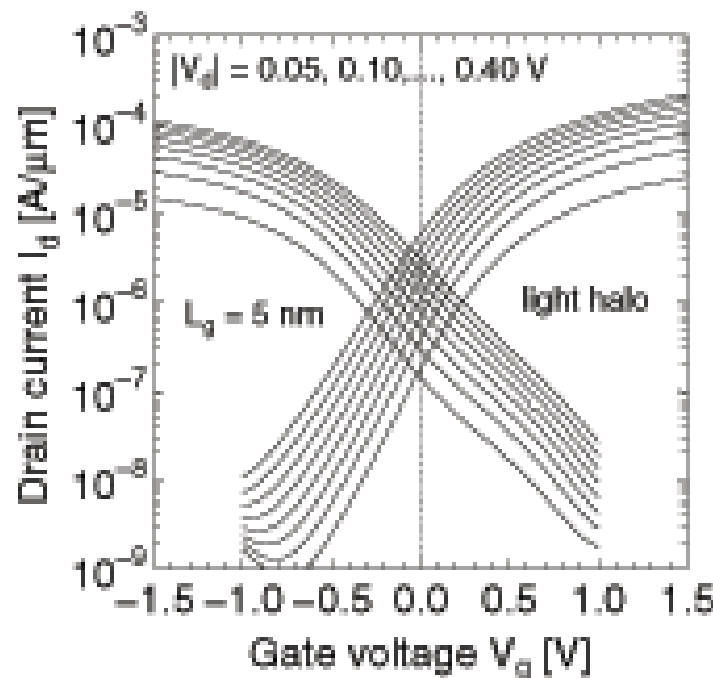


Length of 18 Si atoms



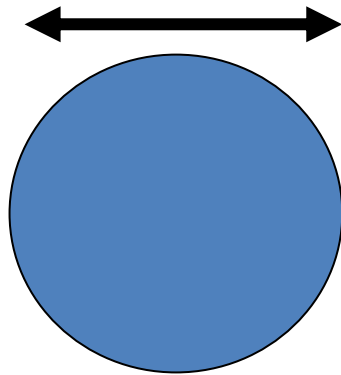
H. Wakabayashi
et.al, NEC

IEDM, 2003



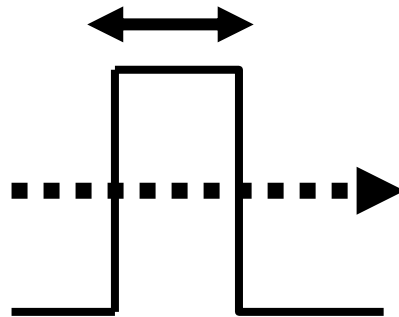
Electron
wave
length

10 nm



Tunneling
distance

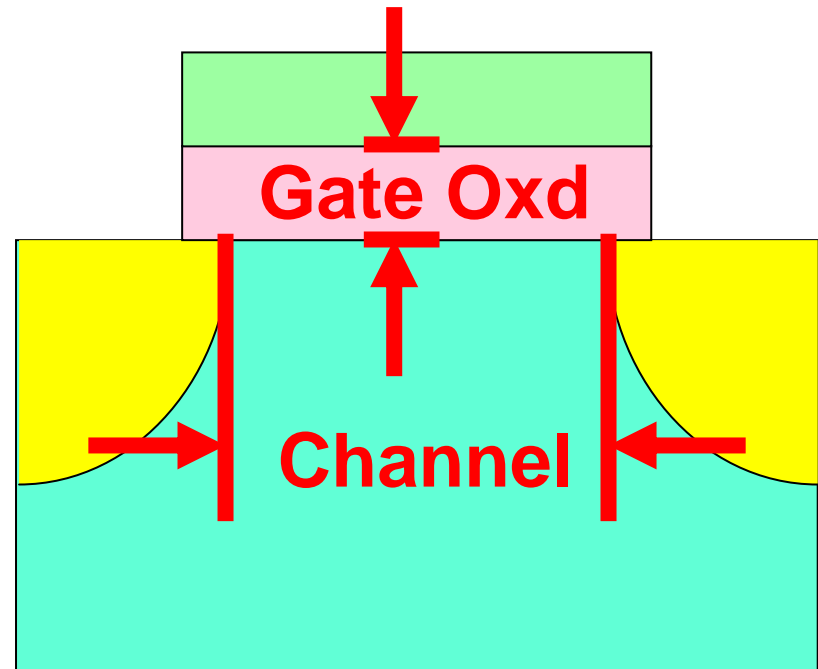
3 nm



Downsizing limit!

Channel length

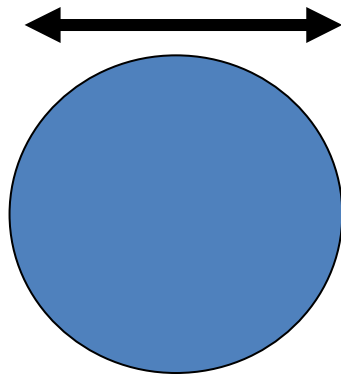
Gate oxide thickness



Prediction now!

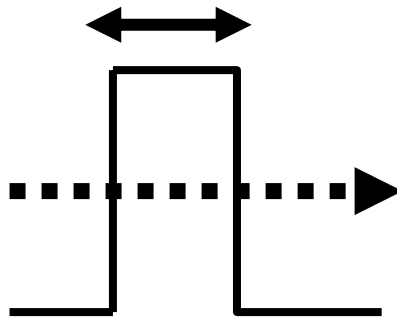
Electron
wave
length

10 nm



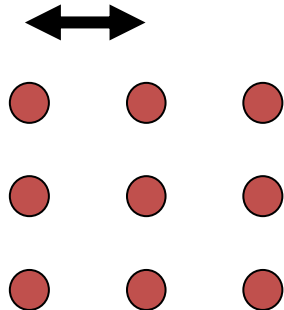
Tunneling
distance

3 nm



Atom
distance

0.3 nm

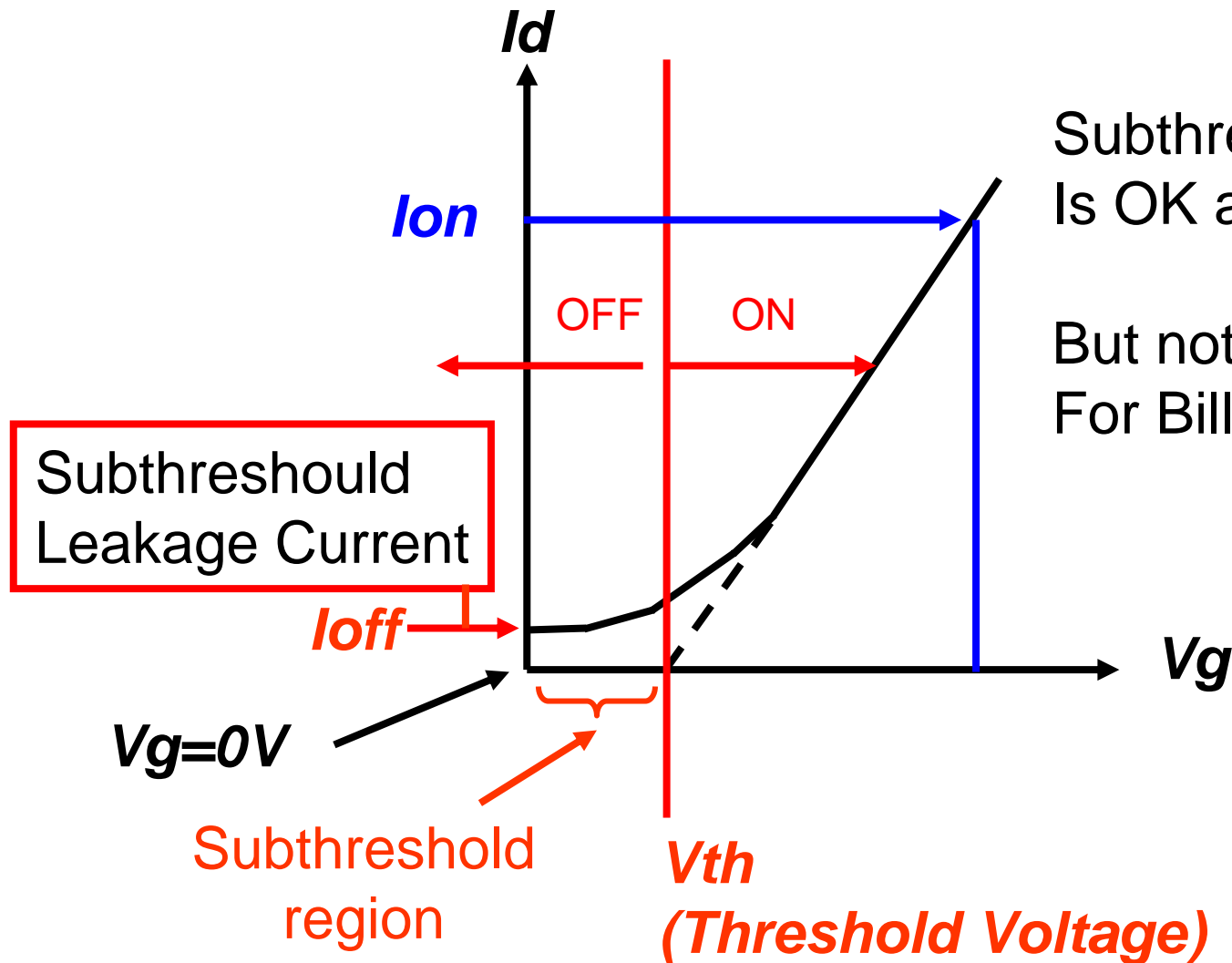


MOSFET operation

$L_g = 2 \sim 1.5 \text{ nm?}$

**Below this,
no one knows future!**

Subthreshold leakage current of MOSFET



Subthreshold Current
Is OK at Single Tr. level

But not OK
For Billions of Trs.

Vth cannot be decreased anymore

Log scale Id plot

significant Ioff increase

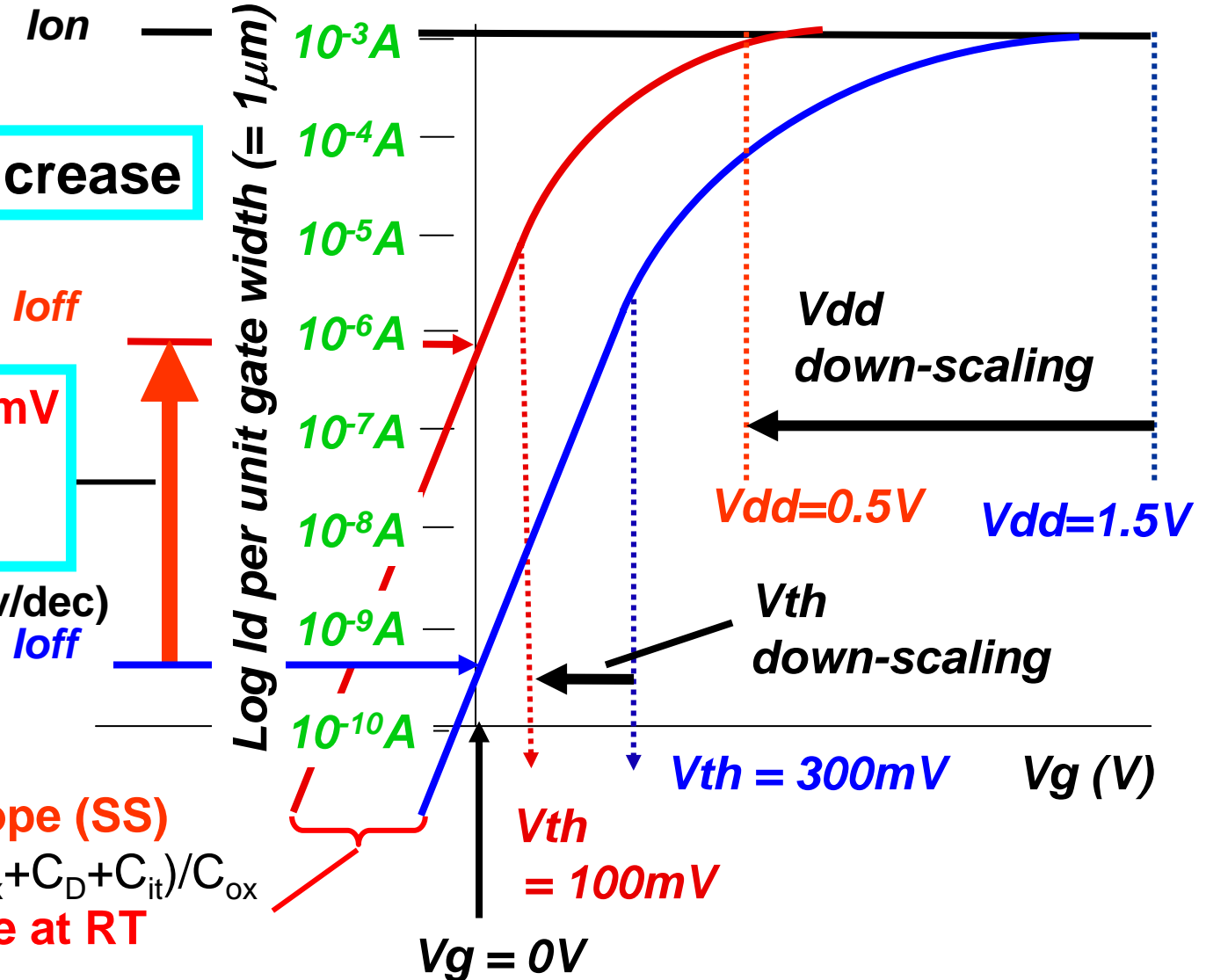
Vth: 300mV → 100mV
Ioff increases with 3.3 decades

$$(300 - 100)\text{mV} / (60\text{mV/dec}) = 3.3 \text{ dec}$$

Subthreshold slope (SS)
 $= (\ln 10)(kT/q)(C_{ox} + C_D + C_{it}) / C_{ox}$
 $> \sim 60 \text{ mV/decade at RT}$

SS value:

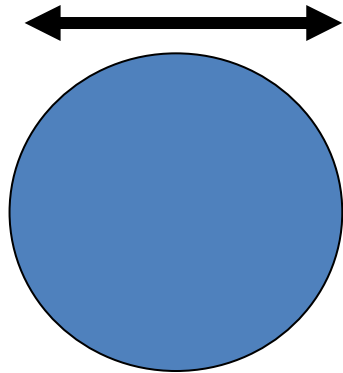
Constant and does not become small with down-scaling



Prediction now!

Electron wave length

10 nm

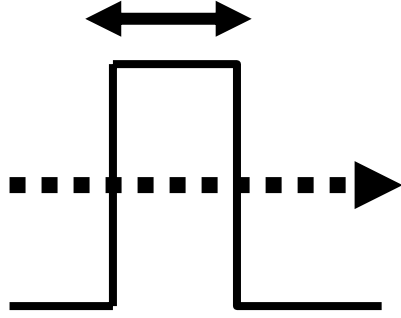


Practical limit for integration

$L_g = 5 \text{ nm?}$

Tunneling distance

3 nm

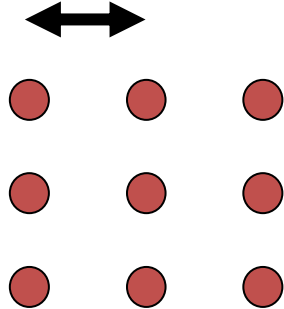


MOSFET operation

$L_g = 2 \sim 1.5 \text{ nm?}$

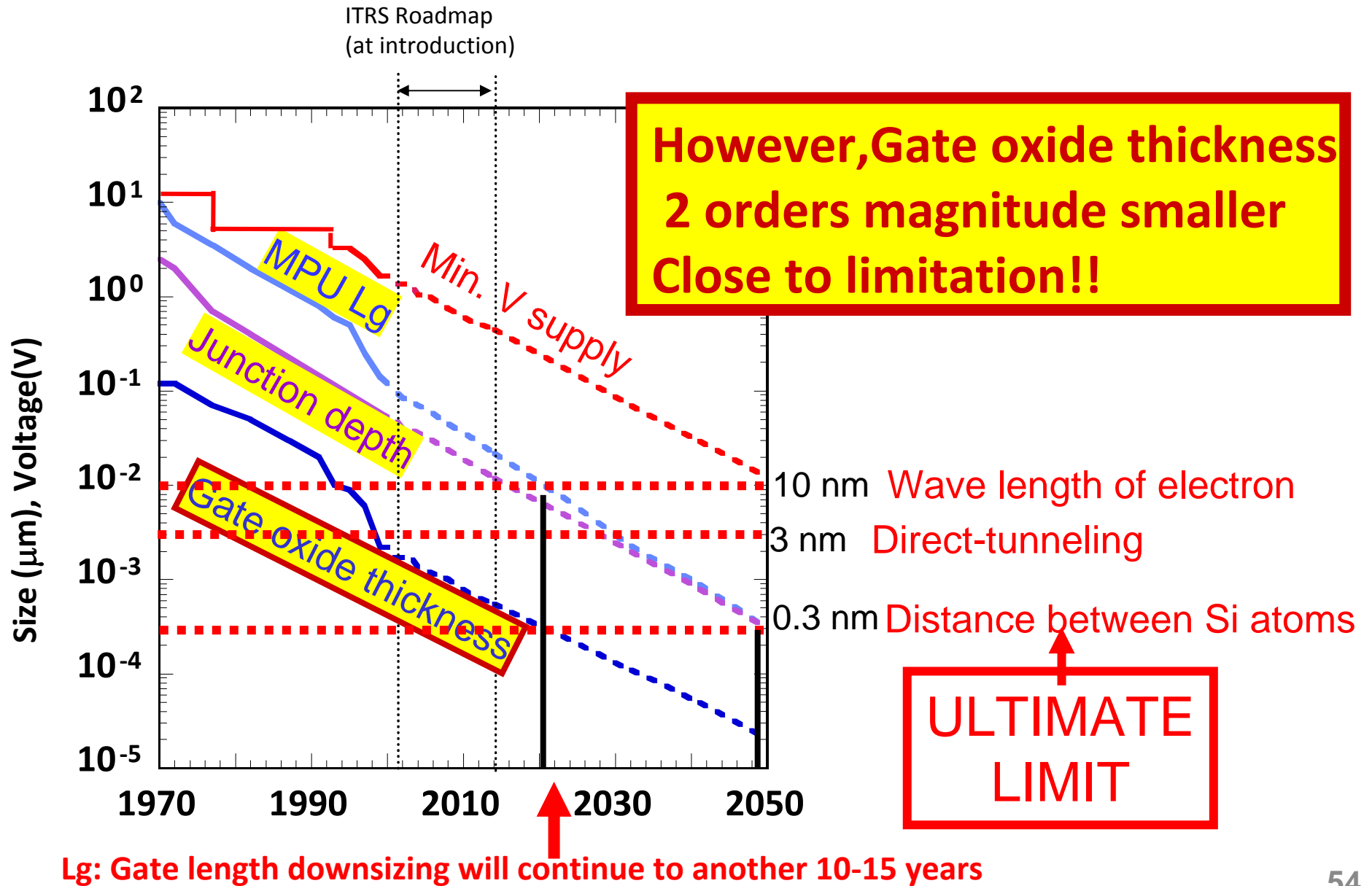
Atom distance

0.3 nm



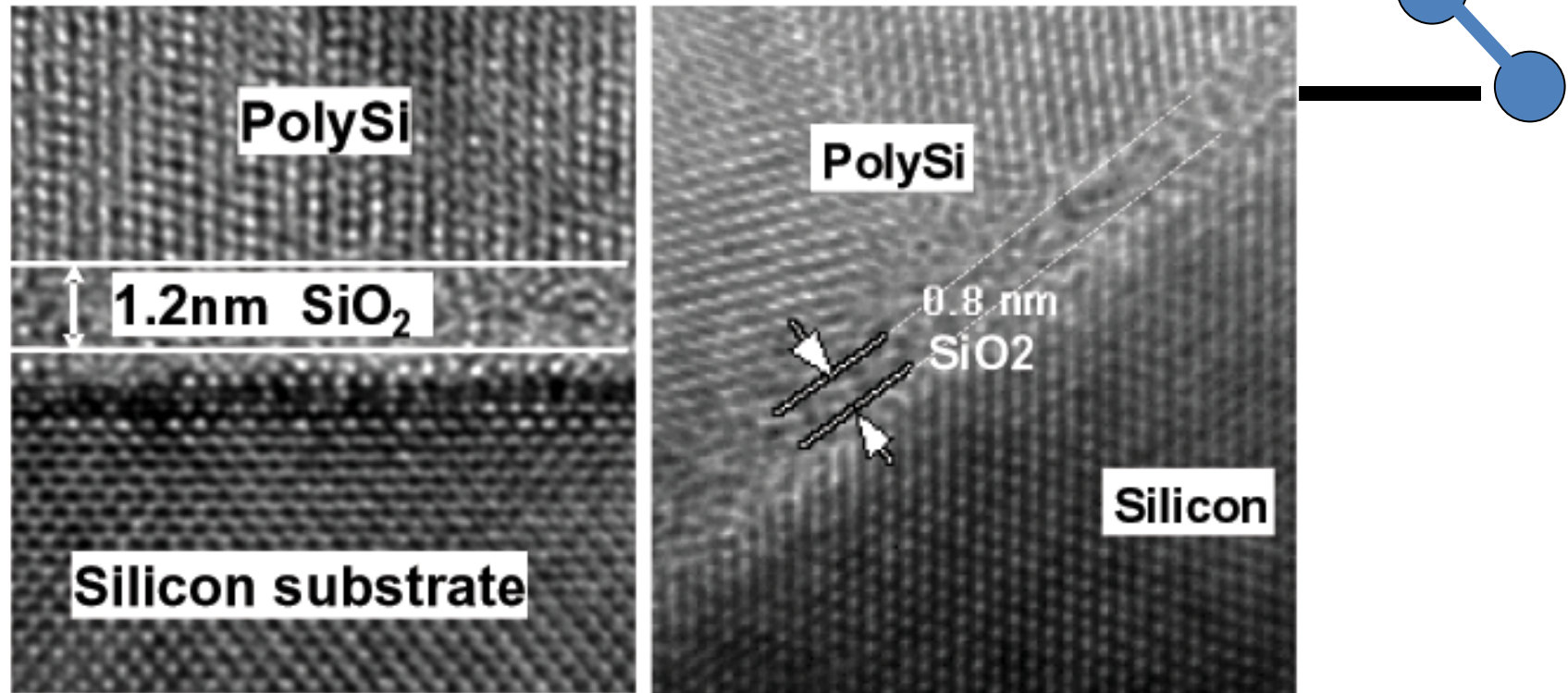
Below this, no one knows future!

Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO₂ in production (90nm logic node)
- 0.8nm physical SiO₂ in research transistors

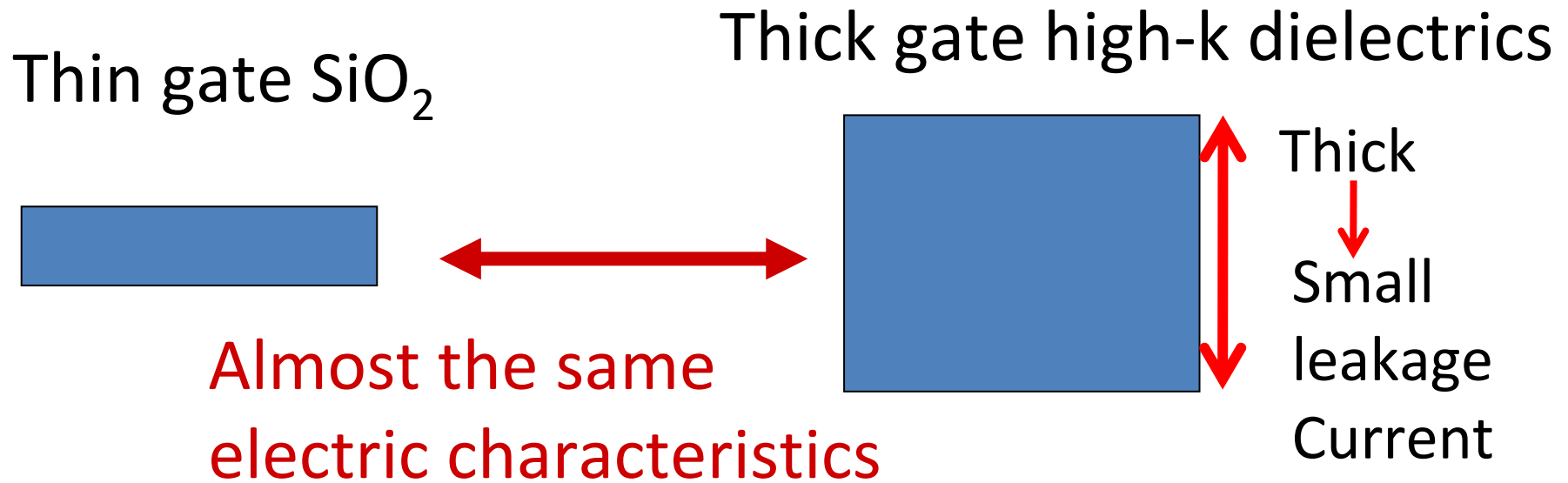
By Robert Chau, IWGI 2003

So, we are now in the limitation
of downsizing?

Do you believe this or do not?

There is a solution! **K: Dielectric Constant**

To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO₂!

Choice of High-k elements for oxide

Candidates 														Gas or liquid at 1000 K											
Unstable at Si interface														Radio active											
H																				He					
Li	Be																			B	C	N	O	F	Ne
Na	Mg																			Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fc	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr								
Rh	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rb	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe								
Cs	Ba		Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn								
Fr	Ra			Rf	Ha	Sg	Ns	Hs	Mt																
		La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu									
		Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr									

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in

- 1) band-offset,**
- 2) dielectric constant**
- 3) thermal stability**

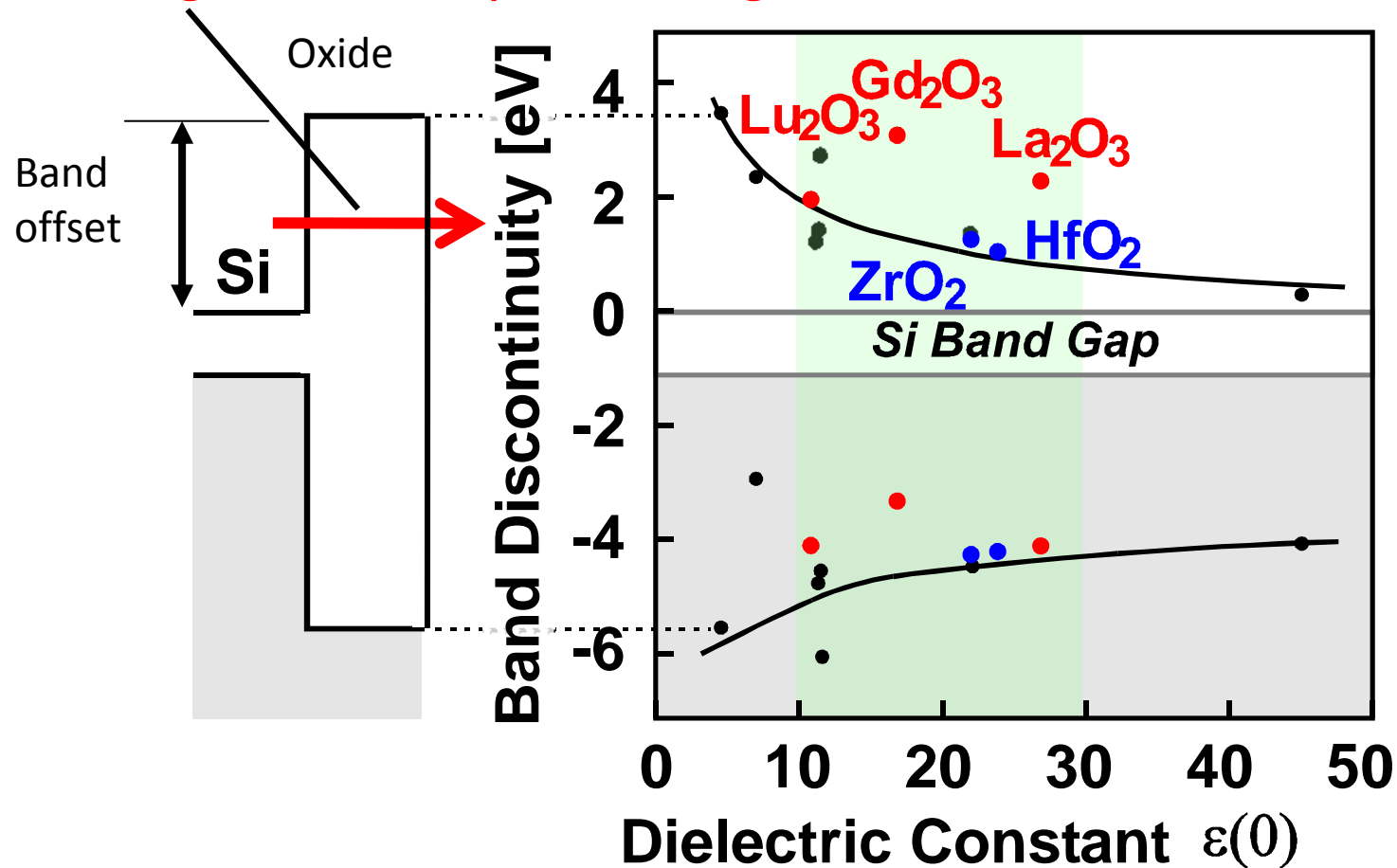
La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

Conduction band offset vs. Dielectric Constant

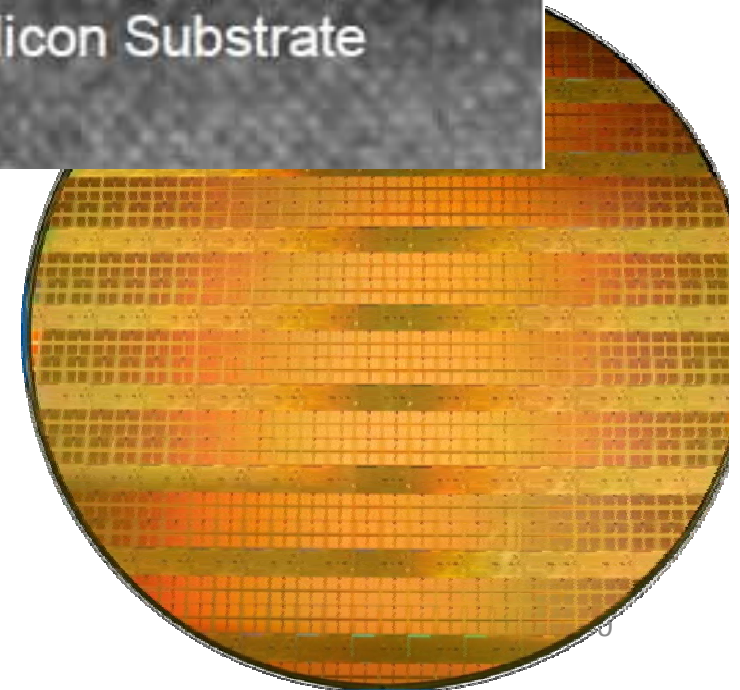
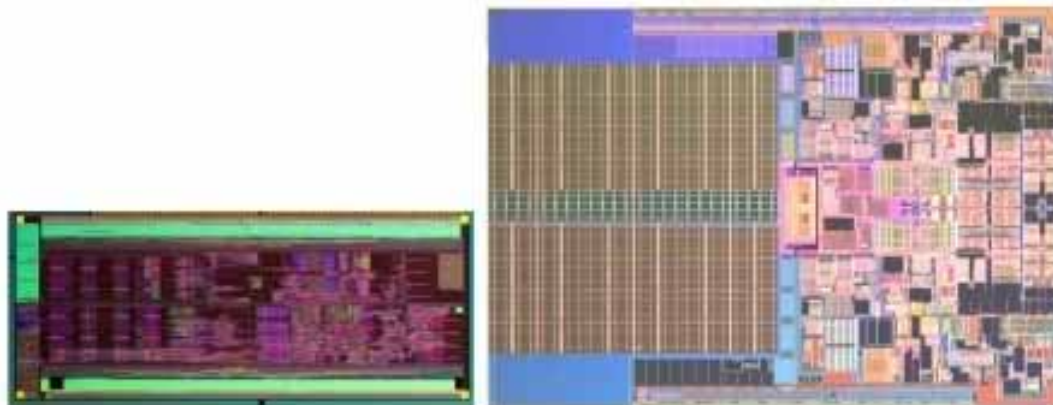
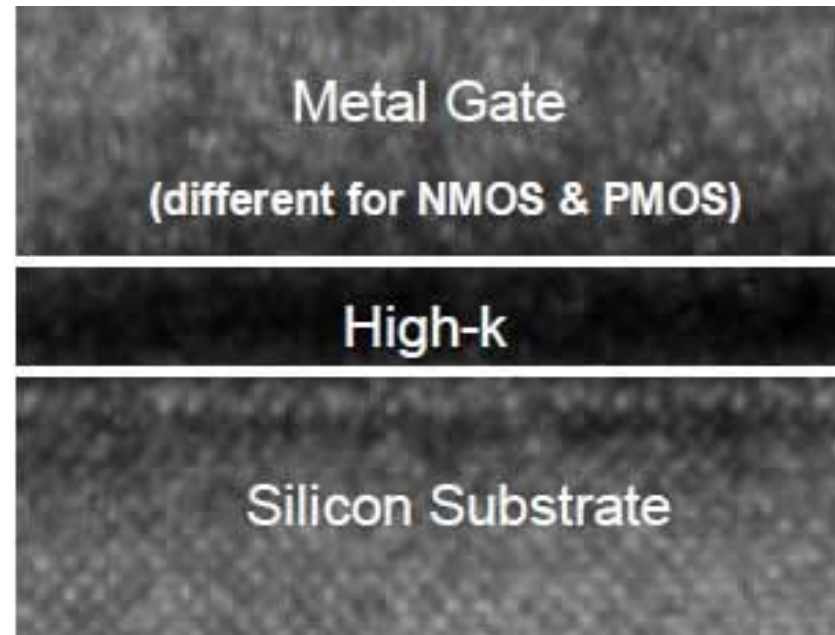
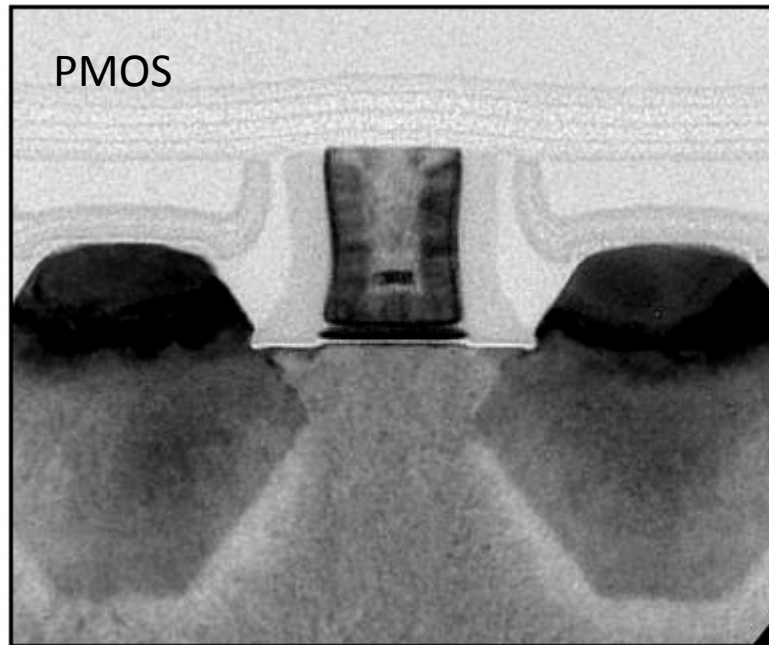
Leakage Current by Tunneling

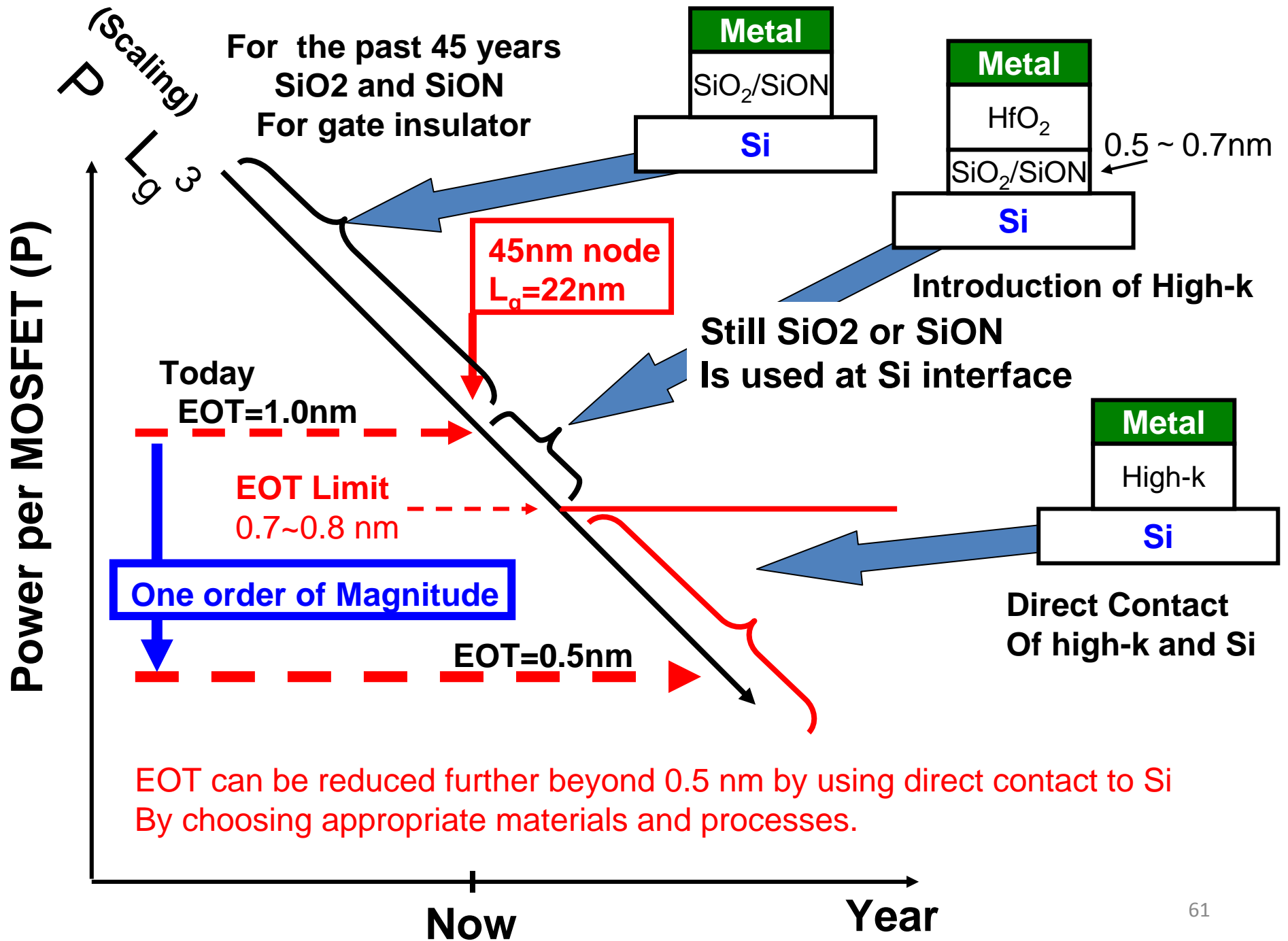


XPS measurement by Prof. T. Hattori, INFOS 2003

High-k gate insulator MOSFETs for Intel: EOT=1nm

EOT: Equivalent Oxide Thickness





Choice of High-k elements for oxide

Candidates														Gas or liquid at 1000 K					
Unstable at Si interface														Radio active					
H														He					
Li	Be													B	C	N	O	F	Ne
Na	Mg													Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr		
Rh	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rb	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe		
Cs	Ba		Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn		
Fr	Ra		Rf	Ha	Sg	Ns	Hs	Mt											
		La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu			
		Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr			

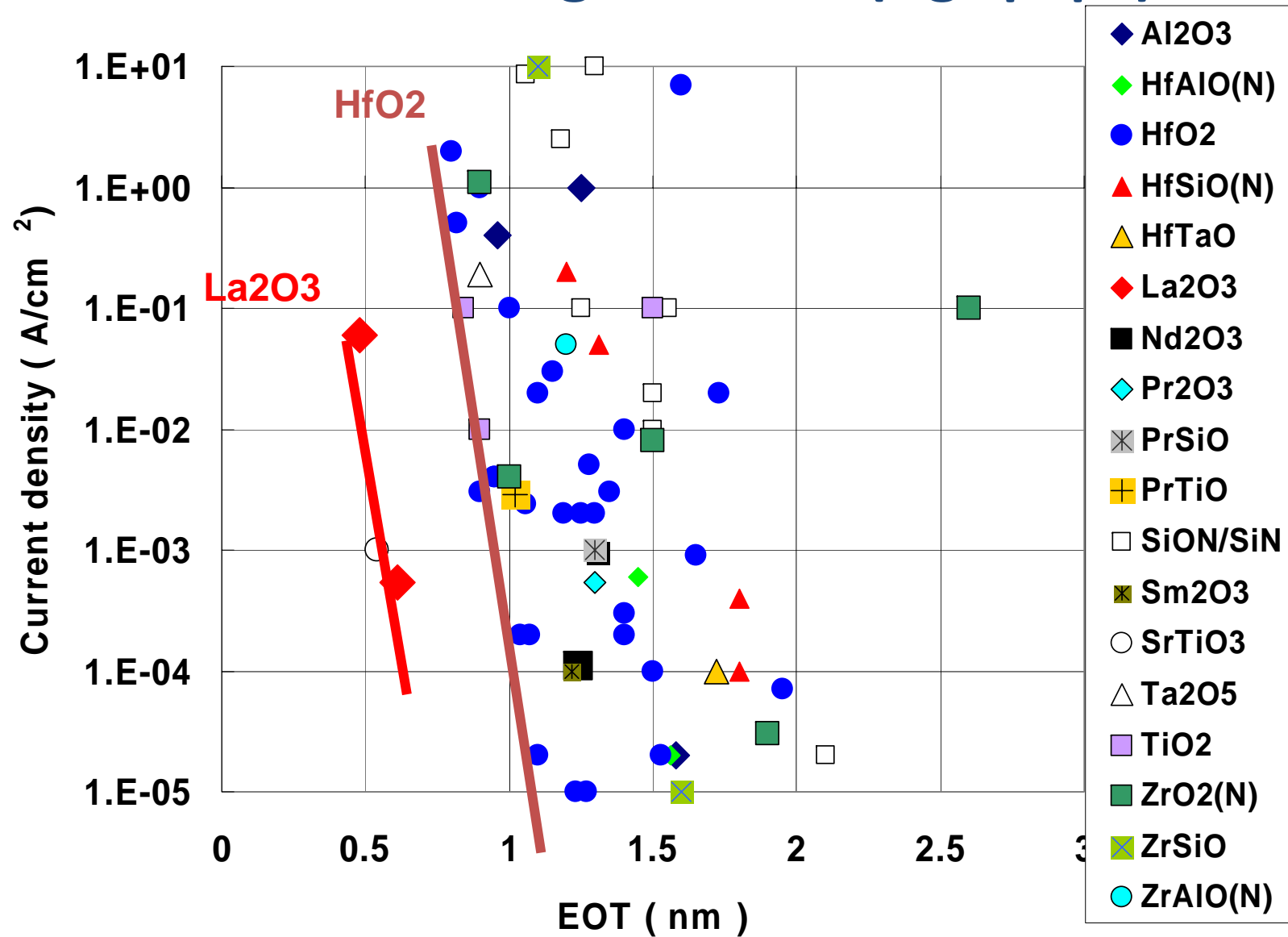
HfO₂ based dielectrics are selected as the first generation materials, because of their merit in

- 1) band-offset,
- 2) dielectric constant
- 3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
 Hubbard and Schlom, J Mater Res 11 2757 (1996)

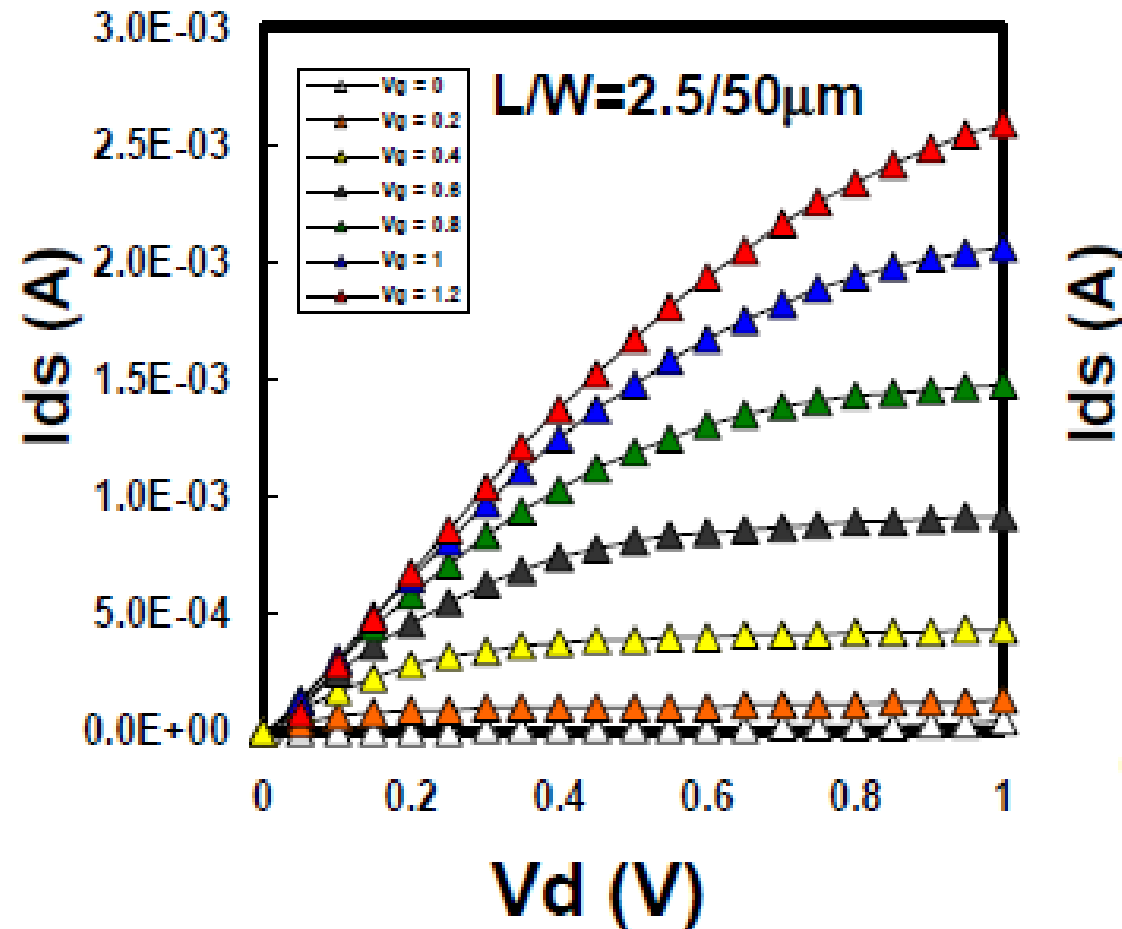
Gate Leakage vs EOT, ($V_g = |1|V$)



EOT = 0.48 nm

Our results

Transistor with La₂O₃ gate insulator



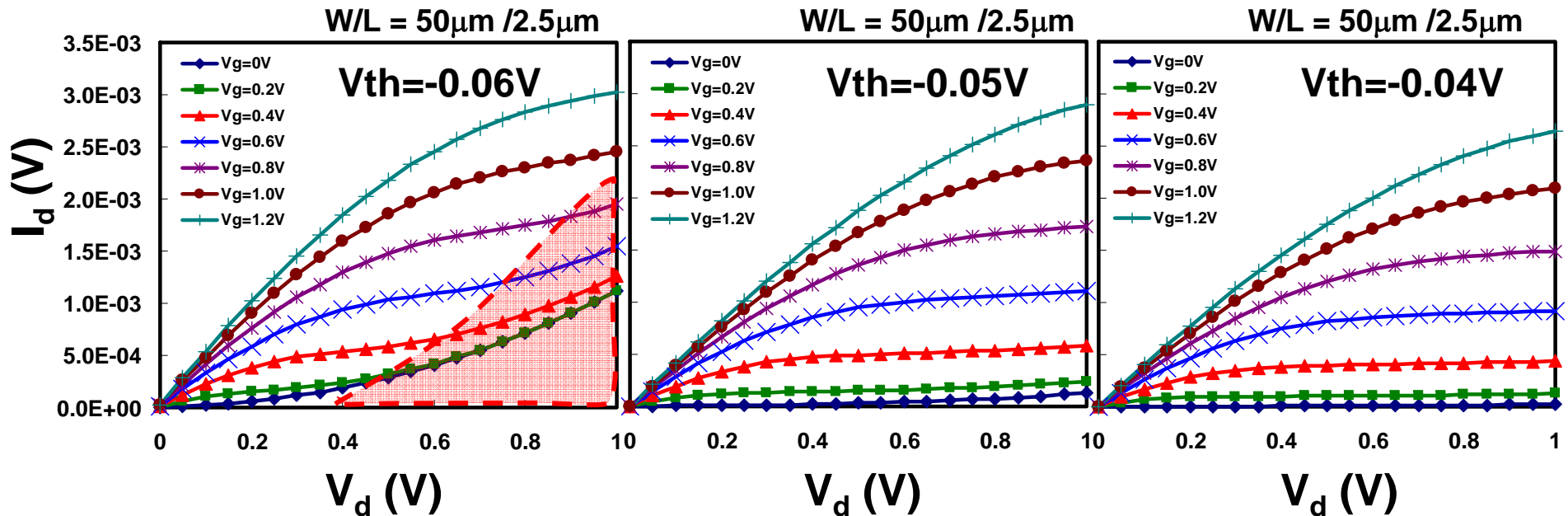
EOT=0.37nm

La2O3

EOT=0.37nm

EOT=0.40nm

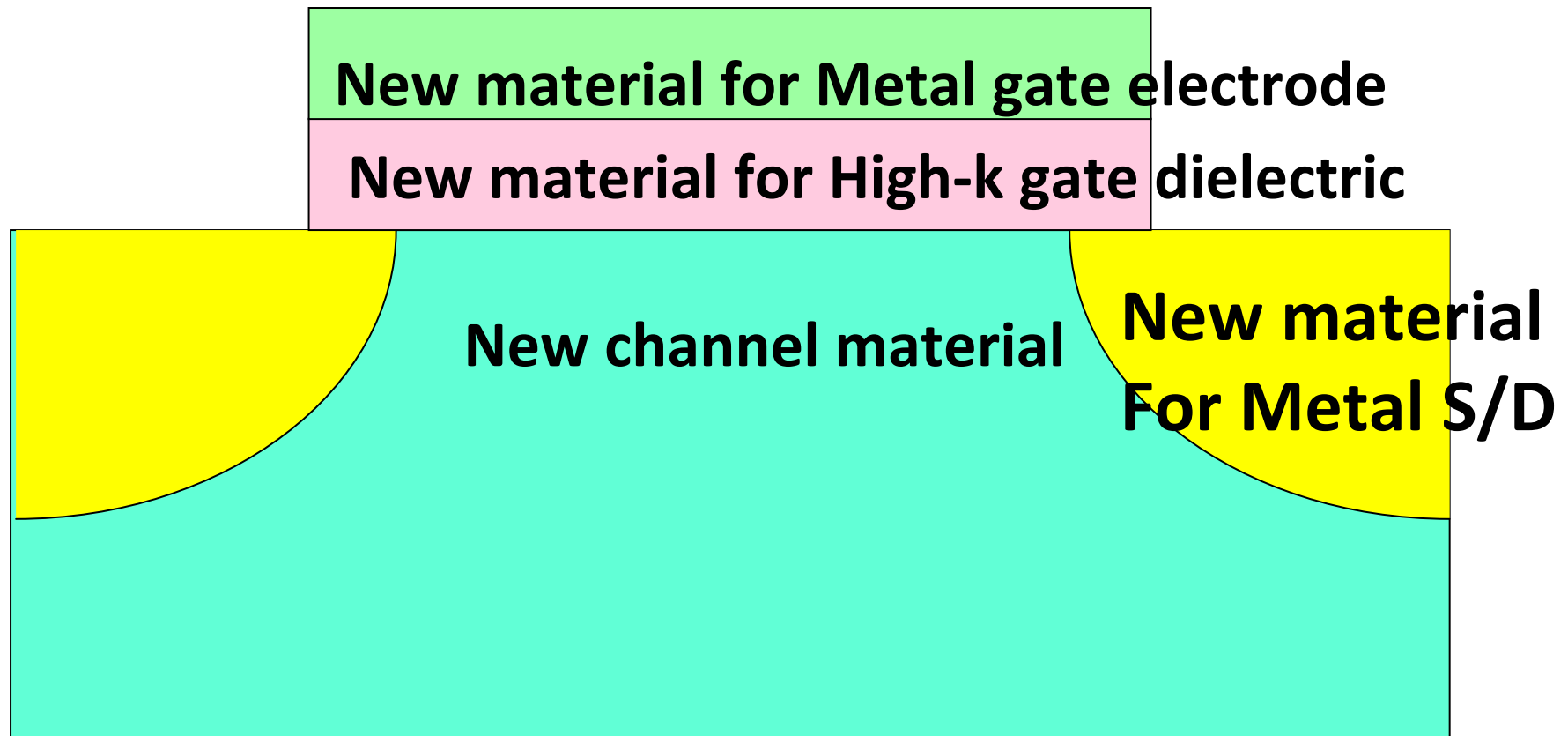
EOT=0.48nm



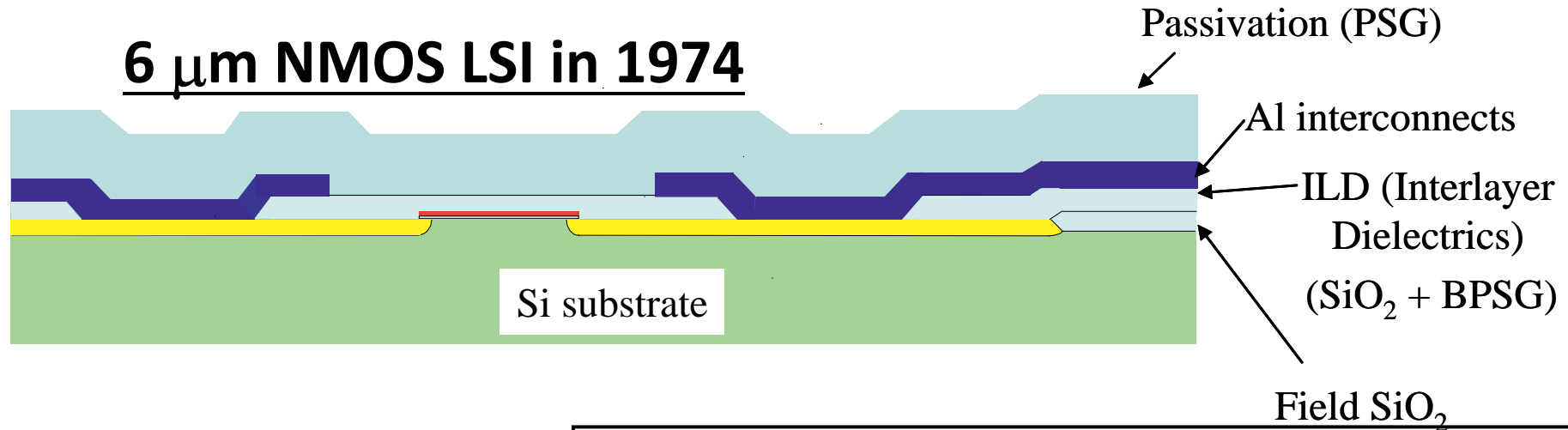
0.48 \rightarrow 0.37nm Increase of I_d at 30%

New material research will give us many future possibilities and the most important for Nano-CMOS!

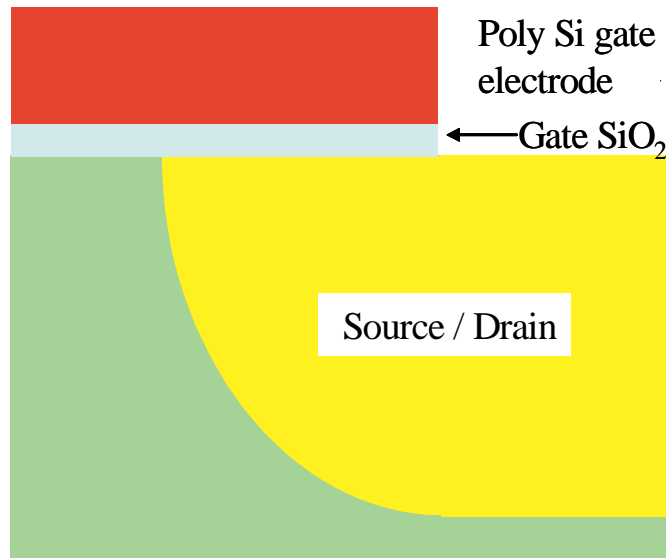
Not only for high-k!



6 μm NMOS LSI in 1974



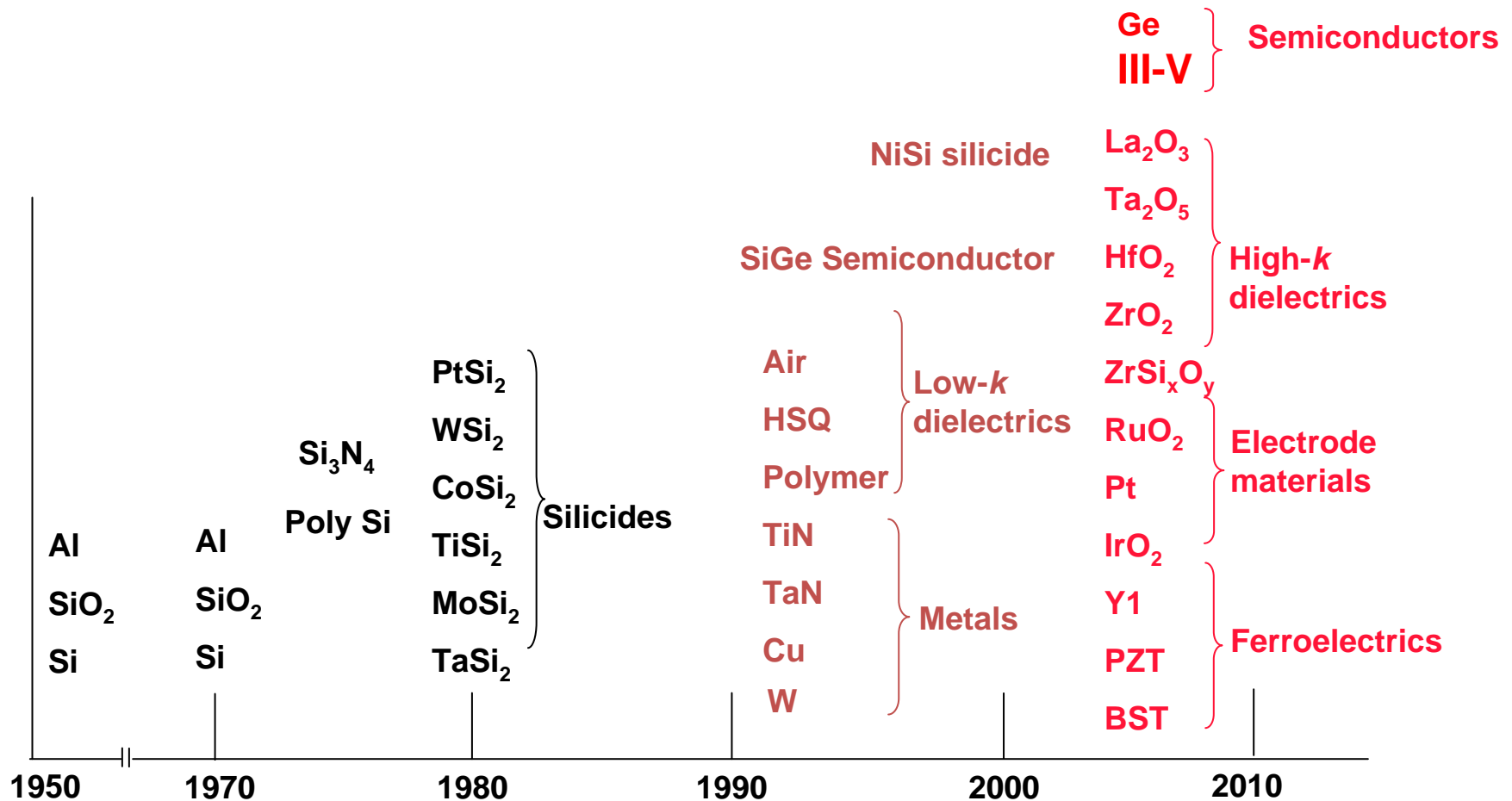
magnification



<u>Layers</u>	<u>Materials</u>	<u>Atoms</u>
1. Si substrate	1. Si	1. Si
2. Field oxide	2. SiO ₂	2. O
3. Gate oxide	3. BPSG	3. P
4. Poly Si	4. Al	4. B
5. S/D	5. PSG	5. Al
6. Interlayer		(H, N, Cl)
7. Aluminum		
8. Passivation		

New materials

Just examples!
Many other candidates

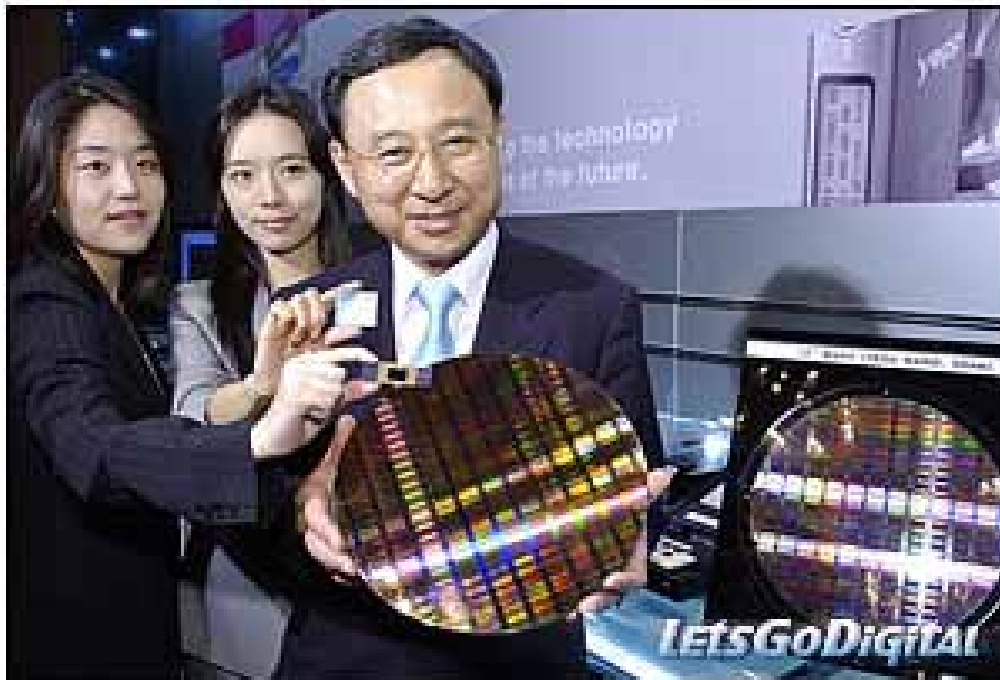


Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Now: After 45 Years from the 1st single MOSFETs

*32 Gb and 16Gb NAND,
SAMSUNG*



NAND flash trend

Capacity	Node	1 st Fabrication	Production
512Mbit	120nm	2000	2001
1Gbit	100nm	2001	2002
2Gbit	90nm	2002	2003
4Gbit	70nm	2003	2004
8Gbit	60nm	2004	2005
16Gbit	50nm	2005	2006
32Gbit	40nm	2006	2008

Even Tbit would be possible in future!

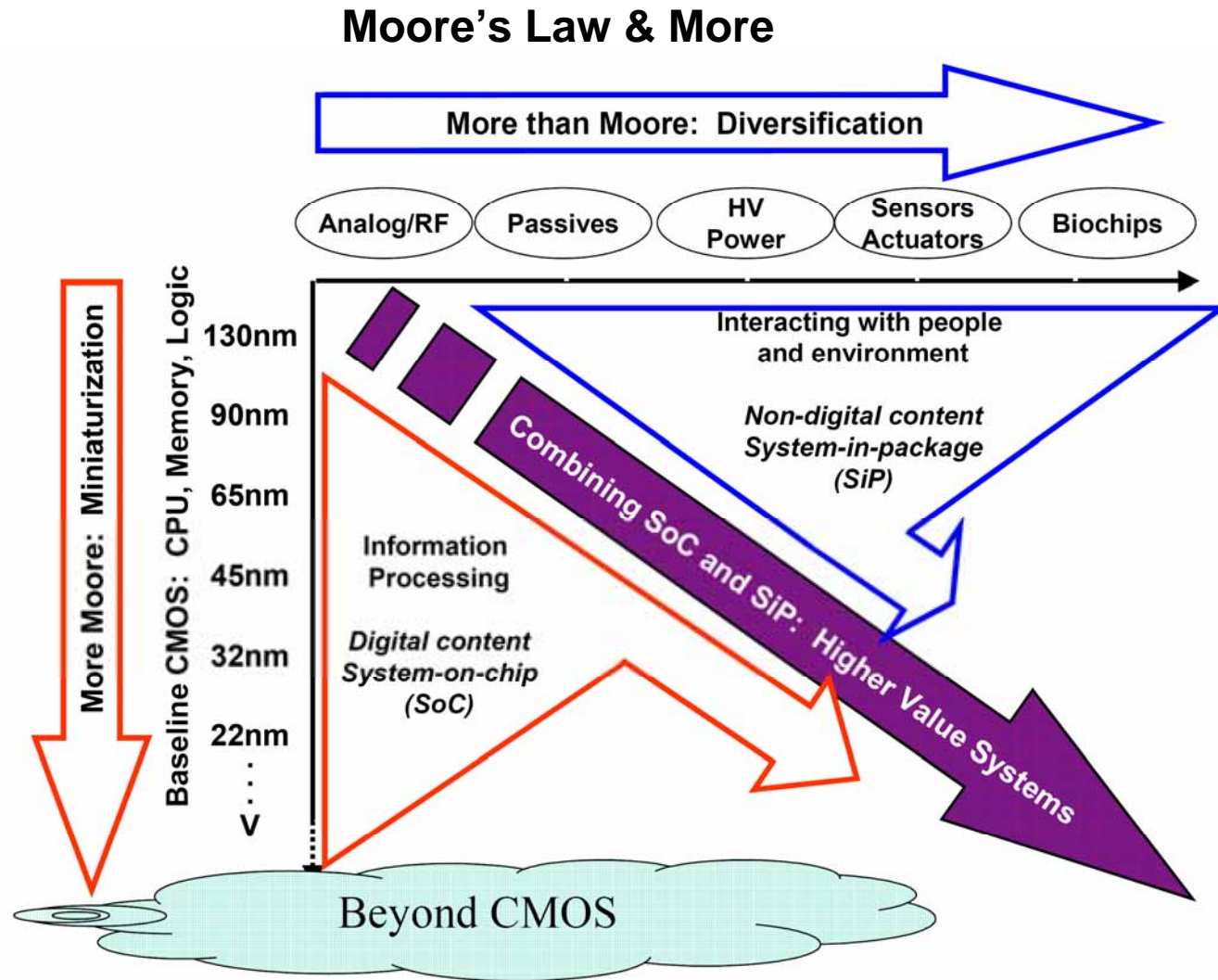
Already 32 Gbit:

larger than that of world population
comparable for the numbers of neurons
in human brain

256Gbit: larger than those of # of stars in galaxies



More Moore and More than Moore

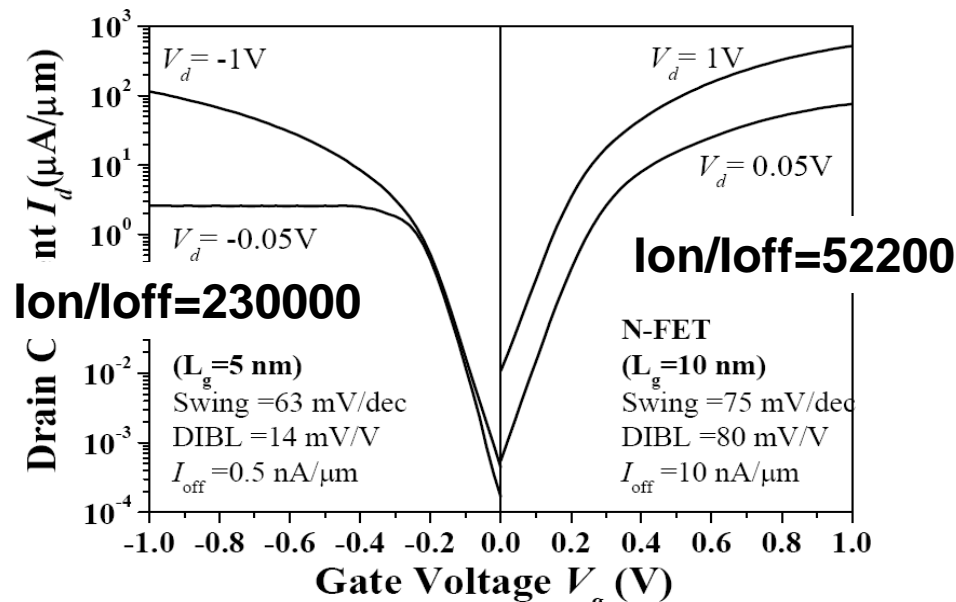
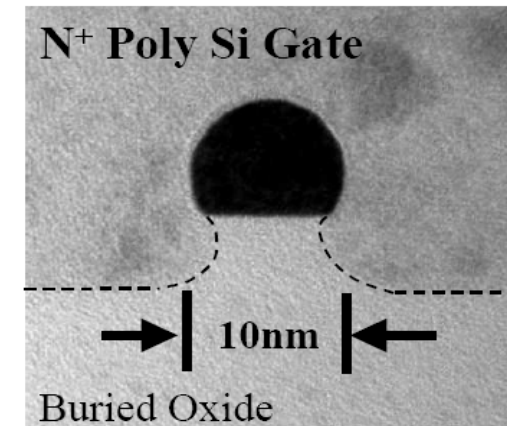
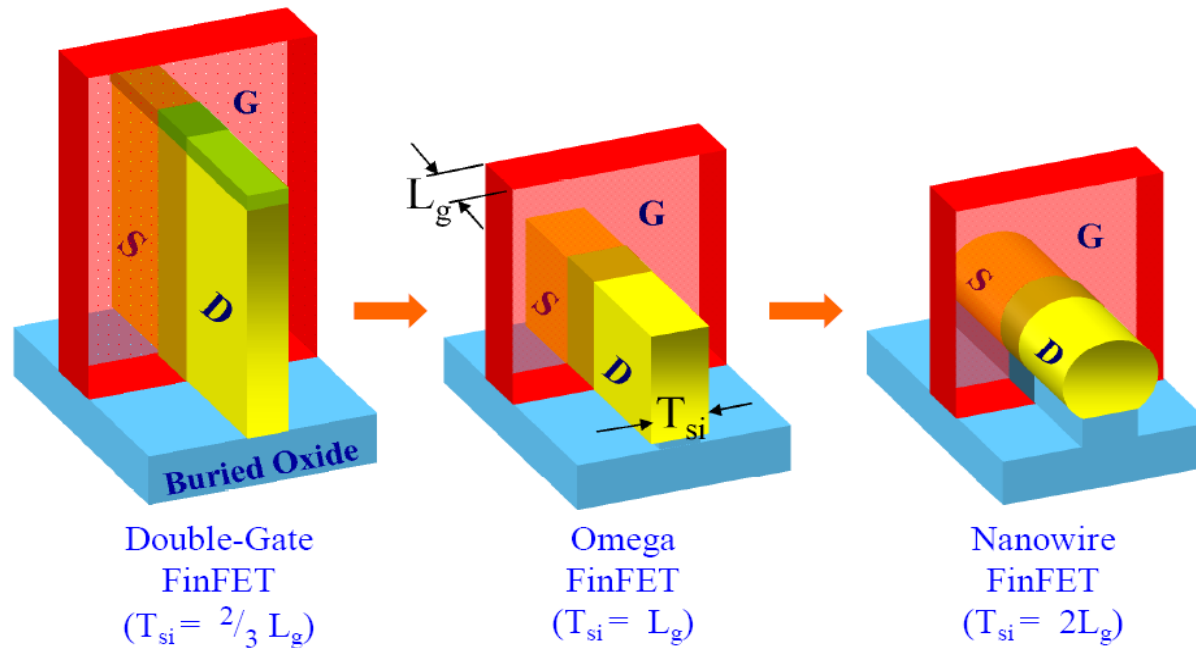


Question what is the other side of the cloud?

ITRS 2005 Edition

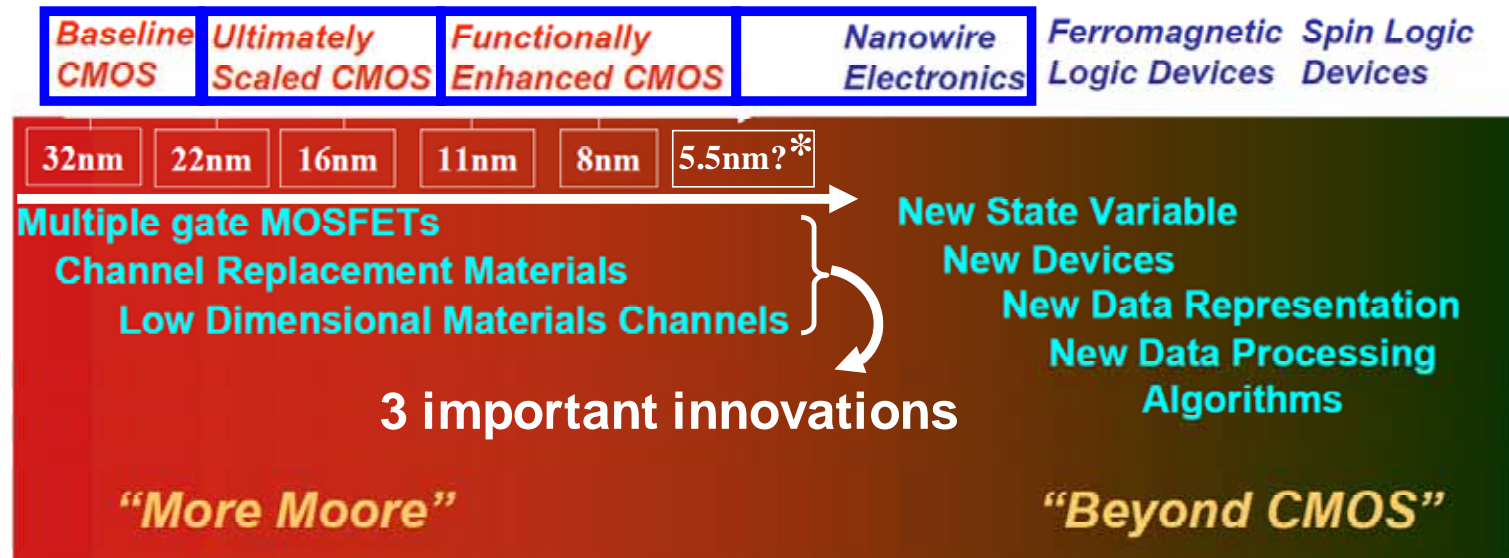
http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

FinFET to Nanowire



Channel conductance is well controlled by Gate even at $L=5\text{nm}$

- There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).
- Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher I_{d-sat} under low V_{dd} .
- Two candidates have emerged for R & D
 1. Nanowire/tube MOSFETs
 2. Alternative channel MOSFETs (III-V, Ge)
- Other Beyond CMOS devices are still in the cloud.



ITRS figure edited by Iwai

Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

Source: Y. Lee., T. Nagata., K. Kakushima., K. Shiraishi, and H. Iwai, IWDTF 2008, Tokyo, November, 2008

Trade off

Carrier scattering probability

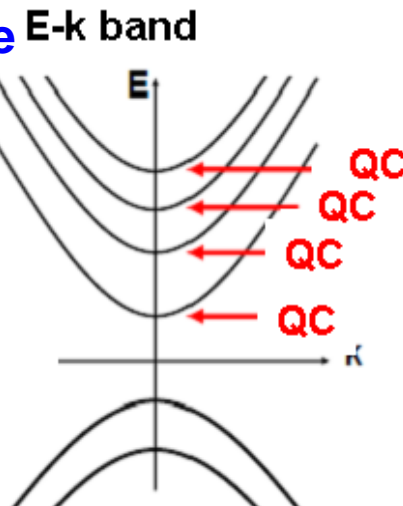
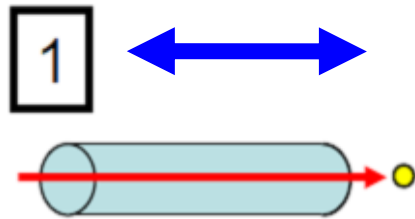
Small

Large

of quantum channel

Small

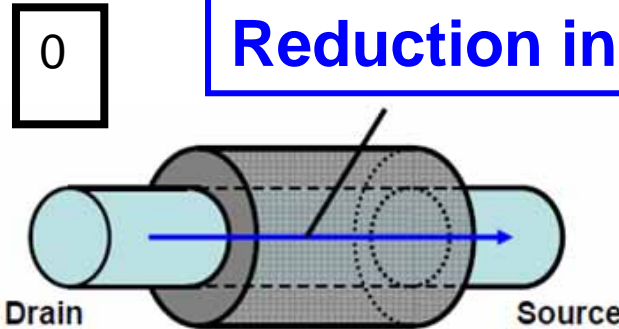
Large



High Conduction (1D)
 $G_0 = 77.8 \mu S / \text{wire}$

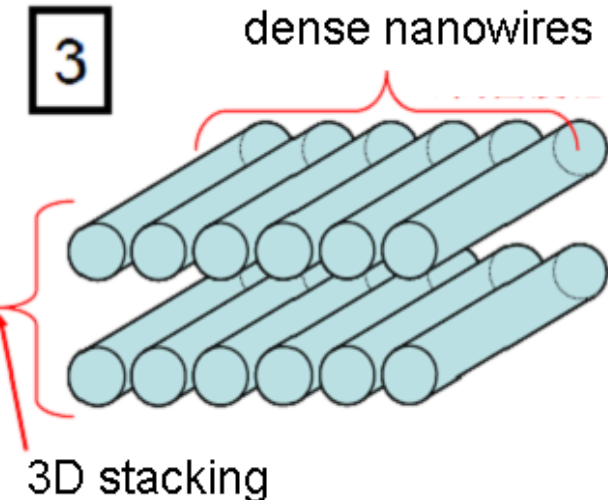
Multiple quantum channel (QC) used for conduction

Reduction in I_{off} (I_{sd} -leak)



Good control of I_{sd} -leak by surrounding gate

Increase in I_{on} (I_{d-sat})



High-density lateral and vertical integration

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1 . Use 1D ballistic conduction

M2 . Increase number of quantum channel

M3 . Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of I_{off} , the Nanowire/tube is also good.

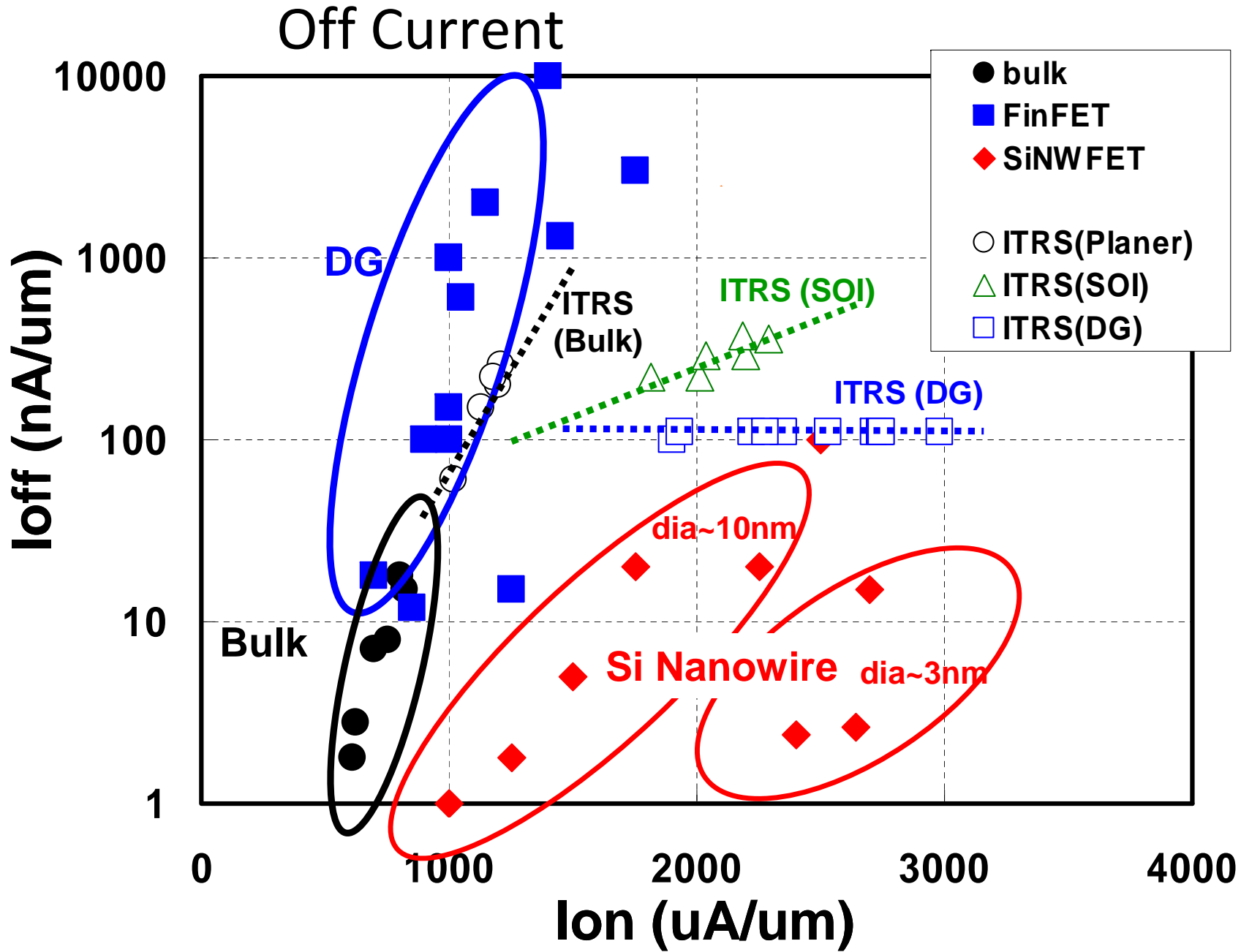
1D conduction per one quantum channel:

$$G = 2e^2/h = 77.8 \mu\text{S/wire or tube}$$

regardless of gate length and channel material

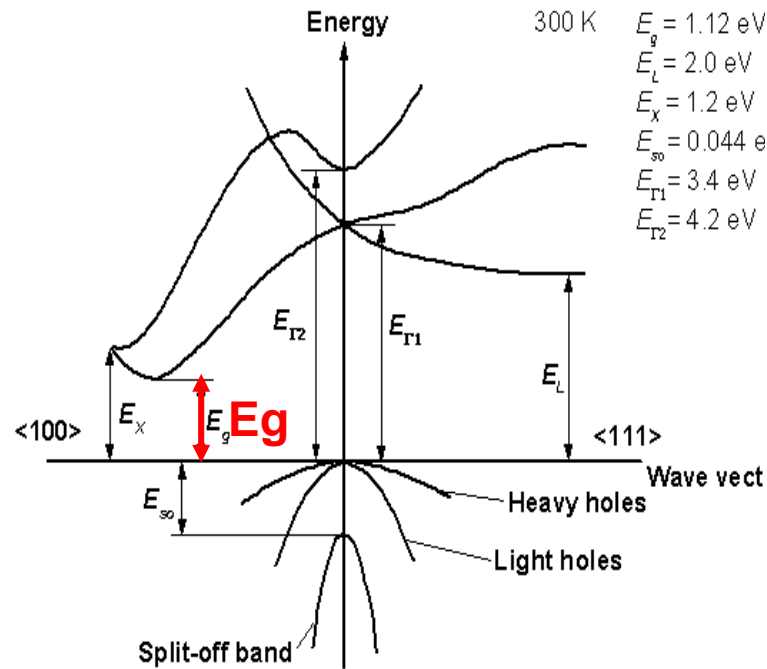
That is $77.8 \mu\text{A/wire}$ at 1V supply

This an extremely high value

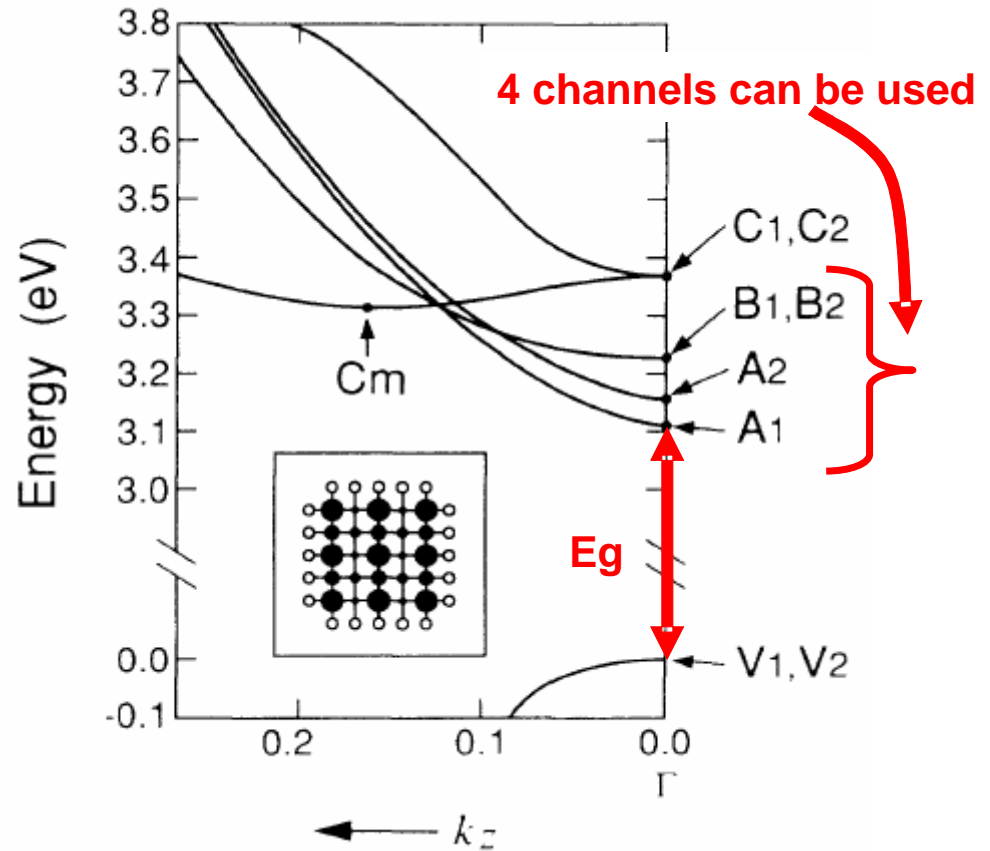


Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



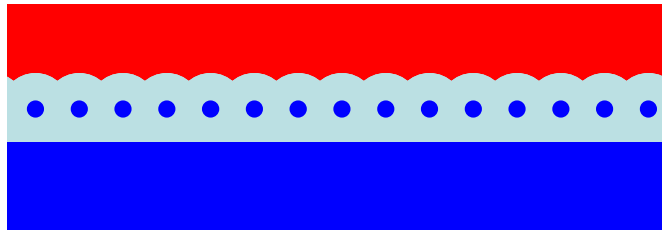
Energy band of Bulk Si



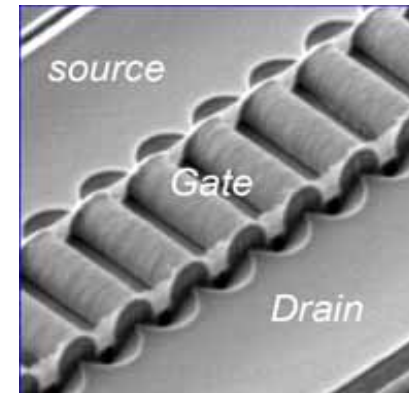
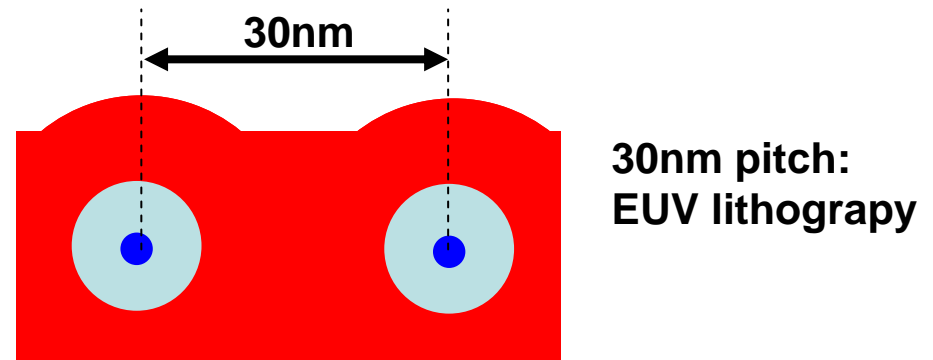
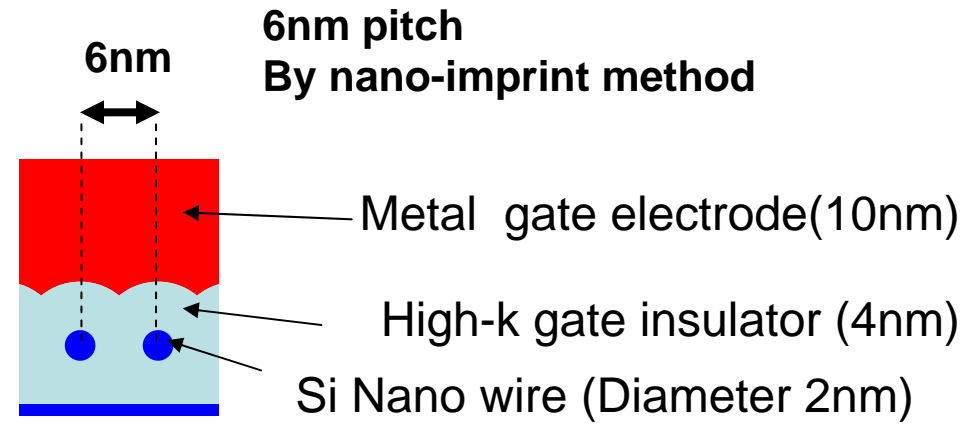
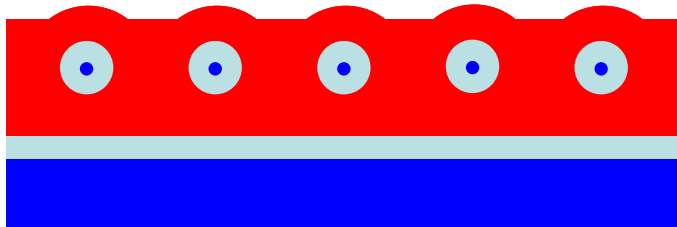
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

Front gate type MOS 165 wires / μm

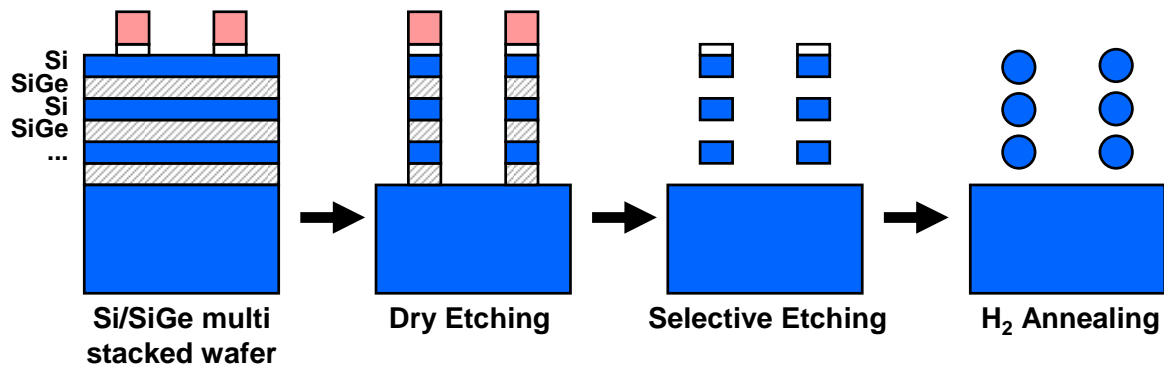
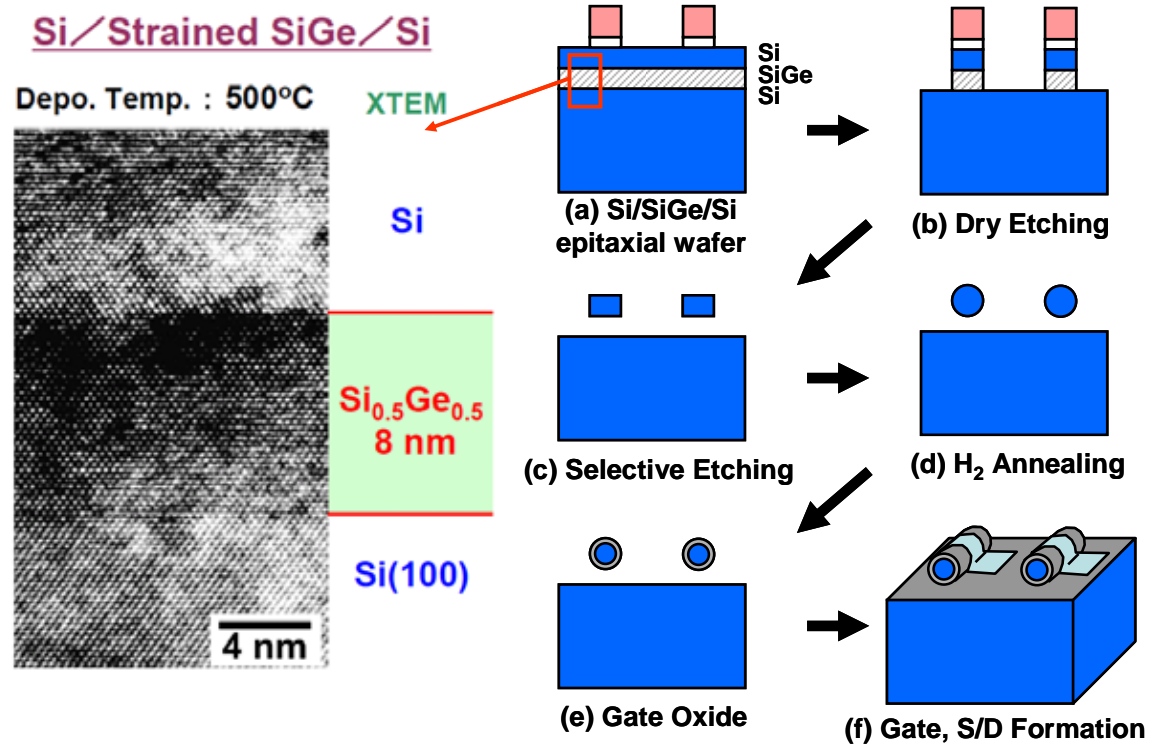


Surrounded gate type MOS 33 wires / μm

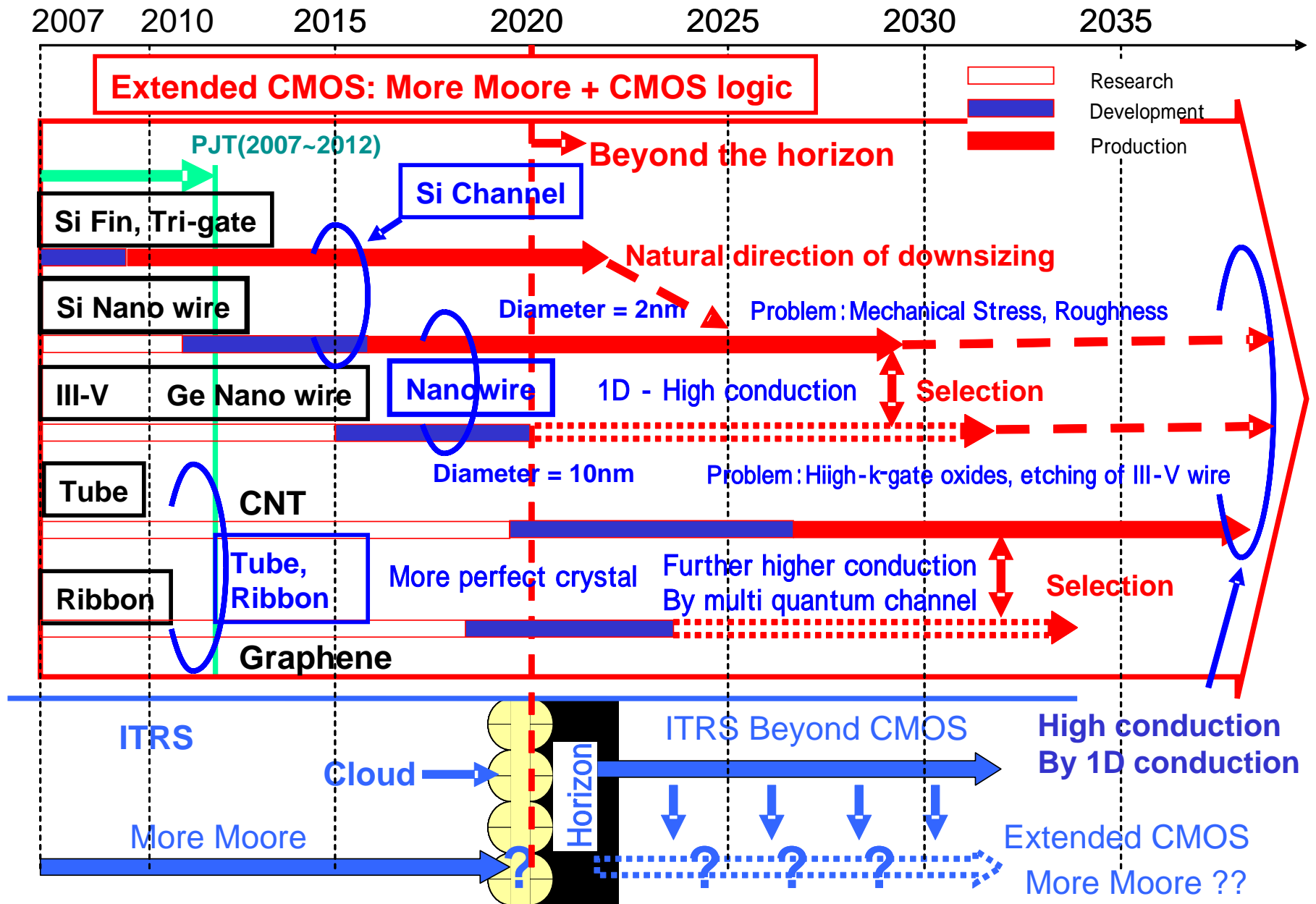


Surrounded gate MOS

Increase the number of wires towards vertical dimension



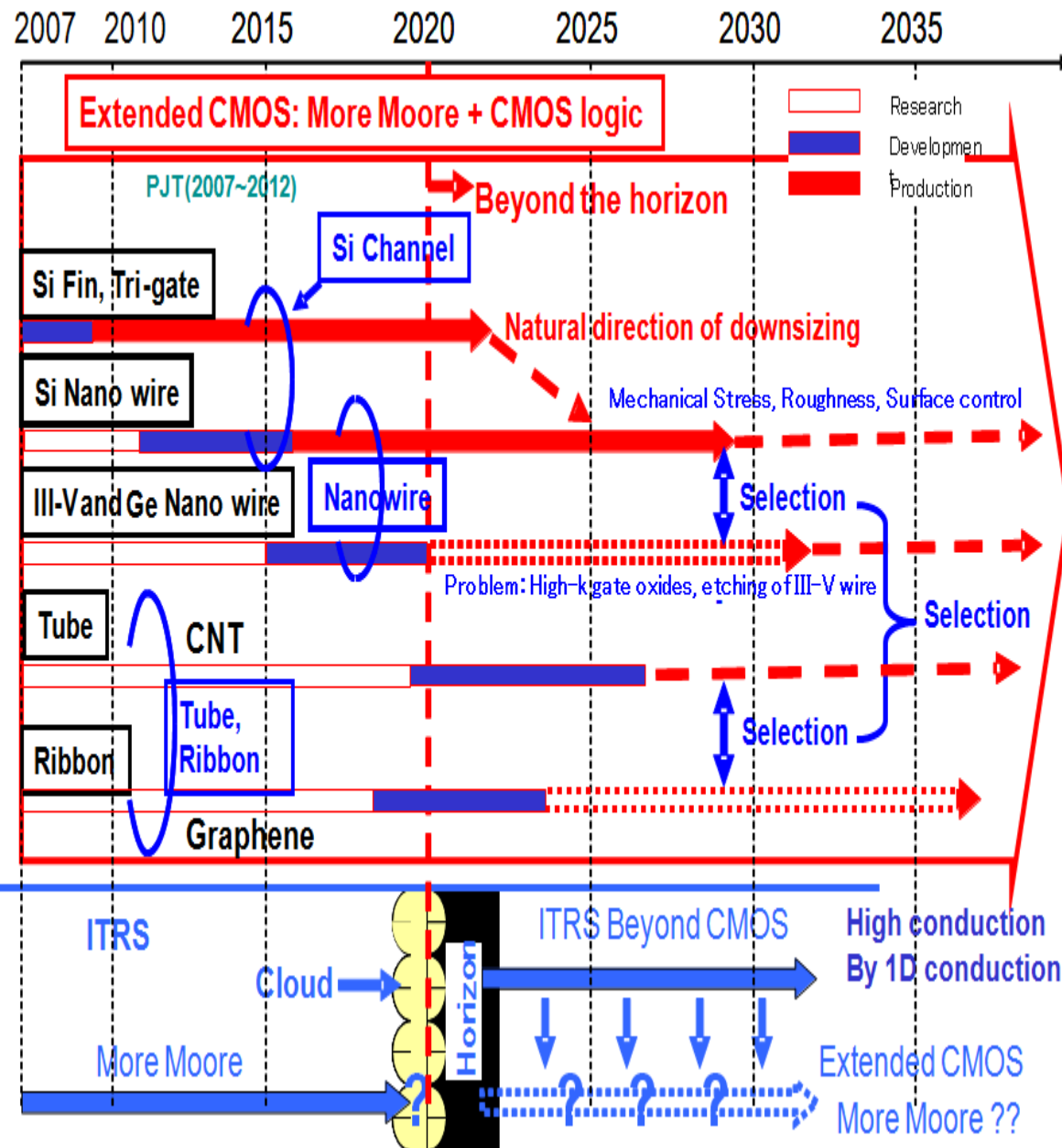
Our new roadmap



Our roadmap for R & D

Source: H. Iwai, IWJT 2008

Current Issues



Si Nanowire

- Control of wire surface property
- Source Drain contact
- Optimization of wire diameter
- Compact I-V model

III-V & Ge Nanowire

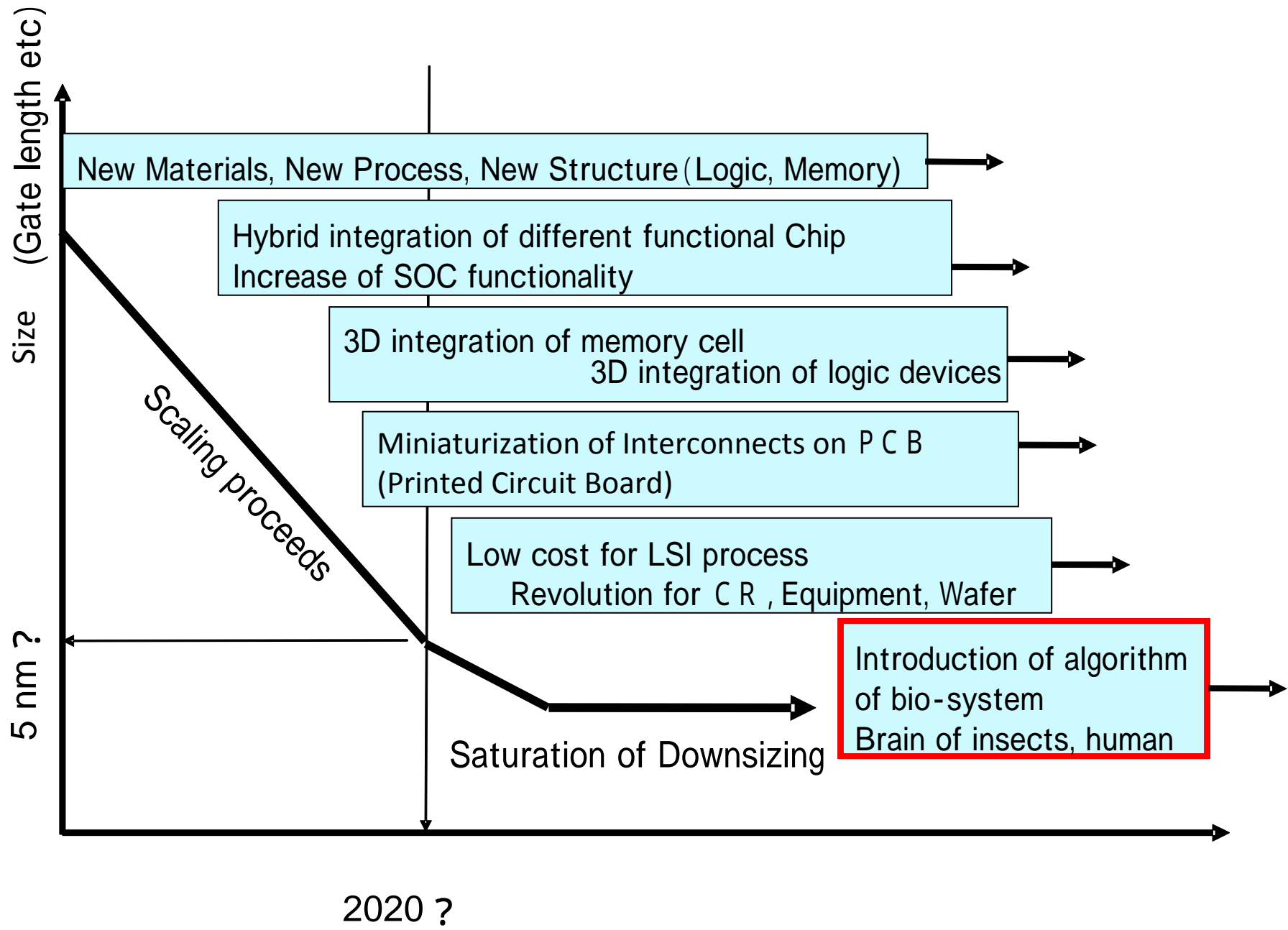
- High-k gate insulator
- Wire formation technique

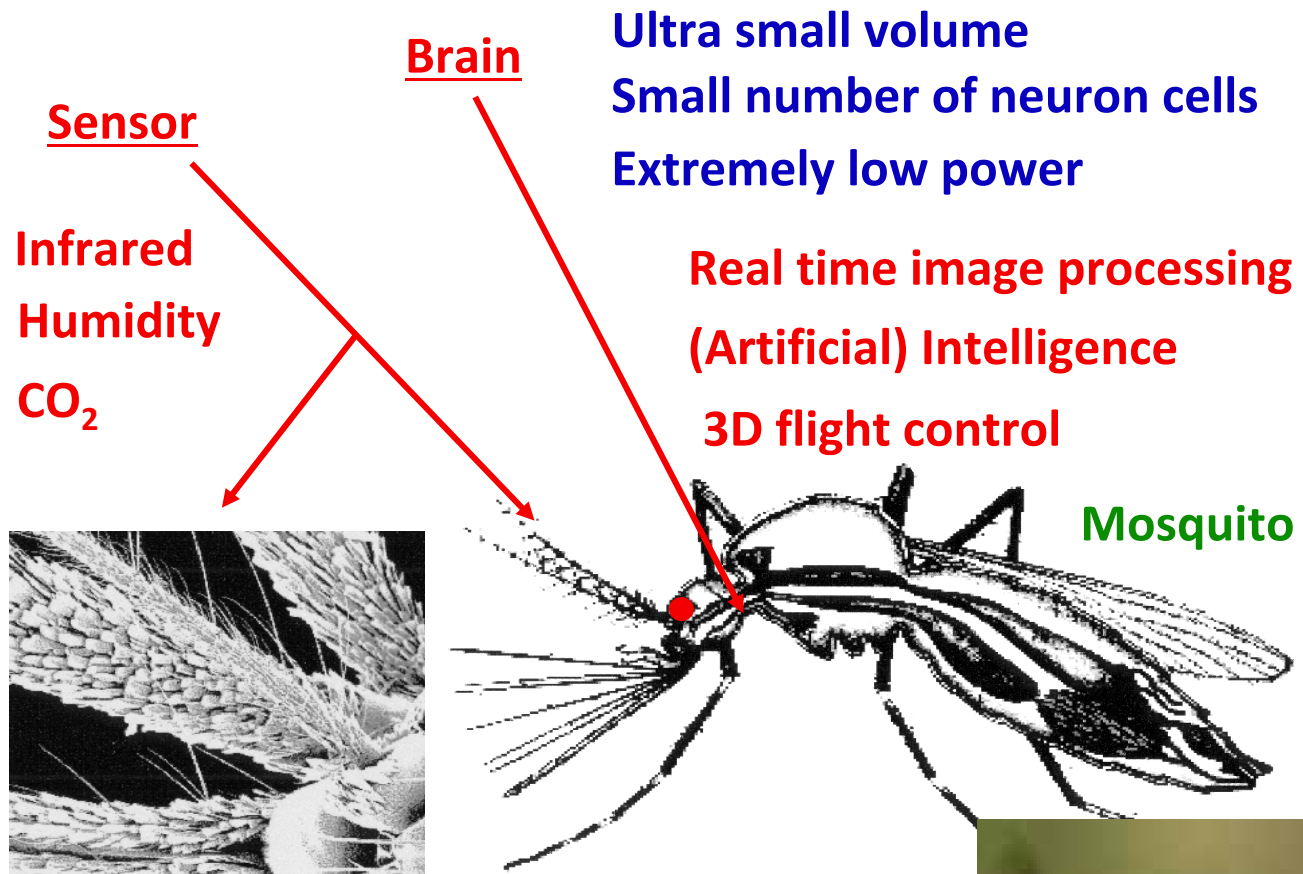
CNT:

- Growth and integration of CNT
- Width and Chirality control
- Chirality determines conduction types: metal or semiconductor

Graphene:

- Graphene formation technique
- Suppression of off-current
- Very small bandgap or no bandgap (semi-metal)
- Control of ribbon edge structure which affects bandgap





System and Algorithm becomes more important!

But do not know how?

Dragonfly is further high performance



Thank you
for your attention!