

Nano-CMOS technology after reaching its scaling limit

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Recently, CMOS downsizing has been accelerated very aggressively in both production and research level, and even transistor operation of a 5 nm gate length CMOS was reported in a conference. However, many serious problems are expected for implementing small-geometry MOSFETs into large scale integrated circuits even for the 32 nm technology node. Furthermore, it is still unclear that we can successfully bring sub-10 nm CMOS LSIs to market, because the anticipated problems with the I_{ON}/I_{OFF} ratio, current drive, variation in the electrical characteristics, yield, reliability and manufacturing cost. Considering the above situation, we have conducted nano-CMOS studies in advance to provide possible solutions to the expected future problems. The conclusion obtained by the study was that, in the nano-CMOS era, aggressive introduction of new materials, processes, structures, and operation concepts is required to solve the problems. Also, new physical analysis techniques and physical model in order to predict and explain the atomic scale phenomena and properties at the new material interfaces are important. Unfortunately, there are no candidates among the so-called "beyond CMOS" or "post-Si" new devices that can really replace CMOS transistors in highly integrated circuits within 20 years. Thus, our opinion is that we need to still continue CMOS-based transistors – CMOS with FinFET, nanowire FET, and even carbon nanotube FET – with "More Moore" approach combining with that of "More than Moore".