Roadmap for 22nm Logic CMOS and Beyond

March 9, 2009

@Heritage Institute of Technology

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Tokyo Institute of Technology

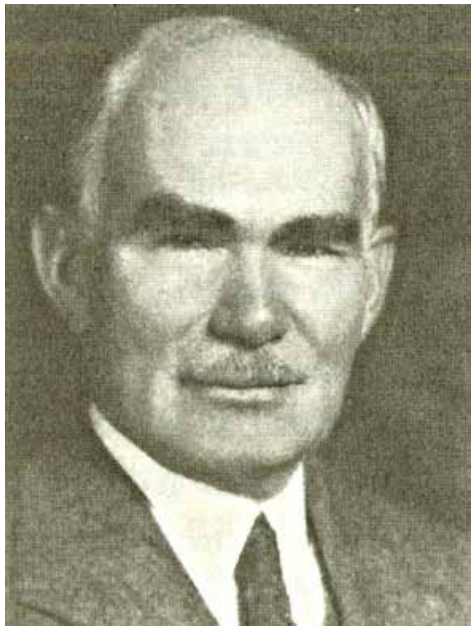
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

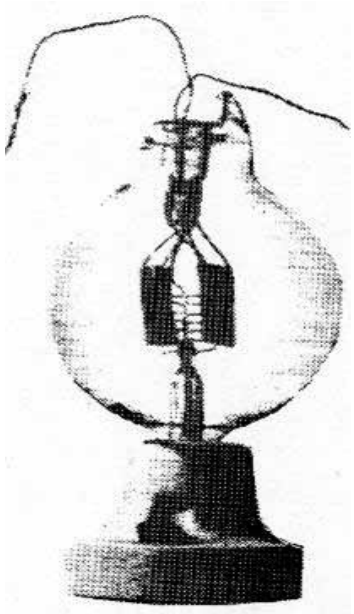
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

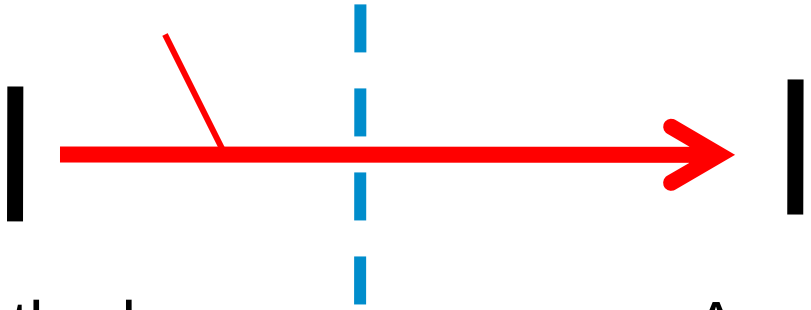


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

4 wives of Lee De Forest

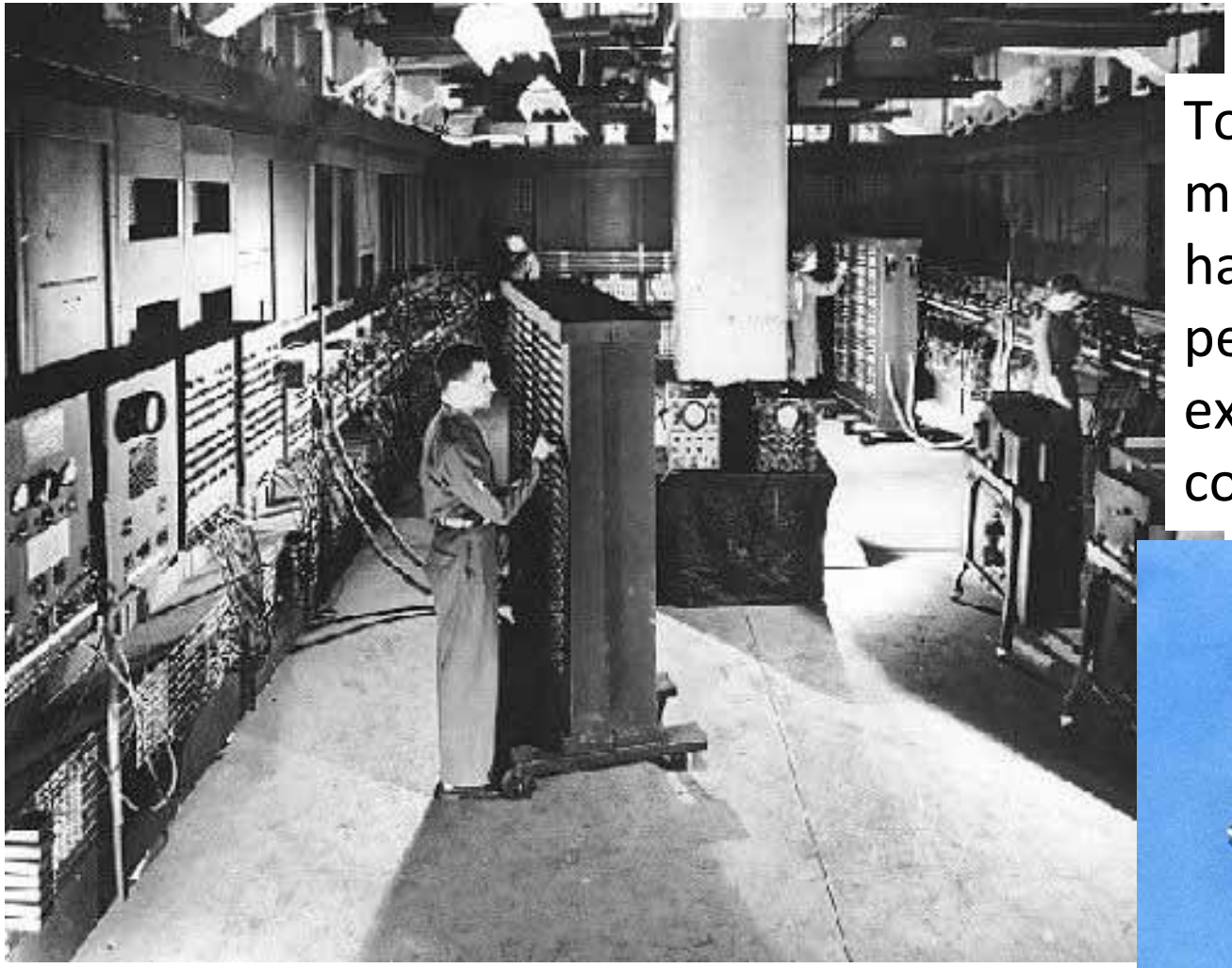
1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress

Mary

Marie

First Computer Eniac: made of huge number of vacuum tubes 1946
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor:
Ge Semiconductor, Bardeen, Brattin
→ Nobel Prize

1948, 1st Junction Bipolar Transistor,
Ge Semiconductor, Schokley
→ Nobel Prize

1958, 1st Integrated Circuits,
Ge Semiconductor, J.Kilby → Nobel Prize

1959, 1st Planar Integrated Circuits,
R.Noice

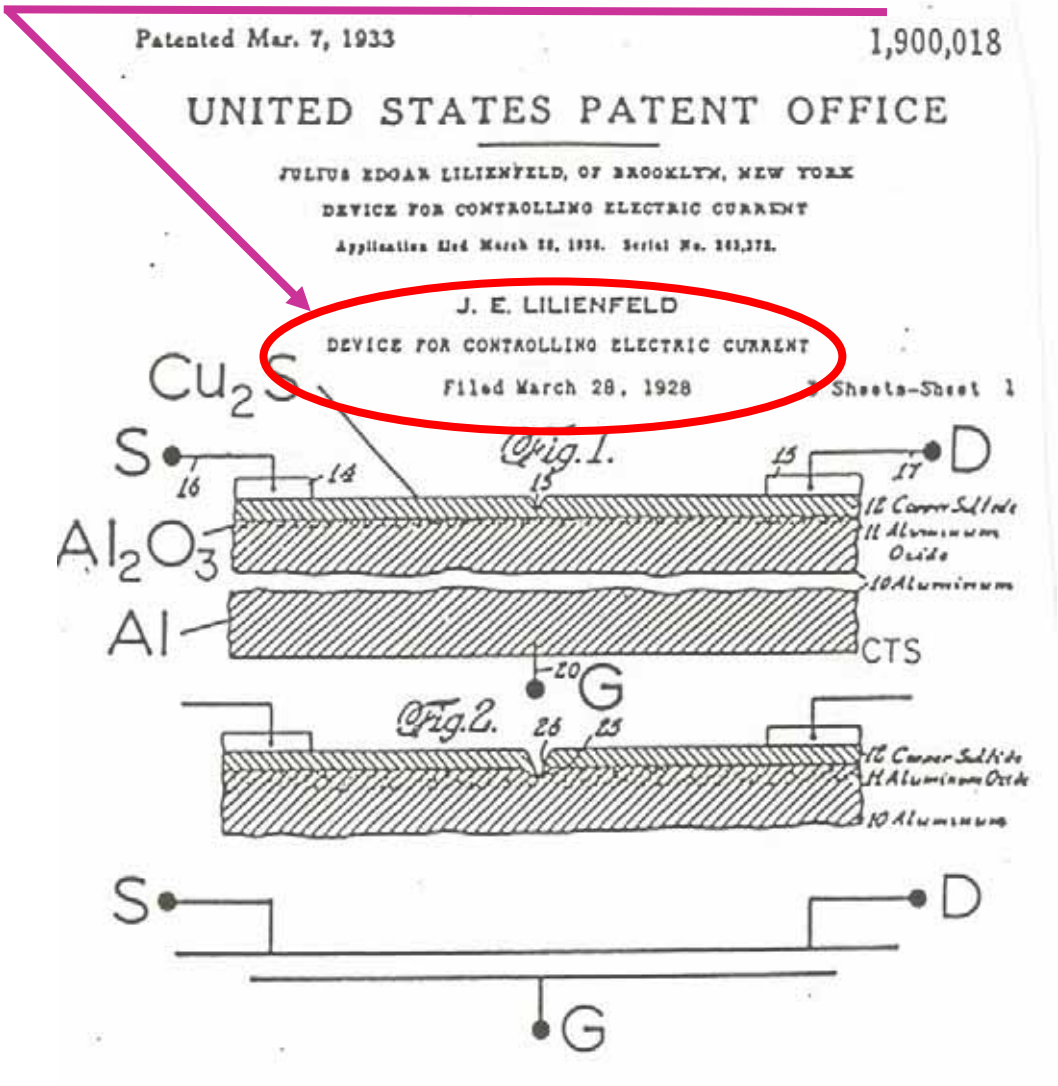
1960, 1st MOS Transistor, Kahng,
Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 263,372.

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 2 Sheets-Sheet 1

Cu_2S

S

D

Al_2O_3

Al

CTS

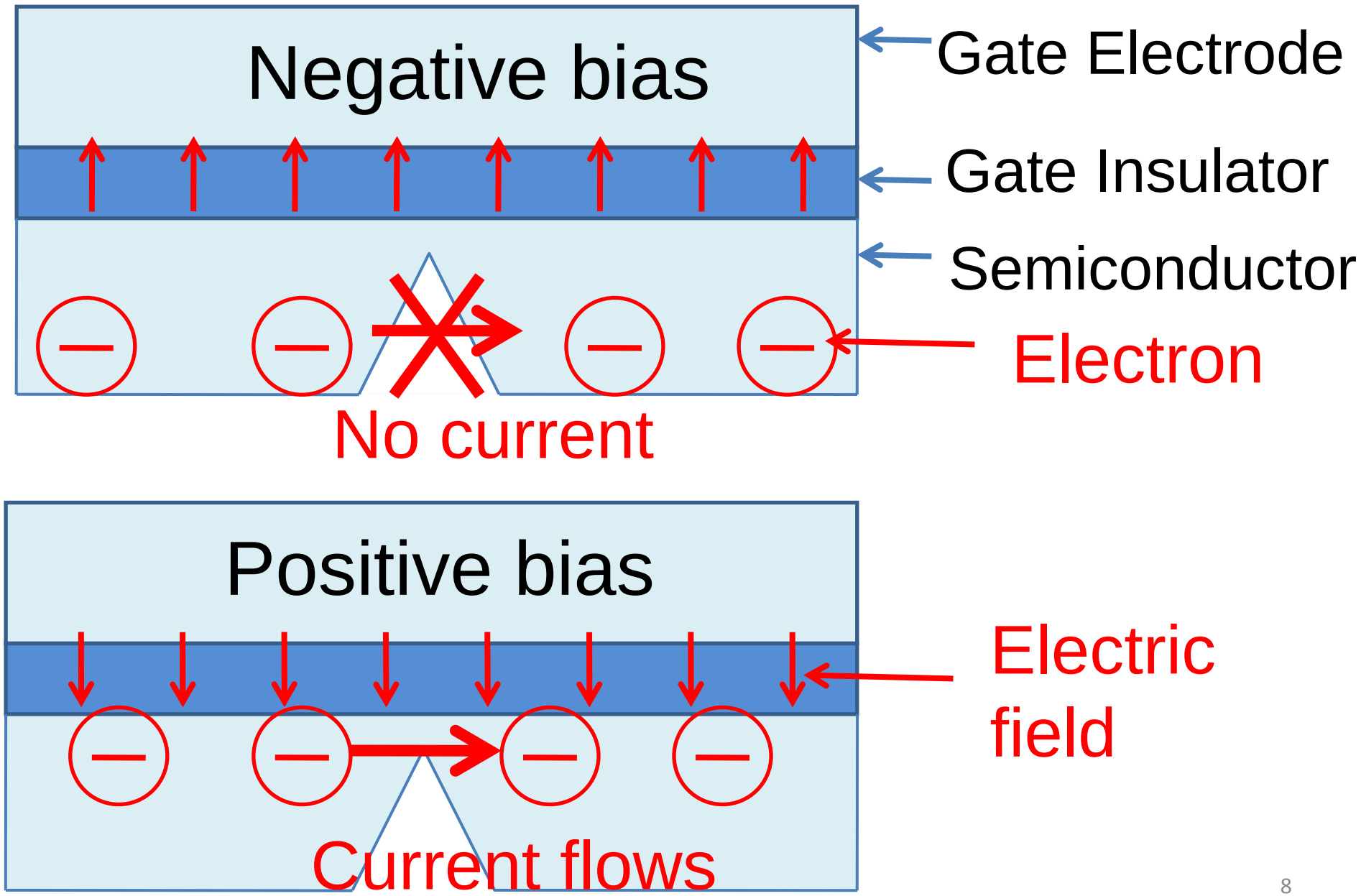
G

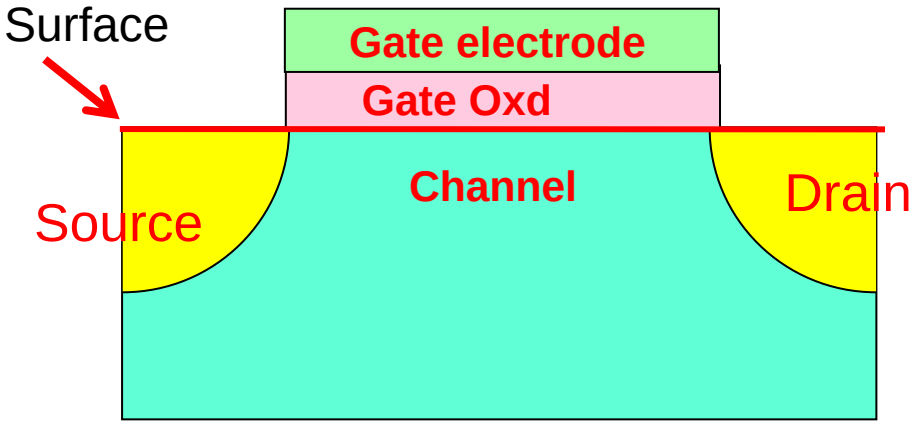
Fig. 1.

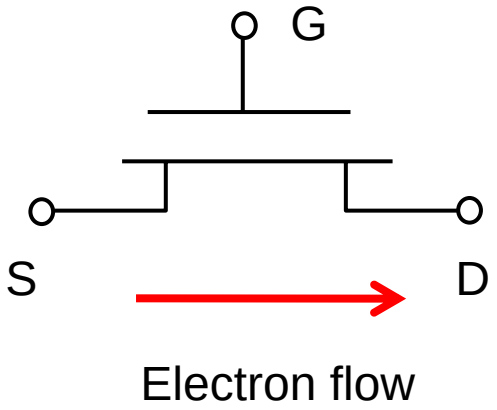
Fig. 2.

J.E.LILIENFELD

Capacitor structure with notch

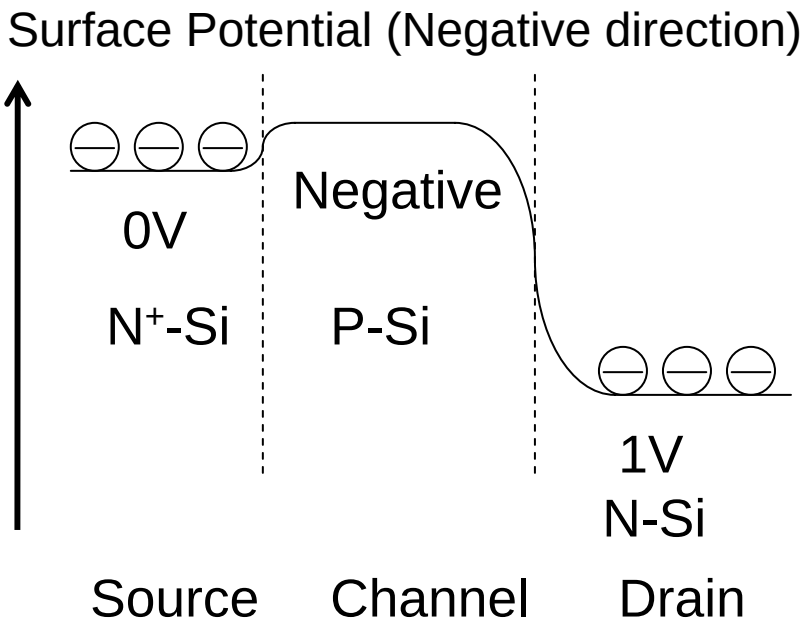


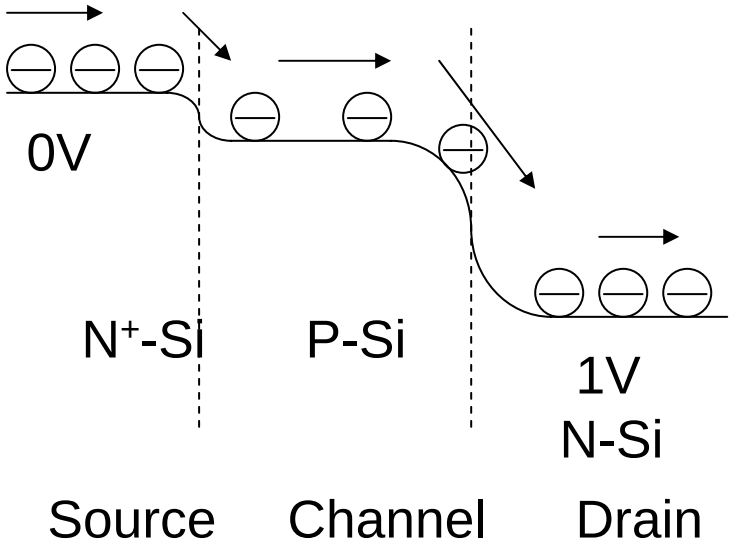




0 bias for gate

Positive bias for gate



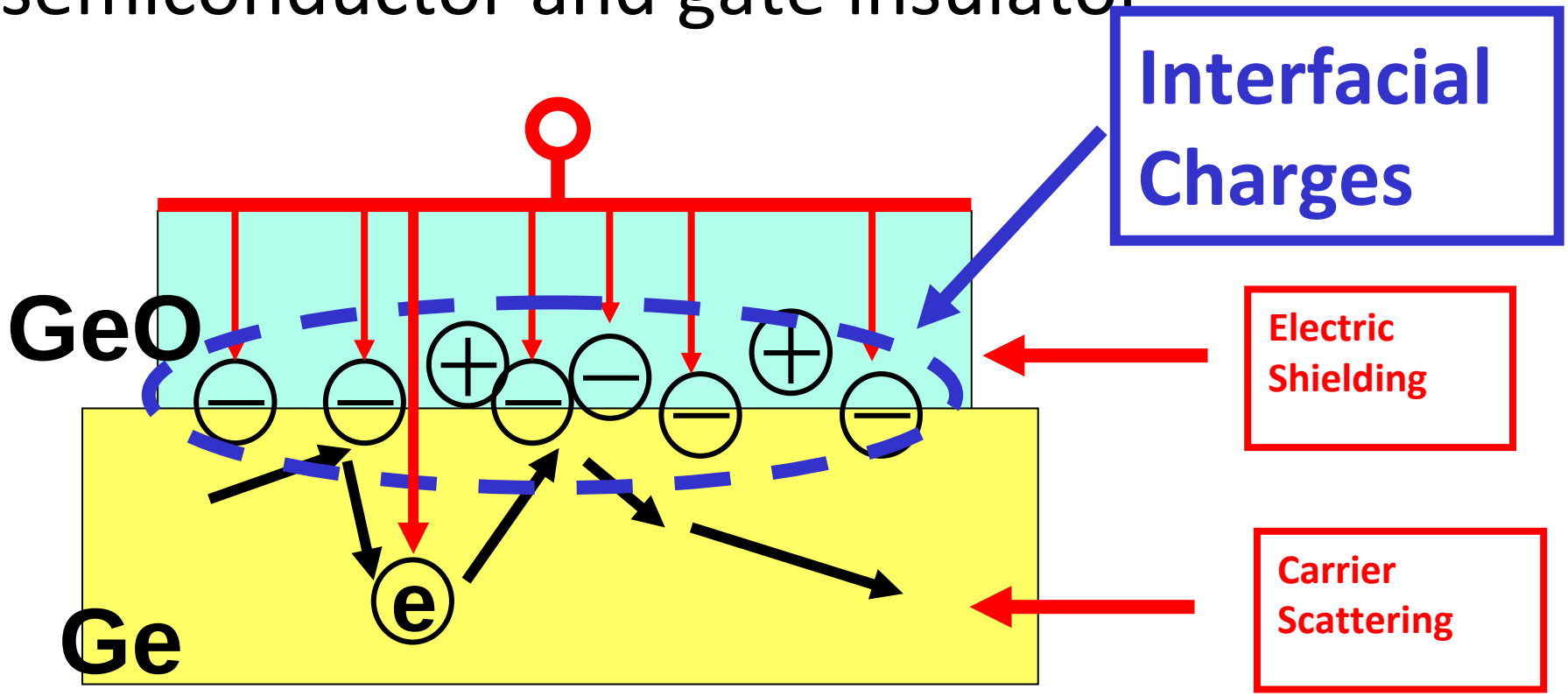


However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator



Drain Current was several orders of magnitude smaller than expected

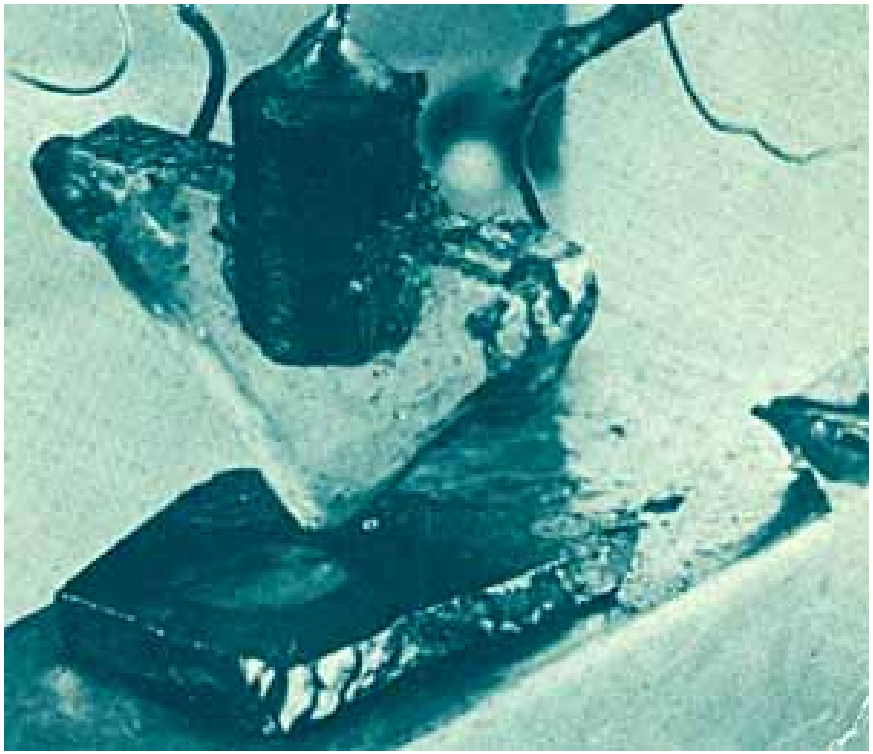
Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor

J. Bardeen W. Bratten,

W. Shockley

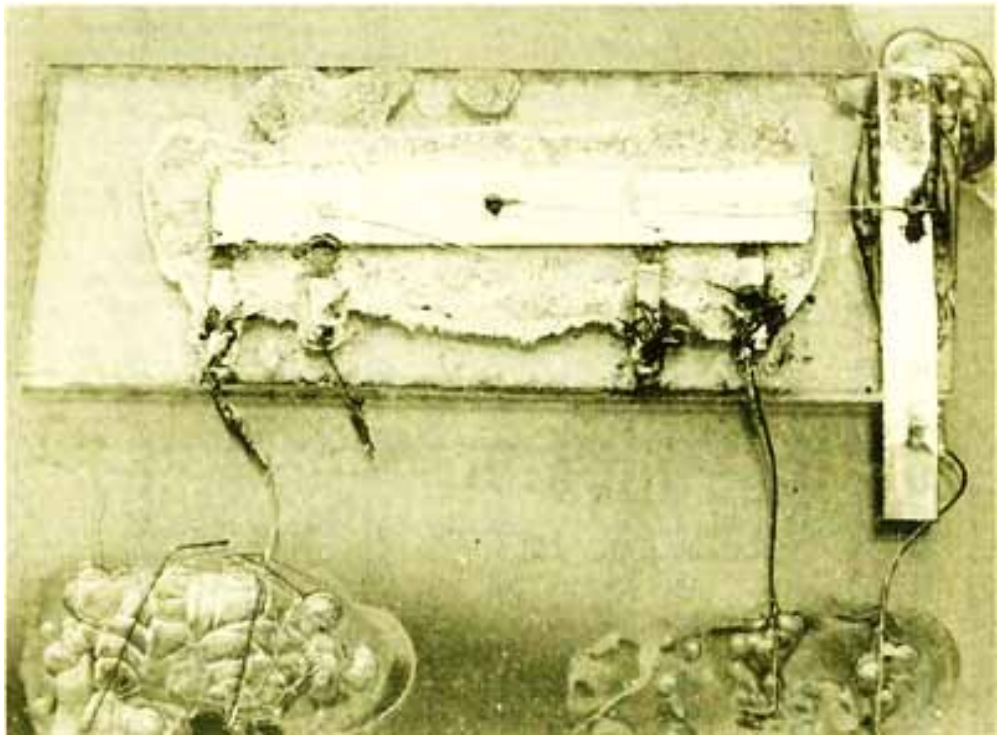


Bipolar using Ge

1958: 1st Integrated Circuit

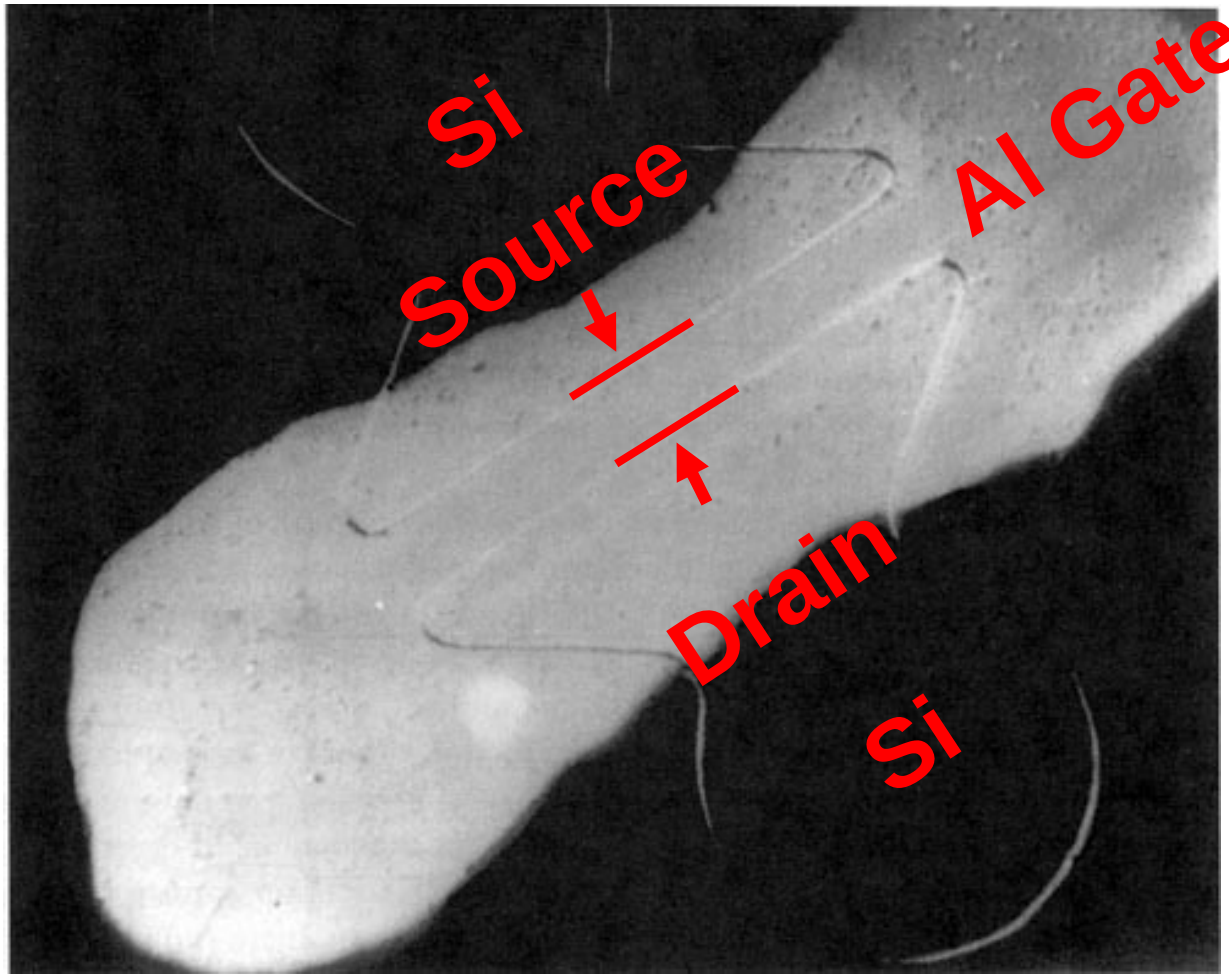
Jack S. Kilby

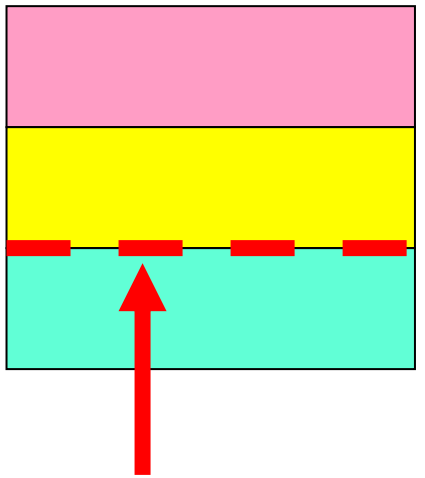
Connect 2 bipolar transistors in the
Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

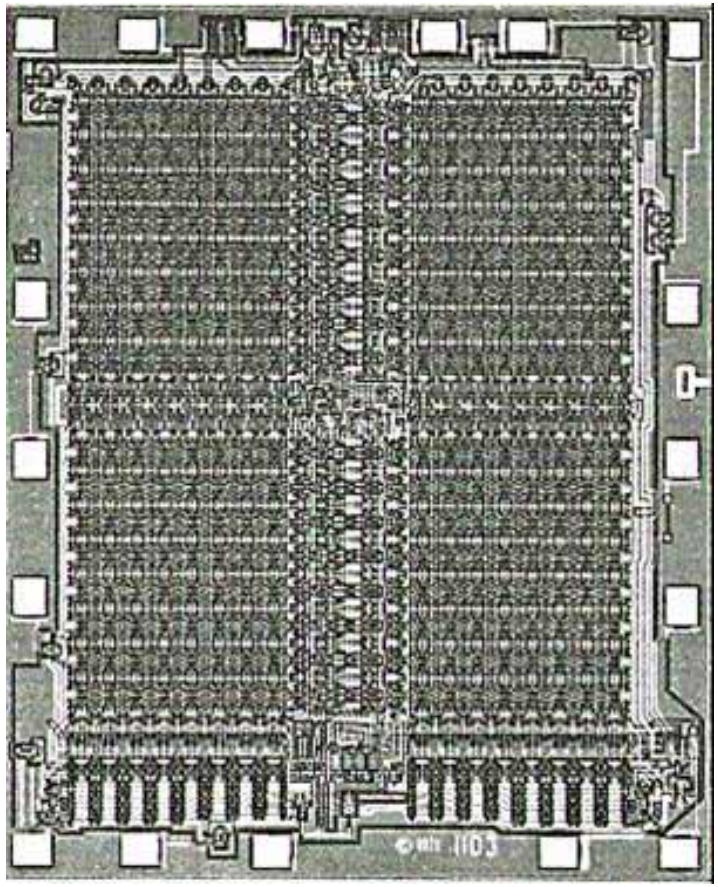
Top View



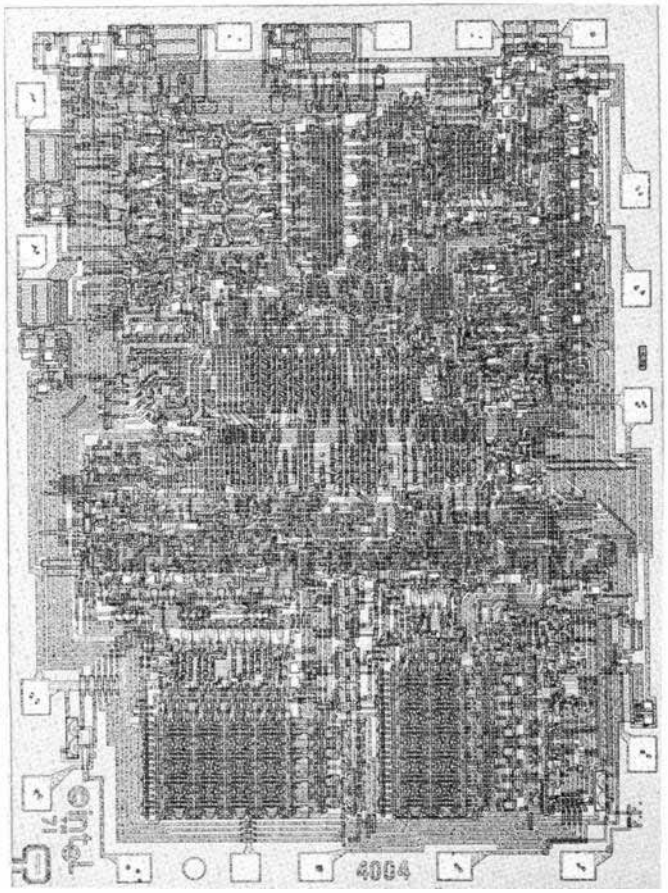


1970,71: 1st generation of LSIs

DRAM Intel 1103



MPU Intel 4004



MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~ 10
1970s	LSI (Large Scale Integrated Circuit)	~1,000
1980s	VLSI (Very Large Scale IC)	~10,000
1990s	ULSI (Ultra Large Scale IC)	~1,000,000
2000s	?LSI (? Large Scale IC)	~1000,000,000

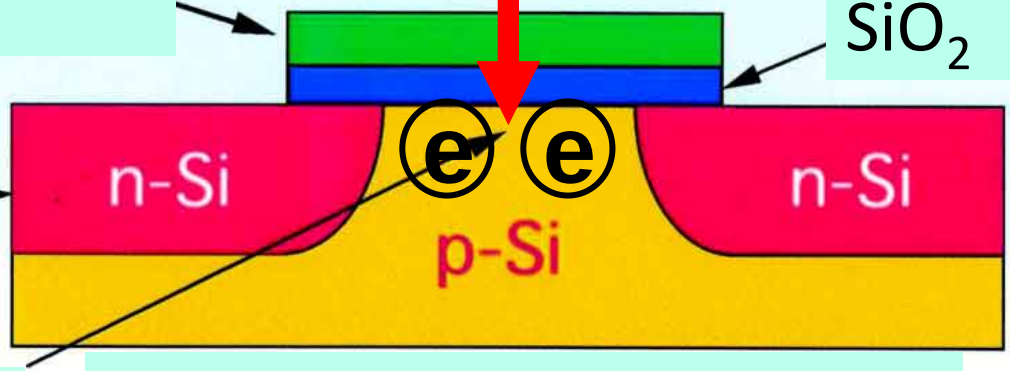
Gate Electrode
Poly Si

Gate Insulator
SiO_2

Substrate
Si

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

Use Gate Field Effect for switching



Gate Electrode
Poly Si

Gate Insulator
SiO_2

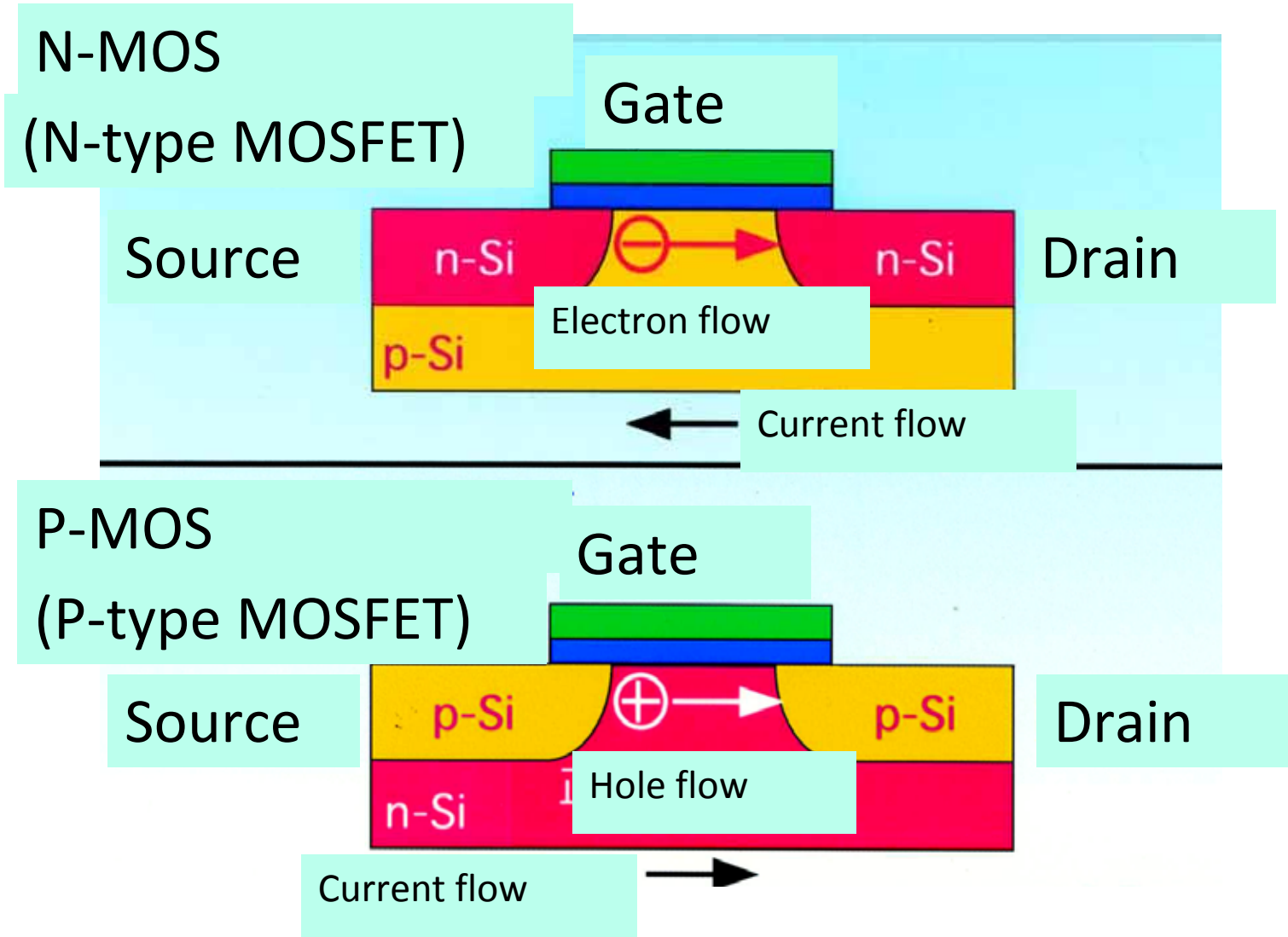
Source

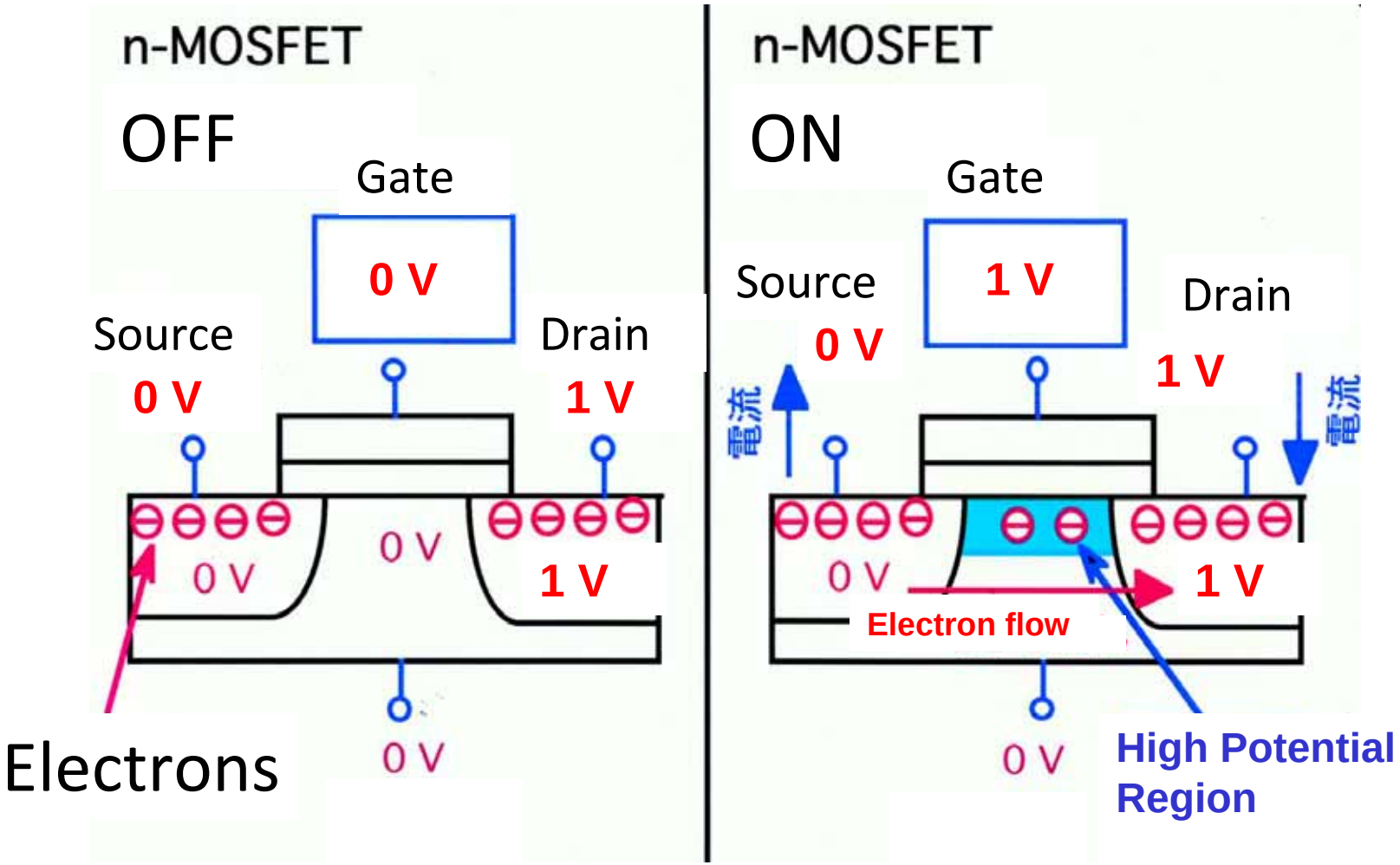
Drain

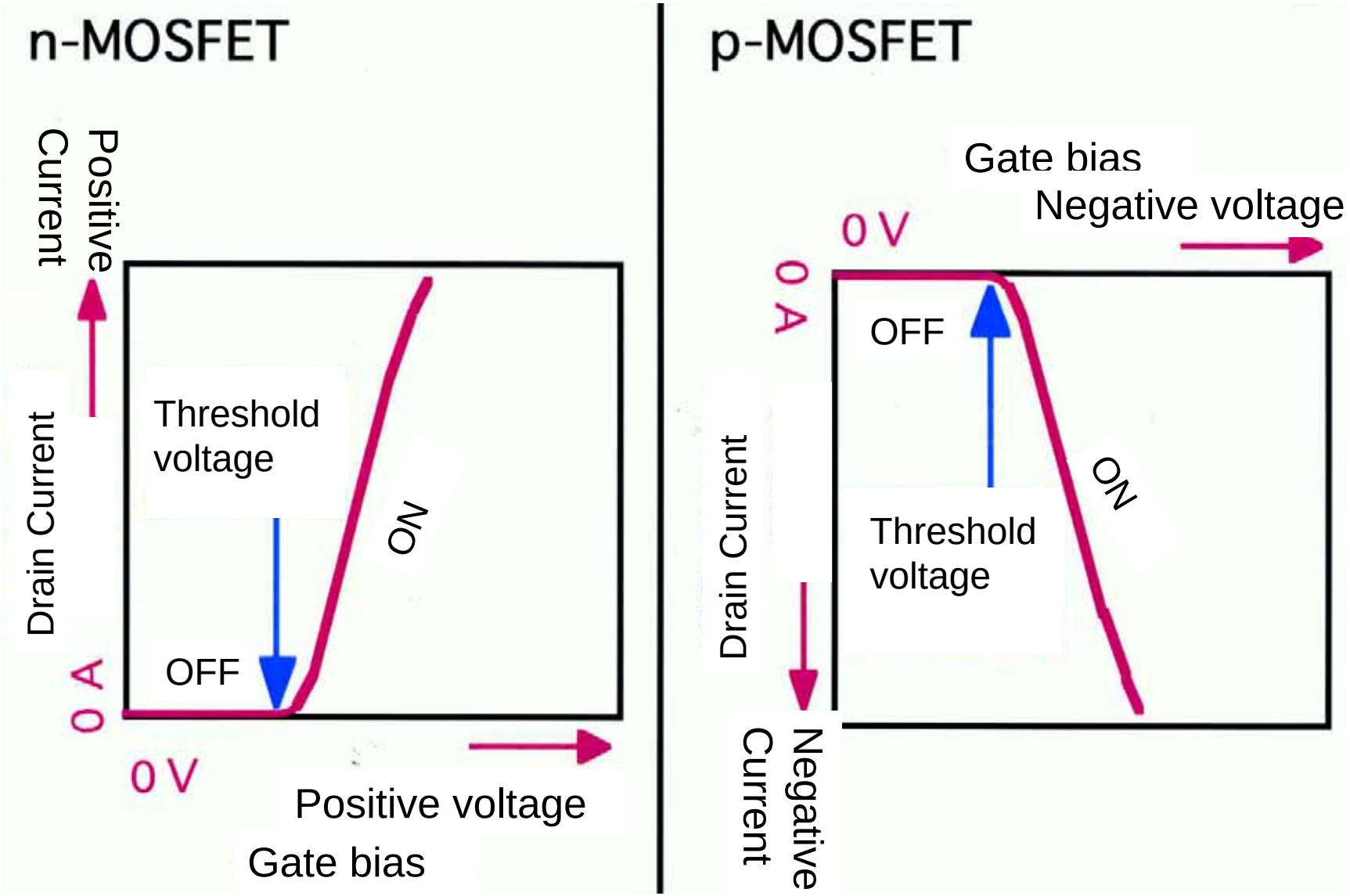
Si
Substrate

Channel

N-MOS (N-type MOSFET)

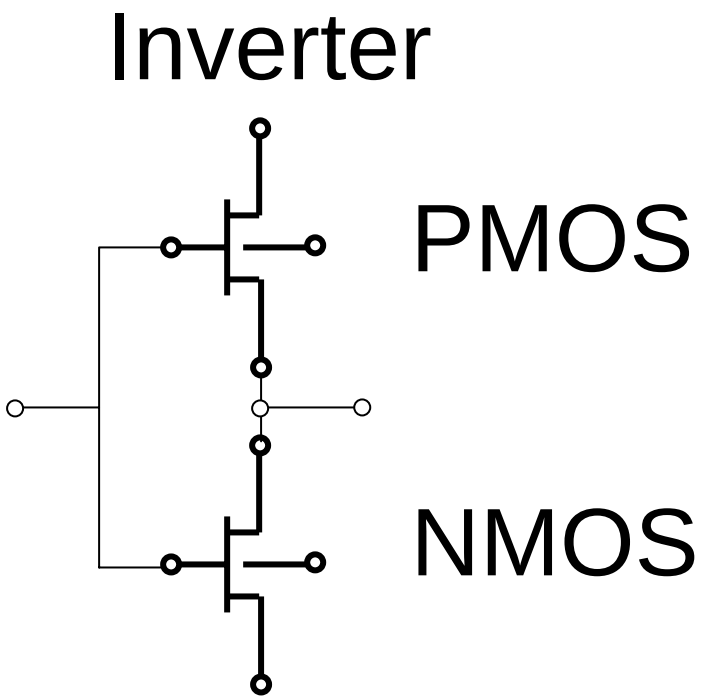

N-MOS
(N-type MOSFET)
Gate
Source
n-Si
n-Si
Drain
Electron flow
p-Si
Current flow
P-MOS
(P-type MOSFET)
Gate
Source
p-Si
p-Si
Drain
Hole flow
n-Si
Current flow


n-MOSFET
OFF
Gate
0 V
Source
0 V
Drain
1 V
0 V
0 V
1 V
0 V
Electrons
n-MOSFET
ON
Gate
1 V
Source
0 V
Drain
1 V
電流
電流
0 V
1 V
Electron flow
0 V
High Potential
Region


n-MOSFET
Positive Current
Drain Current
Threshold voltage
ON
OFF
0 A
0 V
Positive voltage
Gate bias
p-MOSFET
Gate bias
Negative voltage
0 V
0 A
OFF
ON
Threshold voltage
Drain Current
Negative Current

CMOS

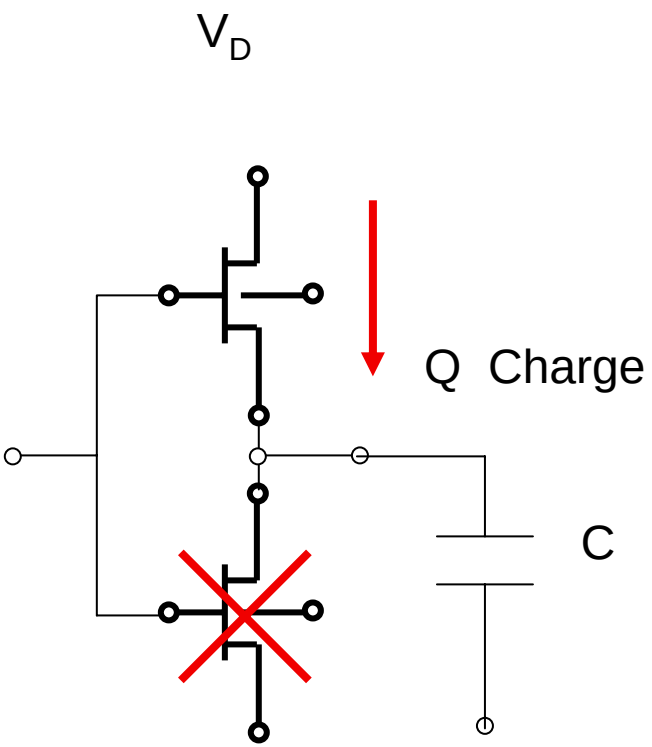
Complimentary MOS

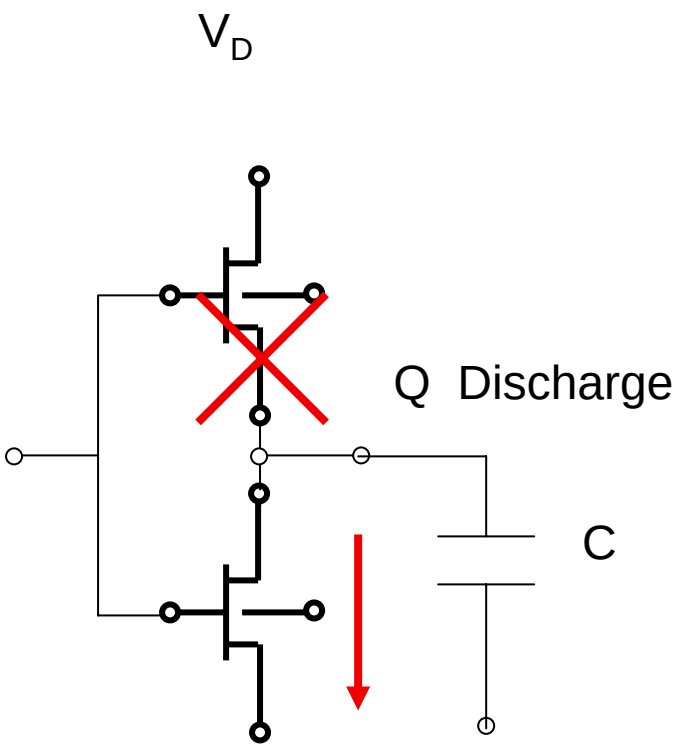


When NMOS is ON, PMOS is OFF

When PMOS is ON, NMOS is OFF

CMOS： Low Power: No DC current from Power supply to the ground





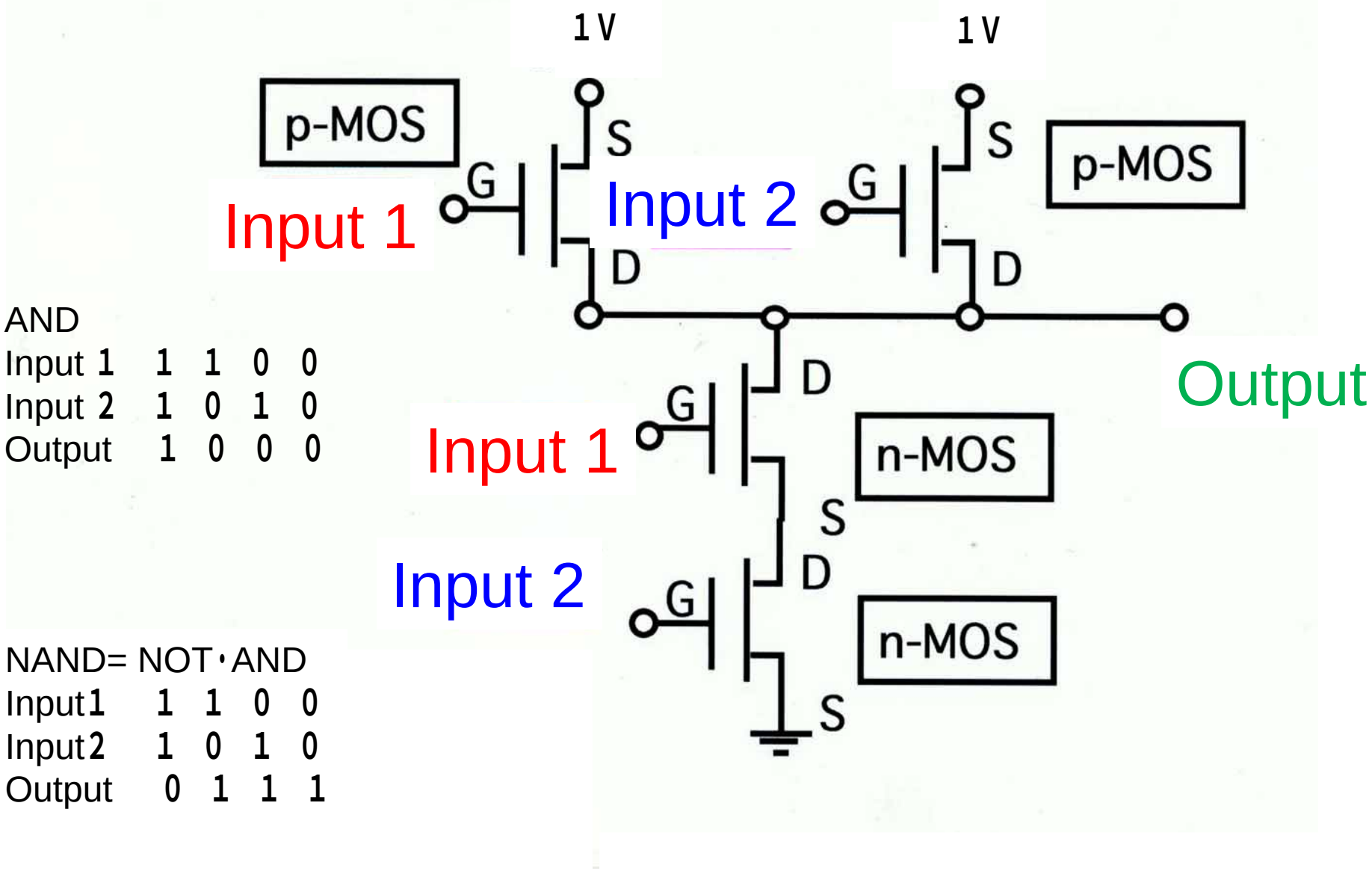
1 cycle

Clock frequency f

$$P = \frac{1}{2} CV_D^2$$

$$P = \frac{1}{2} fCV_D^2$$

2 input NAND Circuit



AND

Input 1	1	1	0	0
Input 2	1	0	1	0
Output	1	0	0	0

NAND= NOT･AND

Input1	1	1	0	0
Input2	1	0	1	0
Output	0	1	1	1

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

→ **Increase clock frequency**

→ **Increase circuit operation speed**

2. **Increase number of Transistors**

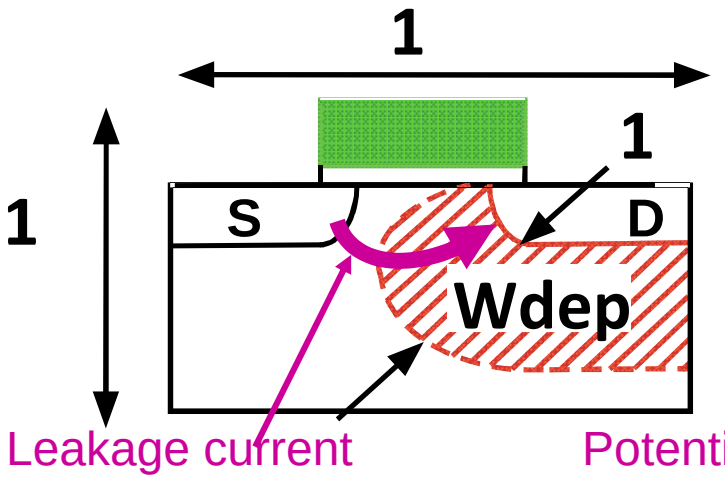
→ **Parallel processing**

→ **Increase circuit operation speed**

Downsizing contribute to the performance increase in double ways

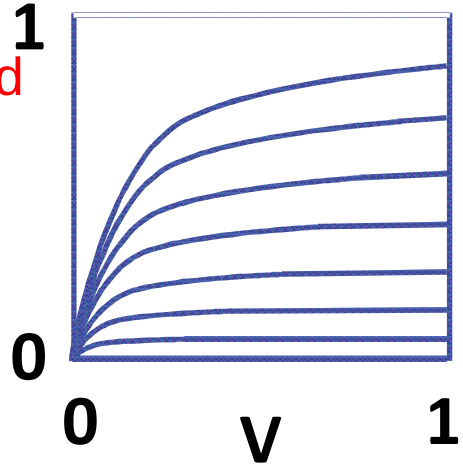
Thus, downsizing of Si devices is the most important and critical issue.

Scaling Method: by R. Dennard in 1974



Wdep: Space Charge Region (or Depletion Region) Width

Wdep has to be suppressed
Otherwise, large leakage between S and D



Leakage current

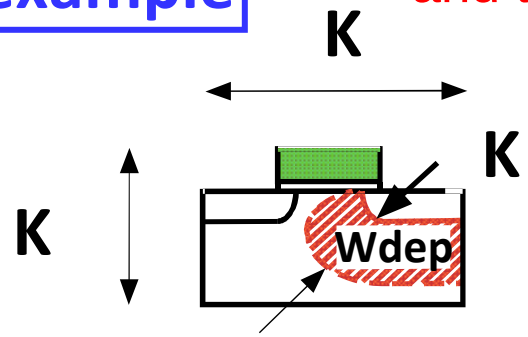
Potential in space charge region is high, and thus, electrons in source are attracted to the space charge region.

K=0.7 for example

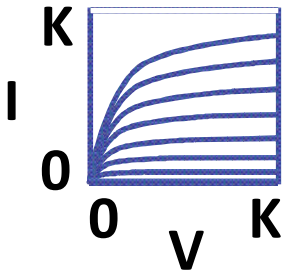
X , Y , Z : K, V : K, Na : 1/K

By the scaling, Wdep is suppressed in proportion, and thus, leakage can be suppressed.

→ Good scaled I-V characteristics



$$Wdep \propto \sqrt{V/Na}$$
$$: K$$



I : K

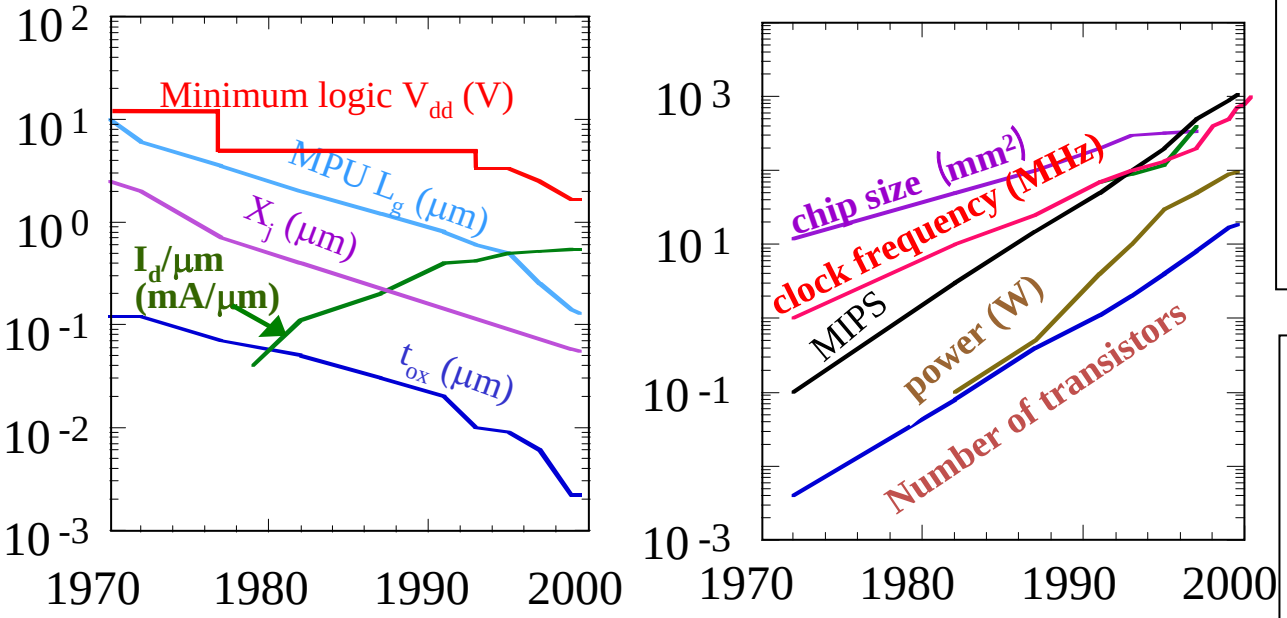
27

Downscaling merit: Beautiful!

Geometry & Supply voltage	L_g, W_g T_{ox}, V_{dd}	K	**Scaling K : K=0.7 for example**
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area → $W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1}(V_g - V_{th}) = KK^{-1}K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ → $KK/K = K$
Switching speed	τ	K	$\tau = C_g V_{dd} / I_d$ → $KK/K = K$
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	α: Scaling factor → **In the past, $\alpha>1$ for most cases**
Integration (# of Tr)	N	α/K^2	N → α/K^2 **$= 1/K^2$, when $\alpha=1$**
Power per chip	P	α	$fNCV^2/2$ → $K^{-1}(\alpha K^{-2})K(K^1)^2 = \alpha$ **$= 1$, when $\alpha=1$**

k= 0.7 and α =1	k= 0.7^2 =0.5 and α =1
Single MOFET	
Vdd → 0.7 Lg → 0.7 Id → 0.7 Cg → 0.7	Vdd → 0.5 Lg → 0.5 Id → 0.5 Cg → 0.5
P (Power)/Clock → $0.7^3 = 0.34$ τ (Switching time) → 0.7	P (Power)/Clock → $0.5^3 = 0.125$ τ (Switching time) → 0.5
Chip	
N (# of Tr) → $1/0.7^2 = 2$ f (Clock) → 1/0.7 = 1.4 P (Power) → 1	N (# of Tr) → $1/0.5^2 = 4$ f (Clock) → 1/0.5 = 2 P (Power) → 1

Actual past downscaling trend until year 2000



Source. Iwai and S. Ohmi, Microelectronics Reliability 42 (2002), pp.1251-1268

Past 30 years scaling

Merit: N, f increase

Demerit: P increase

V_{dd} scaling insufficient

⇩

Additional significant increase in I_d, f, P

Change in 30 years

	Ideal scaling	Real Change		Ideal scaling	Real Change		Ideal scaling	Real Change
L_g	K	10^{-2}	I_d	K (10^{-2})	10^{-1}	f	1/K(10^{2})	10^{3}
t_{ox}	K(10^{-2})	10^{-2}						
V_{dd}	K(10^{-2})	10^{-1}	I_d/μm	1	10^{1}	P	α(10^{1})	10^{5}
						= fαNCV²		
A_{chip}	α	10^{1}	N	α/K²(10^{5})	10^{4}			

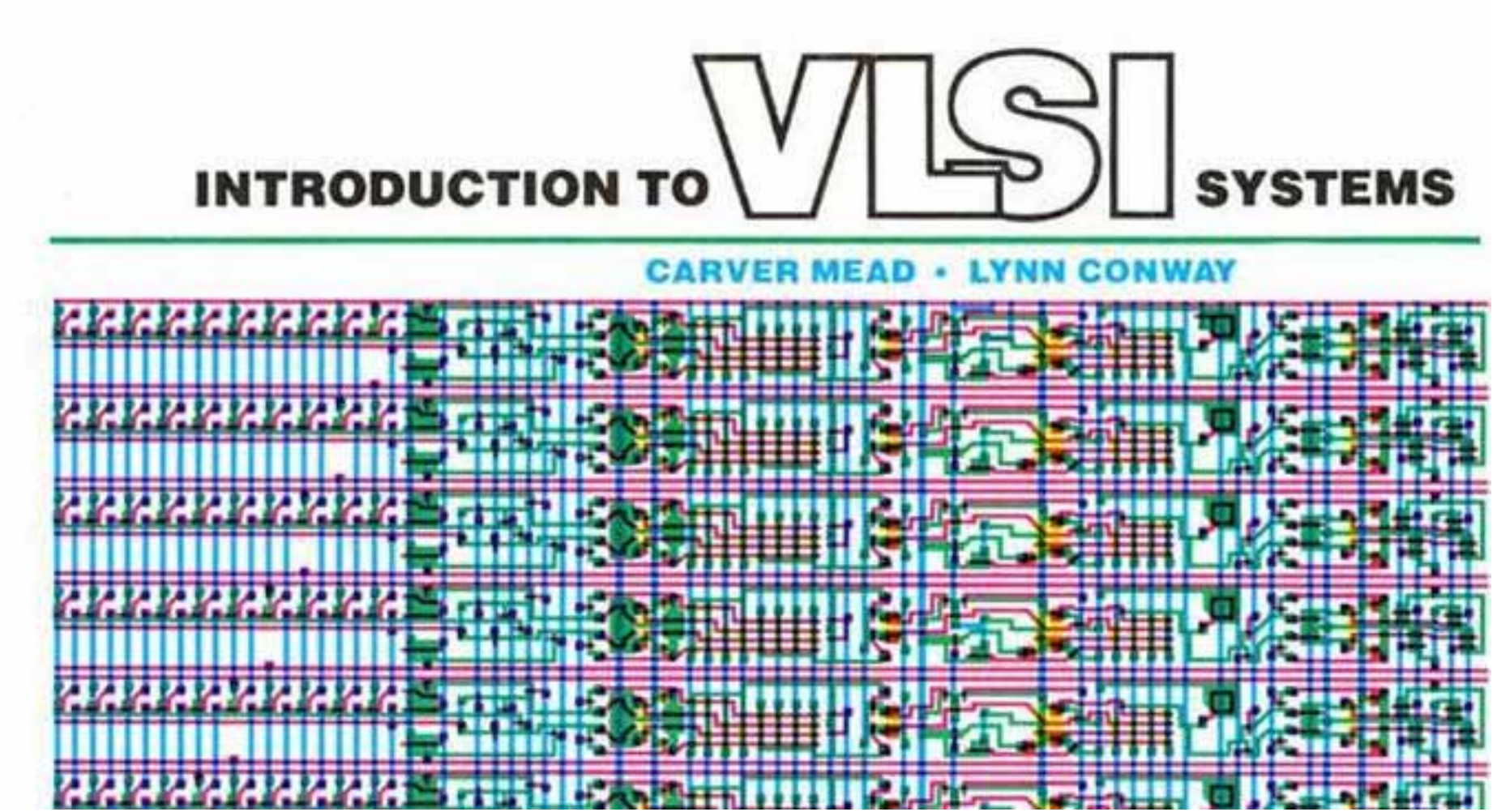
Vd scaling insufficient, α increased → N, Id, f, P increased significantly

Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

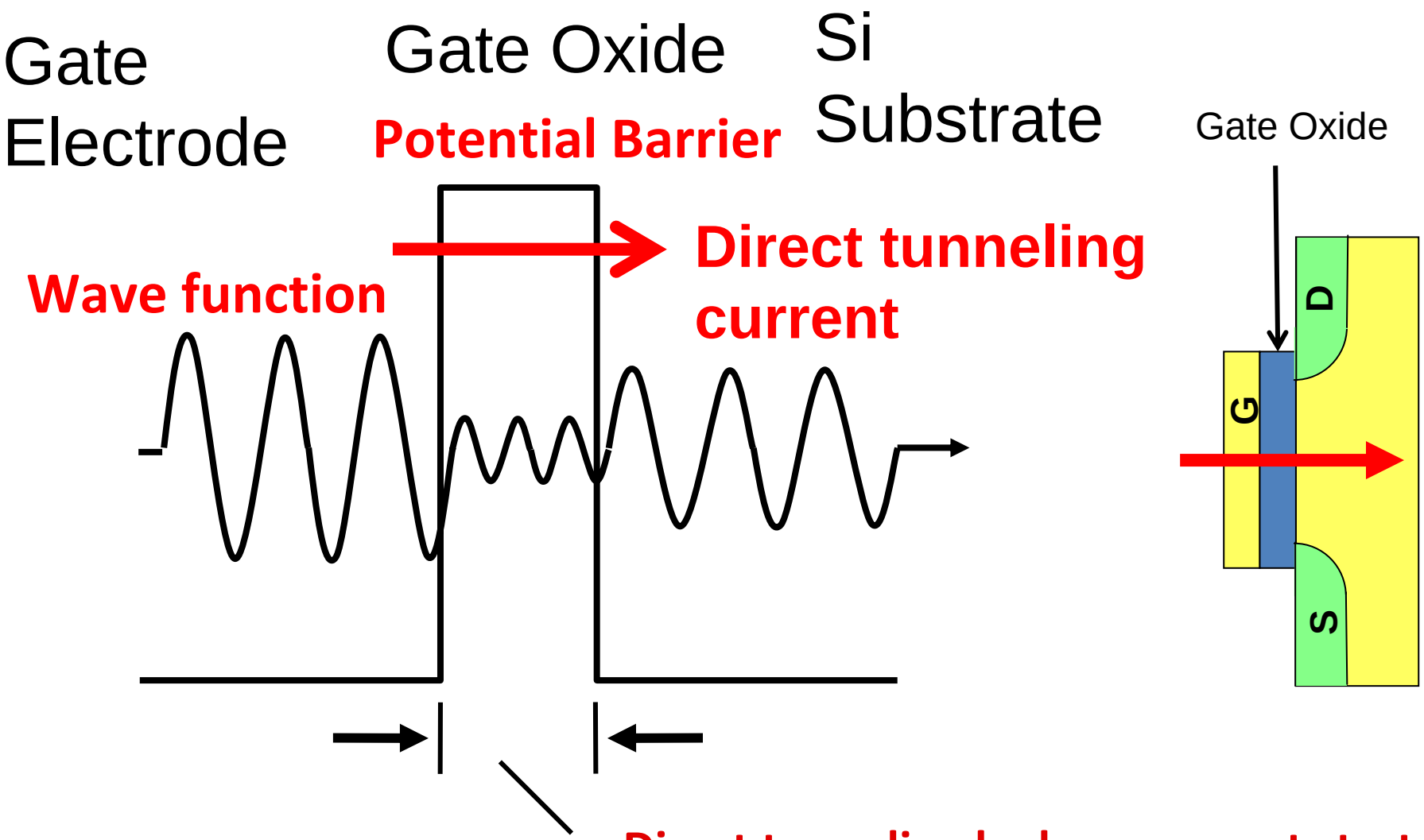


C. Mead L. Conway

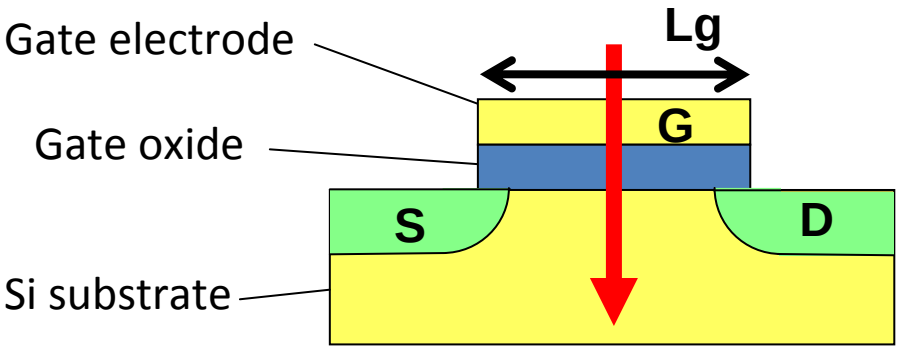
VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide ..... begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect

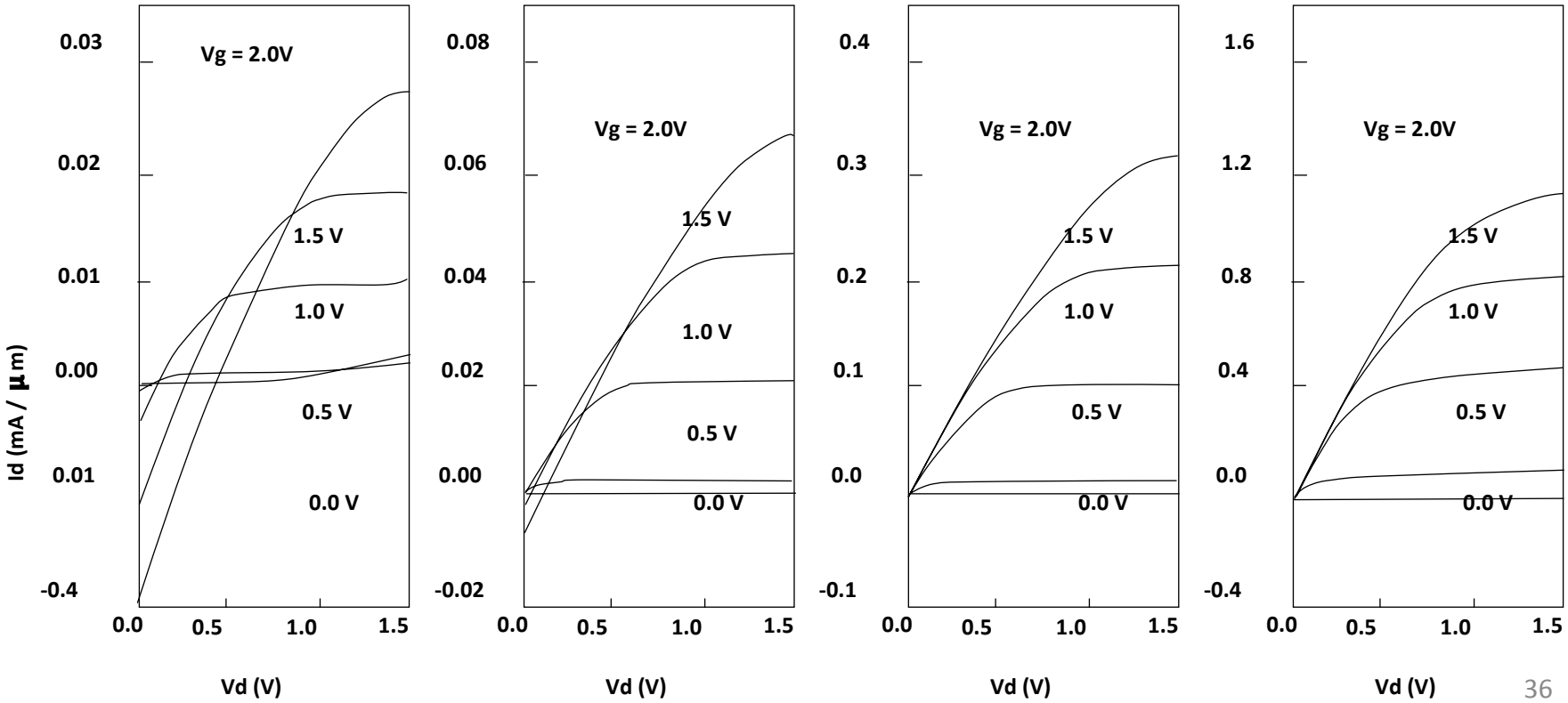


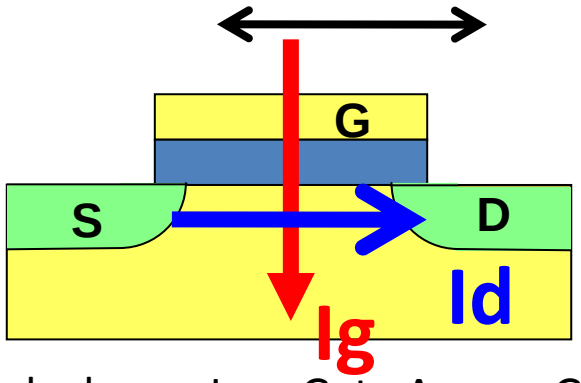
Direct tunneling leakage current start to flow when the thickness is 3 nm.



Direct tunneling leakage was found to be OK! In 1994!

MOSFETs with 1.5 nm gate oxide



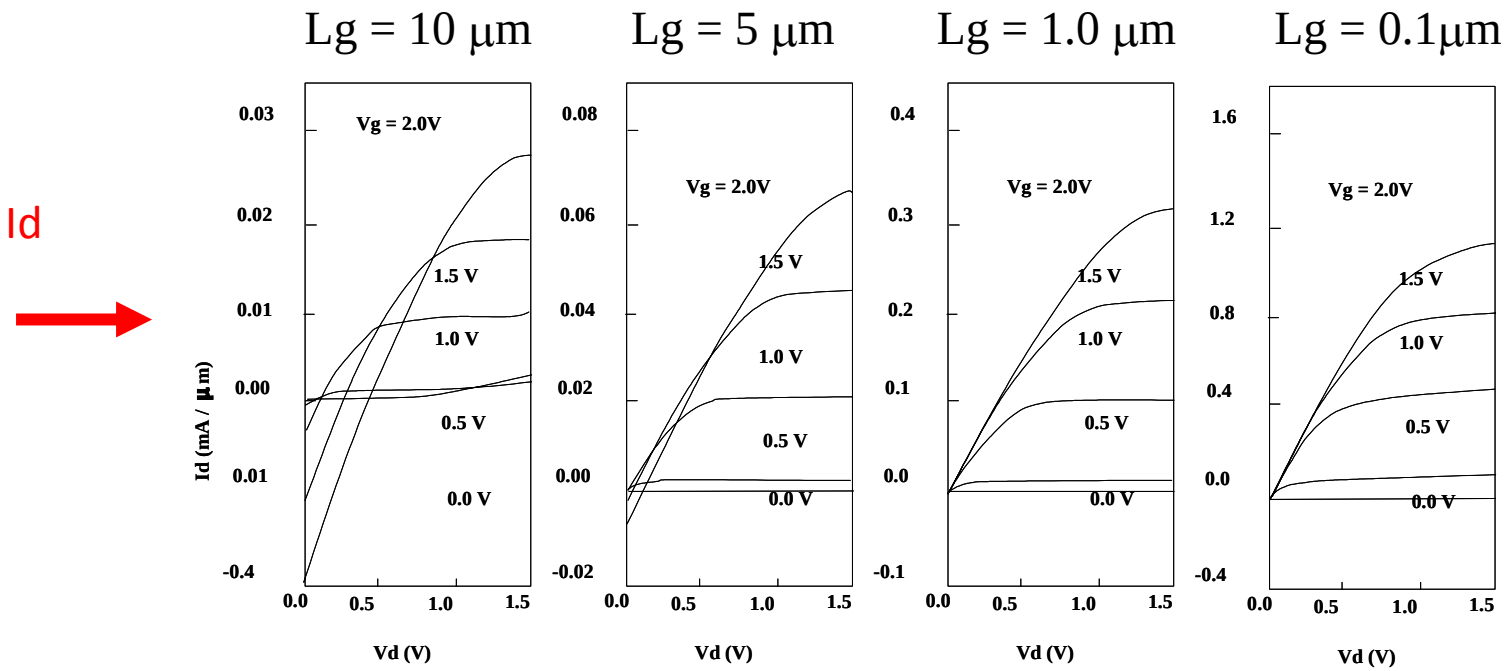


Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

Then, Ig → small, Id → large, Thus, Ig/Id → very small



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

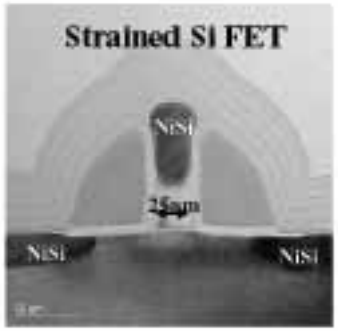
90nm node

Lg=50nm

65nm node

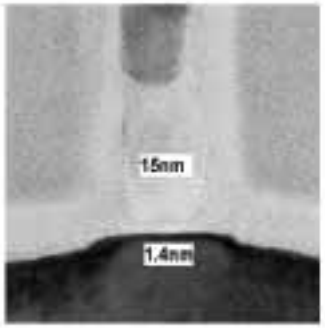
Lg=35nm

45nm node



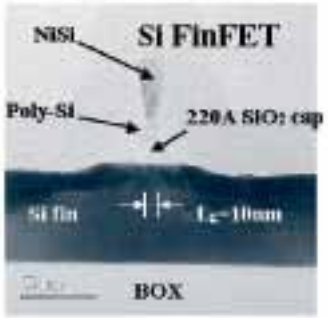
Lg=25nm

32nm node

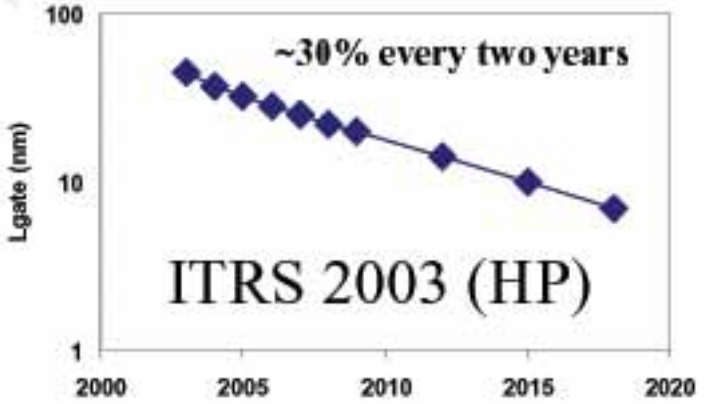


Lg=15nm

22nm node



Lg=10nm

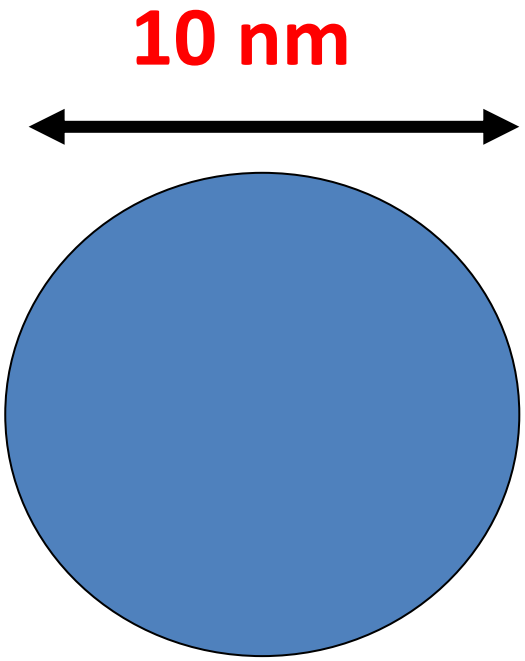


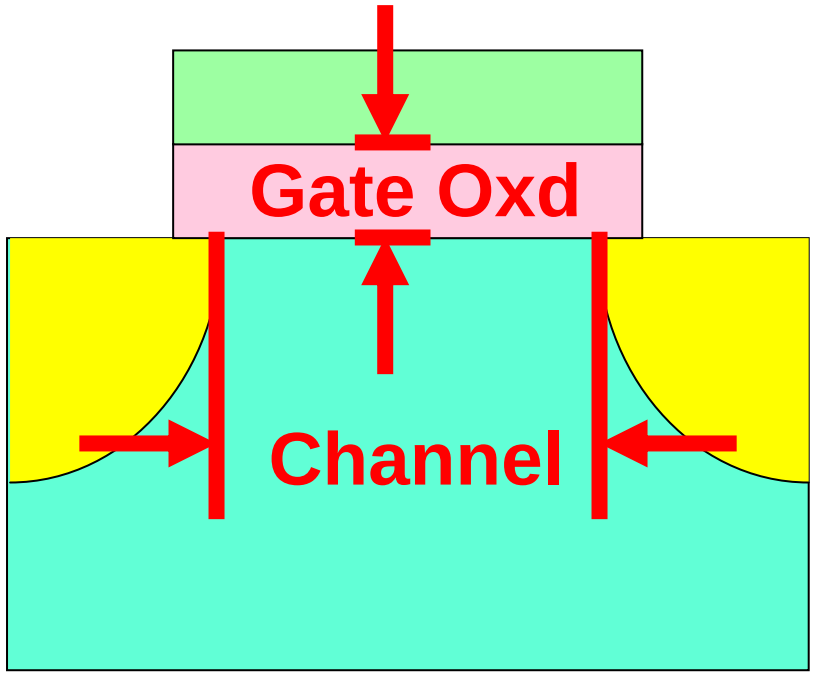
Qi Xinag, ECS 2004, AMD

Downsizing limit?

Channel length?

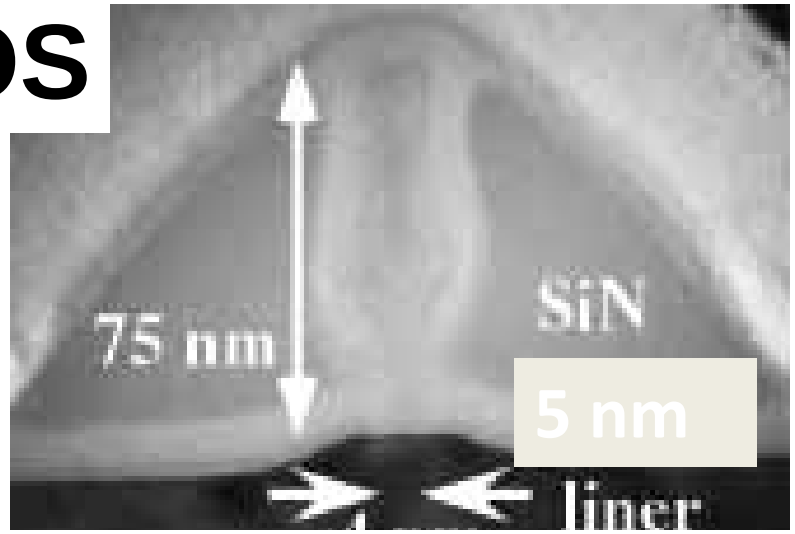
Electron wave length



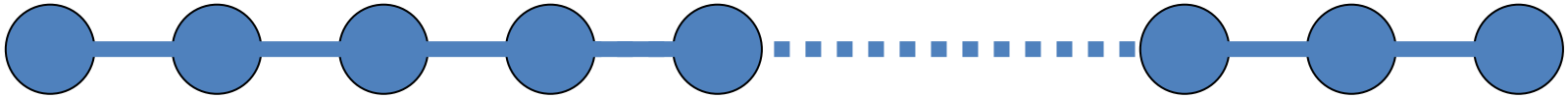


5 nm gate length CMOS

Is a Real Nano Device!!

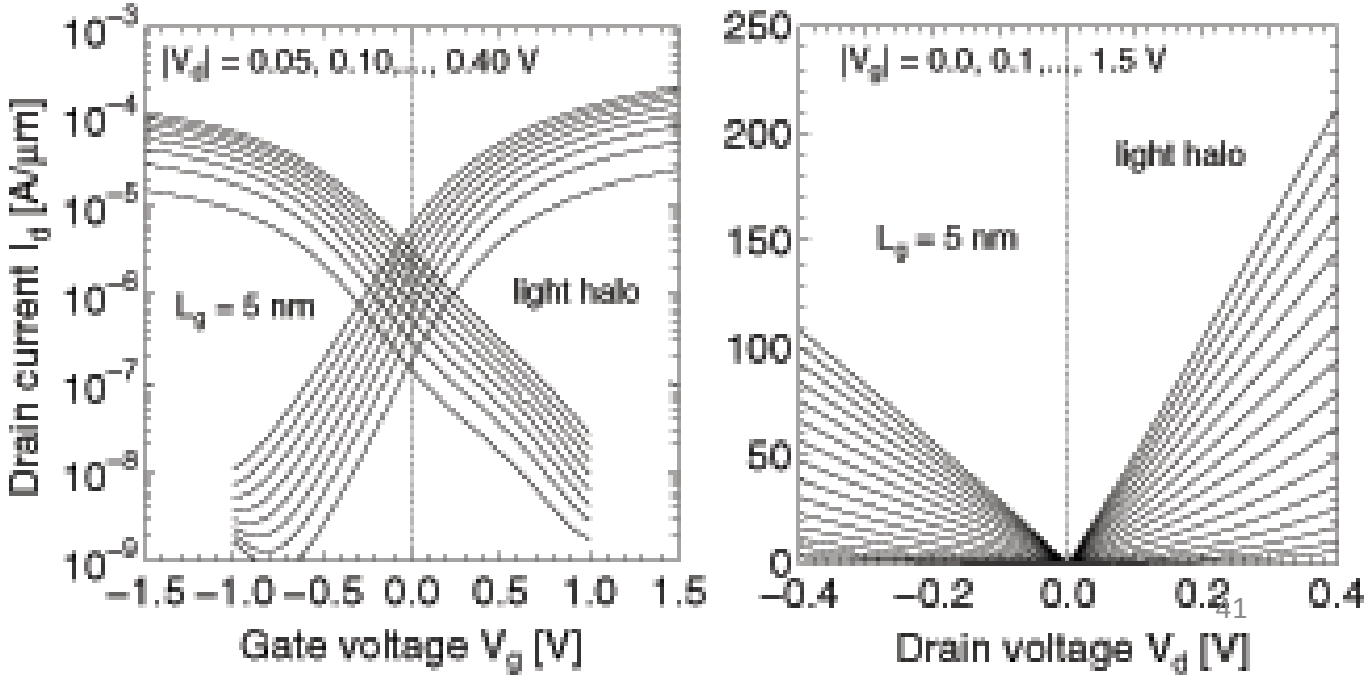


Length of 18 Si atoms



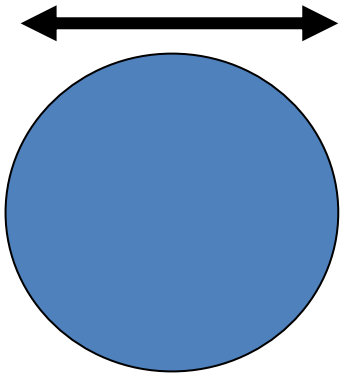
H. Wakabayashi
et.al, NEC

IEDM, 2003



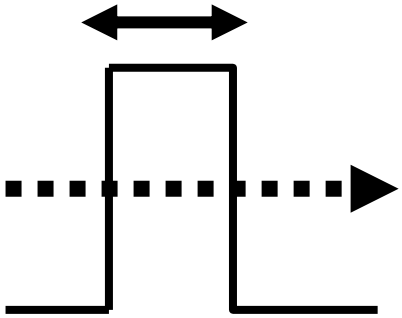
Electron wave length

10 nm



Tunneling distance

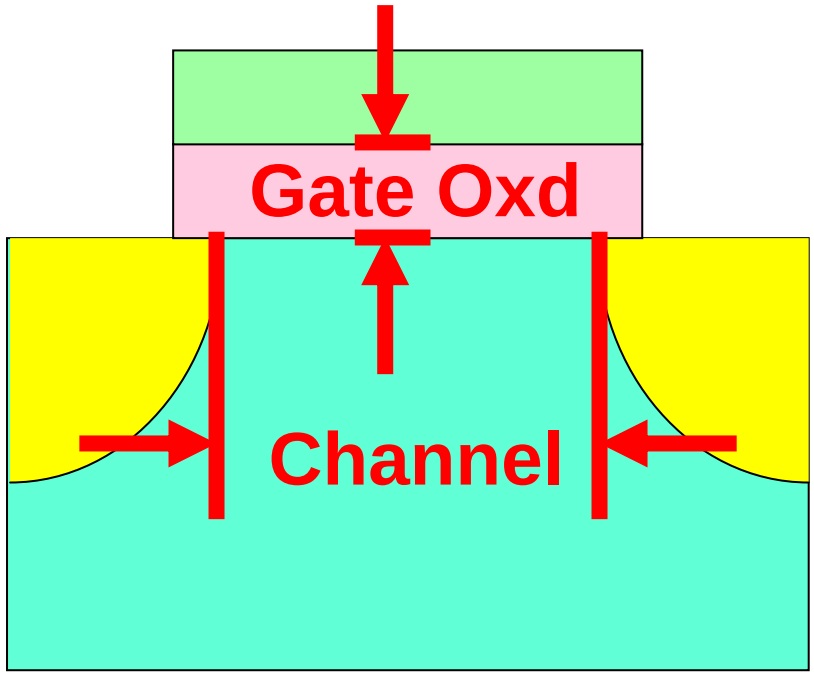
3 nm



Downsizing limit!

Channel length

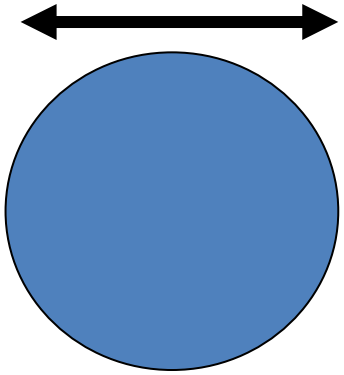
Gate oxide thickness



Prediction now!

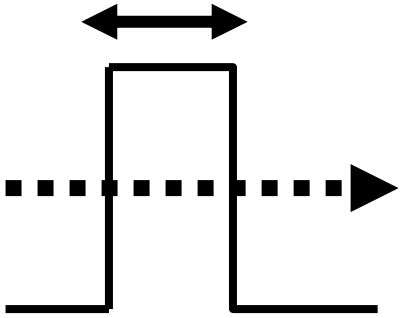
Electron wave length

10 nm



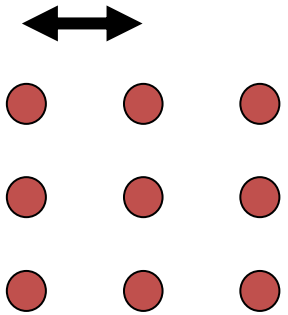
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

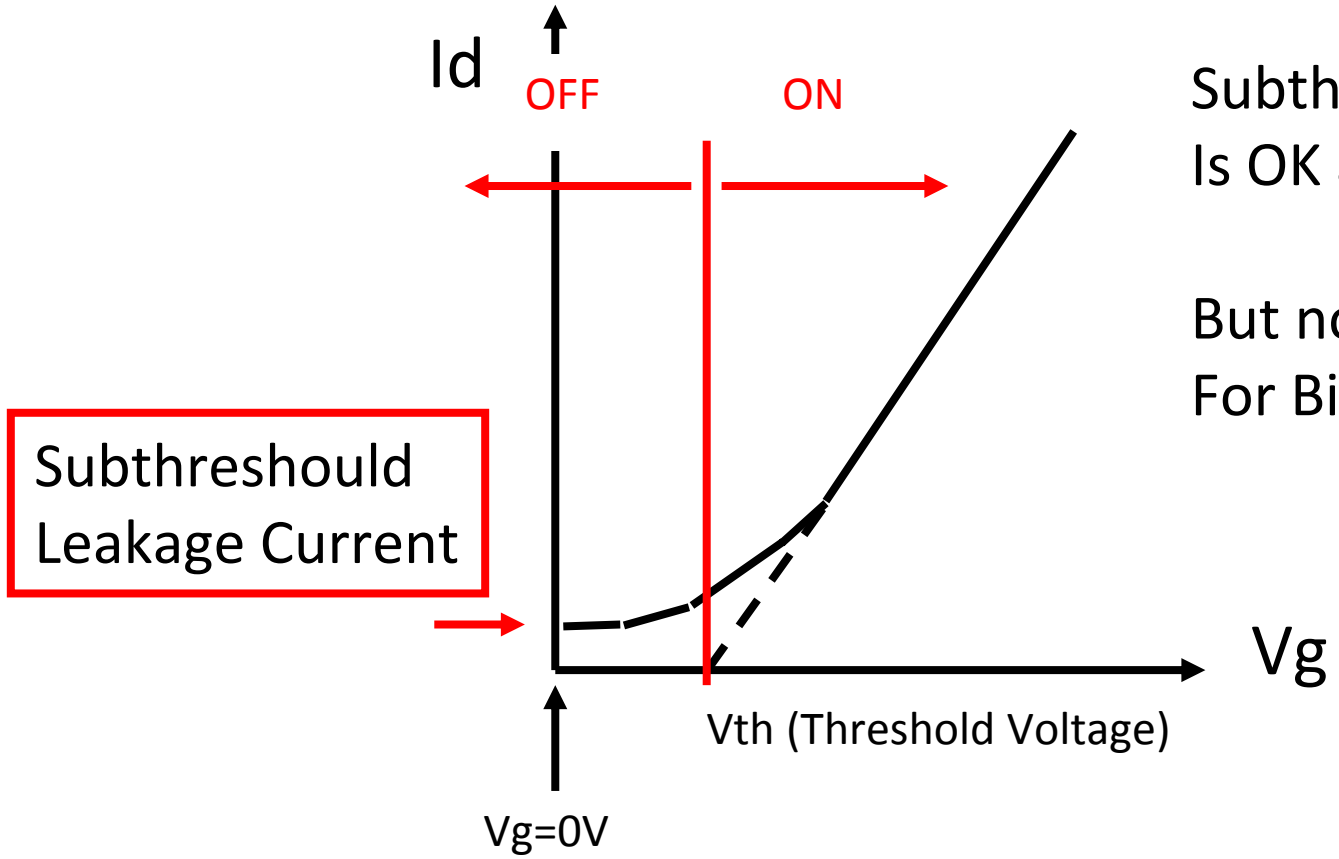
Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Maybe, practical limit around 5 nm.

When Gate length Smaller,

→ Subthrehold Leakage Current Larger

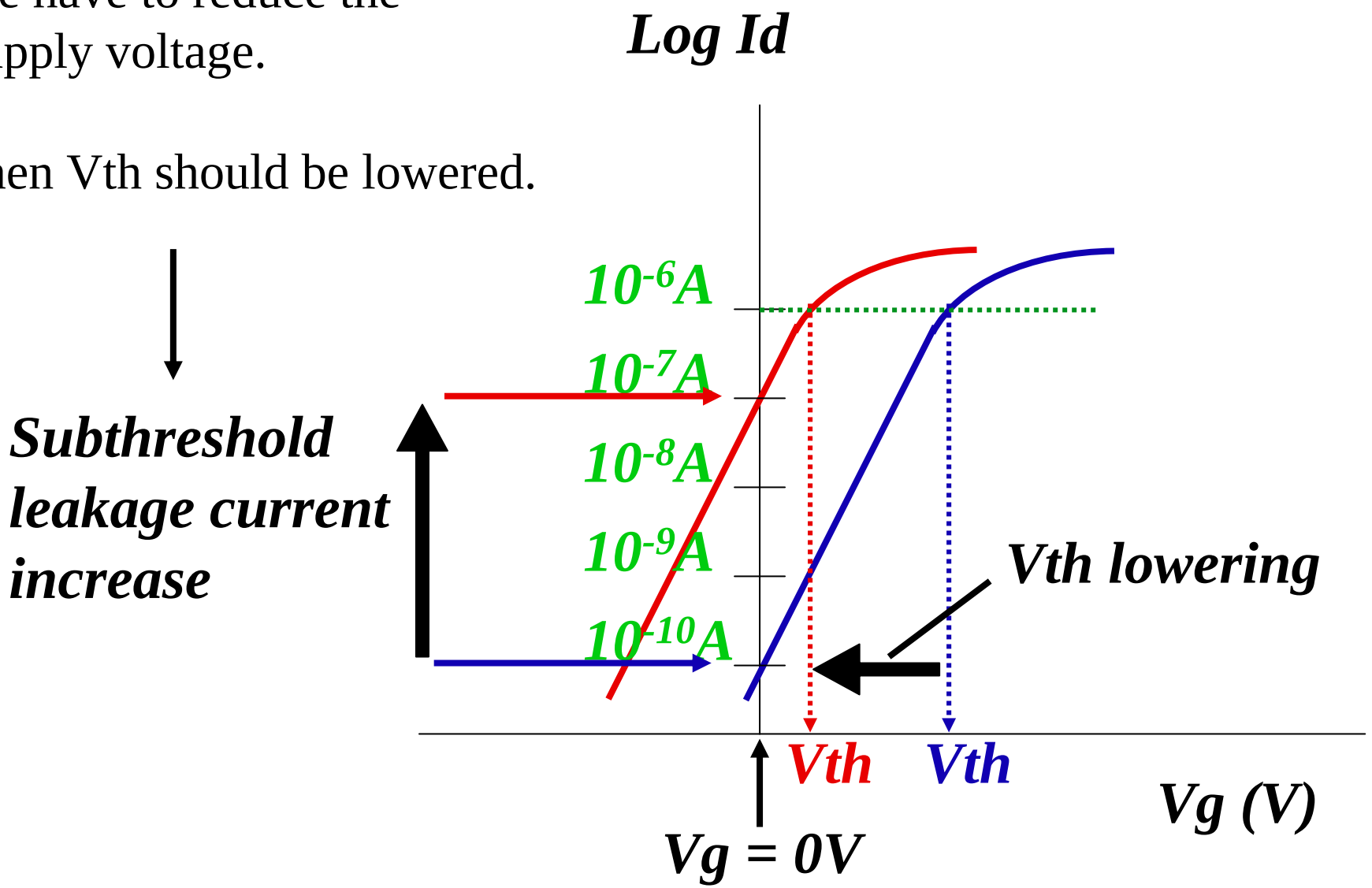


Subthreshold Current
Is OK at Single Tr.

But not OK
For Billions of Trs.

We have to reduce the Supply voltage.

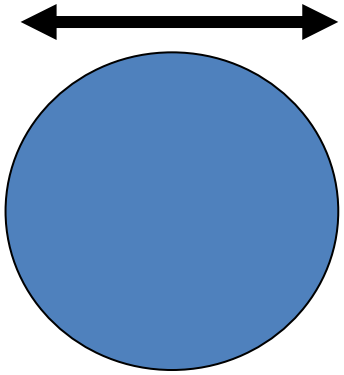
Then Vth should be lowered.



Prediction now!

Electron wave length

10 nm

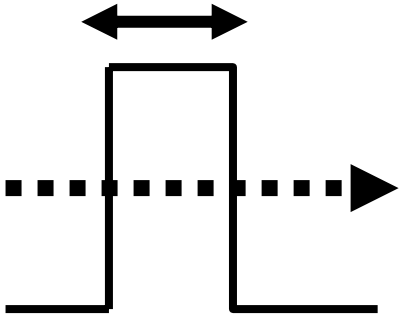


Practical limit for integration

Lg = 5 nm?

Tunneling distance

3 nm



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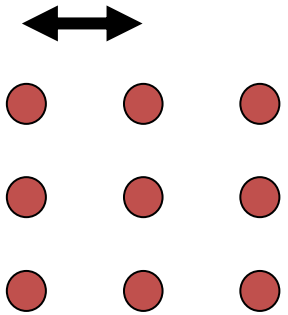
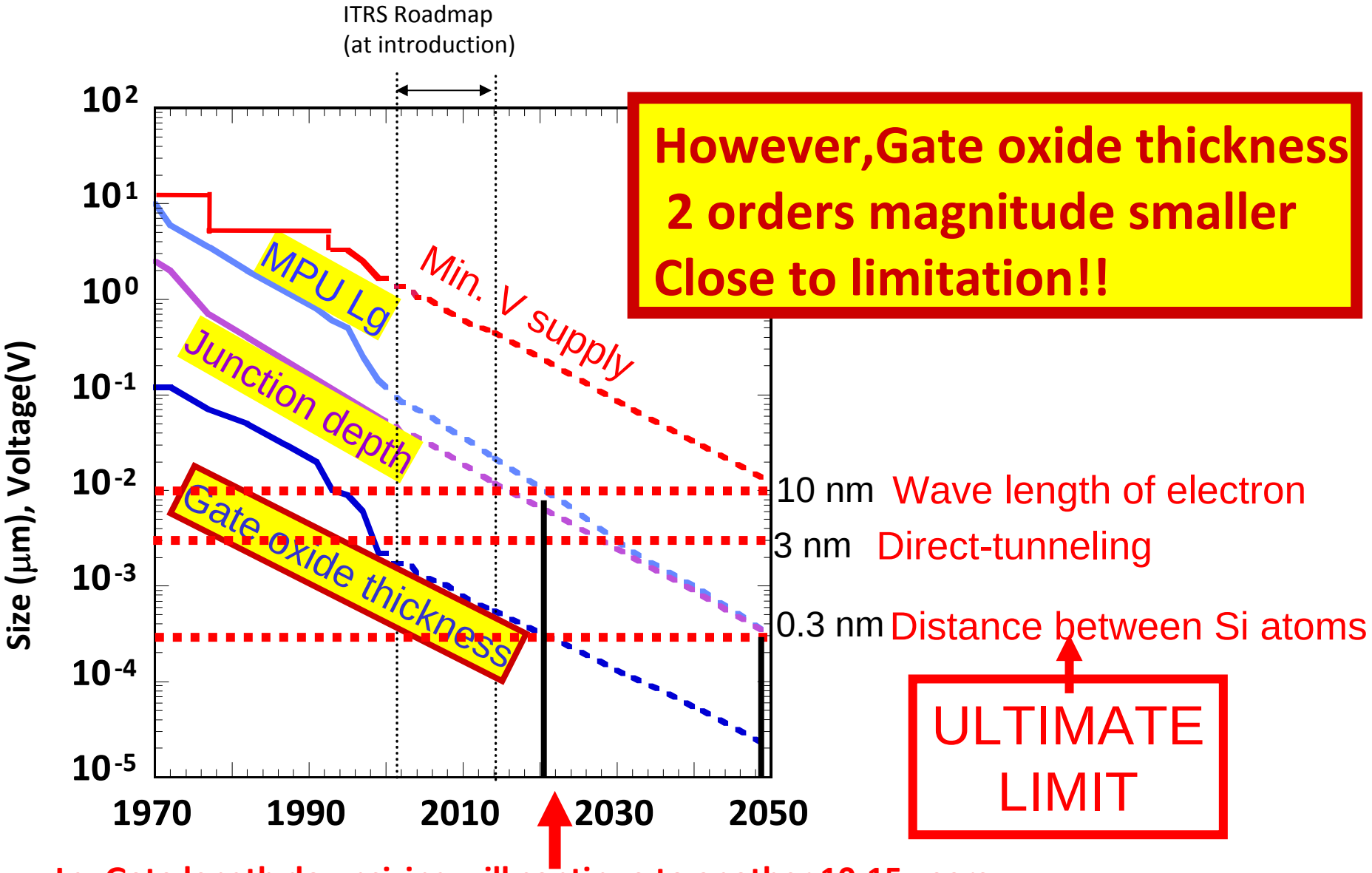


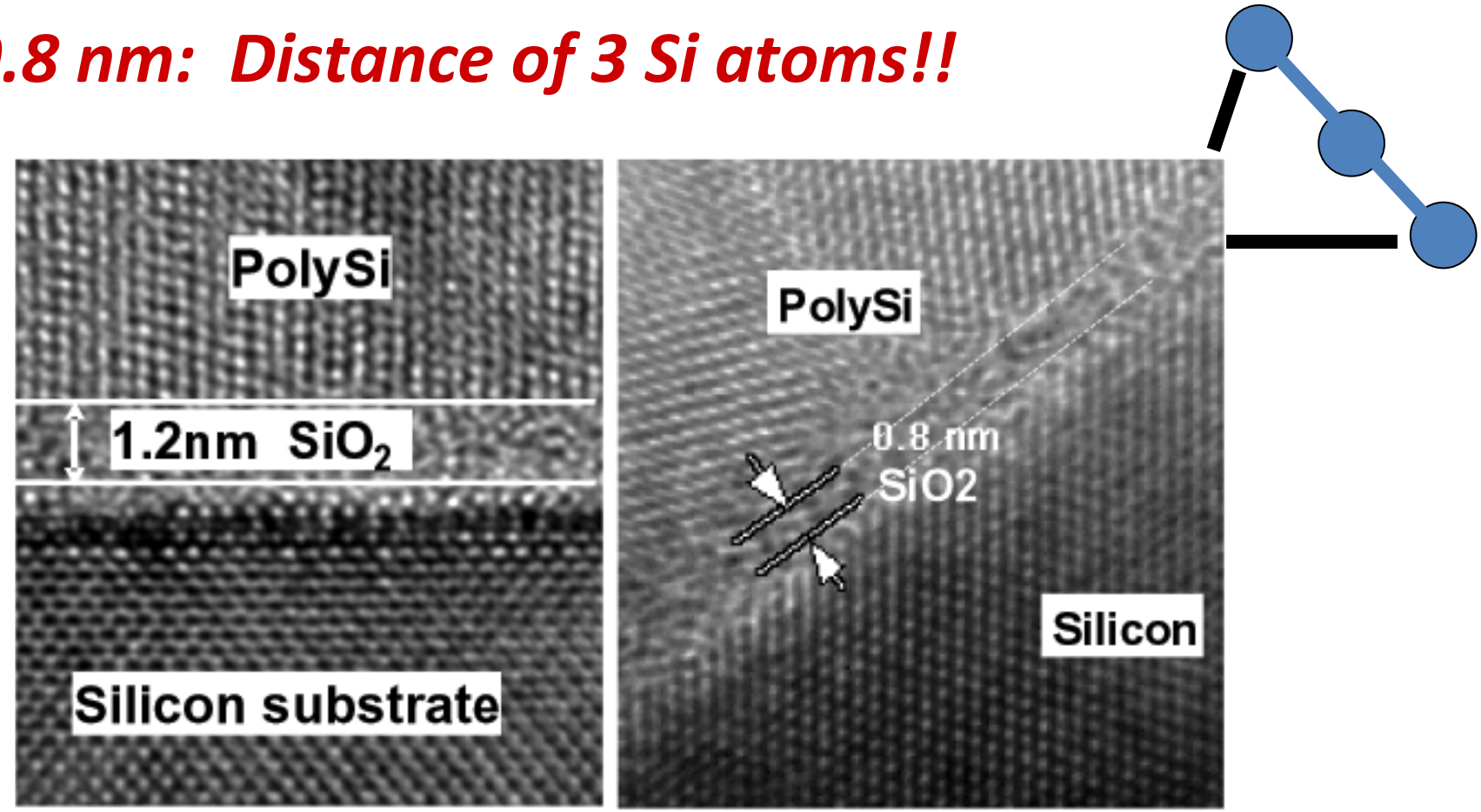
Below this, no one knows future!

Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operates!!

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

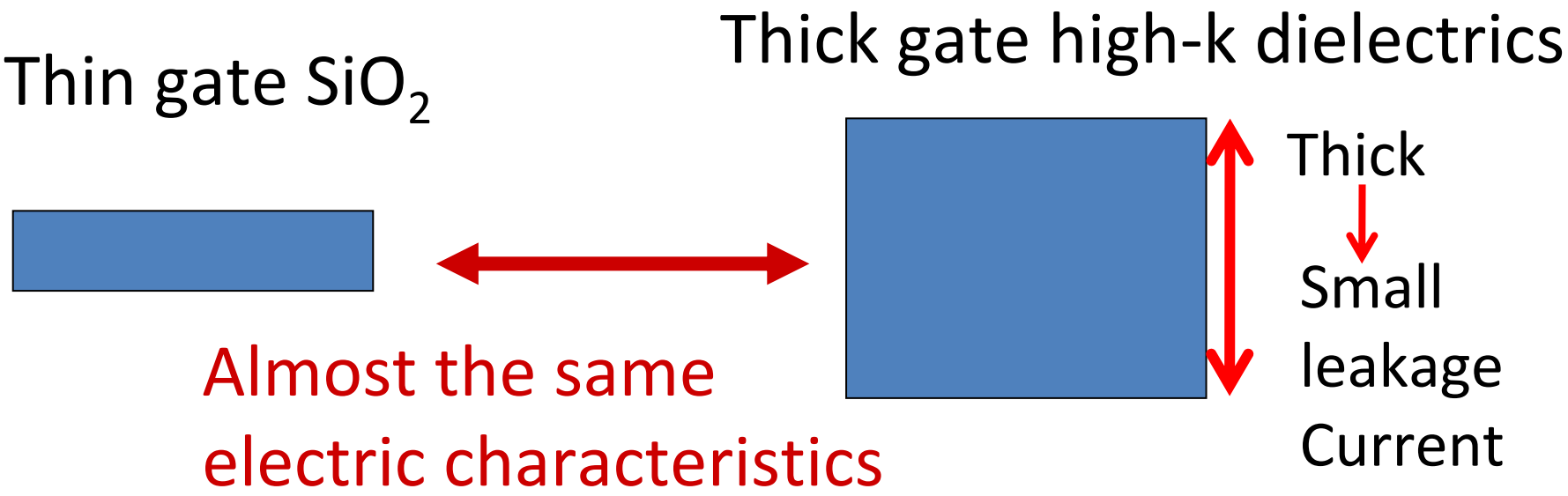
By Robert Chau, IWGI 2003

So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constant

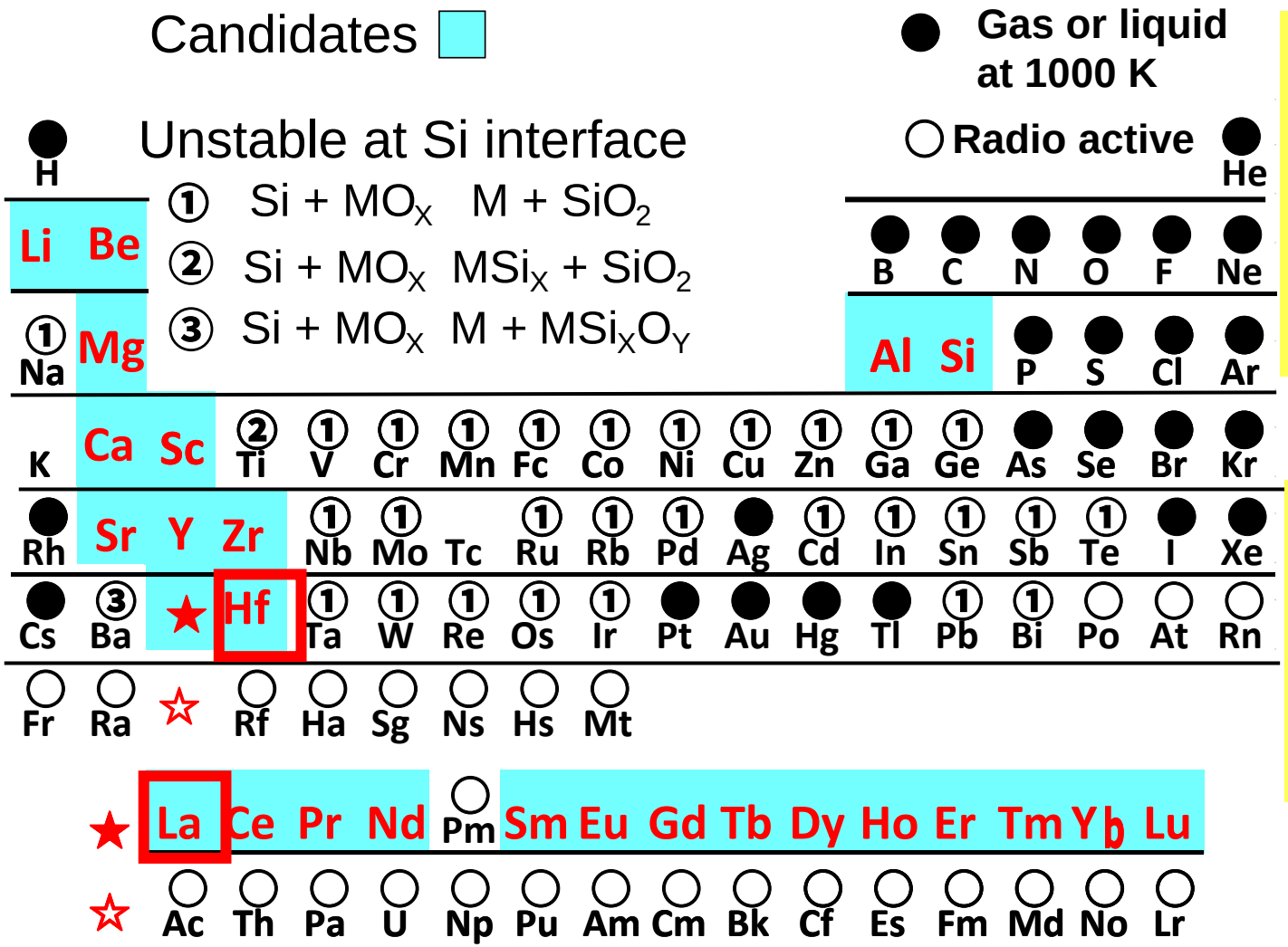
To use high-k dielectrics



However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

Choice of High-k elements for oxide



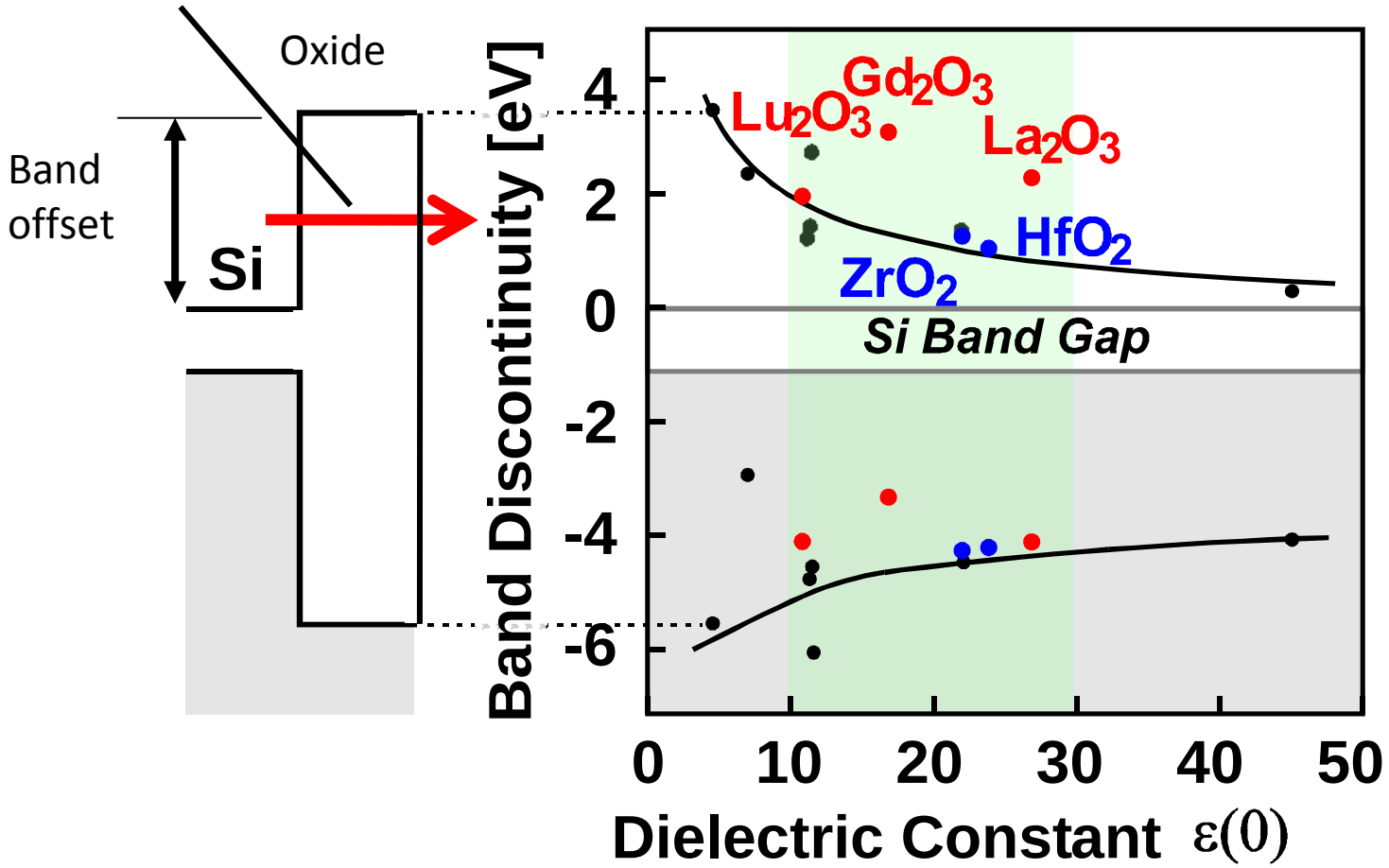
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Conduction band offset vs. Dielectric Constant

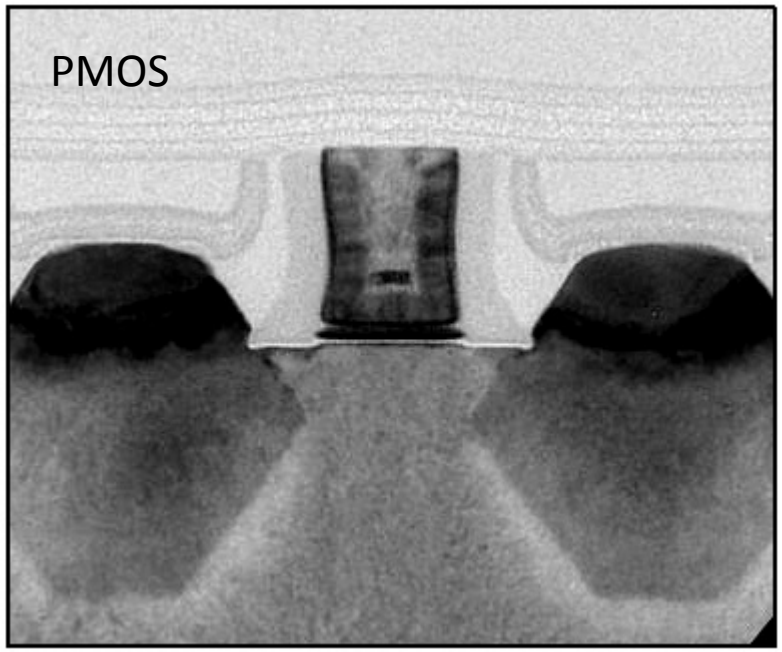
Leakage Current by Tunneling

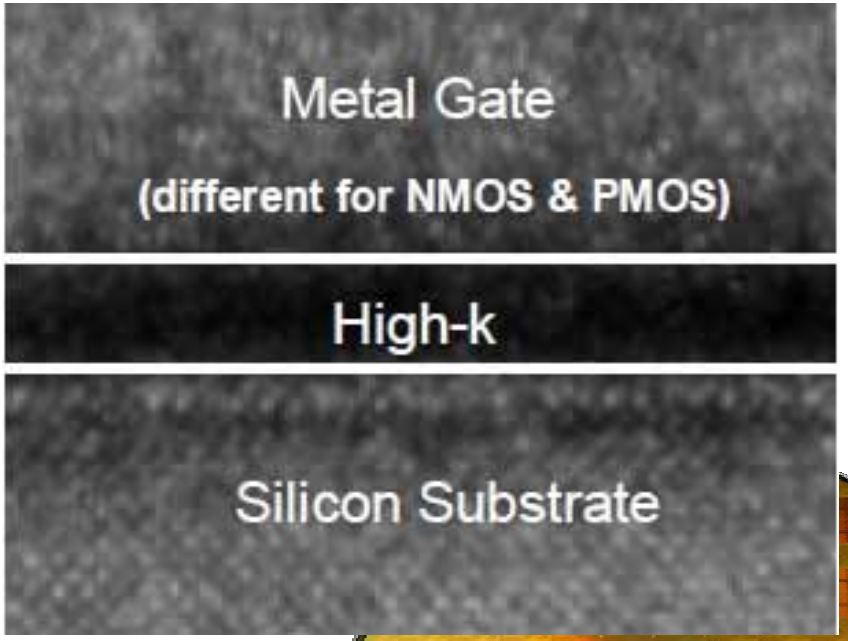


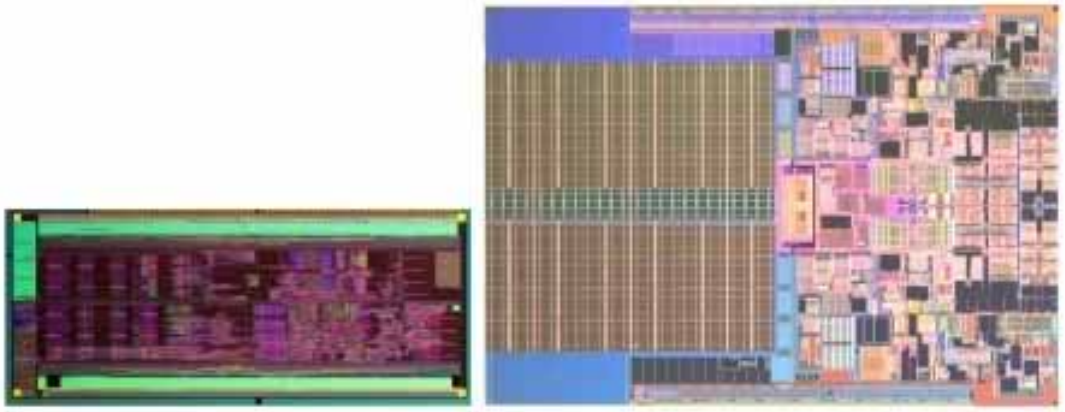
XPS measurement by Prof. T. Hattori, INFOS 2003

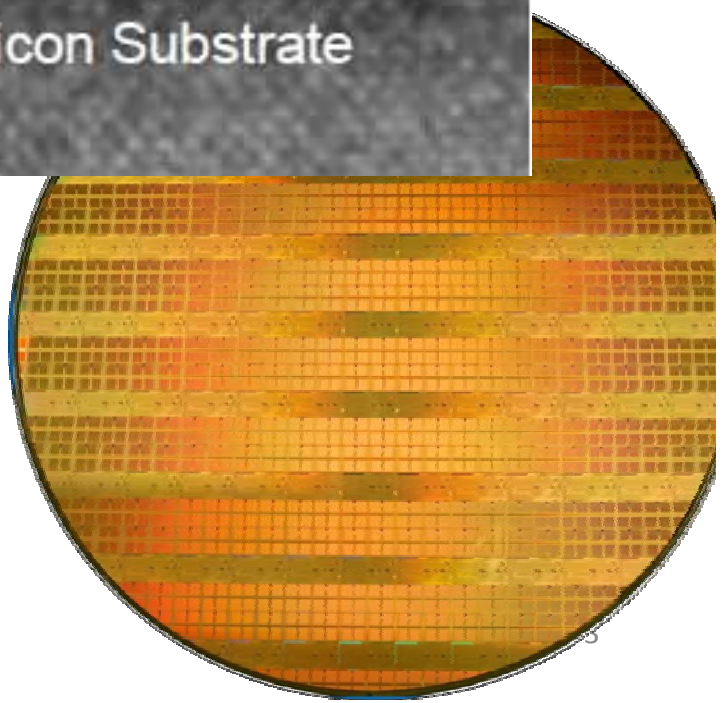
High-k gate insulator MOSFETs for Intel: EOT=1nm

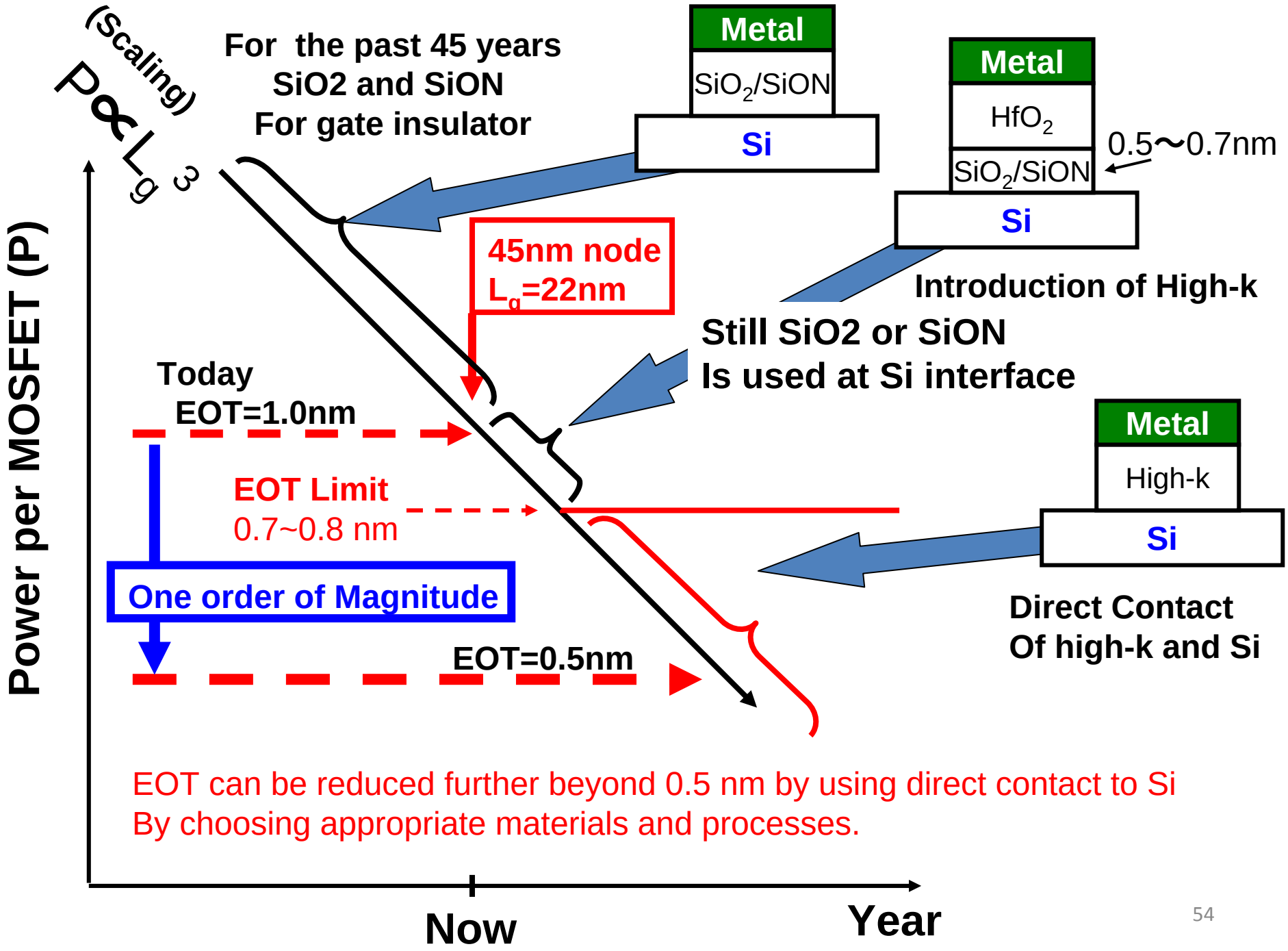
EOT: Equivalent Oxide Thickness



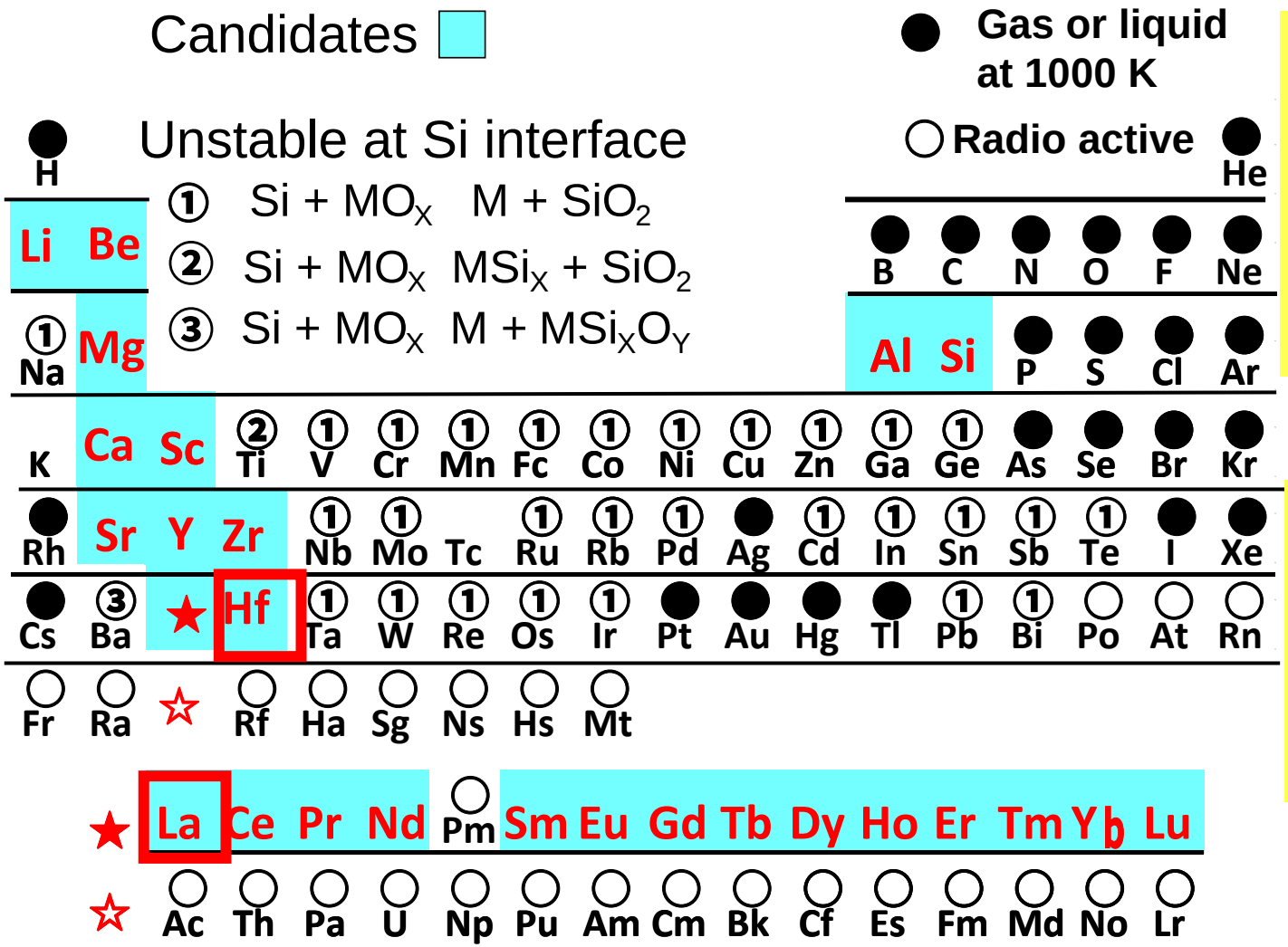







(scaling)
$P \propto L_g^3$
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO_2/SiON
Si
Metal
HfO_2
SiO_2/SiON
Si
0.5~0.7nm
45nm node
L_g=22nm
Introduction of High-k
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
One order of Magnitude
EOT=0.5nm
Metal
High-k
Si
Direct Contact
Of high-k and Si
Power per MOSFET (P)
Now
Year
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

Choice of High-k elements for oxide



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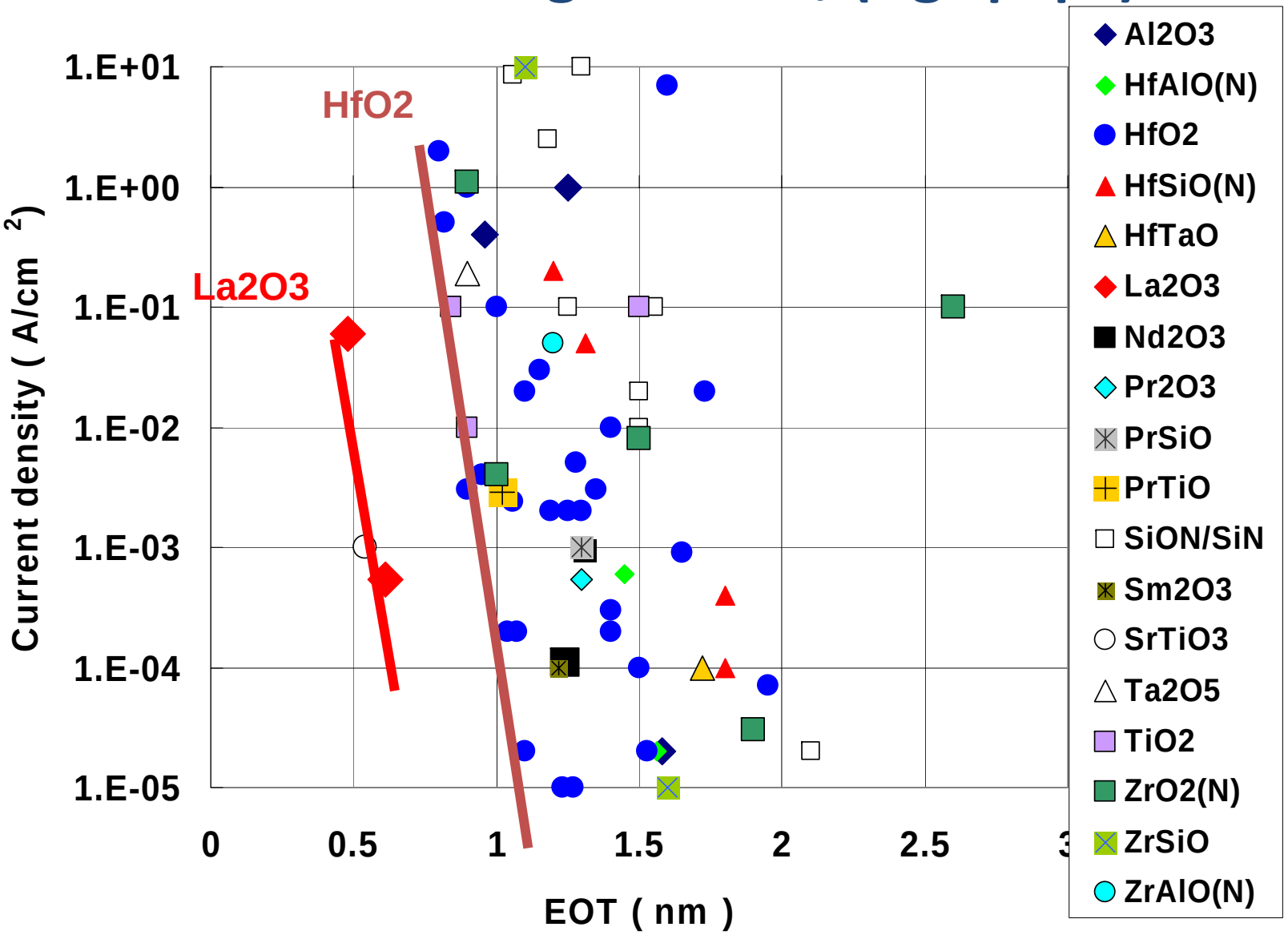
Hubbard and Schlom, J Mater Res 11 2757 (1996)

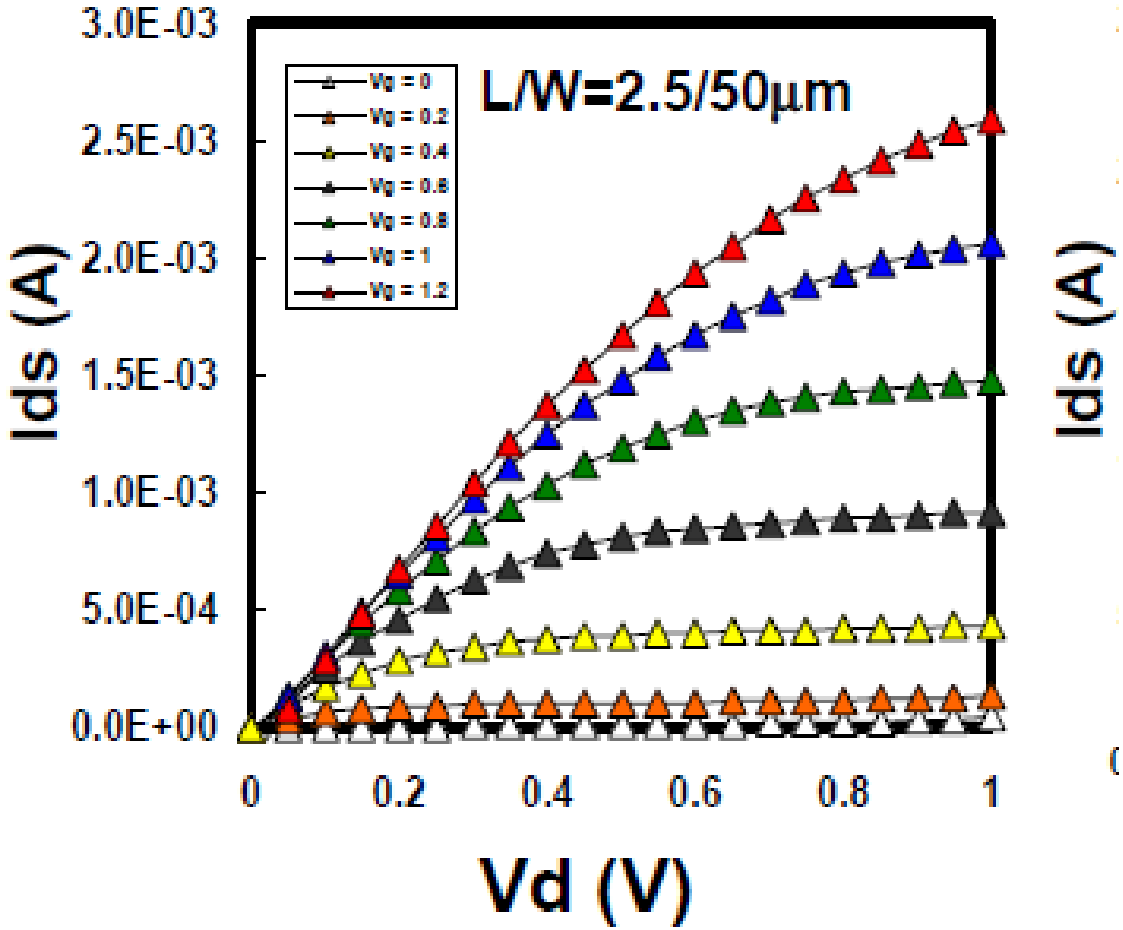
Gate Leakage vs EOT, (Vg=|1|V)



EOT = 0.48 nm

Our results

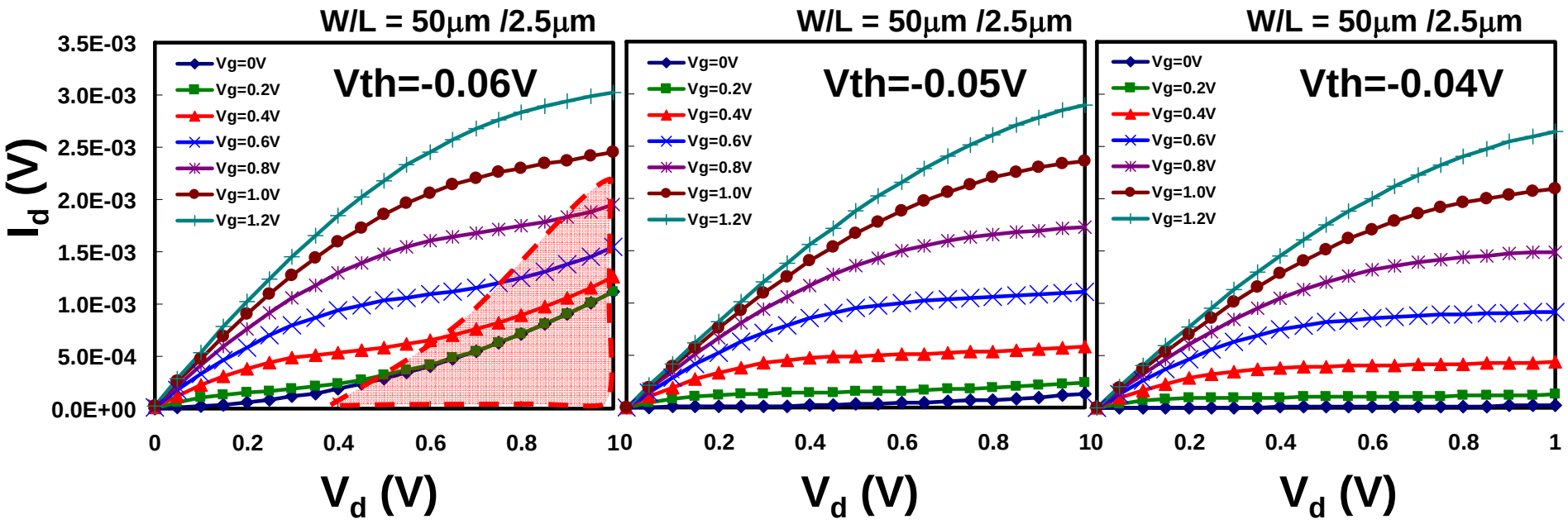
Transistor with La2O3 gate insulator



EOT=0.37nm

La2O3

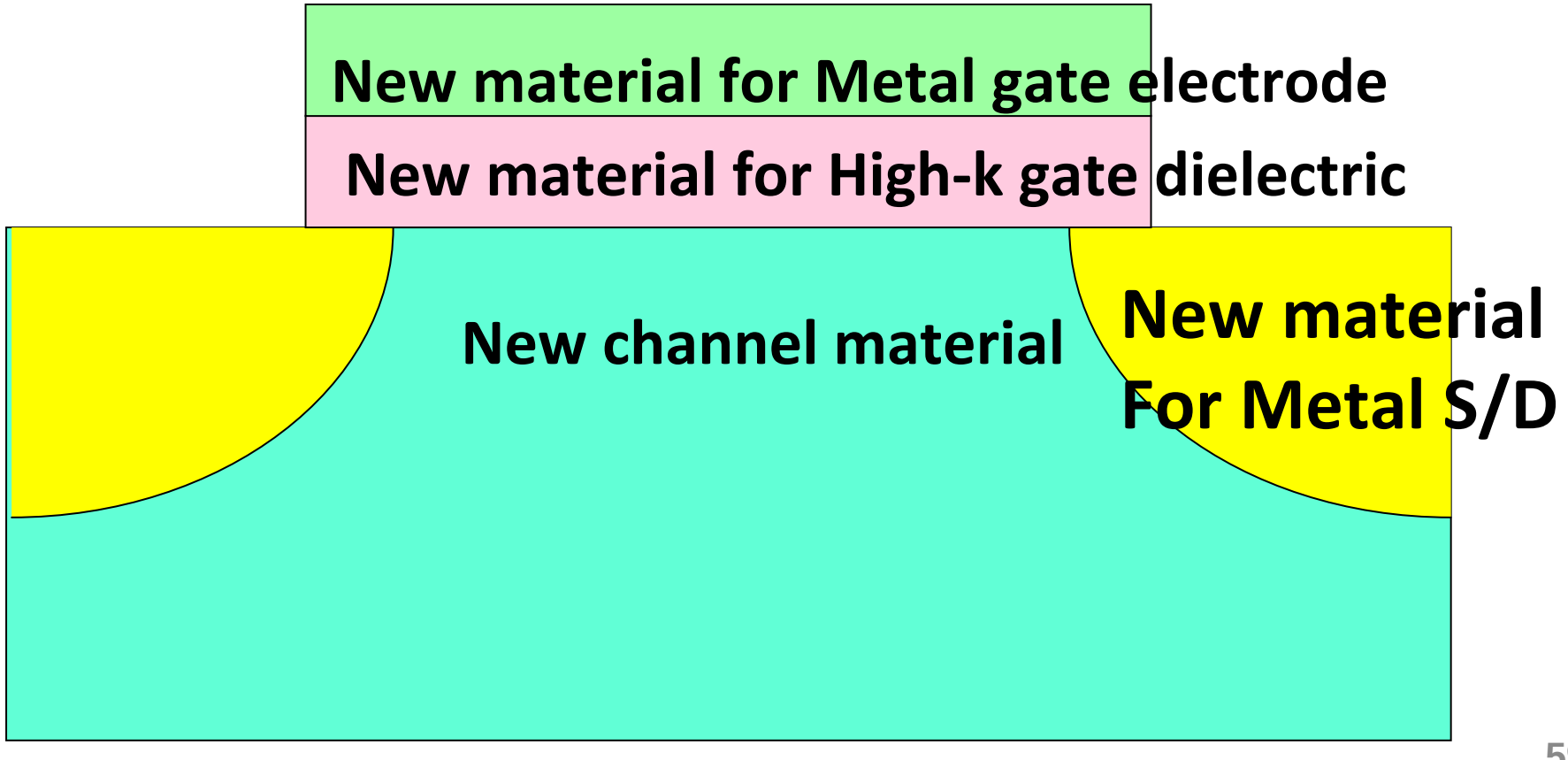
EOT=0.37nm EOT=0.40nm EOT=0.48nm



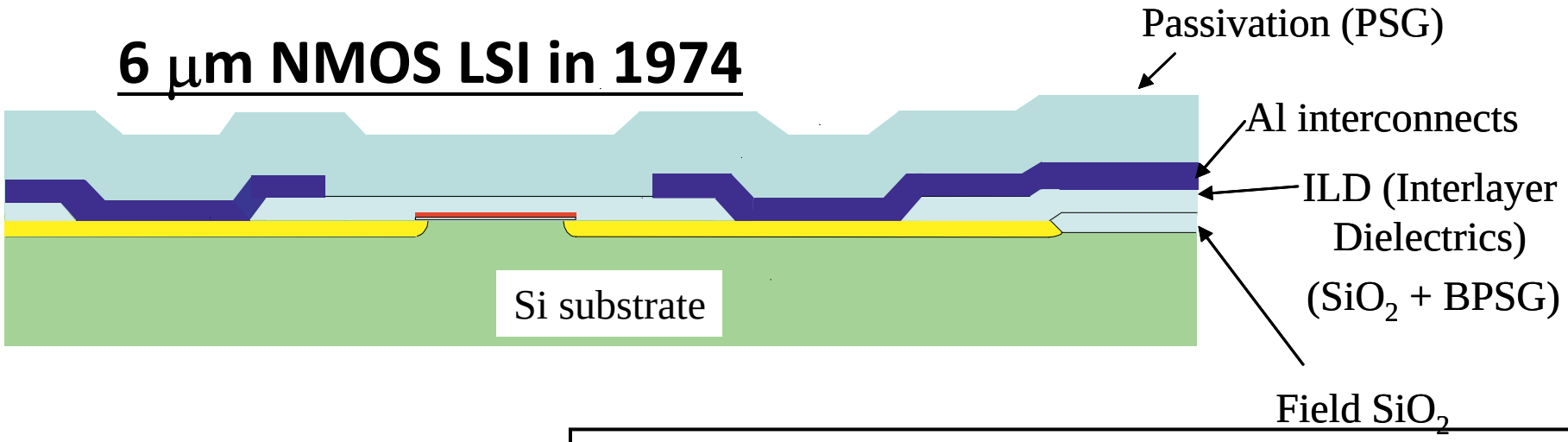
0.48 →0.37nm Increase of Id at 30%

New material research will give us many future possibilities and the most important for Nano-CMOS!

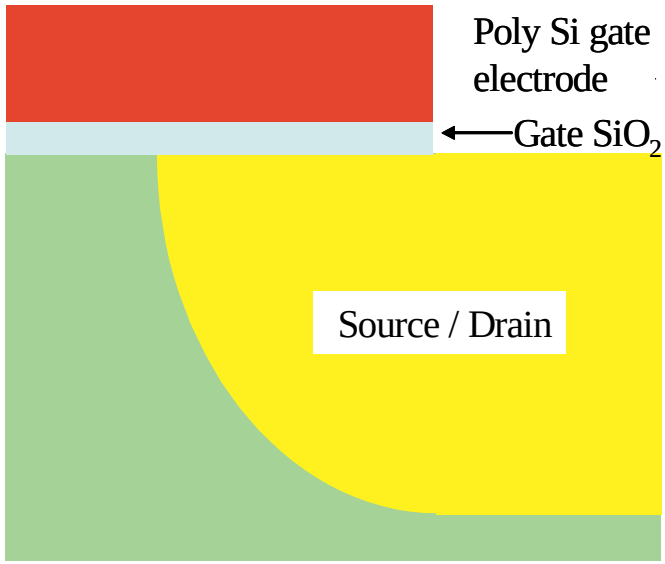
Not only for high-k!



6 μm NMOS LSI in 1974



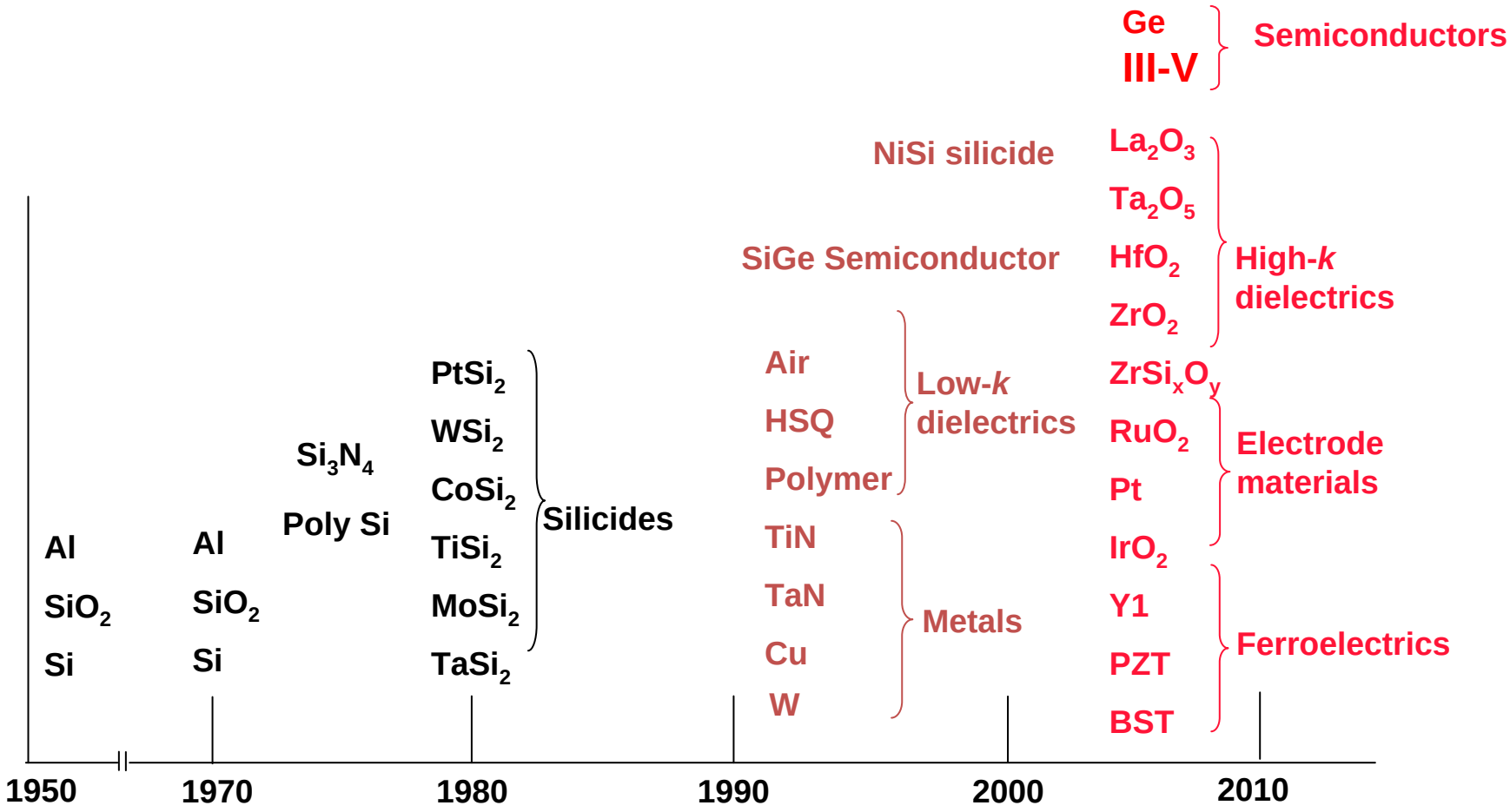
magnification



Layers	Materials	Atoms
1. Si substrate	1. Si	1. Si
2. Field oxide	2. SiO_2	2. O
3. Gate oxide	3. BPSG	3. P
4. Poly Si	4. Al	4. B
5. S/D	5. PSG	5. Al
6. Interlayer		(H, N, Cl)
7. Aluminum		
8. Passivation		

New materials

Just examples!
Many other candidates



Y. Nishi, Si Nano Workshop, 2006,

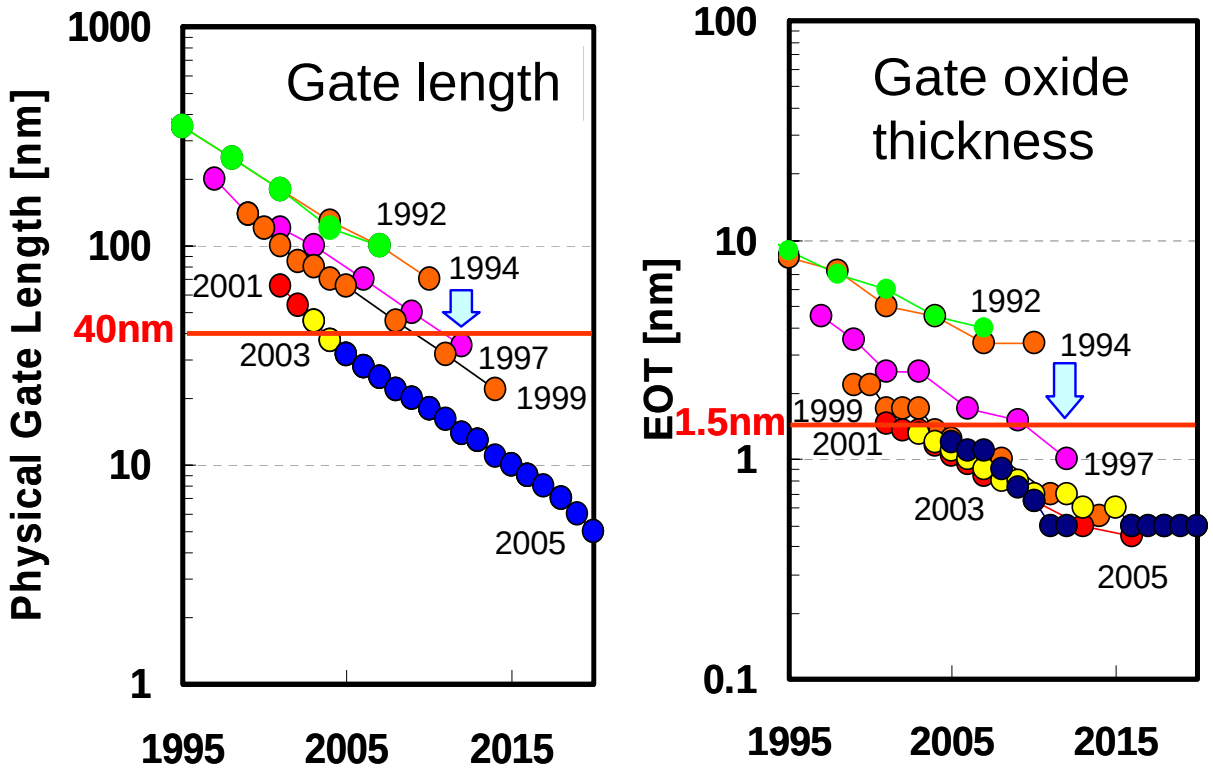
(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

What is a roadmap? What is ITRS?

Roadmap: Prediction of future technologies

ITRS: International Technology Roadmap for Semiconductors

made by SIA (Semiconductor Industry Association with collaboration with Japan, Europe, Korea and Taiwan

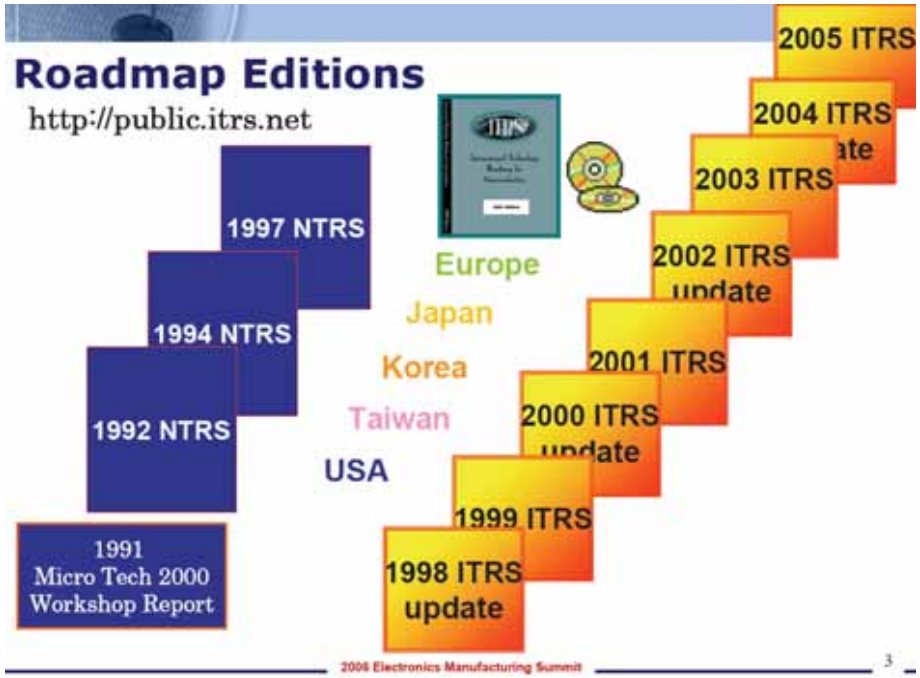


1992 -1997:NTRS (National Technology Roadmap)
1998 - : ITRS (International Technology Roadmap)

2008 ITRS update

2007 ITRS

2006 ITRS update



Now: After 45 Years from the 1st single MOSFETs

32 Gb and 16Gb NAND, SAMSUNG

NAND flash trend

Capacity	Node	1st Fabrication	Production
512Mbit	120nm	2000	2001
1Gbit	100nm	2001	2002
2Gbit	90nm	2002	2003
4Gbit	70nm	2003	2004
8Gbit	60nm	2004	2005
16Gbit	50nm	2005	2006
32Gbit	**40nm**		
256Gbit	**20nm**		

Even Tbit would be possible in future!

Already 32 Gbit:

larger than that of world population
comparable for the numbers of neurons
in human brain

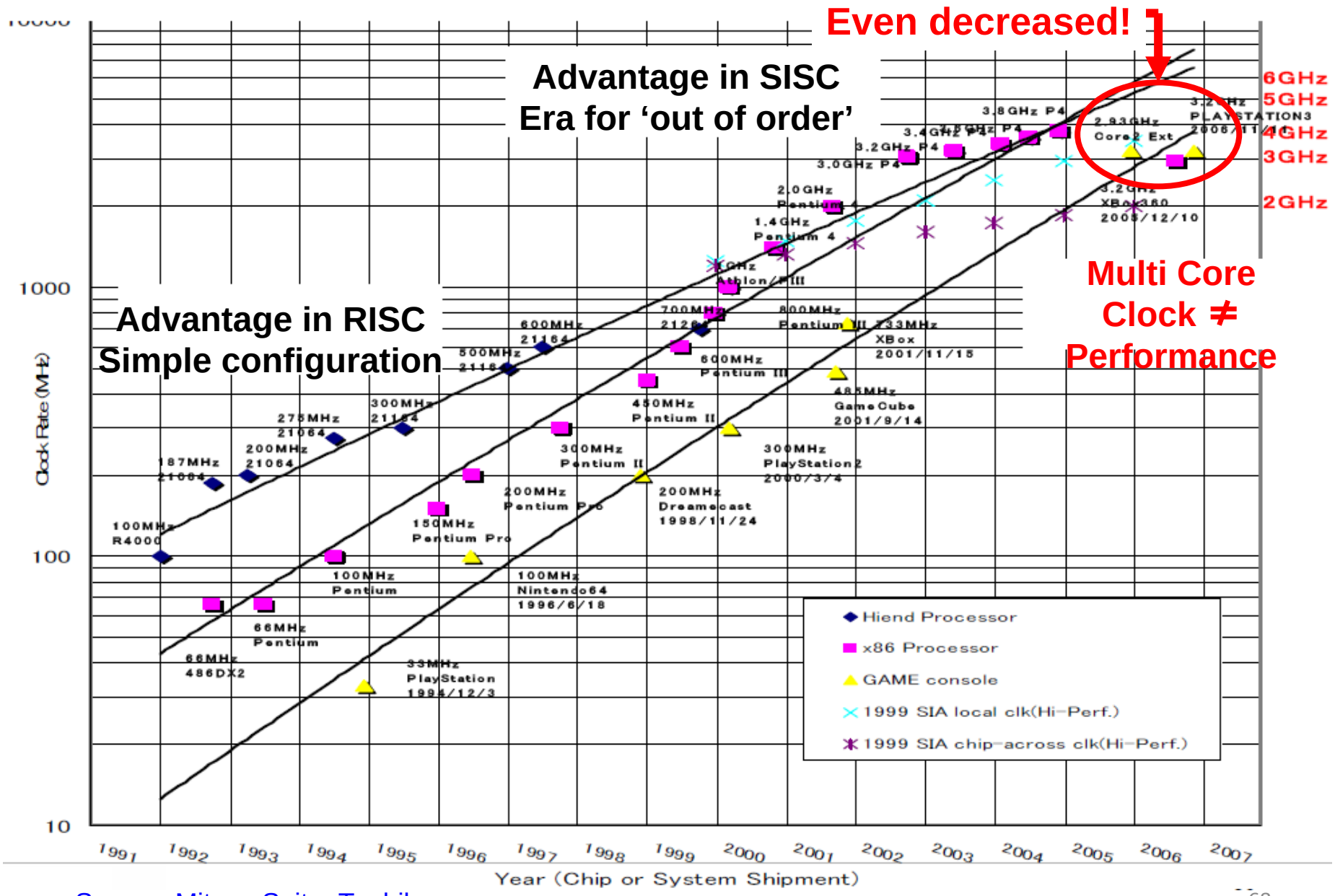
Samsung announced 256 Gbit will be produced in 2010.
Only 4 years from now.
256Gbit: larger than those of # of stars in galaxies

8μm → 6μm → 4μm → 3μm → 2μm → 1.2μm → 0.8μm → 0.5μm

→ 350nm → 250nm → 180nm → 130nm → 90nm → 65nm → 45nm

→ 32nm → 22nm → 16nm → 11nm → 8nm?? → 5.5nm ??

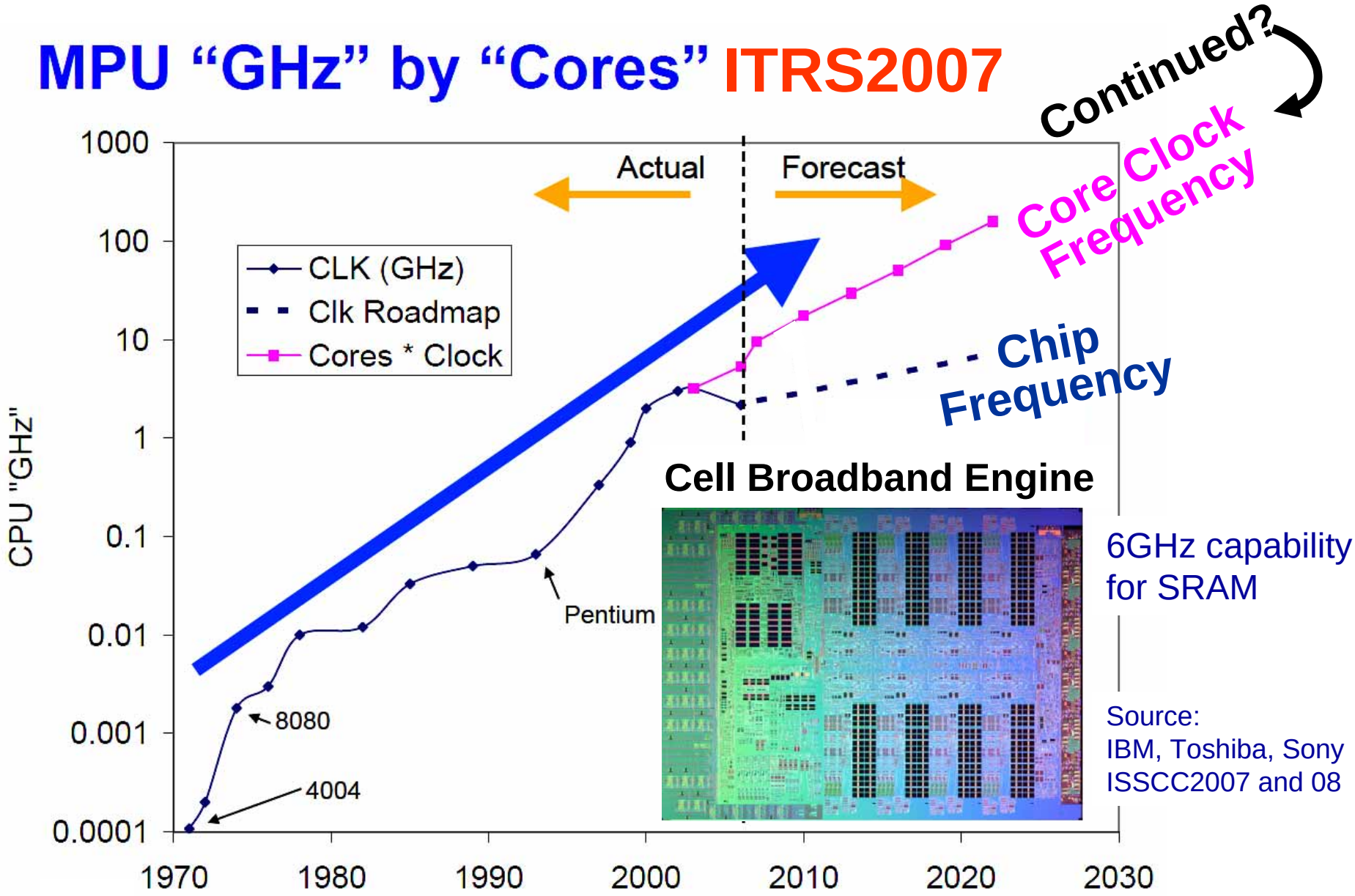
Clock frequency does not increase aggressively anymore.



Source: Mitsuo Saito, Toshiba

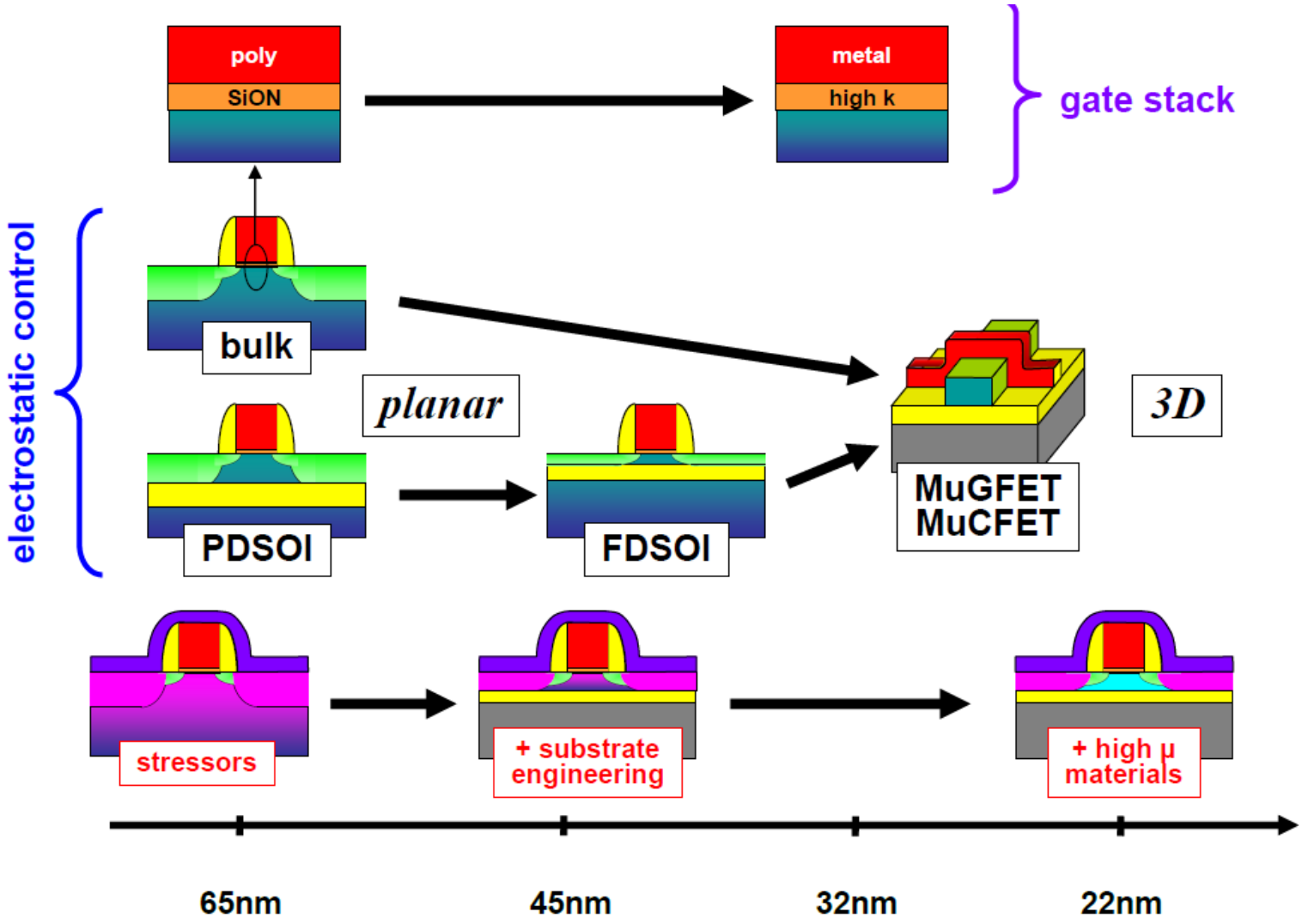
68

MPU "GHz" by "Cores" ITRS2007



Source: 2007 ITRS Winter Public Conf.

Structure and technology innovation (ITRS 2007)



Source: 2008 ITRS Summer Public Conf.

70

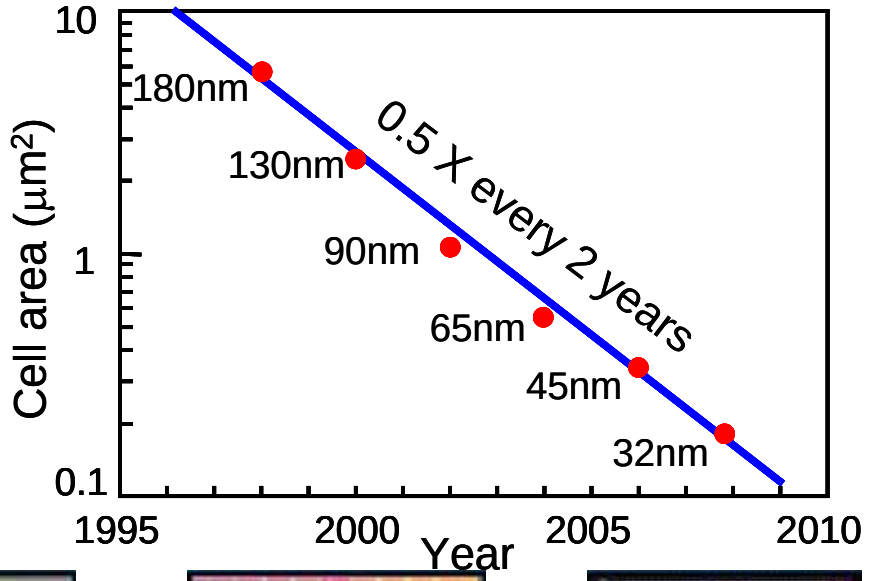
Intel's **SRAM** test chip trend

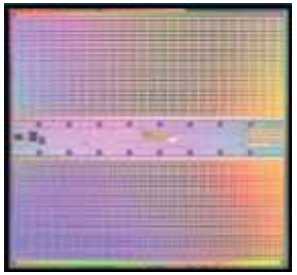
Source: B. Krzanich, S. Natrajan, Intel Developer's Forum 2007
http://download.intel.com/pressroom/kits/events/idffall_2007/BriefingSilicon&TechManufacturing.pdf

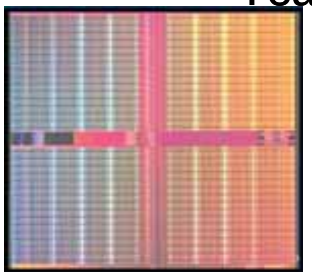
SRAM down-scaling trend has been kept until 32nm and probably so to 22nm

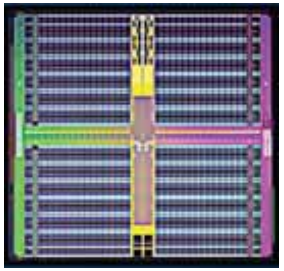
Process name	Lithography	1st production
P1264	65nm	2005
P1266	45nm	2007
P1268	32nm	2009
P1270	22nm	2011

Only schedule has been published





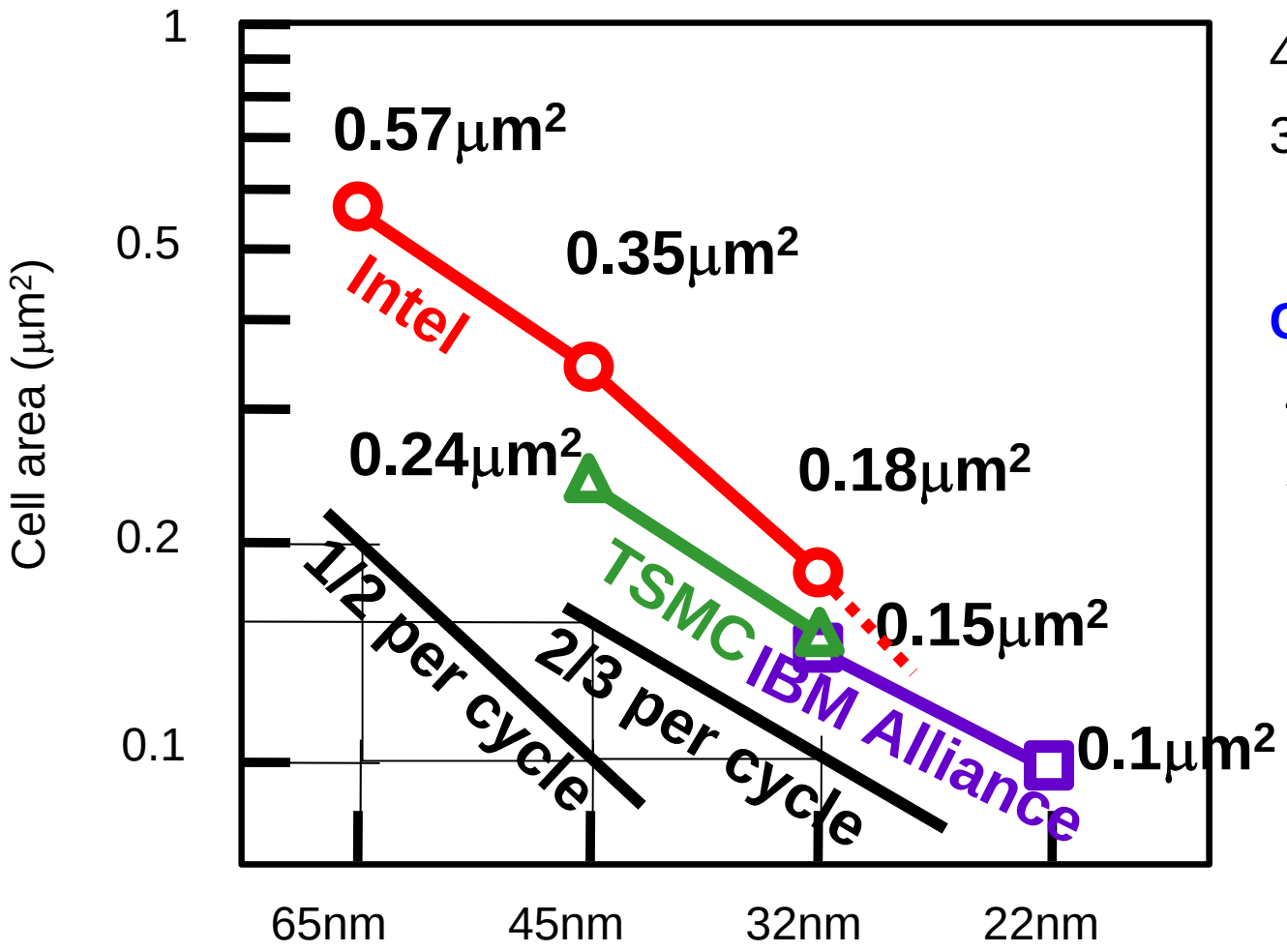




Technology	**90 nm Process**	**65 nm Process**	**45 nm Process**	**32 nm Process**
Cell size	**1.0 μm²cell**	**0.57 μm²cell**	**0.346 μm²cell**	**0.182 μm²cell**
Capacity	50 Mbit	70 Mbit	153 Mbit	291 Mbit
Chip area	109 mm²	110 mm²	119 mm²	118 mm²
Functional Si	February '02	April '04	January '06	September '07

Cell size reduction trends

1/2 or 2/3 per cycle?



Intel

Functional Si

65nm Apr.2004

45nm Jan.2006

32nm Sep.2007

TSMC

Conference (IEDM)

45nm Dec.2007

32nm Dec.2007

IBM Alliance (Consortium)

Conference (IEDM)

32nm Dec.2007

Press release

22nm Aug.2008

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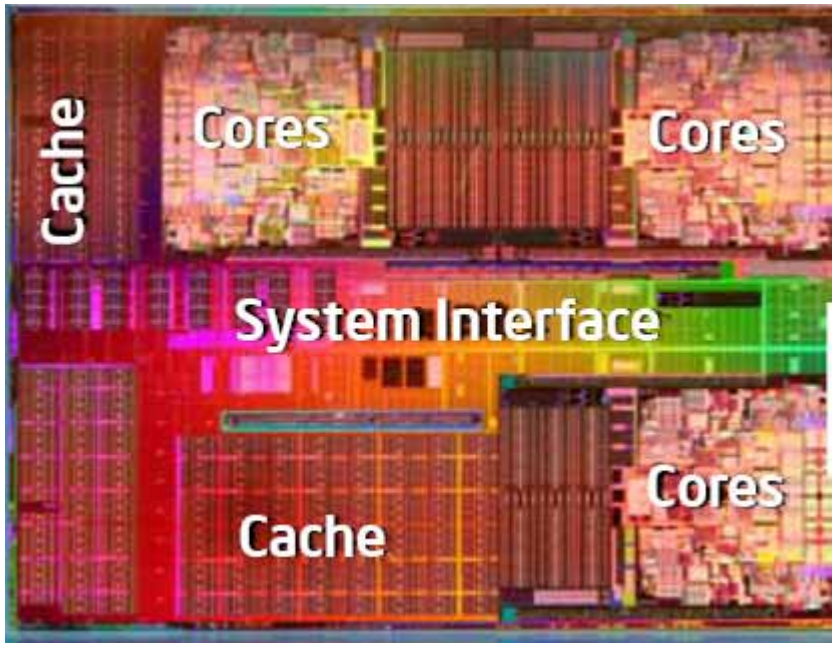
Most Difficult part of SRAM down-scaling is Vdd down-scaling

Density of on-chip cache SRAM memory is high and thus, Vth cannot be down-scaled too much because of large Isd-leak

Also, under low Vdd, read- and write margin degrades, data retention degrade.

Thus, Vdd down-scaling is more severe in SRAM than logic part of the circuits

Intel® Xeon® 7400 Series
(Dunnington)



45 nm high-k6 cores

16MB shared L3 cache

Source: Intel Developer Forum 2008

Cache occupies huge area

→ Cell size of SRAM should be minimized

→ Isd-leak should be minimized

→ Vth are often designed to be higher than Min. logic Vth

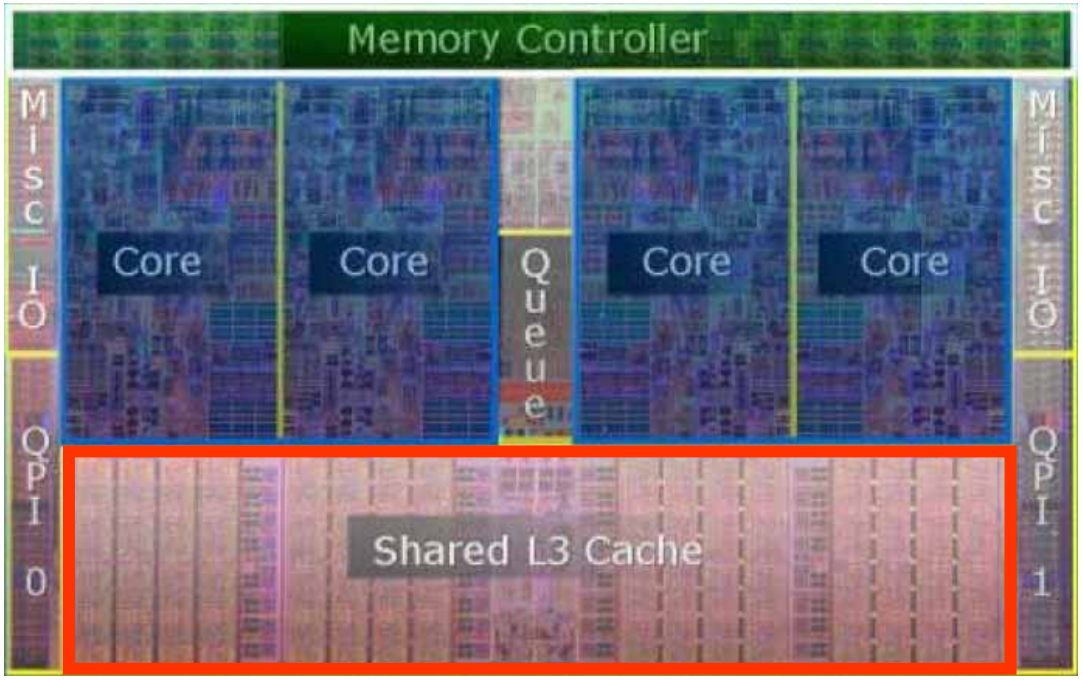
→ Lg are often designed to be larger than Min. logic Lg

Nehalem(Intel) 2,4 or 8 Cores

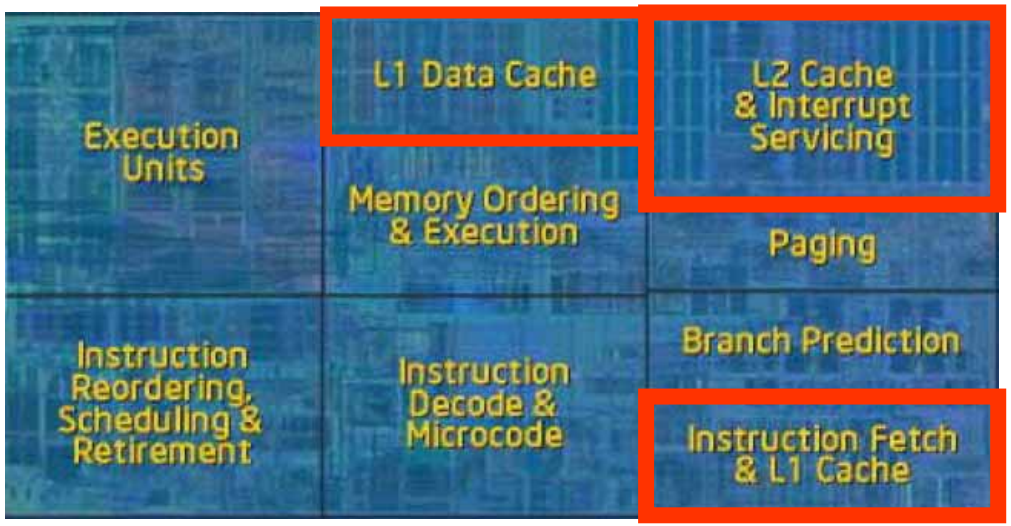
Voltage/Frequency Partitioning

- DDR Vcc
- Core Vcc
- Uncore Vcc

Dynamic Power Management



Chip



Core

8T SRAMCell

32kB L1 I -cache

32kB L1 D-cache

256kB L2 -cache

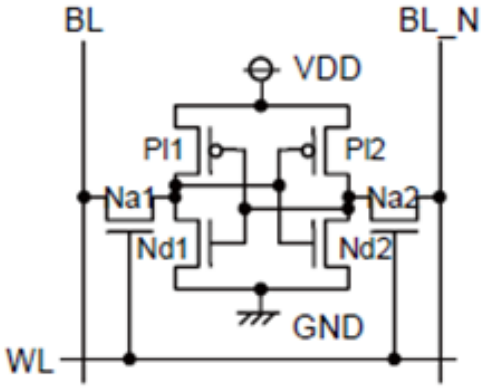
6T SRAMCell

8 MB L3 cache

Source: Intel Developer Forum 2008

6T and 8T Cell

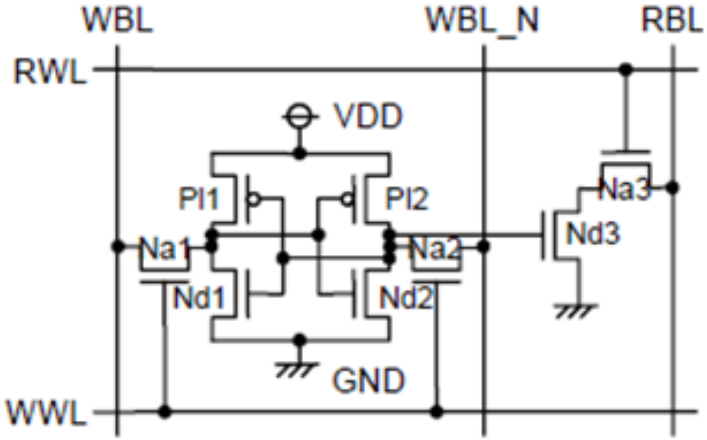
6T Cell



Cell size is small

For high density use

8T Cell



Add separate read function

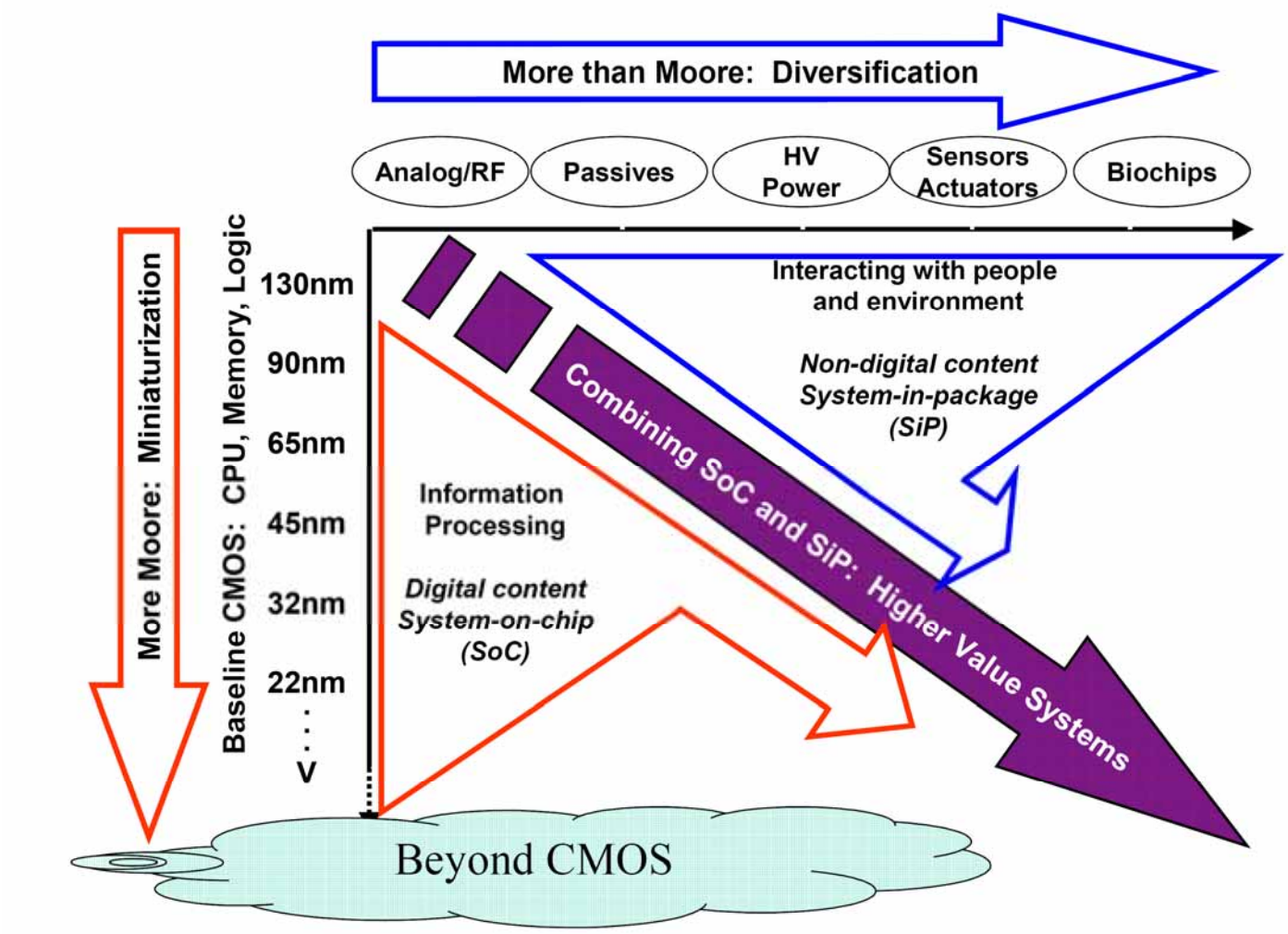
Cell size increase 30%

For low voltage use

Source: Morita et. al, Symp. on VLSI Circ. 2007

More Moore and More than Moore

Moore's Law & More

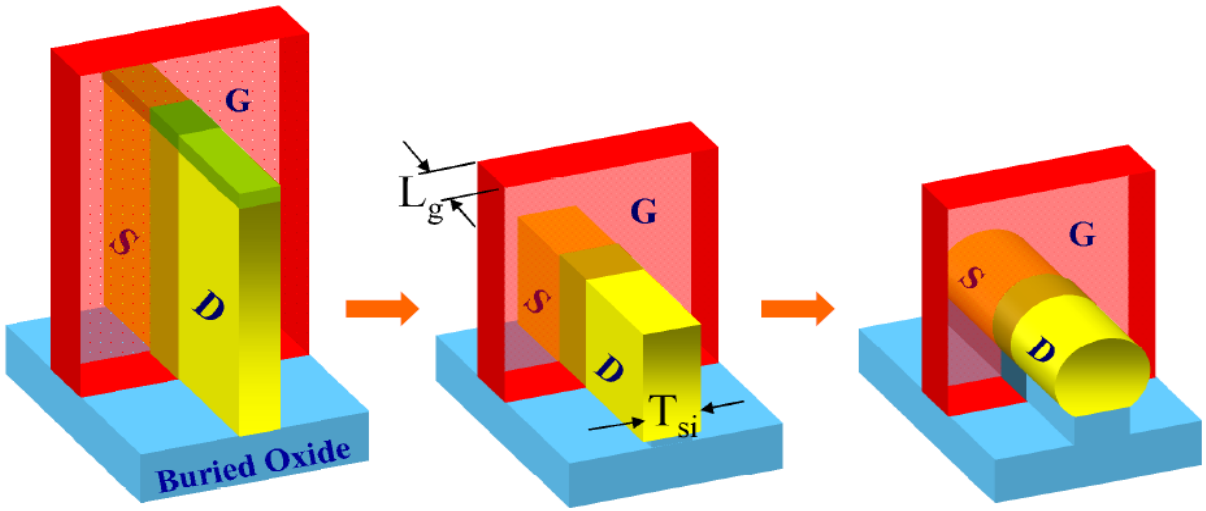


Question what is the other side of the cloud?

ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

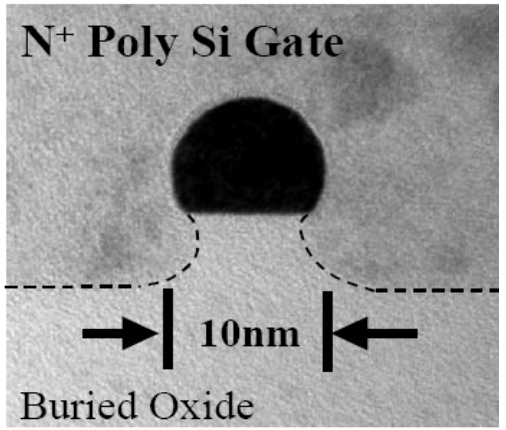
FinFET to Nanowire

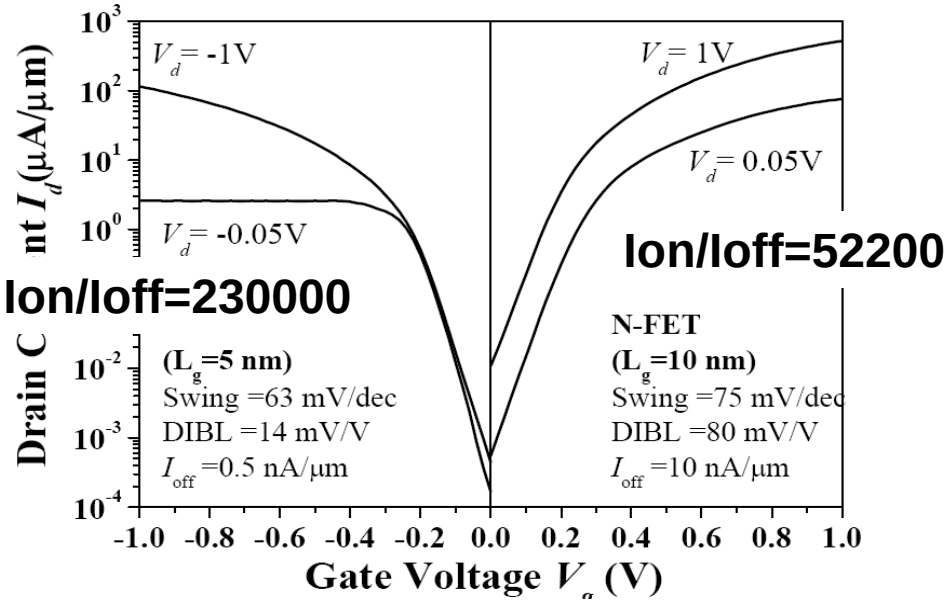


Double-Gate FinFET ($T_{si} = {}^{2}/_{3}\, L_g$)

Omega FinFET ($T_{si} = L_g$)

Nanowire FinFET ($T_{si} = 2L_g$)





Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

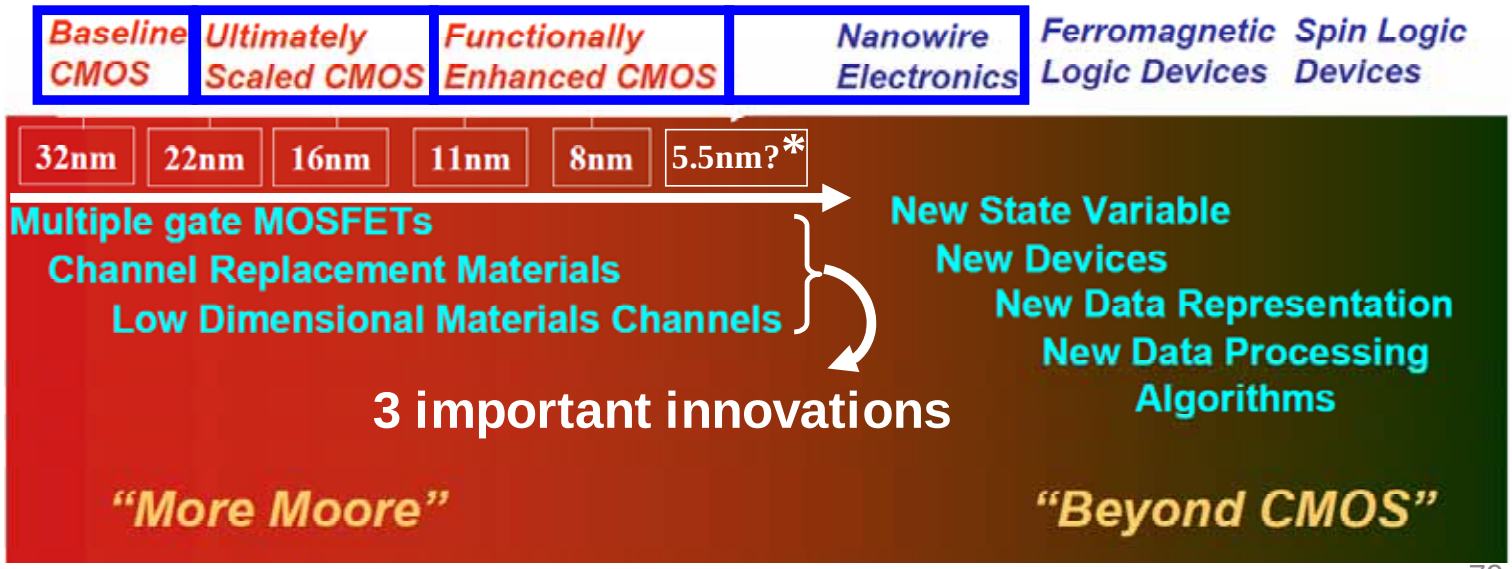
-There will be still 4~6 cycles (or technology generations) left until we reach 11 ~ 5.5 nm technologies, at which we will reach down-scaling limit, in some year between 2020-30 (H. Iwai, IWJT2008).

-Even After reaching the down-scaling limit, we could still continue R & D, seeking sufficiently higher Id-sat under low Vdd.

-Two candidates have emerged for R & D

1. Nanowire/tube MOSFETs
2. Alternative channel MOSFETs (III-V, Ge)

- Other Beyond CMOS devices are still in the cloud.



ITRS figure edited by Iwai

Source: 2008 ITRS Summer Public Conf.

***5.5nm? was added by Iwai**

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Si nanowire FET with Semi-1D Ballistic Transport

Merit of Si-nanowire

Source: Y. Lee., T. Nagata., K. Kakushima., K. Shiraishi, and H. Iwai, IWDTF 2008, Tokyo, November, 2008

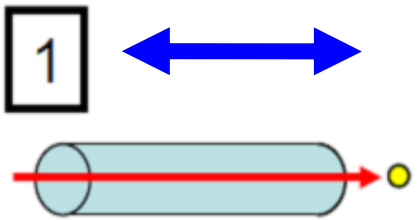
Trade off

Carrier scattering probability

Small **Large**

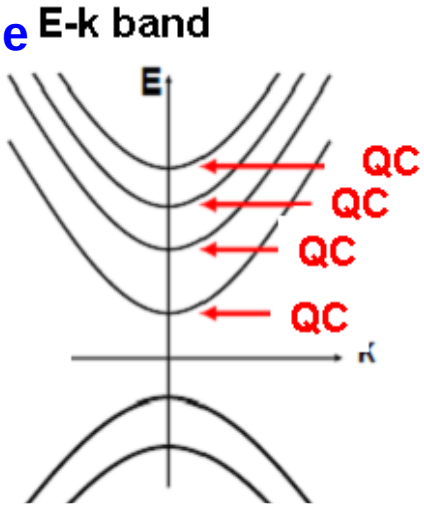
# of quantum channel

Small **Large**

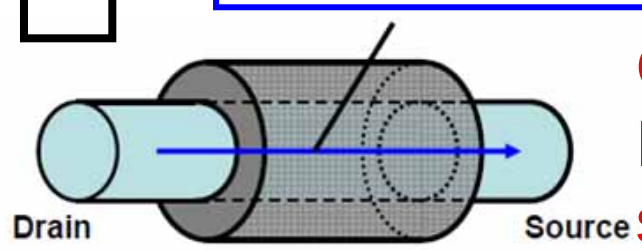


High Conduction (1D)

Go=77.8μS/wire



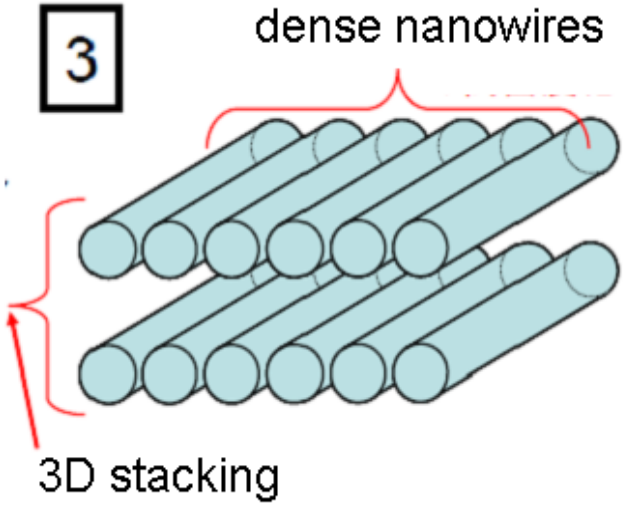
Multiple quantum channel (QC) used for conduction



Reduction in Ioff (Isd-leak)

Good control of Isd-leak by surrounding gate

Increase in Ion (Id-sat)



High-density lateral and vertical integration

Source: T. Ohno, K. Shiraishi, and T. Ogawa, Phys. Rev. Lett. ,1992

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1. Use 1D ballistic conduction

M2. Increase number of quantum channel

M3. Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.

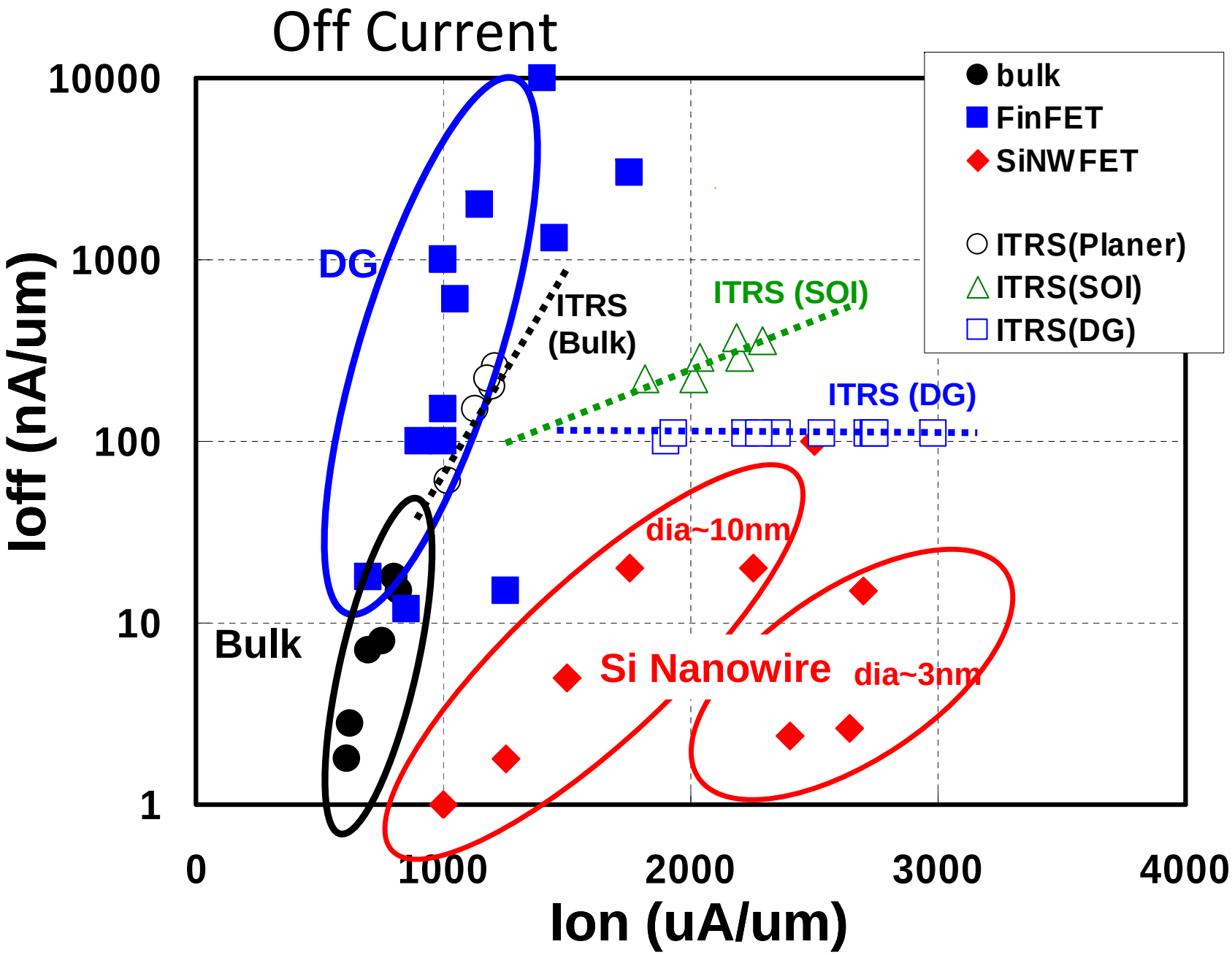
1D conduction per one quantum channel:

$G = 2e^2/h = 77.8\ \mu S$/wire or tube

regardless of gate length and channel material

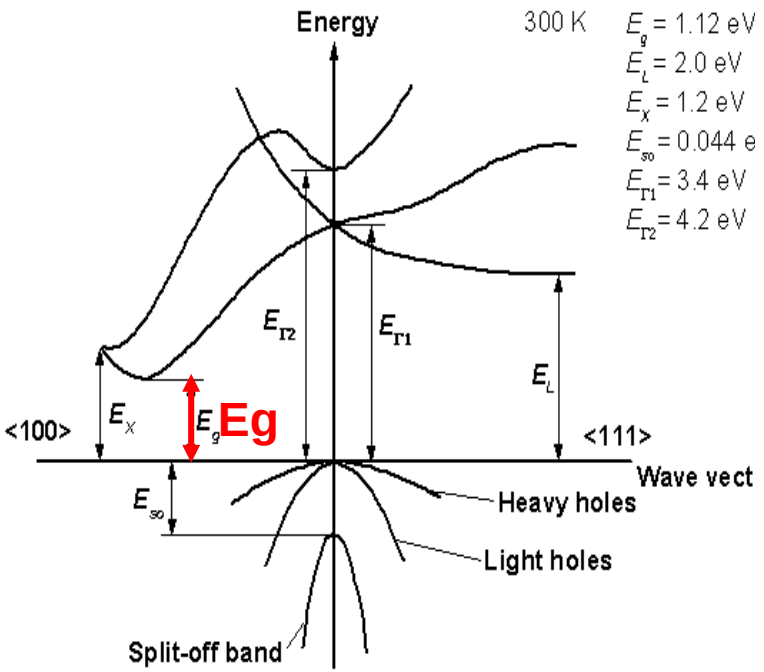
That is 77.8 μA/wire at 1V supply

This an extremely high value

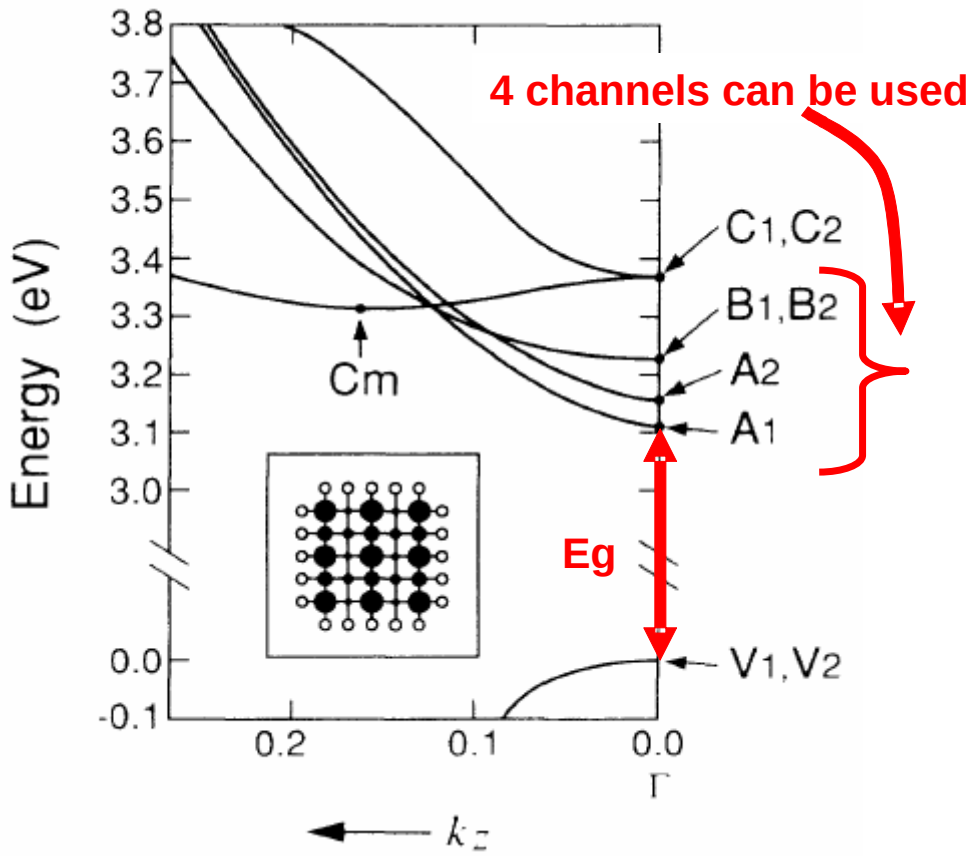

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



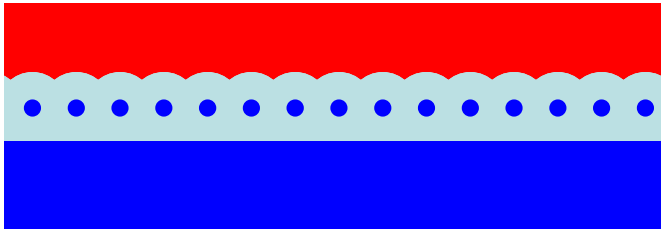
Energy band of Bulk Si



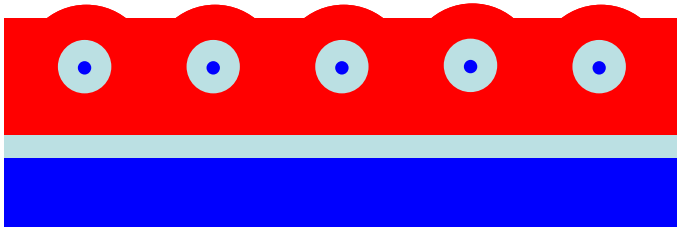
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

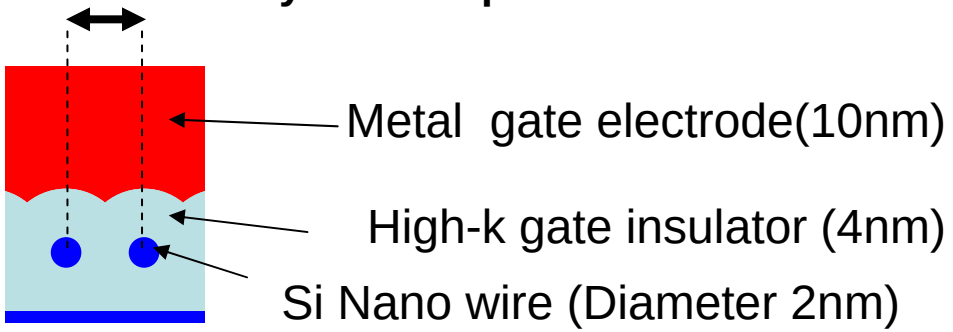
Front gate type MOS 165 wires /μm

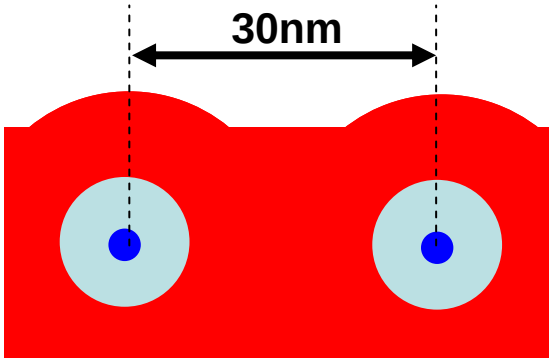


Surrounded gate type MOS 33 wires/μm

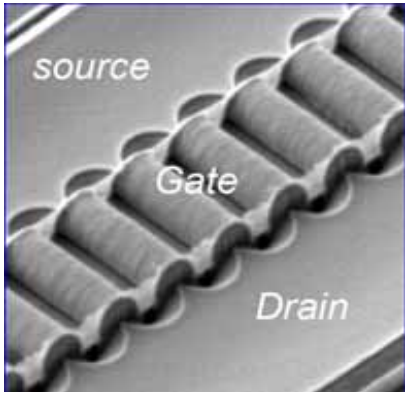


6nm pitch
By nano-imprint method



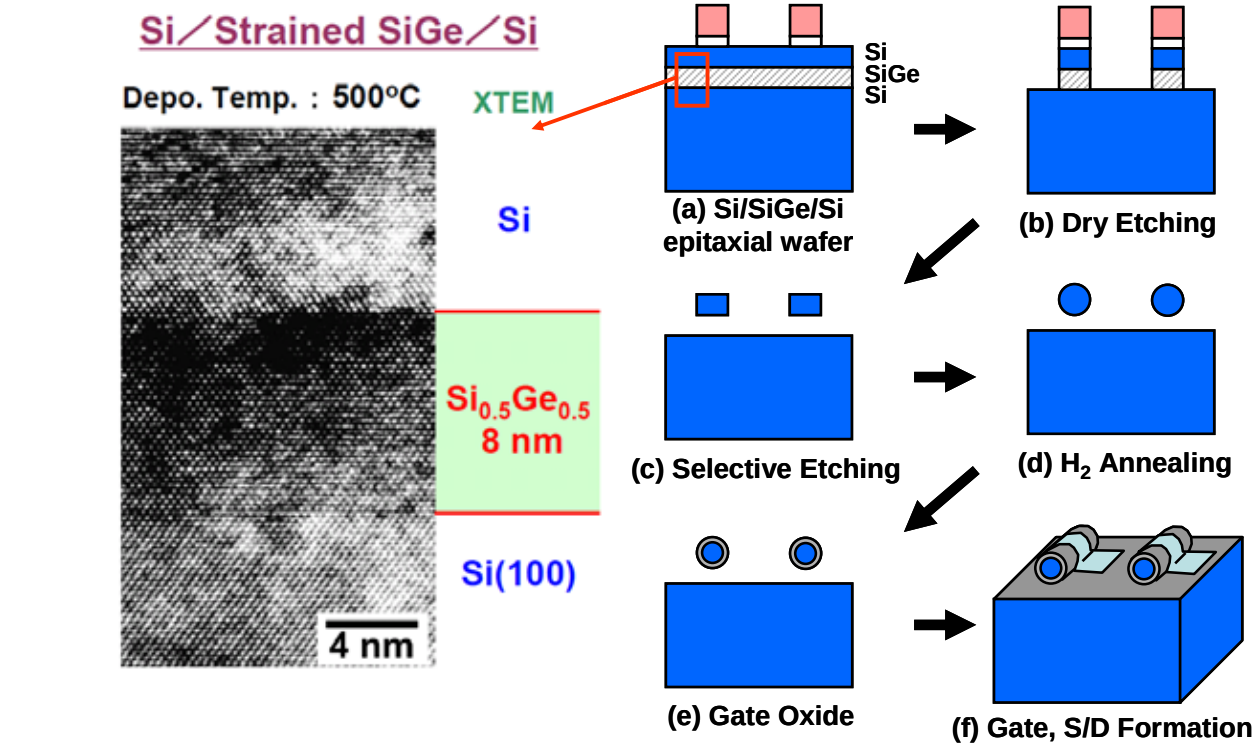


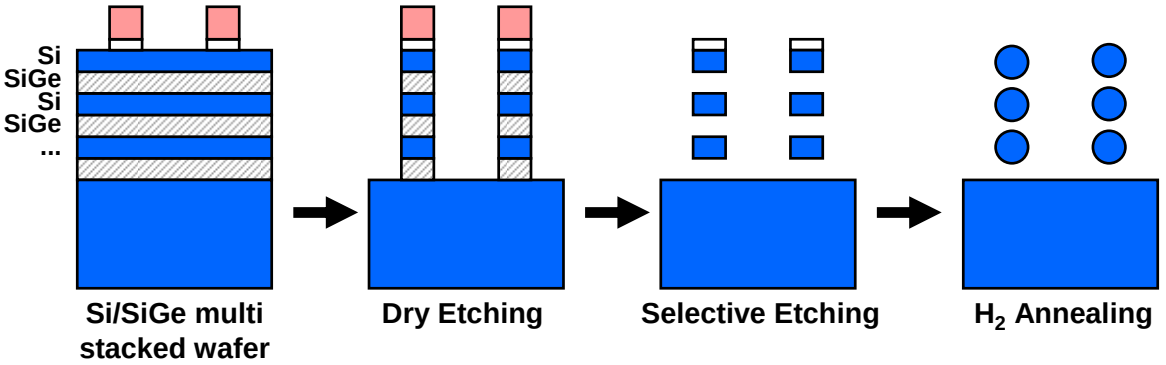
30nm pitch:
EUV lithograpy

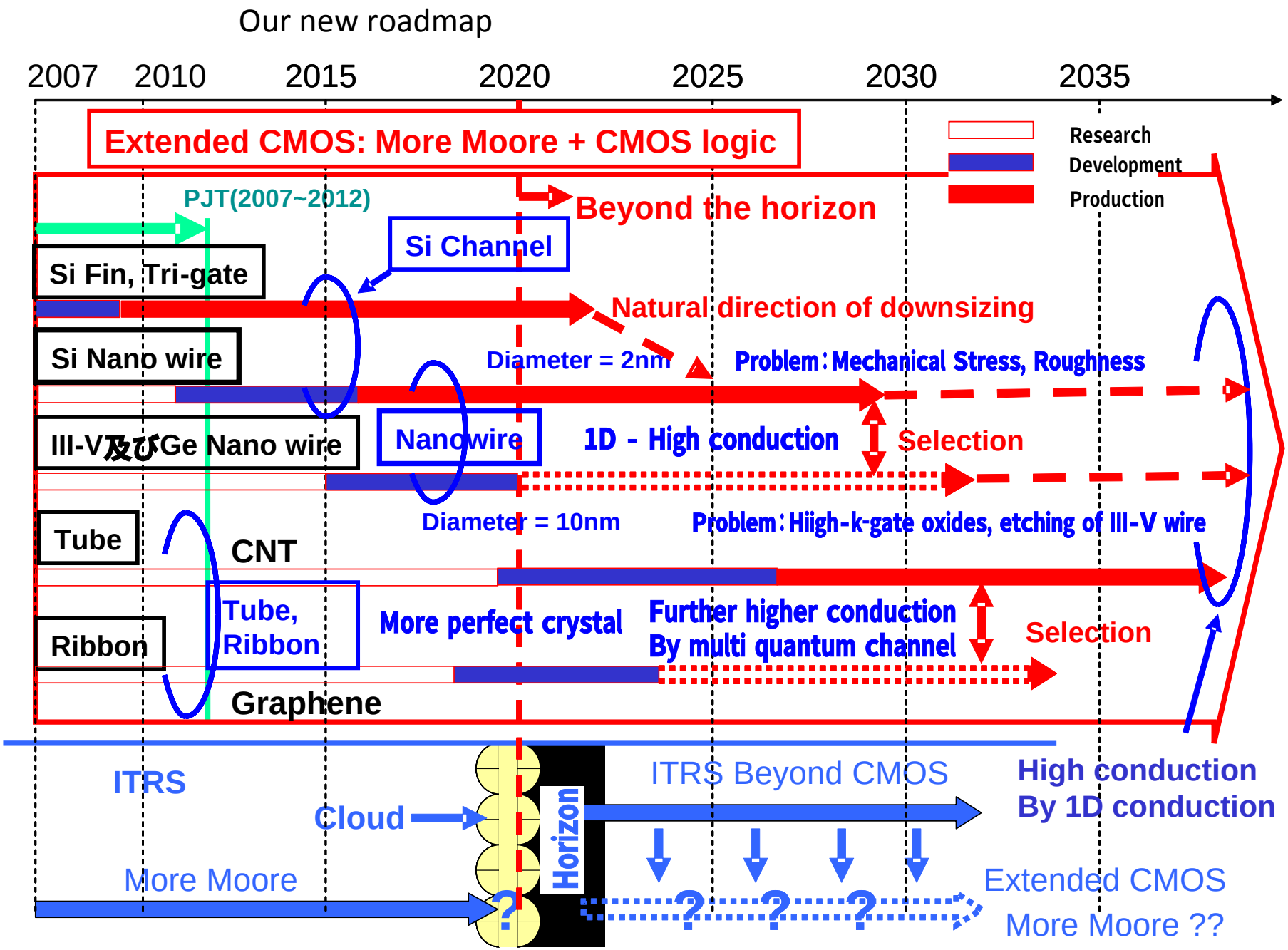


Surrounded gate MOS

Increase the number of wires towards vertical dimension

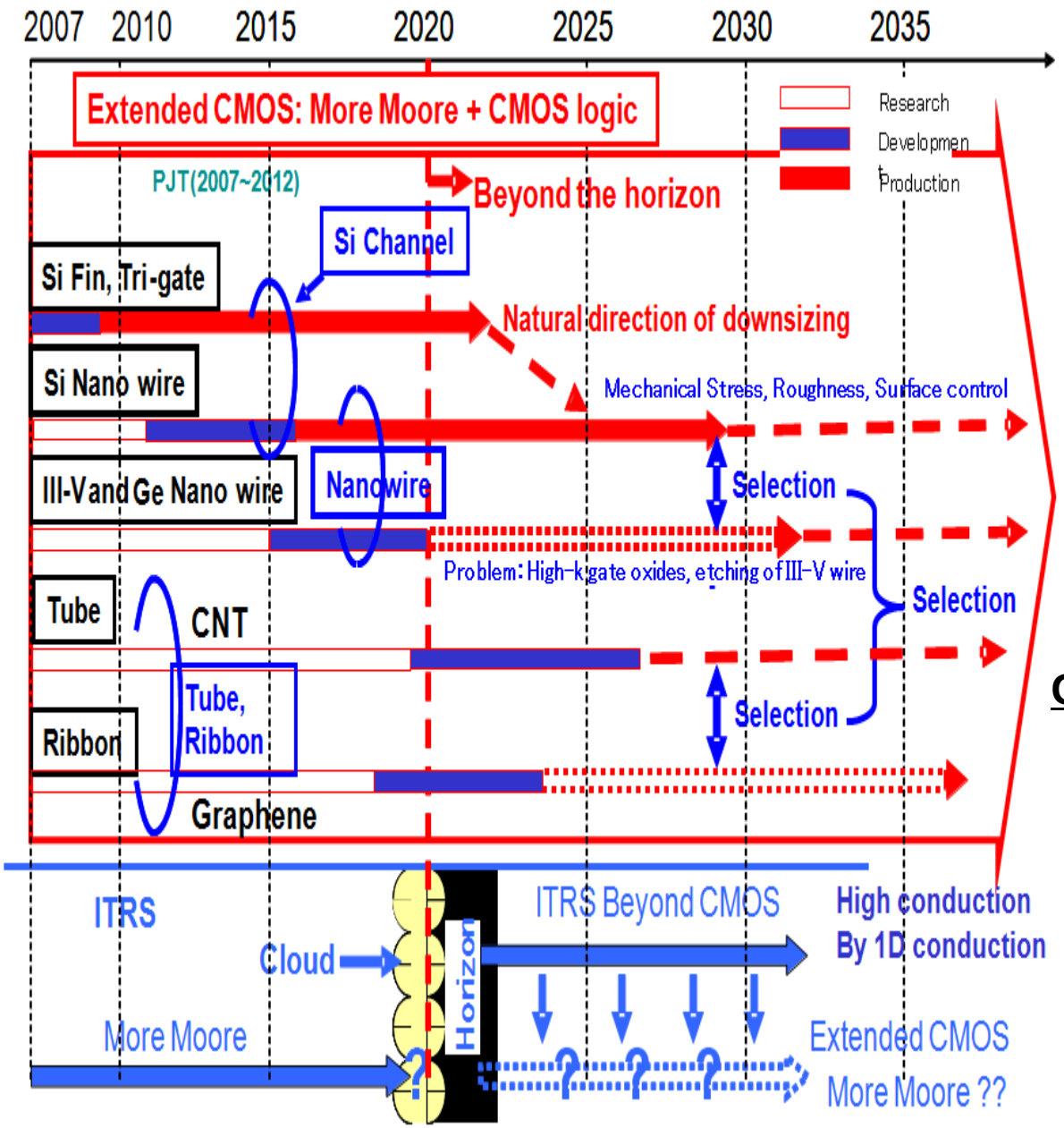





Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V及びGe Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Graphene
ITRS
Cloud
More Moore
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
Extended CMOS
More Moore ??

Our roadmap for R &D

Source: H. Iwai, IWJT 2008



Current Issues

Si Nanowire

Control of wire surface property

Source Drain contact

Optimization of wire diameter

Compact I-V model

III-V & Ge Nanowire

High-k gate insulator

Wire formation technique

CNT:

Growth and integration of CNT

Width and Chirality control

Chirality determines conduction types: metal or semiconductor

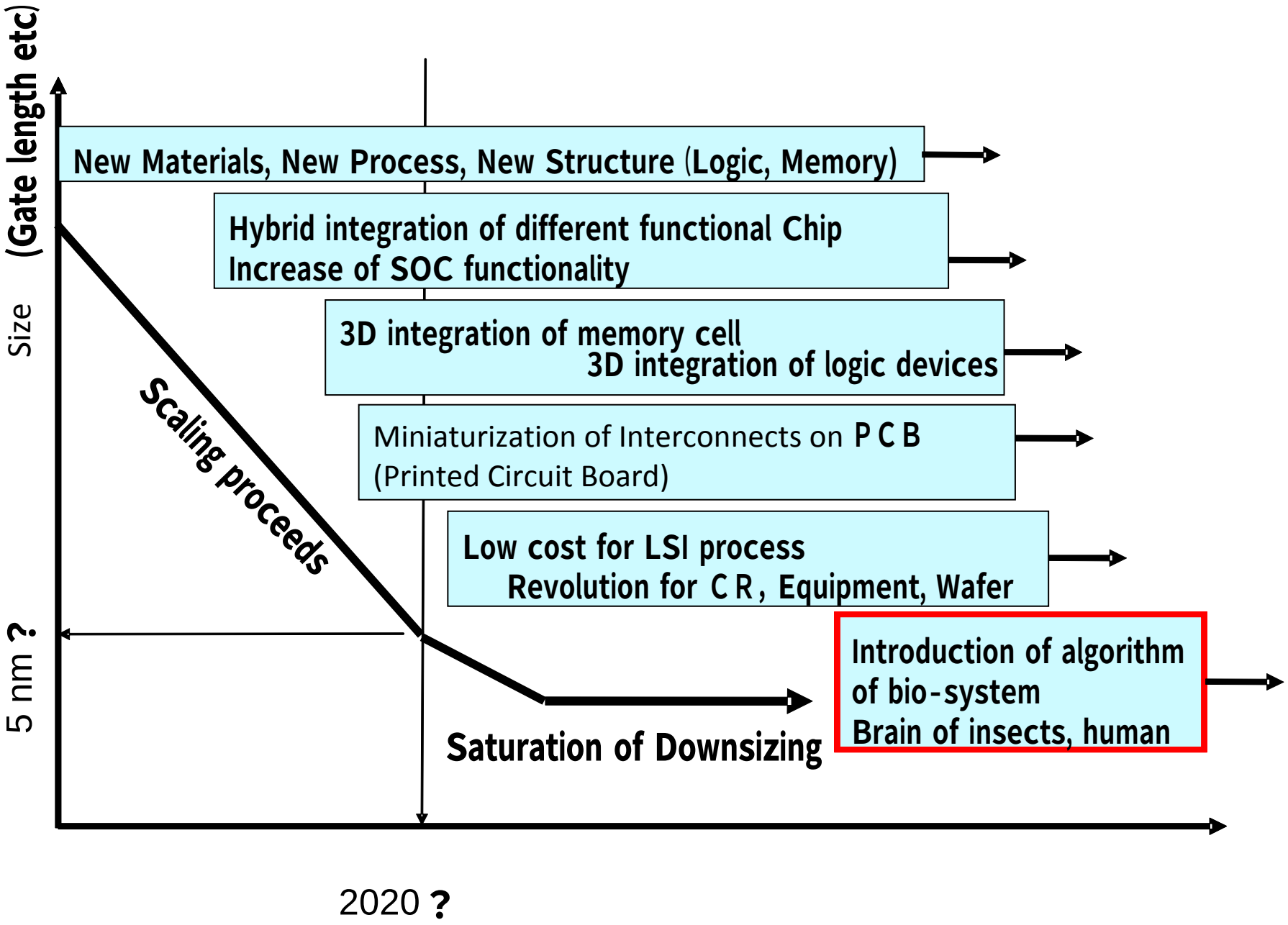
Graphene:

Graphene formation technique

Suppression of off-current

Very small bandgap or no bandgap (semi-metal)

Control of ribbon edge structure which affects bandgap


(Gate length etc)
Size
New Materials, New Process, New Structure (Logic, Memory)
Hybrid integration of different functional Chip
Increase of SOC functionality
3D integration of memory cell
3D integration of logic devices
Miniaturization of Interconnects on P C B
(Printed Circuit Board)
Low cost for LSI process
Revolution for C R, Equipment, Wafer
Introduction of algorithm
of bio-system
Brain of insects, human
Scaling proceeds
Saturation of Downsizing
5 nm ?
2020 ?

Brain

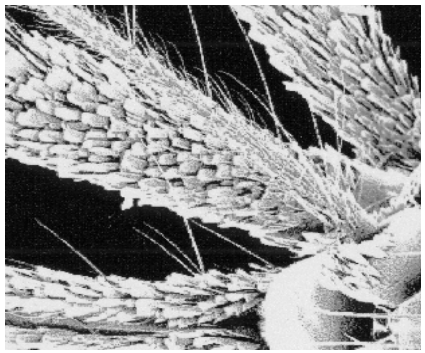
Ultra small volume
Small number of neuron cells
Extremely low power

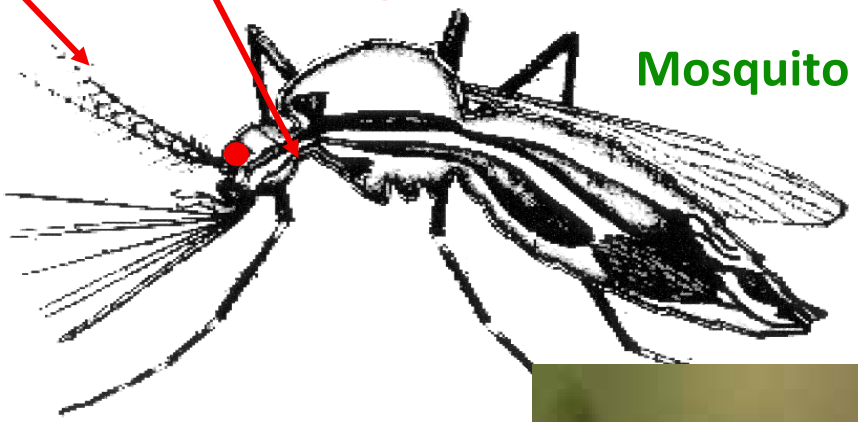
Sensor

Infrared
Humidity
CO_2

Real time image processing
(Artificial) Intelligence
3D flight control

Mosquito





System and Algorism becomes more important!

But do not know how?

Dragonfly is further high performance

Thank you
for your attention!