Past and future for micro- and nano-electronics, focusing on Si integrated circuits technology

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Toyo Institute of Technology
CMOS Technology: Indispensable for our human society

All the human activities are controlled by CMOS living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:
There is no computer in banks, and world economical activities immediately stop.

Cellarer phone dose not exists
CMOS experienced continuous progress for many years

<table>
<thead>
<tr>
<th>Name of Integrated Circuits</th>
<th>Number of Transistors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960s IC (Integrated Circuits)</td>
<td>~</td>
</tr>
<tr>
<td>1970s LSI (Large Scale Integrated Circuit)</td>
<td>~1,000</td>
</tr>
<tr>
<td>1980s VLSI (Very Large Scale IC)</td>
<td>~10,000</td>
</tr>
<tr>
<td>1990s ULSI (Ultra Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
<tr>
<td>2000s ?LSI (? Large Scale IC)</td>
<td>~1,000,000</td>
</tr>
</tbody>
</table>
Exponential Cost Reduction

Cost per Transistor

As the number of transistors goes UP
Cost per transistor goes DOWN

Source: WSJ/Silicon Valley

SPIE Microlithography 2006, San Jose, Ca USA
In 100 years, the size reduced by one million times. There have been many devices from stone age. We have never experienced such a tremendous reduction of devices in human history.
Downsizing

1. Reduce Capacitance
   - Reduce switching time of MOSFE
   - Reduce power consumption

2. Increase number of Transistors
   - Increase functionality
   - Parallel processing
   - Increase circuit operation speed

Thus, downsizing of Si devices is the most important and critical issue.
First Computer Eniac: made of huge number of vacuum tubes 1944. Big size, huge power, short life time filament.

Today's pocket PC has much higher performance with extremely low power consumption.
Many people wanted to say about the limit.
Past predictions were not correct!!

<table>
<thead>
<tr>
<th>Period</th>
<th>Expected limit(size)</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>Late 1970’s</td>
<td>1μm:</td>
<td>SCE</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.5μm:</td>
<td>S/D resistance</td>
</tr>
<tr>
<td>Early 1980’s</td>
<td>0.25μm:</td>
<td>Direct-tunneling of gate SiO</td>
</tr>
<tr>
<td>Late 1980’s</td>
<td>0.1μm:</td>
<td>‘0.1μm brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>50nm:</td>
<td>‘Red brick wall’ (various)</td>
</tr>
<tr>
<td>2000</td>
<td>10nm:</td>
<td>Fundamental?</td>
</tr>
</tbody>
</table>
Historically, many predictions of the limit of downsizing VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.
Direct-tunneling effect

Potential Barrier

Wave function
Direct tunneling leakage was found to be OK! In 1994 MOSFETs with 1.5 nm gate oxide. Direct tunneling leakage current starts to flow when the thickness is 3 nm.
Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!

Some one will think for you
Transistor Scaling Continues

- 90nm node: Lg=50nm
- 65nm node: Lg=35nm, Lg=25nm
- 45nm node: Strained Si FET
- 32nm node: Lg=15nm
- 22nm node: Lg=10nm

Graph: Lg (nm) vs. Year

- ITRS 2003 (HP): ~30% every two years

Qi Xinag, ECS 2004, AM
Downsizing limit?

Channel length?

Electron wave length

10 nm

Gate Oxid

Channel
5 nm gate length CMOS
Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC
IEDM, 2003
Electron wave length
10 nm

Tunneling distance
3 nm

Atom distance
0.3 nm

Downsizing limit!
Channel length
Gate oxide thickness
Prediction now!

- **Electron wave length**: 10 nm
- **Tunneling distance**: 3 nm
- **Atom distance**: 0.3 nm

**MOSFET operation**

- **Lg = 2 ~ 1.5 nm?**
- **Below this, no one knows future!**
History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking

\[ C, V \propto \frac{C}{L} \]

\[ \text{Switching speed} \quad CV/I \quad \rightarrow \quad \text{Decrease} \]

\[ \text{Power consumption} \quad CV^2/2 \quad \rightarrow \quad \text{Decrease} \]

\[ \text{Integration density:} \quad 1/L^2 \quad \rightarrow \quad \text{Increase} \]

1970 \hspace{2cm} 2007

Gate length \hspace{2cm} 10,000 nm \hspace{2cm} 25 nm

Gate Oxd Thickness \hspace{2cm} 100 nm \hspace{2cm} 1 nm
For the past 45 years, SiO2 and SiON have been used for gate insulator materials. Today, EOT=1.0nm. EOT Limit is 0.7~0.8 nm. One order of magnitude improvement is achieved.

45nm node, Lg=22nm, HfO2 direct contact of high-k and Si. Still SiO2 or SiON is used at Si interface.

Now, EOT=0.5nm. 22nm node, Lg=11nm. Direct contact of high-k and Si. Metal layer is introduced.
Choice of High-k elements for oxide

Candidates

- Gas or liquid at 1000 K
- Radio active

- H
- He
- Ne
- Li
- Be
- Mg
- Na
- K
- Ca
- Sc
- Ti
- V
- Cr
- Mn
- Fe
- Co
- Ni
- Cu
- Zn
- Ga
- Ge
- As
- Se
- Br
- Kr
- Rb
- Sr
- Y
- Zr
- Nb
- Mo
- Tc
- Ru
- Rh
- Pd
- Ag
- Cd
- In
- Sn
- Sb
- Te
- I
- Xe
- Cs
- Ba
- Fr
- Ra
- Rf
- Ha
- Sg
- Ns
- Hs
- Mt

Unstable at Si interface
- Si + MOₓ M + SiO₂
- Si + MOₓ MSiₓ + SiO₂
- Si + MOₓ M + MSiₓOᵧ

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant
3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

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R. Hauser, IEDM Short Course, 1999
EOT = 0.48 nm   Our results

Transistor with La2O3 gate insulator
CMOS downsizing is critically important

However now, many people expect that we will reach limit in 2020.

Totally, new paradigm after reaching the downsizing limit.

What will be?
After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.
After 2020

4 reasons for no downsizing anymore or No decrease in gate length

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.
   Ballistic ← No scattering of carriers in channel
   Thus, all the carrier from the source reach drain

2. Increase of Off-current (Subthreshold current)

3. No decrease of Gate capacitance by parasitic components

4. Increase in production cost.
After 2020

What will be the world with no gate length reduction?
More Moore and More than Moore

Moore’s Law & More

More than Moore: Diversification
- Analog/RF
- Passives
- HV Power
- Sensors
- Actuators
- Biochips

More Moore: Miniaturization
- 130nm
- 90nm
- 65nm
- 45nm
- 32nm
- 22nm
- ... V

Beyond CMOS

Combining SoC and SiP: Higher Value Systems

Non-digital content System-in-package (SiP)

Interacting with people and environment

Information Processing

Question what is the other side of the cloud?

ITRS 2005 Edition

<table>
<thead>
<tr>
<th>Device</th>
<th>FET</th>
<th>RSFQ</th>
<th>1D structures</th>
<th>Resonant Tunneling Devices</th>
<th>SET</th>
<th>Molecular</th>
<th>QCA</th>
<th>Spin transistor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell Size</strong></td>
<td>100 nm</td>
<td>0.3 µm</td>
<td>100 nm</td>
<td>100 nm</td>
<td>40 nm</td>
<td>Not known</td>
<td>60 nm</td>
<td>100 nm</td>
</tr>
<tr>
<td><strong>Density (cm⁻²)</strong></td>
<td>3E9</td>
<td>1E6</td>
<td>3E9</td>
<td>3E9</td>
<td>6E10</td>
<td>1E12</td>
<td>3E10</td>
<td>3E9</td>
</tr>
<tr>
<td><strong>Switch Speed</strong></td>
<td>700 GHz</td>
<td>1.2 THz</td>
<td>Not known</td>
<td>1 THz</td>
<td>1 GHz</td>
<td>Not known</td>
<td>30 MHz</td>
<td>700 GHz</td>
</tr>
<tr>
<td><strong>Circuit Speed</strong></td>
<td>30 GHz</td>
<td>250–800 GHz</td>
<td>30 GHz</td>
<td>30 GHz</td>
<td>1 GHz</td>
<td>&lt;1 MHz</td>
<td>1 MHz</td>
<td>30 GHz</td>
</tr>
<tr>
<td><strong>Switching Energy, J</strong></td>
<td>2×10⁻¹⁸</td>
<td>&gt;1.4×10⁻¹⁷</td>
<td>2×10⁻¹⁸</td>
<td>&gt;2×10⁻¹⁸</td>
<td>&gt;1.5×10⁻¹⁷</td>
<td>1.3×10⁻¹⁶</td>
<td>&gt;1×10⁻¹⁸</td>
<td>2×10⁻¹⁸</td>
</tr>
<tr>
<td><strong>Binary Throughput, GBit/ns/cm²</strong></td>
<td>86</td>
<td>0.4</td>
<td>86</td>
<td>86</td>
<td>10</td>
<td>N/A</td>
<td>0.06</td>
<td>86</td>
</tr>
</tbody>
</table>

We HAVE IDENTIFIED NO VIABLE EMERGING LOGIC TECHNOLOGIES for Information Processing beyond CMOS
We could keep the Moore’s law after 2020
Without downswing the gate length

What is Moore’s law.
Keep increase of the number of components. Cost per components decreases!

Gordon Moore
We could keep the Moore’s law after 2020
Without downswing the gate length

What is Moore’s law.
  → to increase the number (#) of Tr. In a chip

Now, # of Tr. in a chip is limited by power.
  → key issue is to reduce the power.
  → to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.
Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004
Selection of MOSFET structure for high conduction: Nano-wire or Nano-tube FETs is promising.

3 methods to realize High-conduction at Low voltage:
M1. Use 1D ballistic conduction
M2. Increase number of quantum channel
M3. Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.
1D conduction per one quantum channel:

\[ G = \frac{2e^2}{h} = 77.8 \, \mu\text{S/wire or tube} \]

regardless of gate length and channel material

That is 77.8 \( \mu \text{A/wire} \) at 1V supply

This an extremely high value

However, already 20mA/wire was obtained experimentally by Samsung
The graph shows the off current (Ioff) in nanamperes per micrometer (nA/um) plotted against the on current (Ion) in microamperes per micrometer (uA/um) for different types of transistors. The categories include bulk, FinFET, SiNWFET, and GeNWFET. The ITRS standards for planar, SOI, and double-gate (DG) architectures are also indicated. The graph highlights the performance comparisons with diameters of approximately 3nm and 10nm, emphasizing the differences in current capabilities between bulk and Si nanowire transistors.
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

300 K
$E_g = 1.12 \text{ eV}$
$E_L = 2.0 \text{ eV}$
$E_x = 1.2 \text{ eV}$
$E_v = 0.044 \epsilon$
$E_{T1} = 3.4 \text{ eV}$
$E_{T2} = 4.2 \text{ eV}$

4 channels can be used

Energy band of 3 x 3 Si wire
Maximum number of wires per 1 µm

Front gate type MOS
- 165 wires /µm

Surrounded gate type MOS
- 33 wires/µm

6nm pitch
- By nano-imprint method

30nm pitch:
- EUV lithography

- Metal gate electrode (10nm)
- High-k gate insulator (4nm)
- Si Nano wire (Diameter 2nm)
Increase the number of wires towards vertical dimension

Si/Strained SiGe/Si
Depo. Temp. : 500°C

(a) Si/SiGe/Si epitaxial wafer
(b) Dry Etching
(c) Selective Etching
(d) H₂ Annealing
(e) Gate Oxide
(f) Gate, S/D Formation

Si/SiGe multi stacked wafer
Dry Etching
Selective Etching
H₂ Annealing
Our new roadmap

- **Extended CMOS: More Moore + CMOS logic**
  - Si Fin, Tri-gate
  - Si Nano wire
  - III-V & Ge Nano wire
  - Tube
  - Ribbon
  - CNT
  - Tube, Ribbon
  - Graphene

- PJT (2007~2012)

- Beyond the horizon
- Natural direction of downsizing
- Diameter = 2nm
- Selection
- Diameter = 10nm

- High conduction
- By 1D conduction

- ITRS
- More Moore

- ITRS Beyond CMOS
- Extended CMOS
- More Moore ??
Miniaturization of Interconnects on PCB (Printed Circuit Board)
Dragonfly is further high performance

**Brain**
- Ultra small volume
- Small number of neuron cells
- Extremely low power
- Real time image processing
- (Artificial) Intelligence
- 3D flight control

**Sensor**
- Infrared
- Humidity
- CO₂

**System and Algorism becomes more important!**

But do not know how?
Thank you for your attention!