Future of NanoCMOS after Scaling Limit

September 8, 2008

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Bogota, Columbia

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Tokyo Institute of Technology

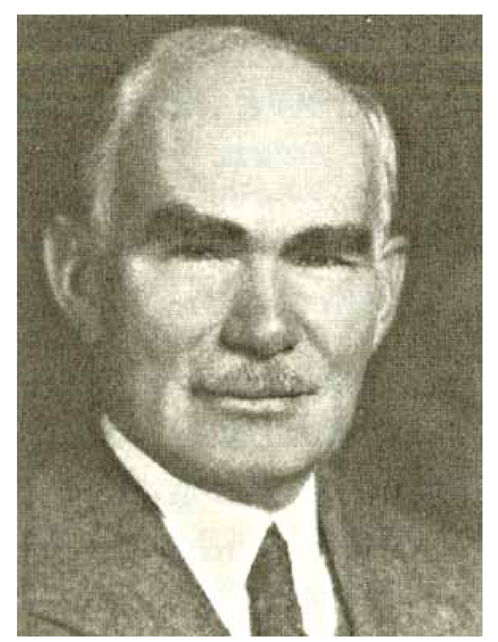
- There were many inventions in the 20th century:

  Airplane, Nuclear Power generation, Computer,

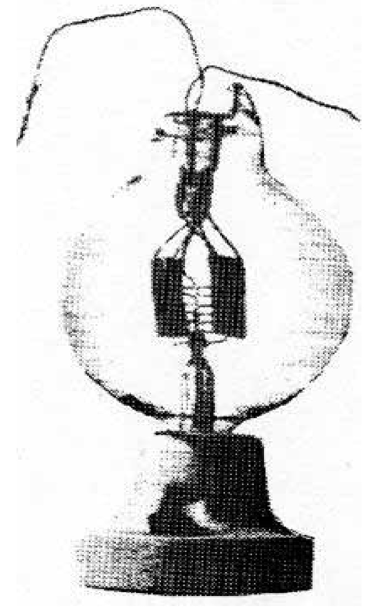
  Space aircraft, etc
- However, everything has to be controlled by electronics
- Electronics

  Most important invention in the 20th century
- What is Electronics: To use electrons,

  Electronic Circuits

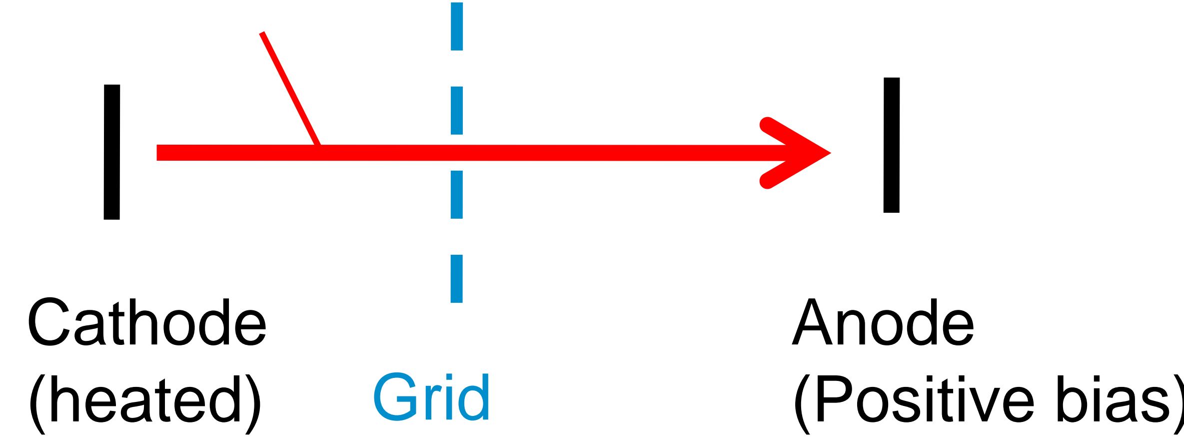


Lee De Forest



Electronic Circuits started by the invention of vacuum tube (Triode) in 1906

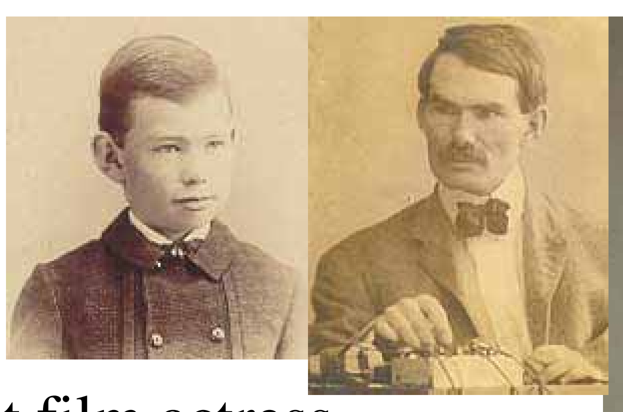
Thermal electrons from cathode controlled by grid bias



Same mechanism as that of transistor

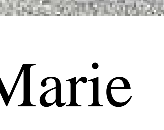
4 wives of Lee De Forest

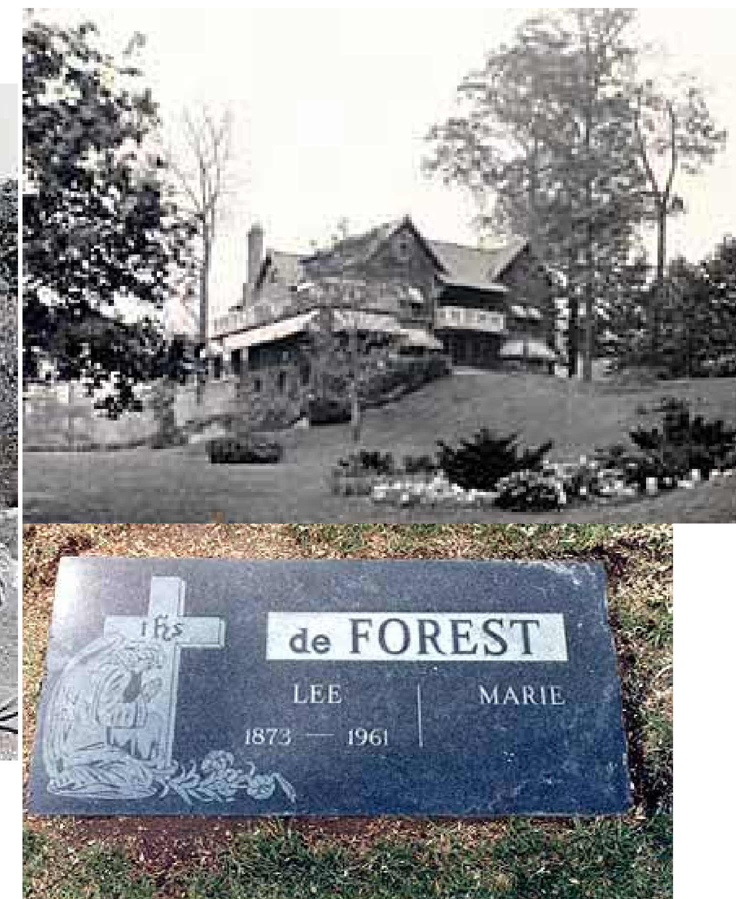
1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress



Mary

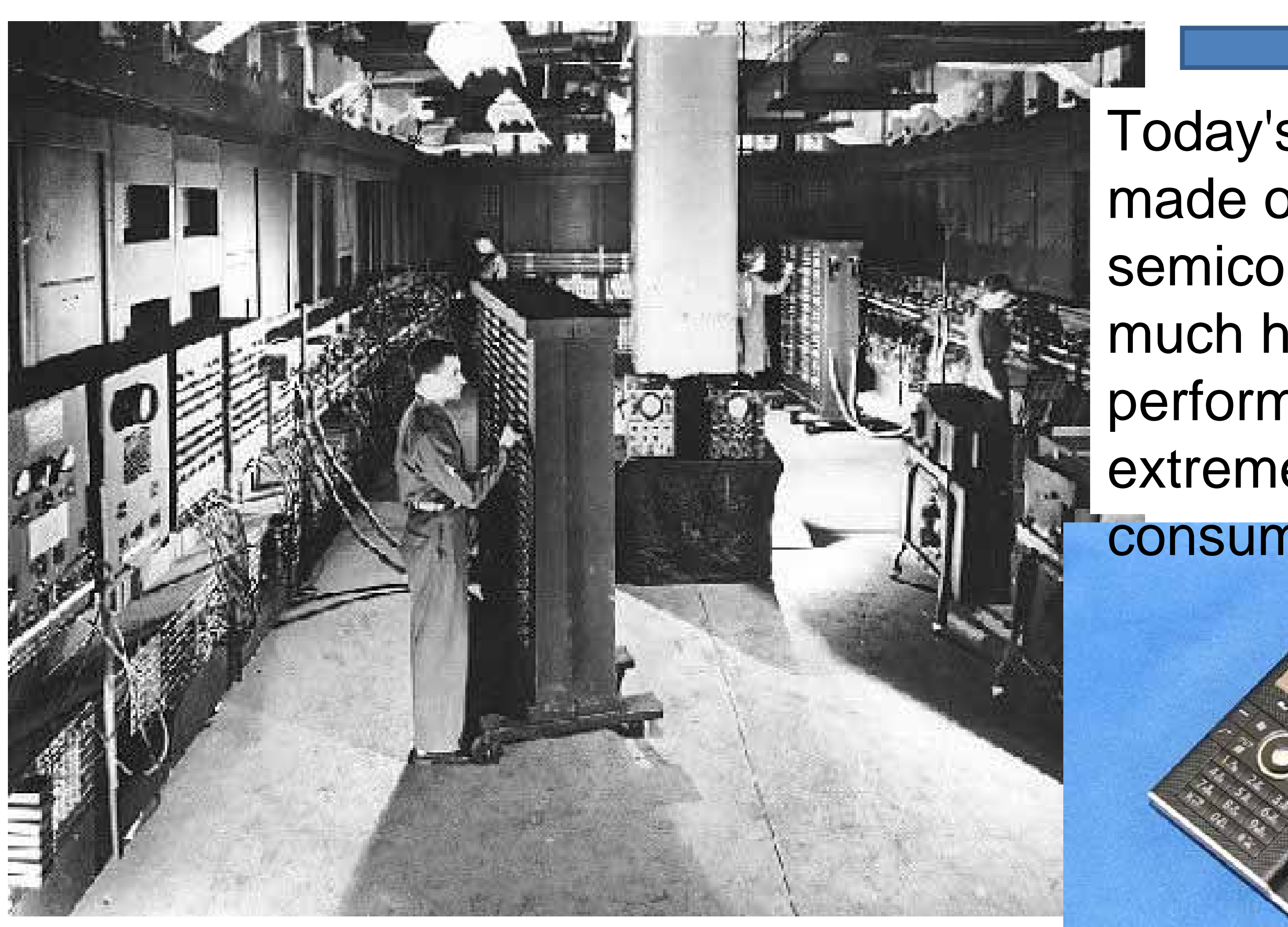
Marie





First Computer Eniac: made of huge number of vacuum tubes 19
Big size, huge power, short life time filament

→ dreamed of replacing vacuum tube with solid-state device



Today's pocket PC made of semiconductor has much higher performance with extremely low power consumption

History of Semiconductor devices

1947, 1st Point Contact Bipolar Transistor:
Ge Semiconductor, Bardeen, Brattin
→ Nobel Prize

1948, 1st Junction Bipolar Transistor,
Ge Semiconductor, Schokley
→ Nobel Prize

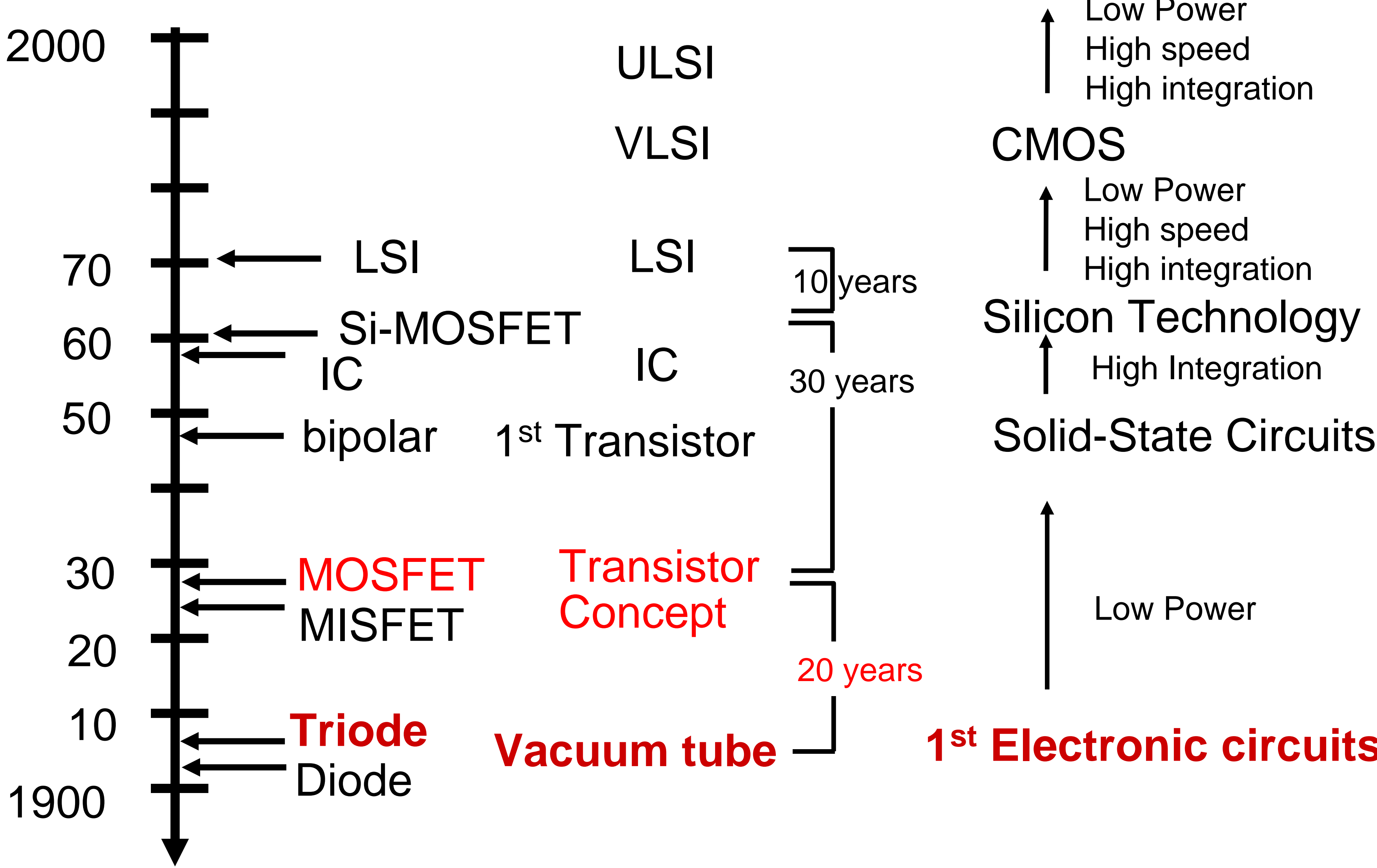
1958, 1st Integrated Circuits,
Ge Semiconductor, J.Kilby → Nobel Prize

1959, 1st Planar Integrated Circuits,
Noice

1960, 1st MOS Transistor, Kahng,
Si Semiconductor

1963, 1st CMOS Circuits, C.T. Sah and F. Wanlass

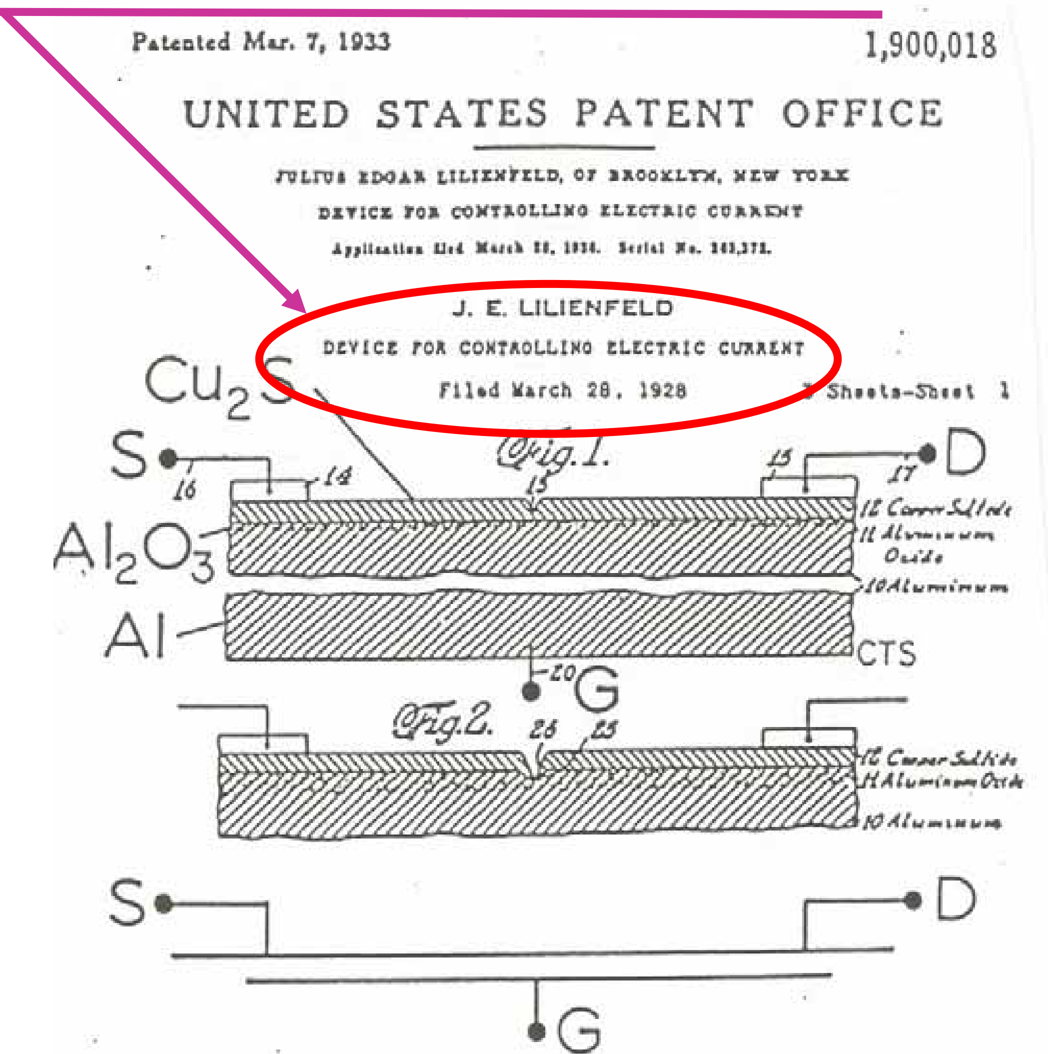
History of Electronic Devices



J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



J.E.LILIENFELD

Capacitor structure with notch

Negative bias

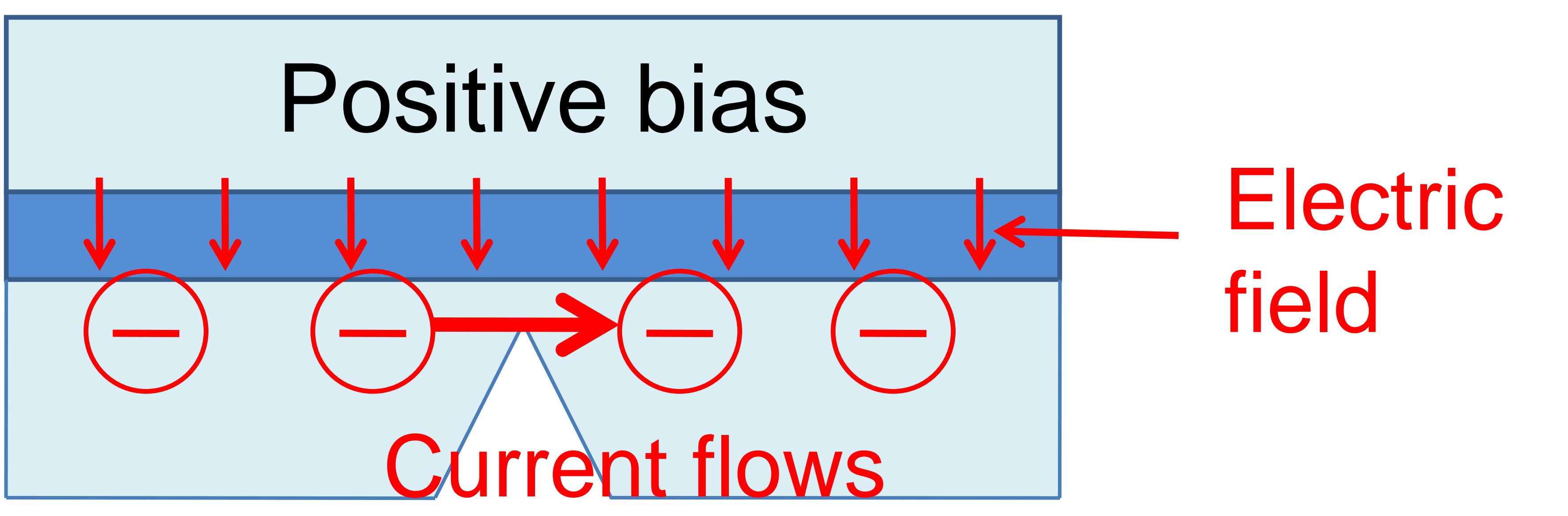
Gate Electrode

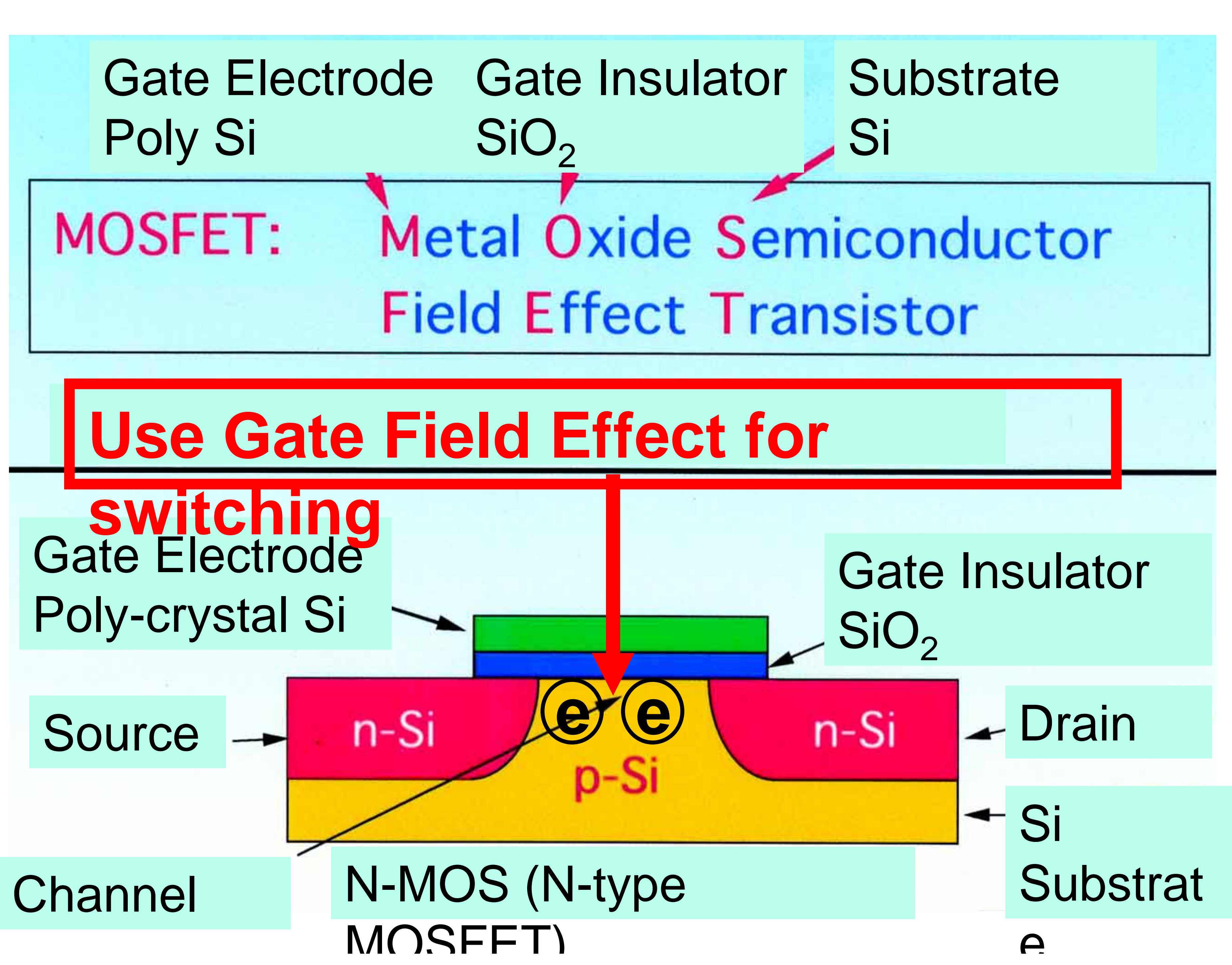
Gate Insulator

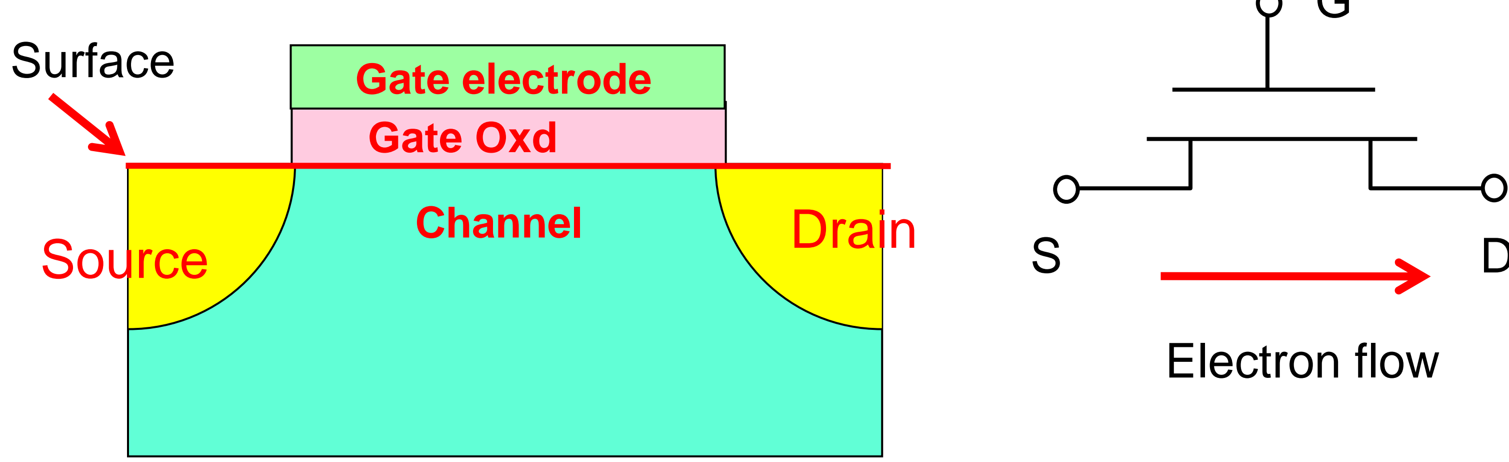
Semiconductor

Electron

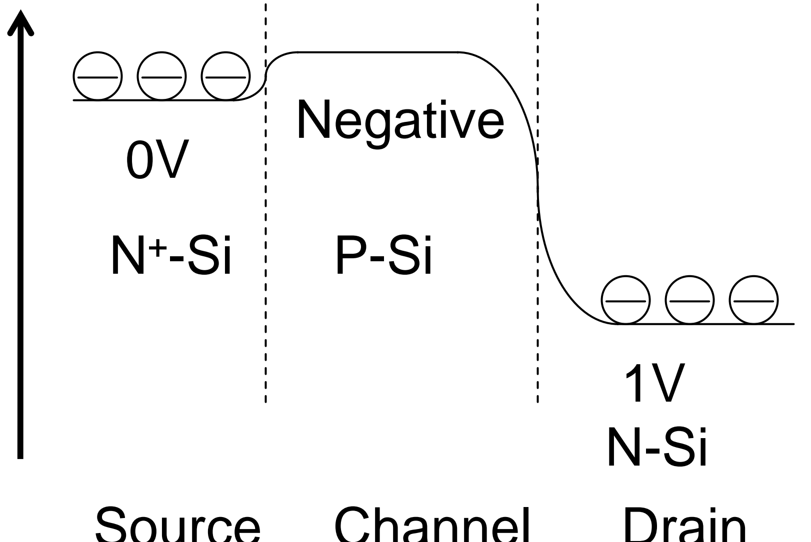
No current



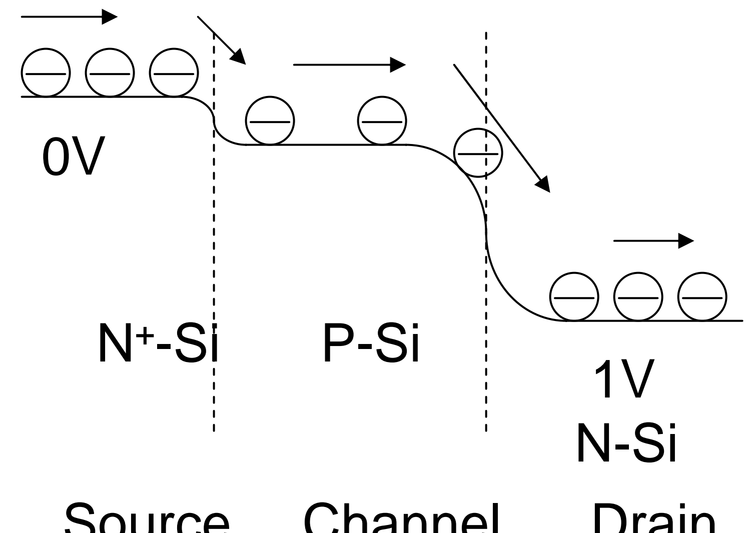

Gate Electrode
Poly Si
Gate Insulator
SiO_2
Substrate
Si
MOSFET: Metal Oxide Semiconductor
Field Effect Transistor
Use Gate Field Effect for switching
Gate Electrode
Poly-crystal Si
Gate Insulator
SiO_2
Source
n-Si
e
e
n-Si
Drain
p-Si
Si
Substrate
Channel
N-MOS (N-type MOSFET)

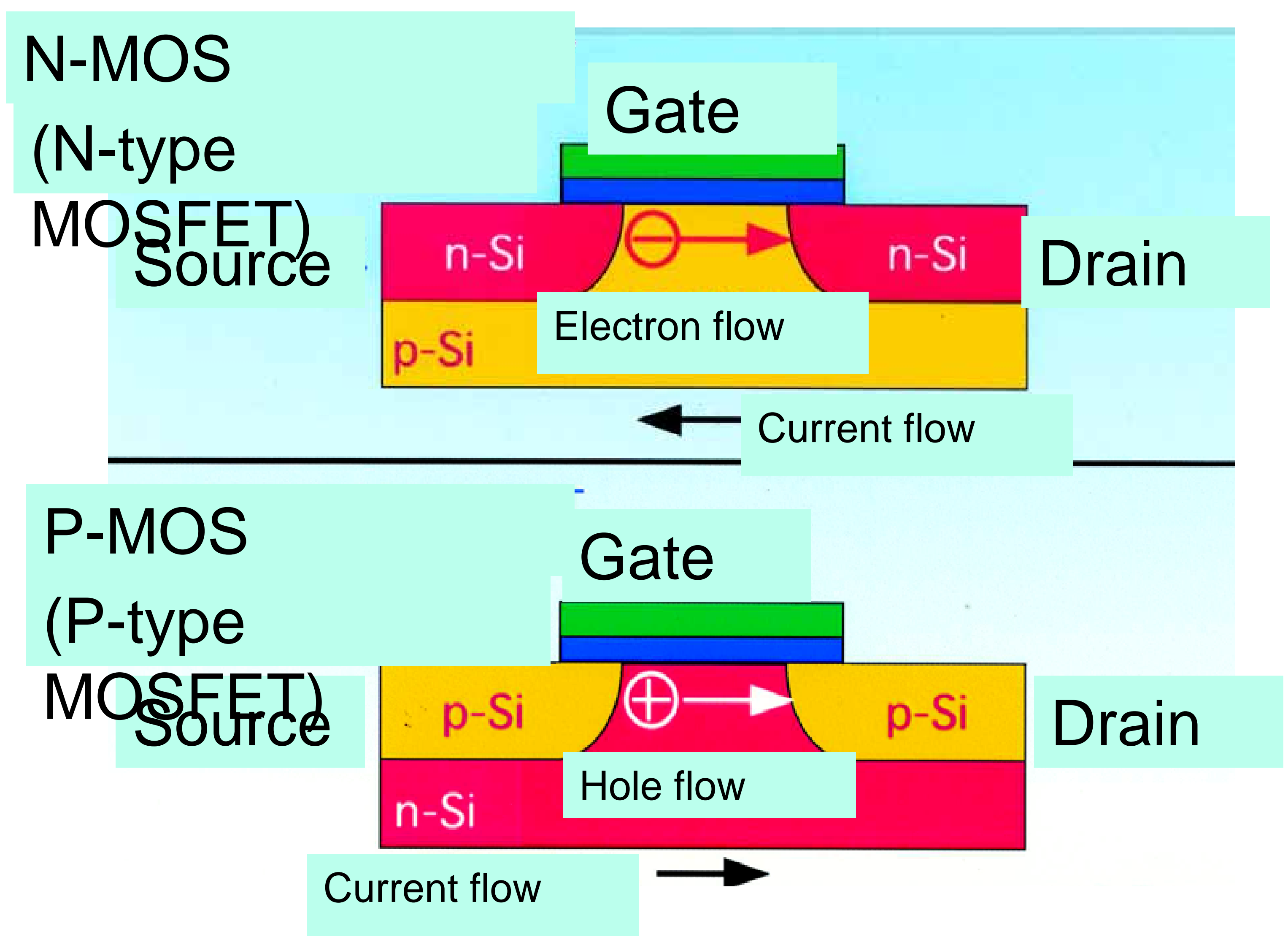


0 bias for gate



Positive bias for gate



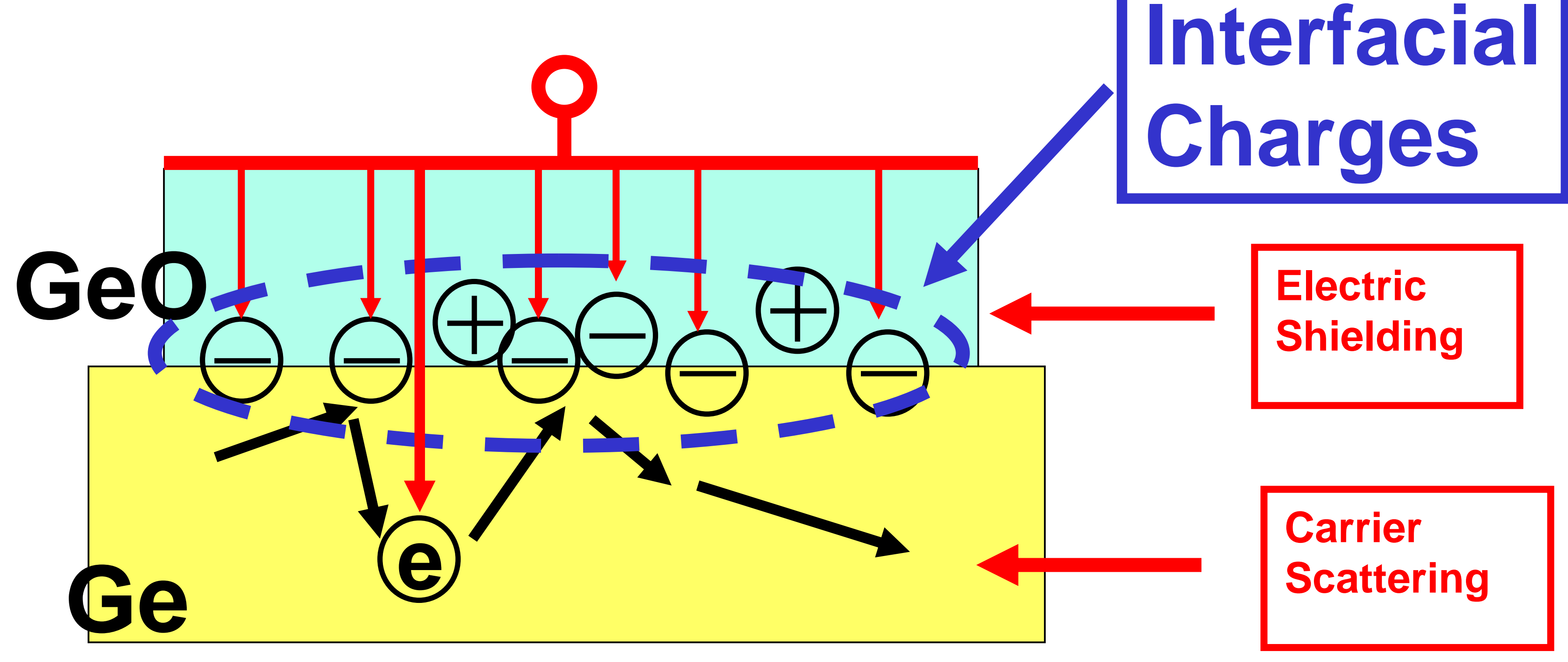

N-MOS
(N-type
MOSFET)
Gate
Source
n-Si
n-Si
Drain
p-Si
Electron flow
Current flow
P-MOS
(P-type
MOSFET)
Gate
Source
p-Si
p-Si
Drain
n-Si
Hole flow
Current flow

However, no one could realize MOSFET operation for more than 30 years.

Because of very bad interface property between the semiconductor and gate insulator

Even Shockley!

Very bad interface property between the semiconductor and gate insulator

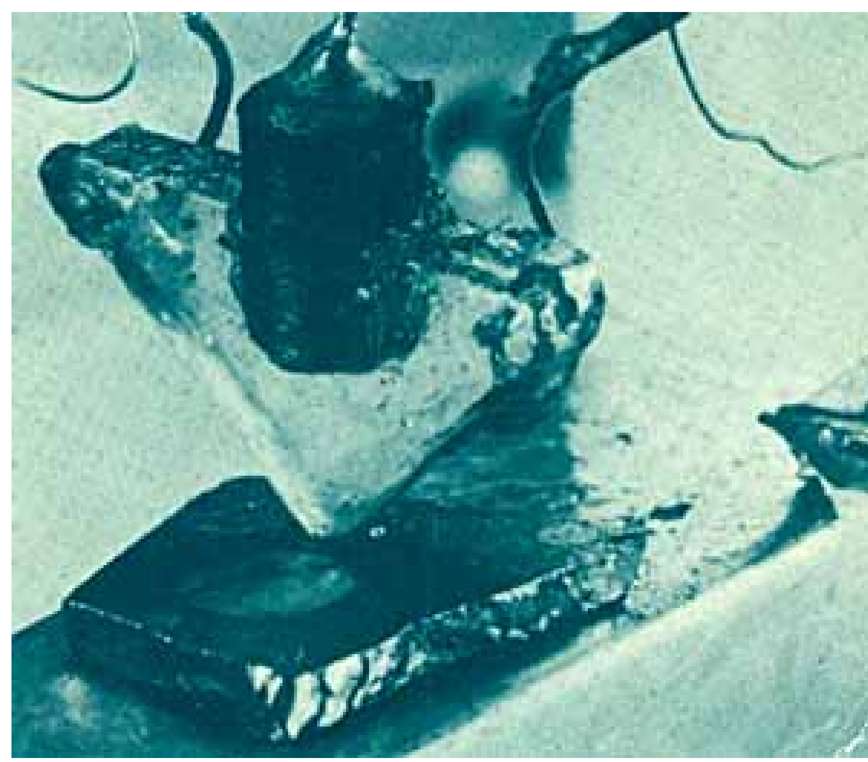


Drain Current was several orders of magnitude sm than expected

Even Shockley!

However, they found amplification phenomenon when investigating Ge surface when putting needles.
This is the 1st Transistor:
Not Field Effect Transistor,
But Bipolar Transistor (another mechanism)

1947: 1st transistor



Bipolar using Ge

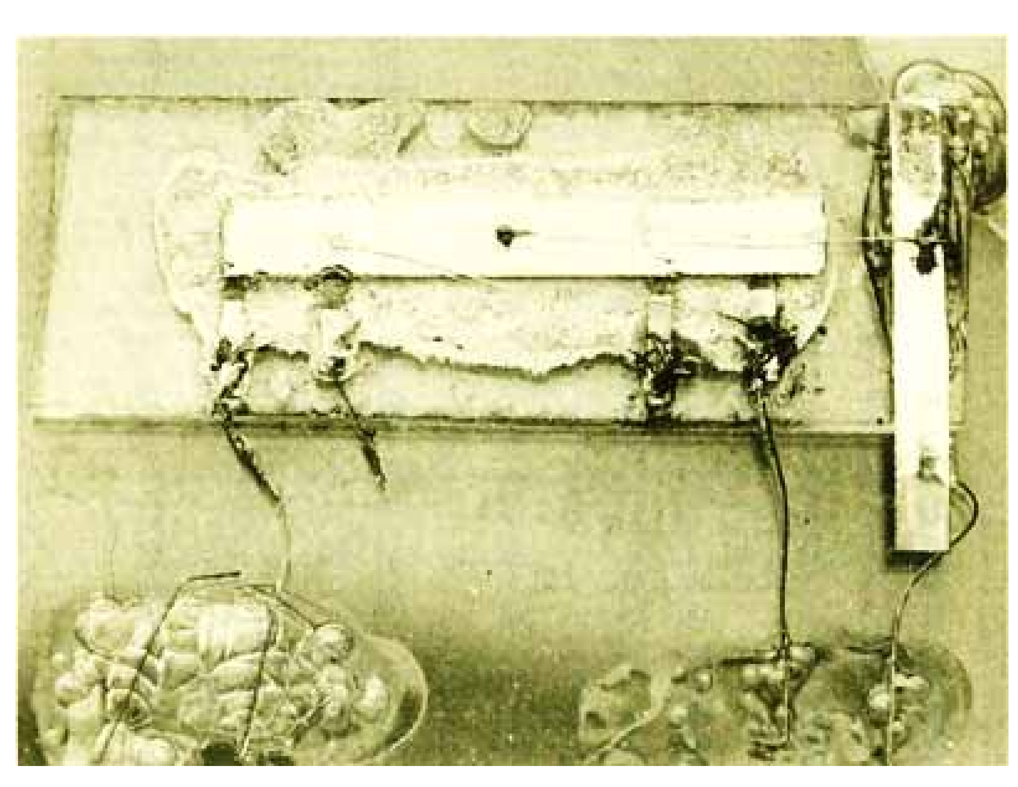
J. Bardeen W. Bratten,

W. Shockley

1958: 1st Integrated Circuit

Jack S. Kilby

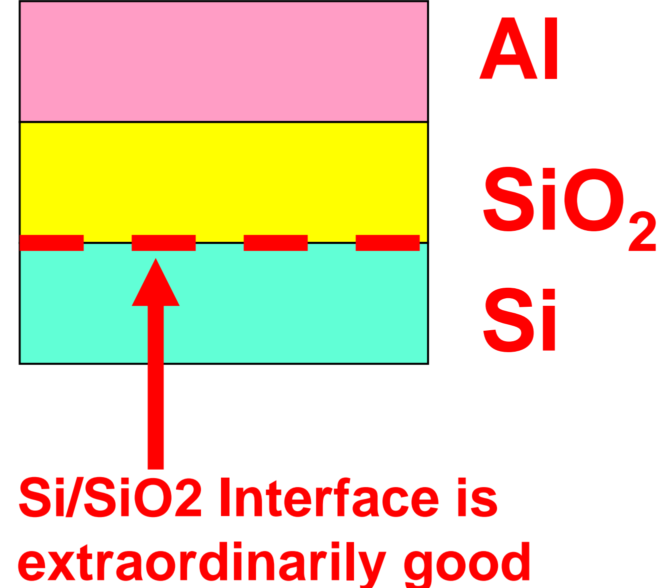
Connect 2 bipolar transistors in the Same substrate by bonding wire.



1960: First MOSFET
by D. Kahng and M. Atalla

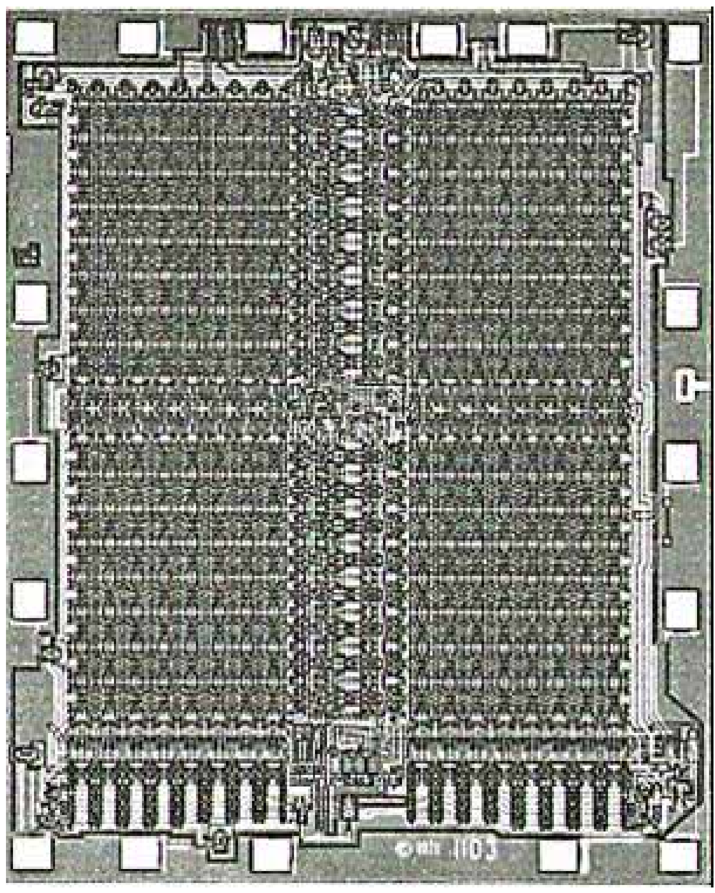
Top View

Si
Source
Al Gate
Drain
Si

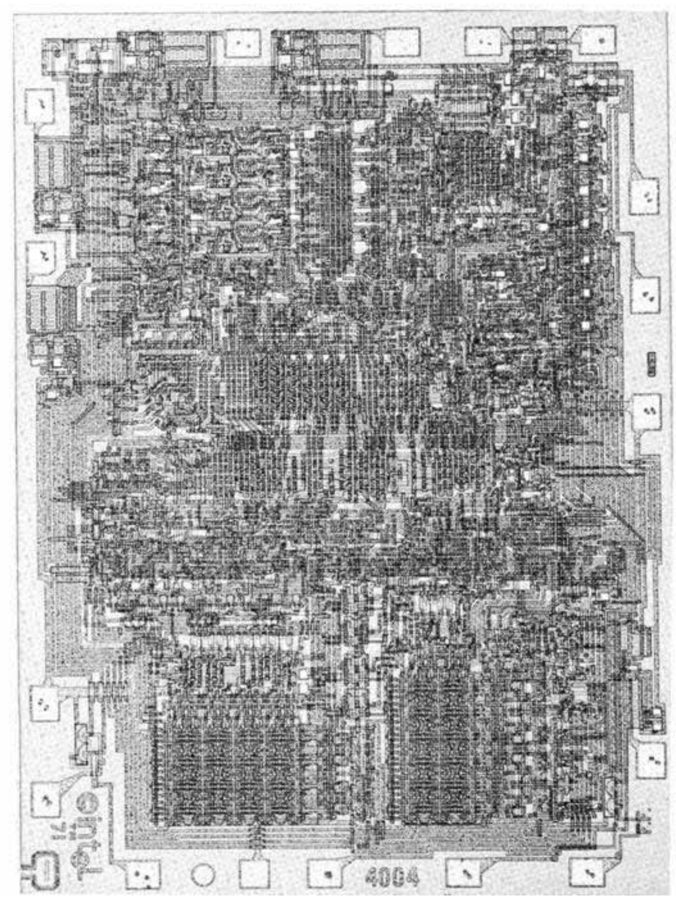


1970,71: 1st generation of LSIs

DRAM Intel 1103

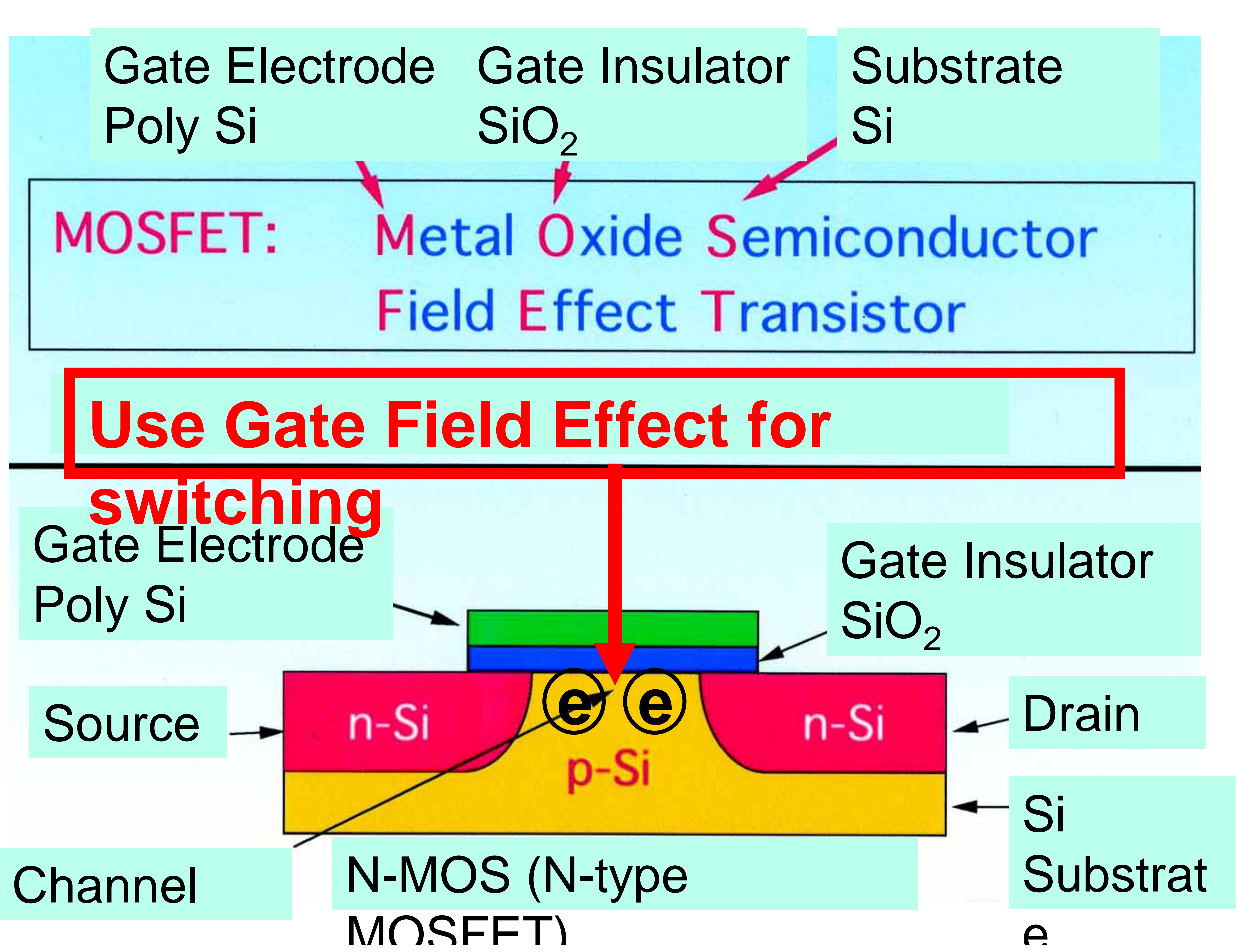


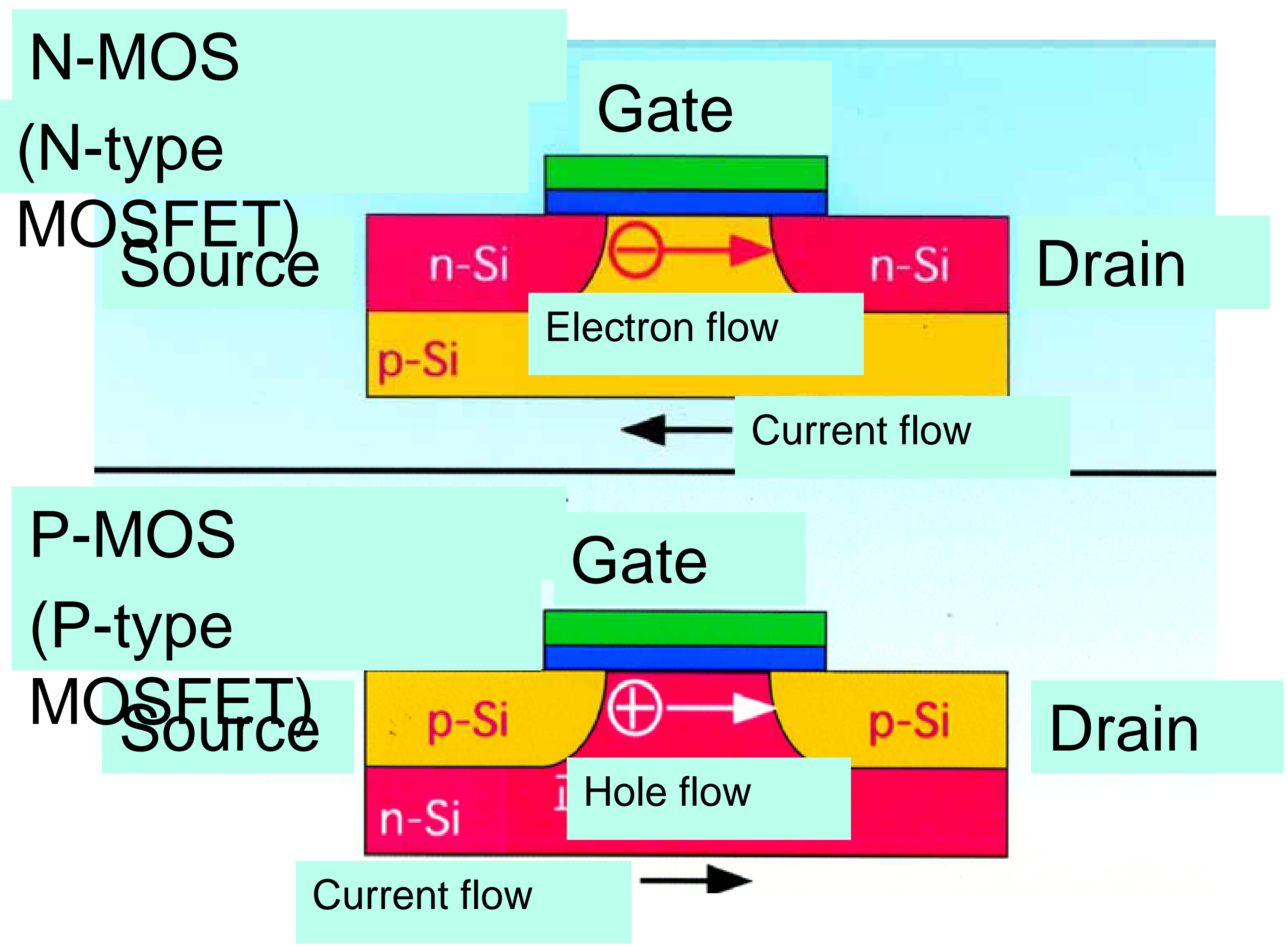
MPU Intel 4004

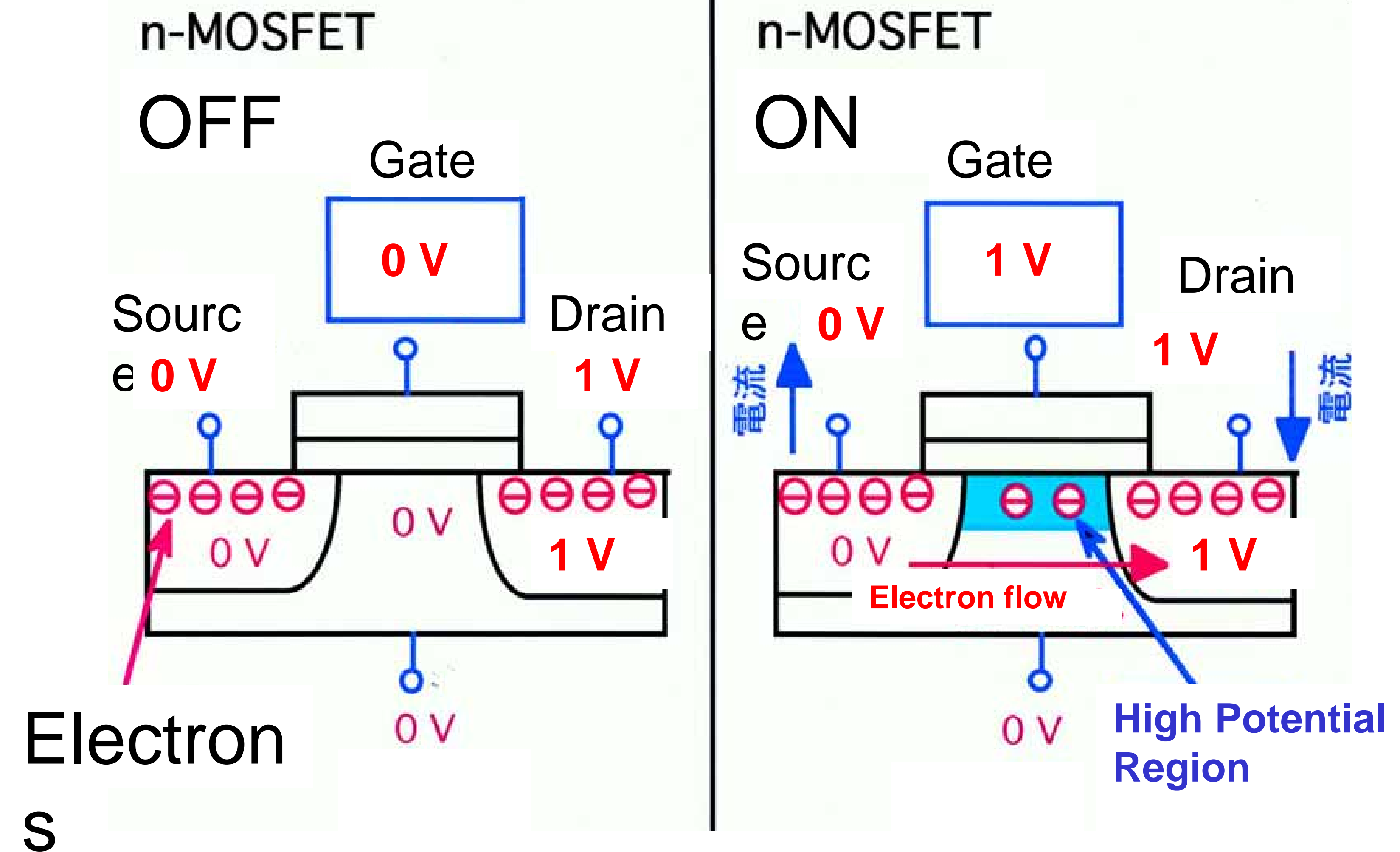


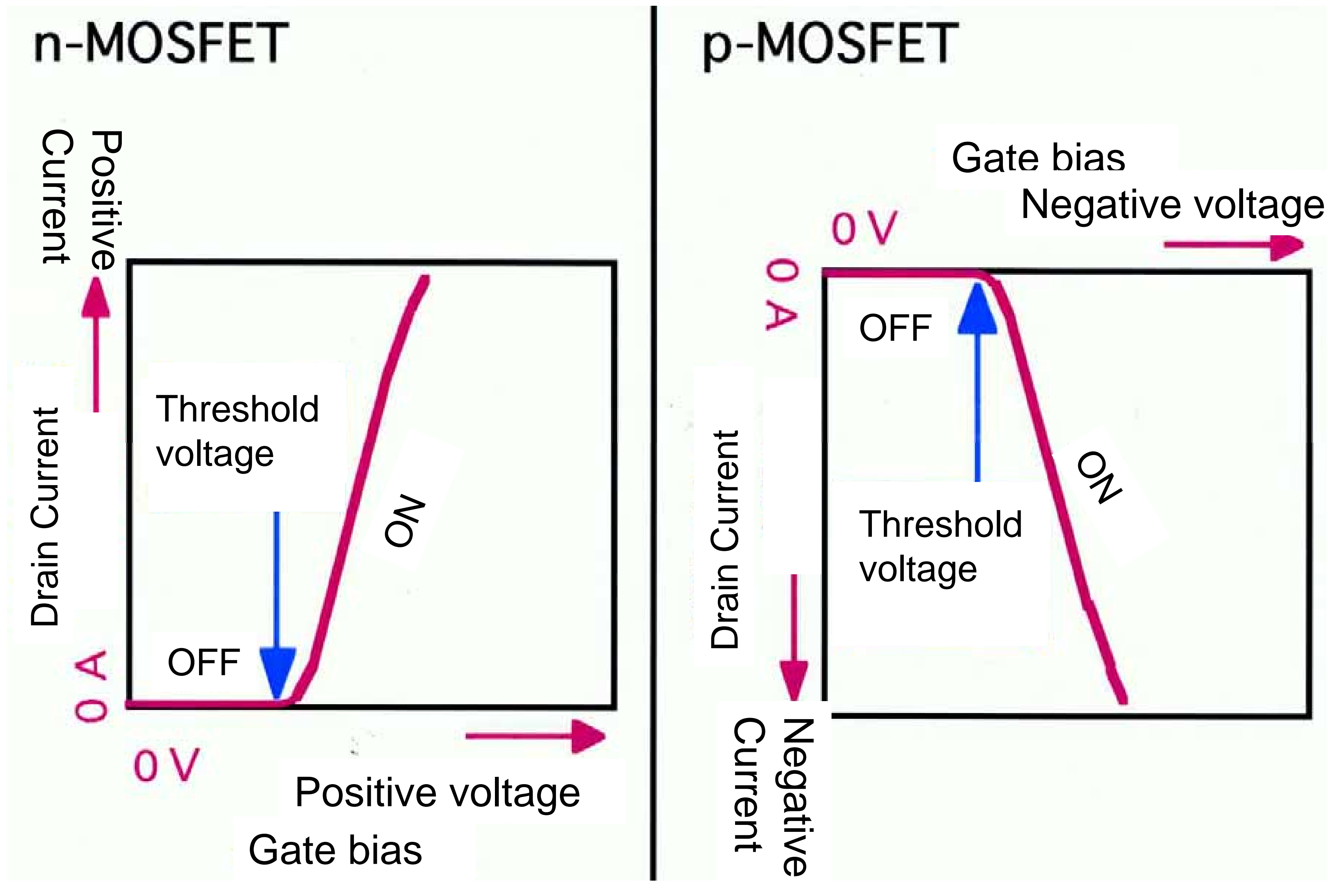
MOS LSI experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~
1970s	LSI (Large Scale Integrated Circuit)	~1,0
1980s	VLSI (Very Large Scale IC)	~10,0
1990s	ULSI (Ultra Large Scale IC)	~1,000,0
2000s	?LSI (? Large Scale IC)	~1000,000

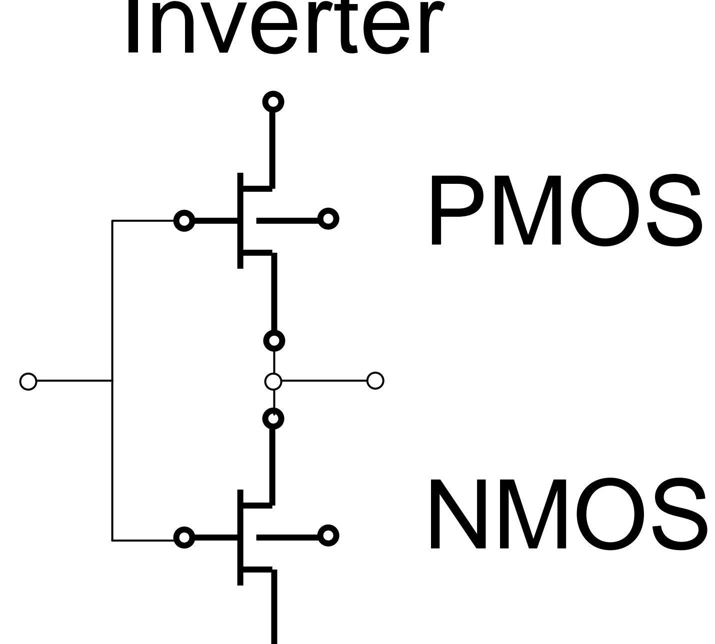

Gate Electrode
Poly Si
Gate Insulator
SiO_2
Substrate
Si
MOSFET: Metal Oxide Semiconductor
Field Effect Transistor
Use Gate Field Effect for switching
Gate Electrode
Poly Si
Gate Insulator
SiO_2
Source
n-Si
e
e
n-Si
Drain
p-Si
Si Substrate
Channel
N-MOS (N-type MOSFET)


N-MOS
(N-type
MOSFET)
Gate
Source
n-Si
n-Si
Drain
Electron flow
p-Si
Current flow
P-MOS
(P-type
MOSFET)
Gate
Source
p-Si
p-Si
Drain
Hole flow
n-Si
Current flow


n-MOSFET
OFF
Gate
0 V
Sourc
e 0 V
Drain
1 V
0 V
0 V
1 V
0 V
Electron
s
n-MOSFET
ON
Gate
1 V
Sourc
e 0 V
Drain
1 V
電流
電流
0 V
1 V
Electron flow
0 V
High Potential
Region

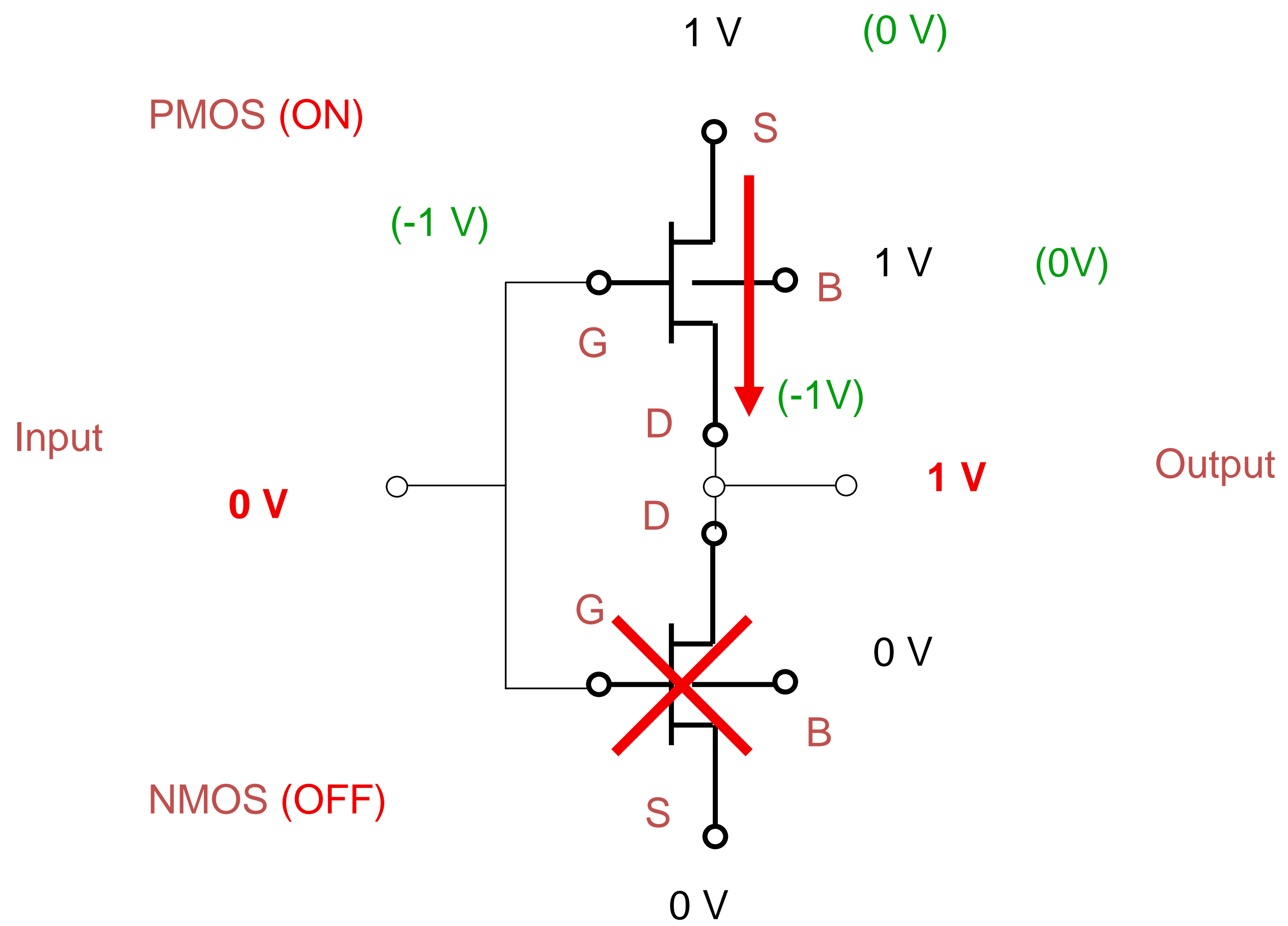

n-MOSFET
Positive Current
Drain Current
Threshold voltage
ON
OFF
0 A
0 V
Positive voltage
Gate bias
p-MOSFET
Gate bias
Negative voltage
0 V
0 A
OFF
ON
Drain Current
Threshold voltage
Negative Current

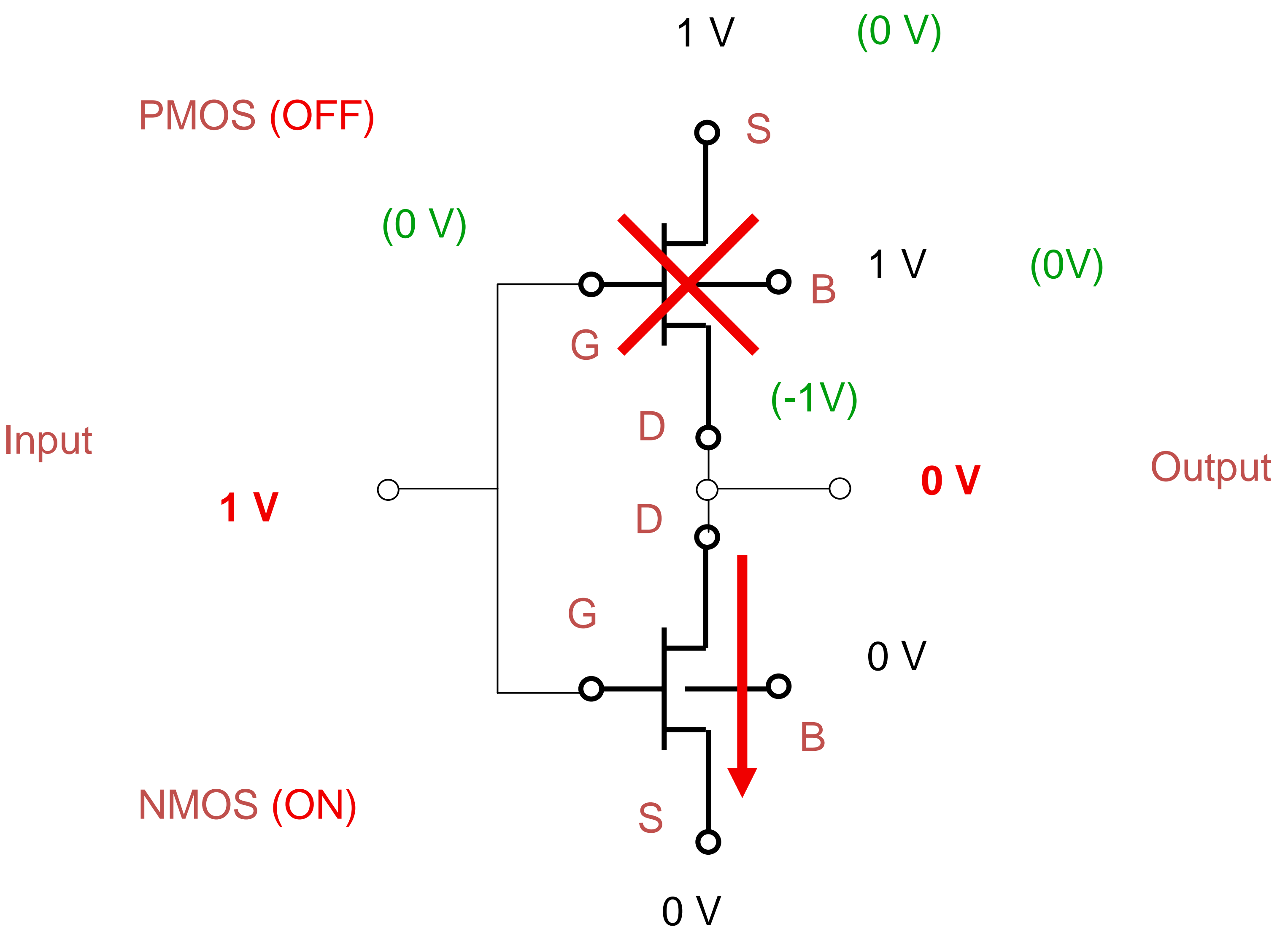
Complimentary MOS



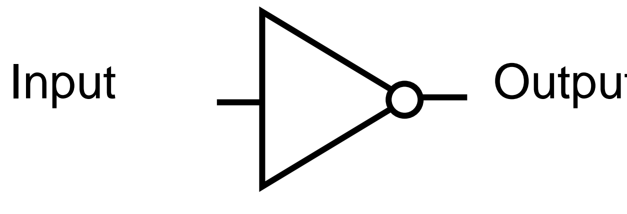
When NMOS is ON, PMOS is OFF

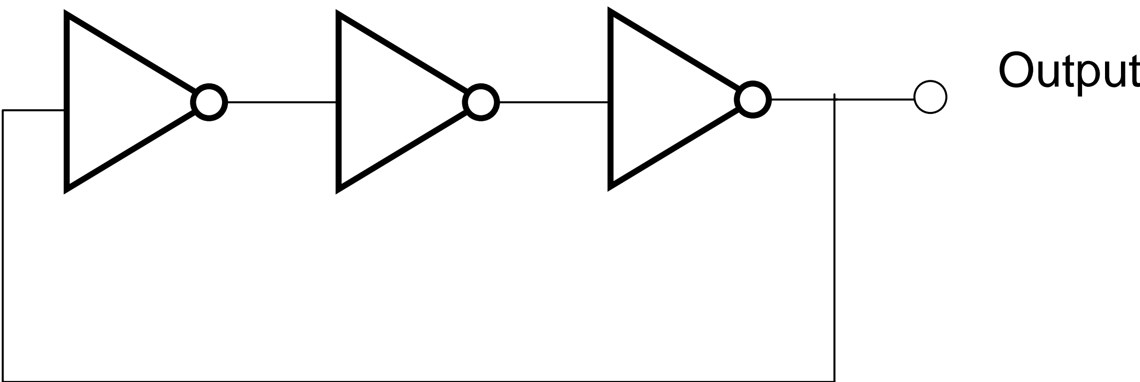
When PMOS is ON, NMOS is OFF


1 V
(0 V)
PMOS (ON)
S
(-1 V)
1 V
(0V)
B
G
(-1V)
D
Input
Output
0 V
1 V
D
G
0 V
B
NMOS (OFF)
S
0 V

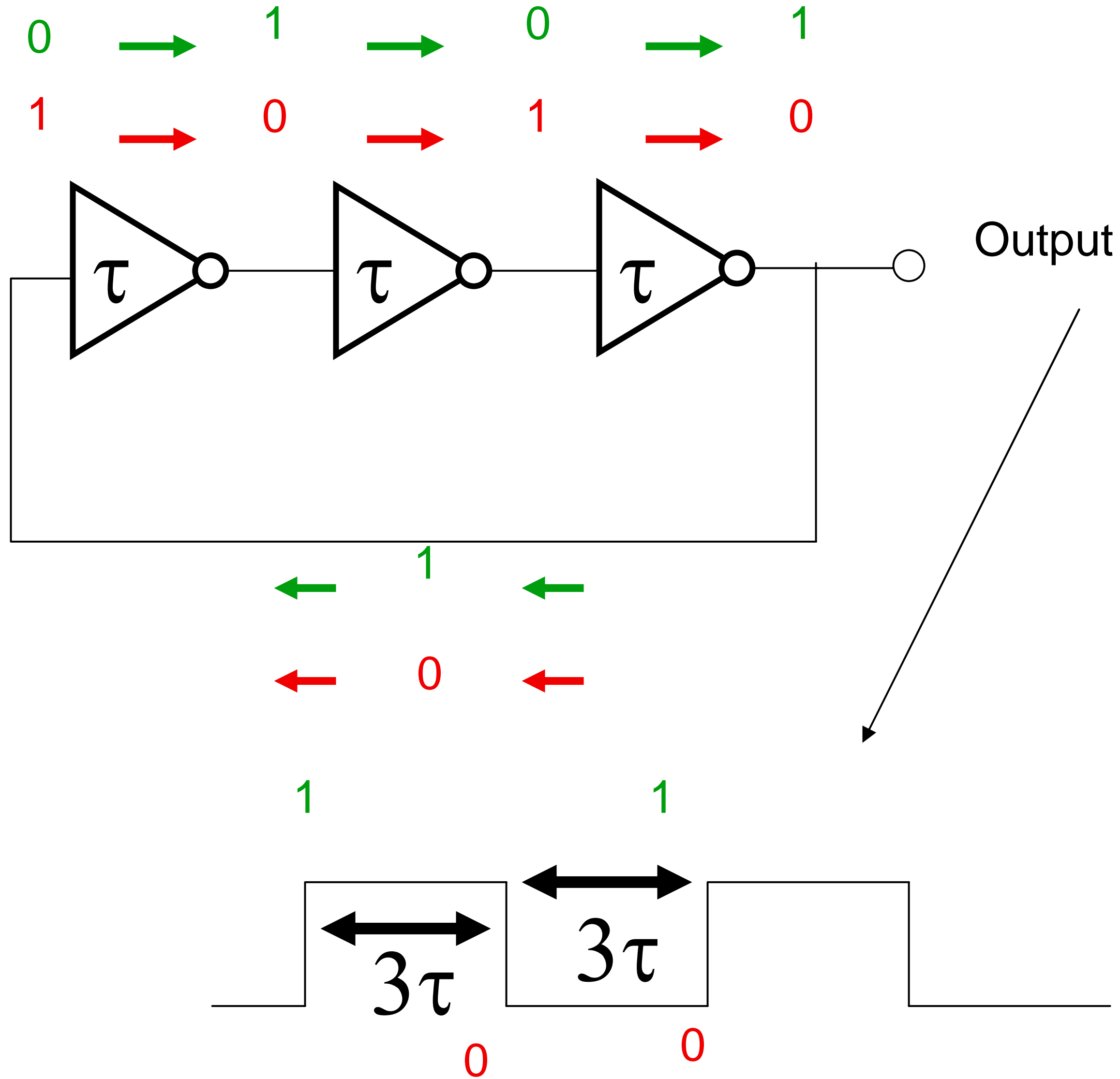

1 V
(0 V)
PMOS (OFF)
S
(0 V)
B
1 V
(0V)
G
(-1V)
Input
D
1 V
0 V
Output
D
G
0 V
B
NMOS (ON)
S
0 V

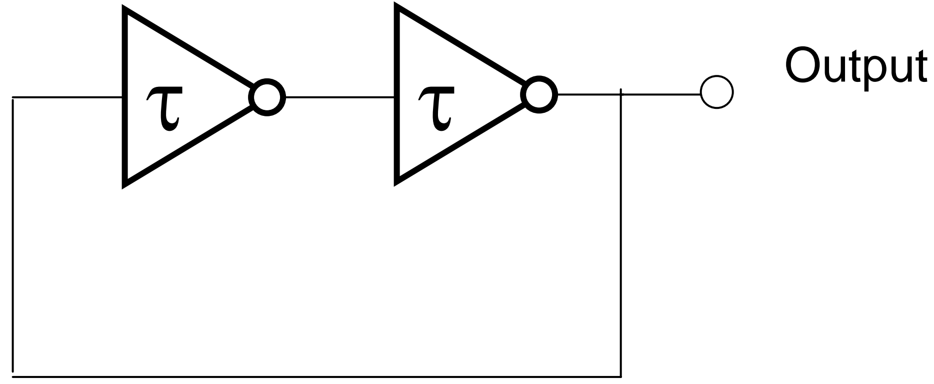
Inverter



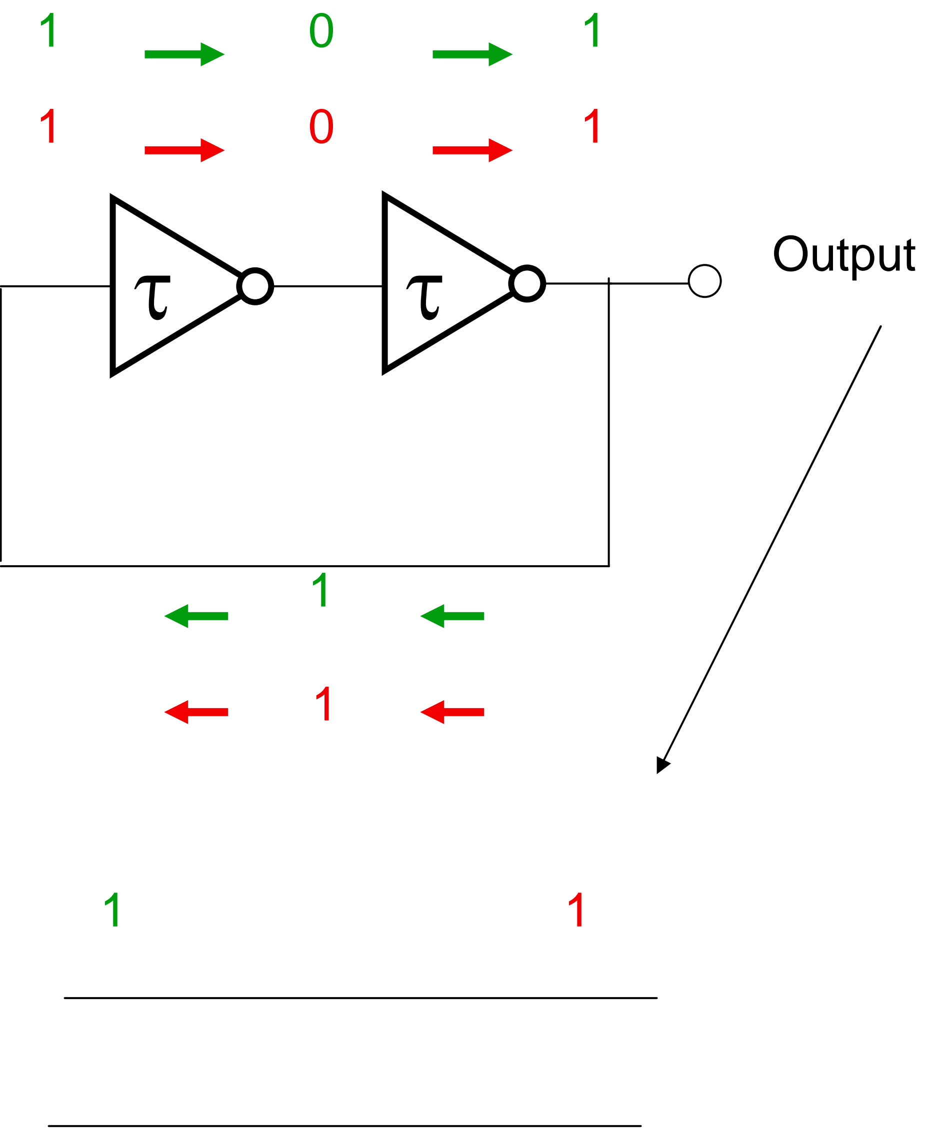


Oscillator

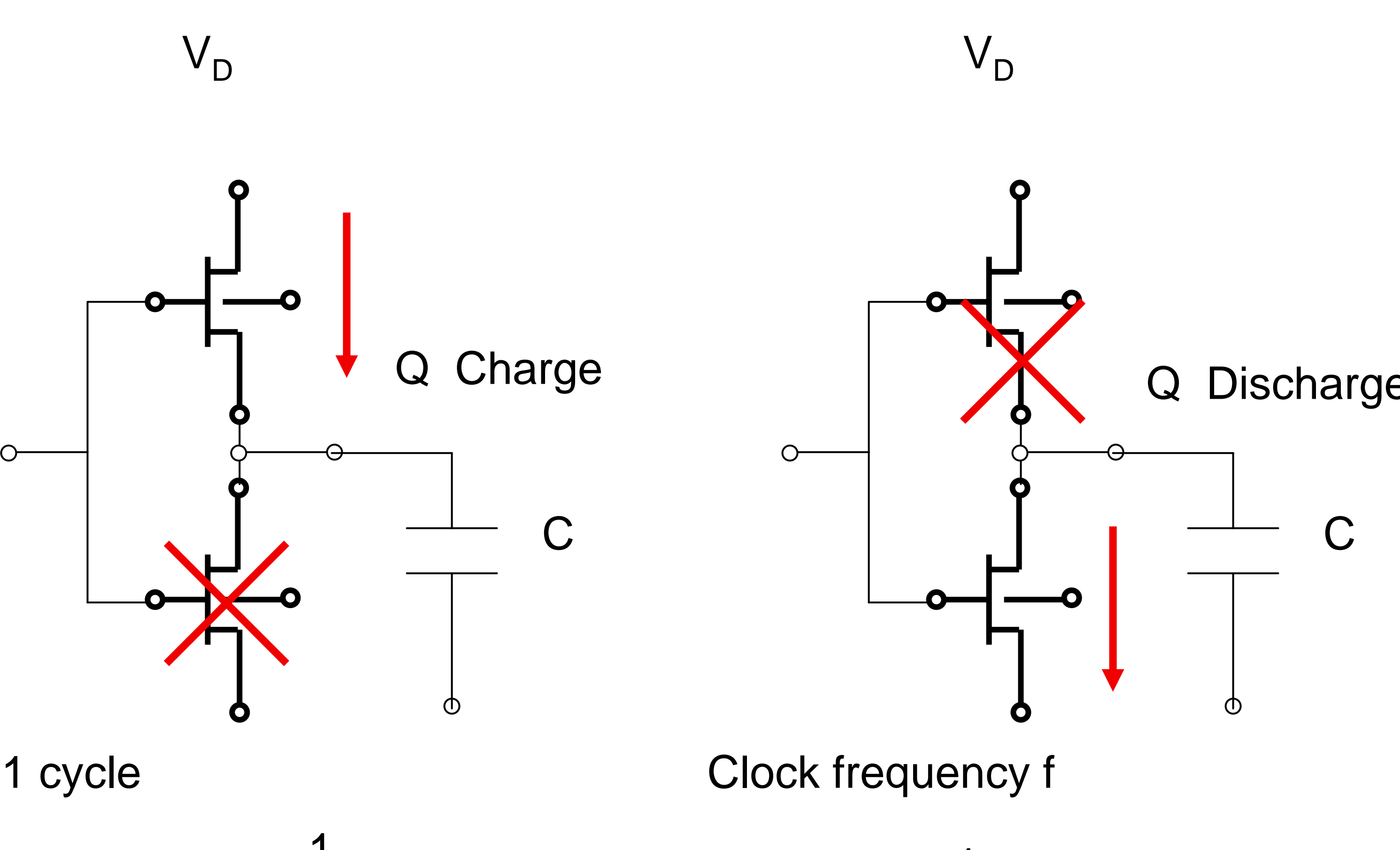



τ
τ
Output

Latch (Memory)



CMOS： Low Power: No DC current from Power supply to the ground



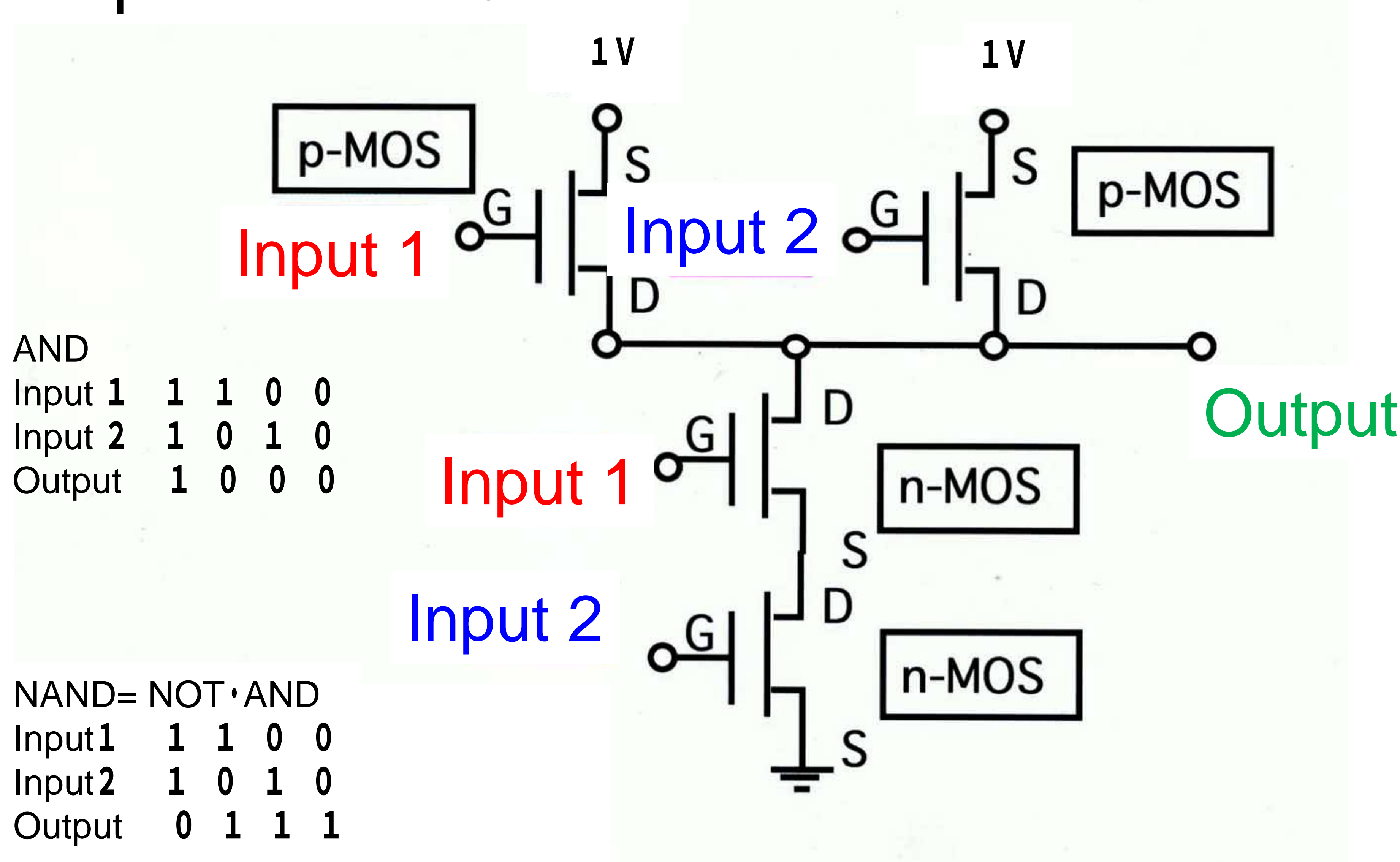
1 cycle

$$P = \frac{1}{2} C V_D^2$$

Clock frequency f

$$P = \frac{1}{2} f C V_D^2$$

2 input NAND Circuit



Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

Cellarer phone dose not exists

Exponential Cost Reduction

Cost per Transistor

10
10^{0}
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}

10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}

'68 '72 '76 '80 '84 '88 '92 '96 '00 '04

As the number of transistors goes UP

Cost per transistor goes DOWN

Source: WSTS/Dataquest/Intel

Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFE**

Reduce power consumption

2. **Increase number of Transistors**

Increase functionality

→ **Parallel processing**

→ **Increase circuit operation sp**

Thus, downsizing of Si devices is the most important and critical issue.

Keep increase of the number of components.
Cost per components decreases!

MOORE'S LAW

transistors

10,000,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
1,000

Dual-Core Intel® Itanium® 2 Processor
Intel® Itanium® 2 Processor
Intel® Itanium® Processor
Intel® Pentium® 4 Processor
Intel® Pentium® III Processor
Intel® Pentium® II Processor
Intel® Pentium® Processor
Intel486™ Processor
Intel386™ Processor
286
8086
8080
8008
4004

1970 1975 1980 1985 1990 1995 2000 2005 2010

Gordon Moore

http://www.intel.com/technology/mooreslaw/index.htm

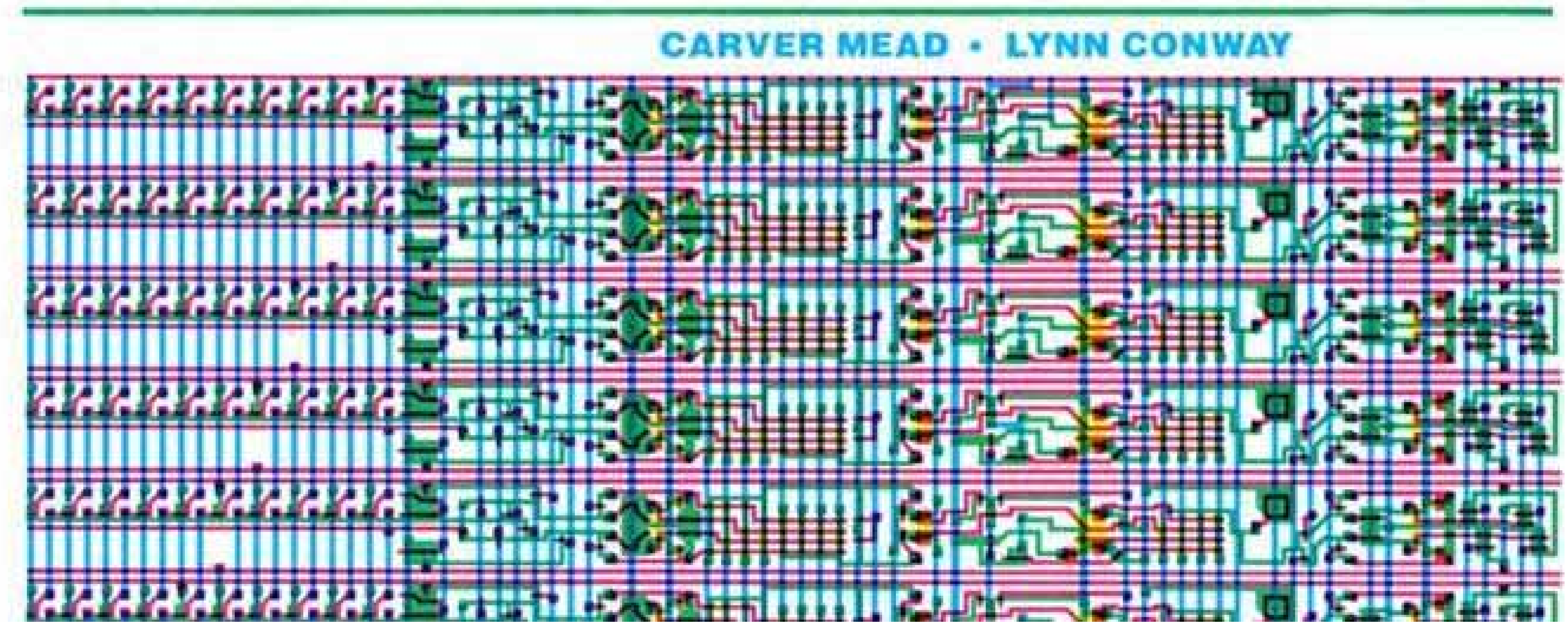
Many people wanted to say about the limit.

Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate Si(
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

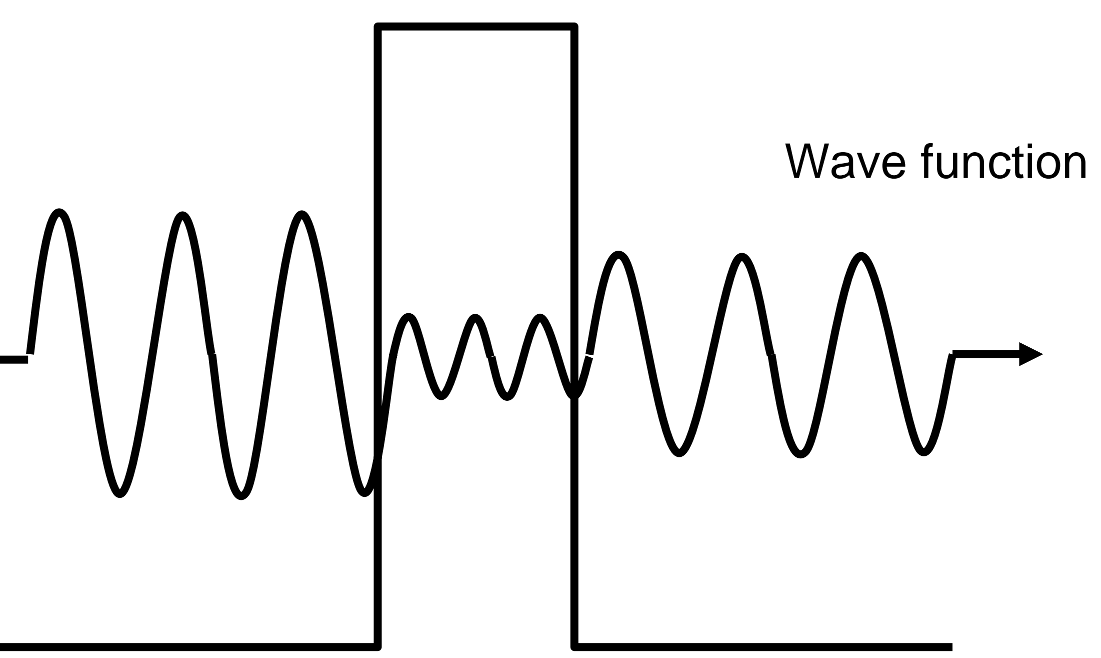


C. Mead L. Conway

VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



Gate electrode

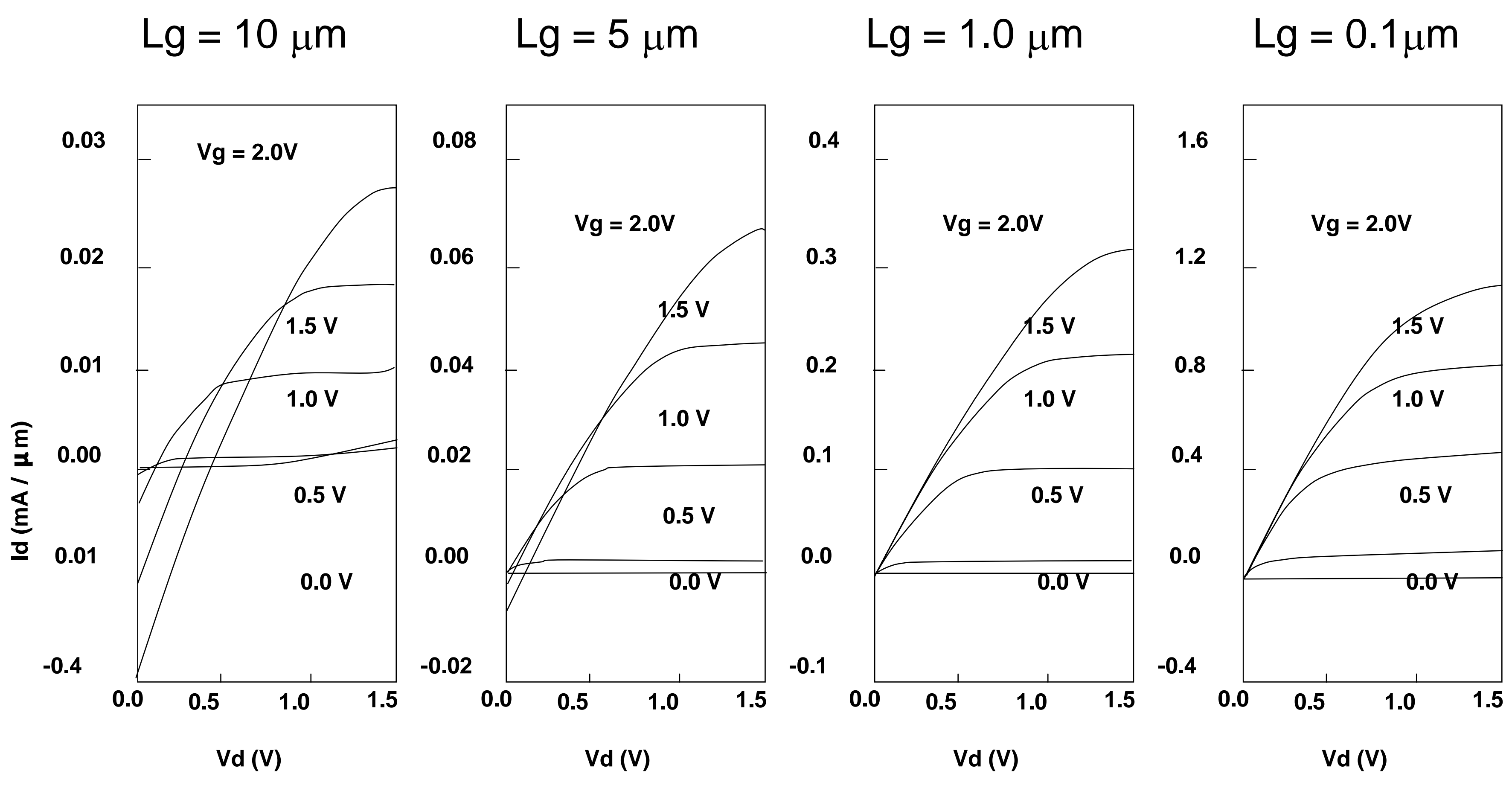
Gate oxide

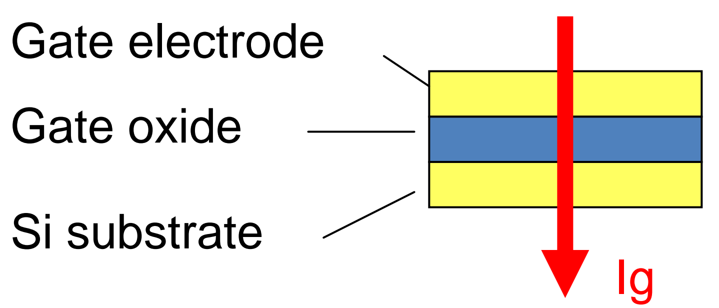
Si substrate

Direct tunneling leakage current start to flow when the thickness is 3 nm.

Direct tunneling leakage was found to be OK! In 1994

MOSFETs with 1.5 nm gate oxide





Direct tunneling leakage current start to flow when the thickness is 3 nm.

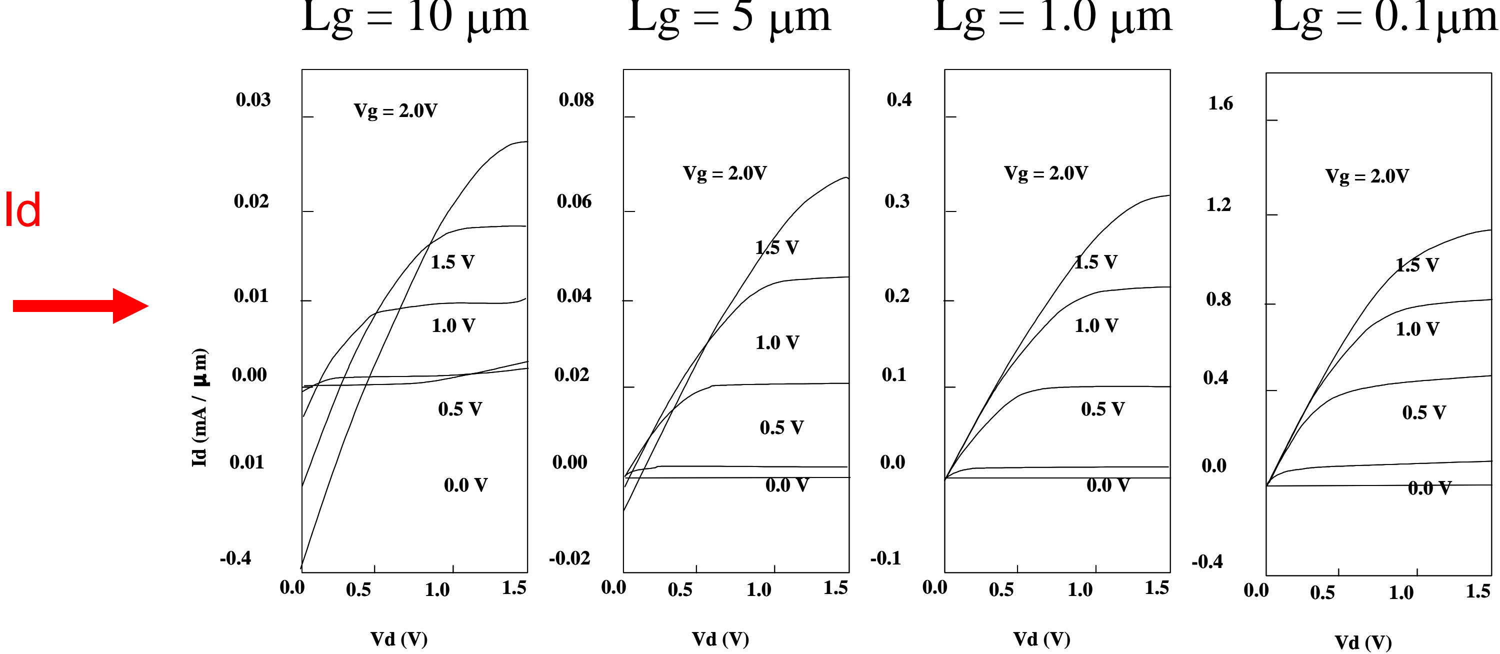
Gate oxd thickness

Gate length

Gate leakage: Ig $\propto$ Gate Area $\propto$ Gate length (Lg)

Drain current: Id $\propto$ 1/Gate length (Lg)

Lg → small,
Then, Ig → small, Id → large, Thus, Ig/Id → very small



Do not believe a text book statement, blindly!

Never Give Up!

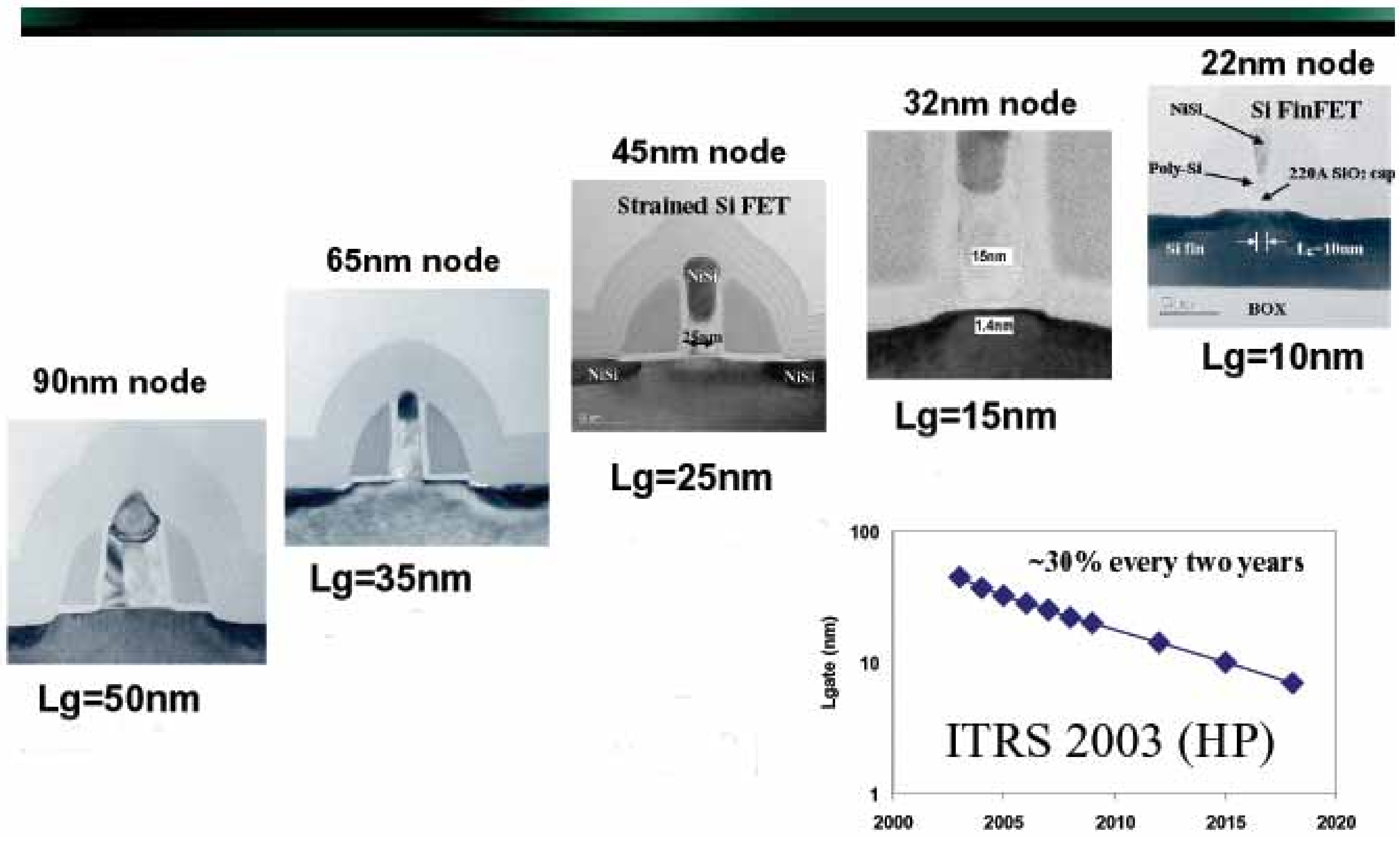
No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

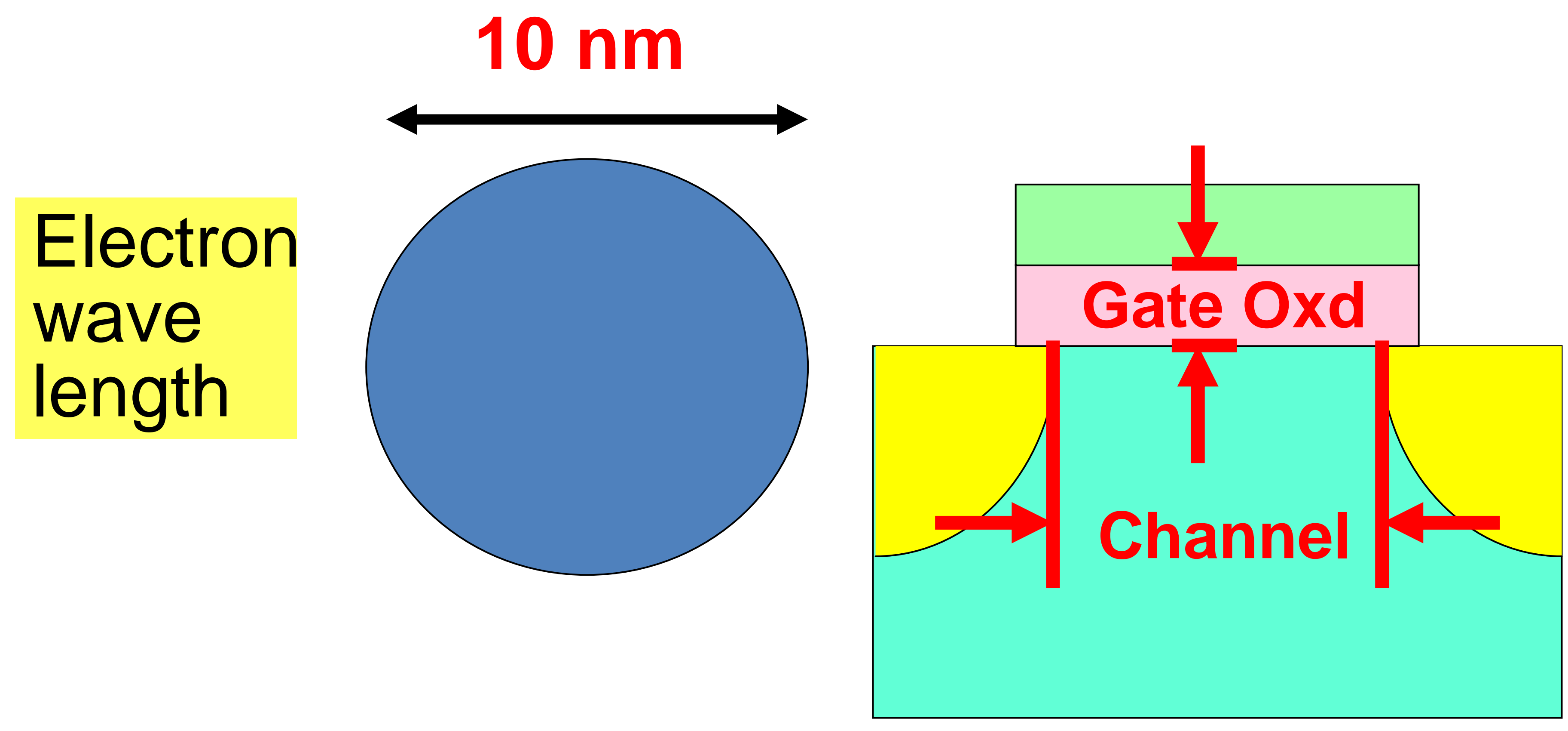
Transistor Scaling Continues



Qi Xinag, ECS 2004, AM

Downsizing limit?

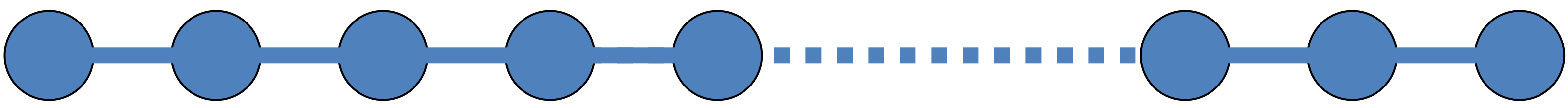
Channel length?



5 nm gate length CMOS

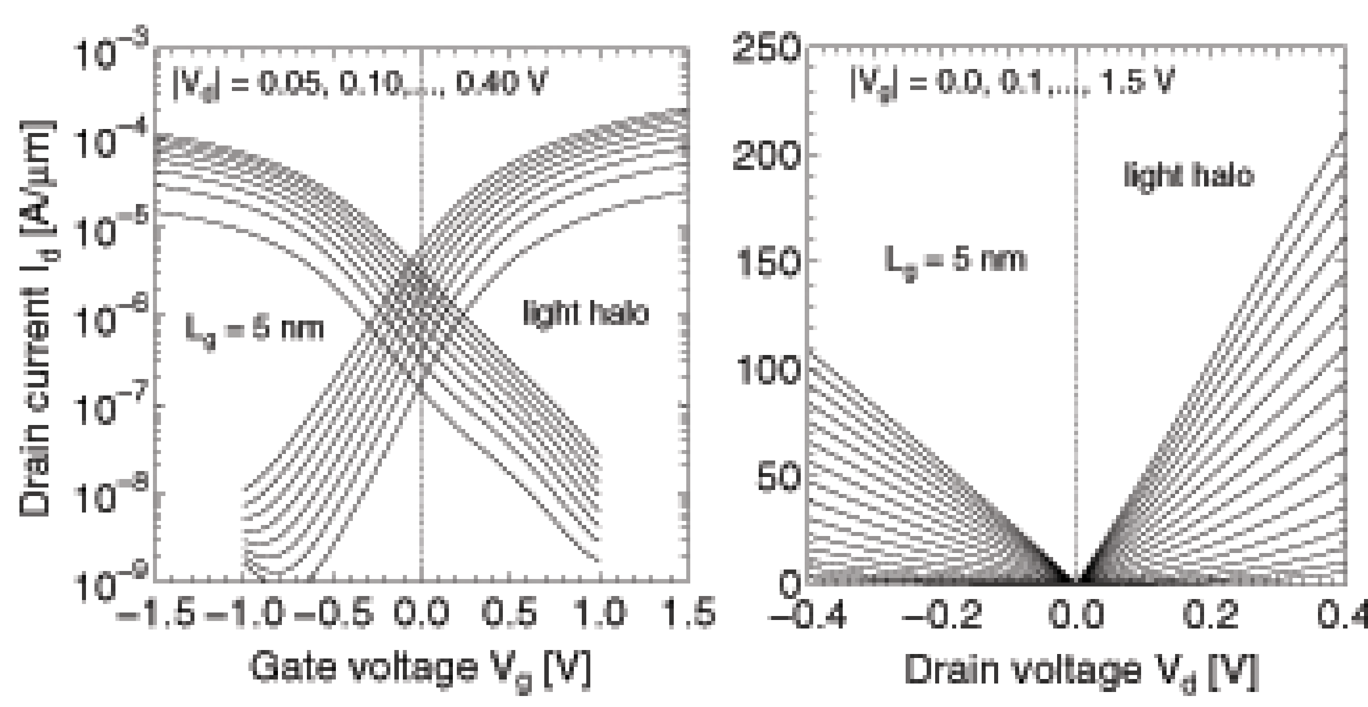
Is a Real Nano Device!!

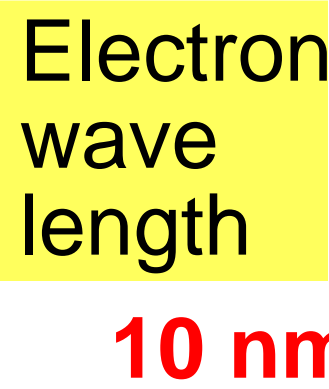
Length of 18 Si atoms

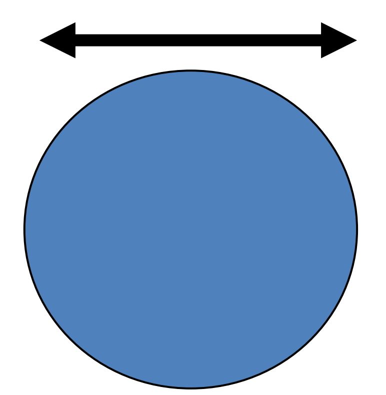


H. Wakabayashi et.al, NEC

IEDM, 2003

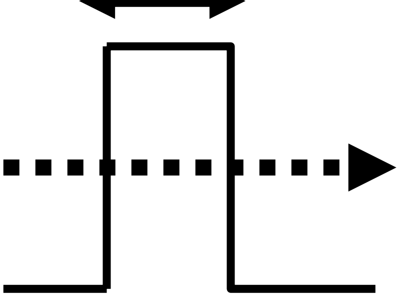






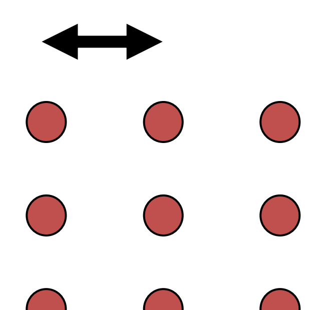
10 nm

Tunneling distance



3 nm

Atom distance

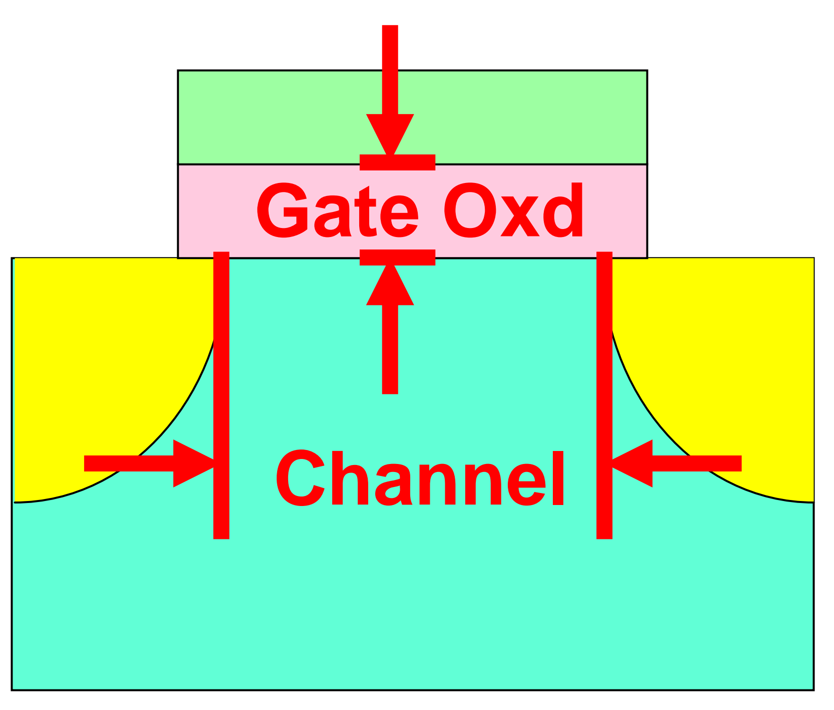


0.3 nm

<u>Downsizing limit!</u>

Channel length

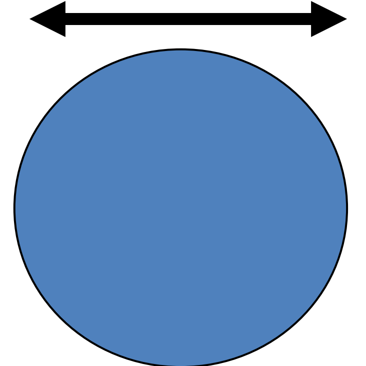
Gate oxide thickness



Prediction now!

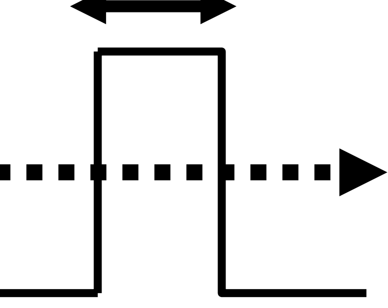
Electron wave length

10 nm



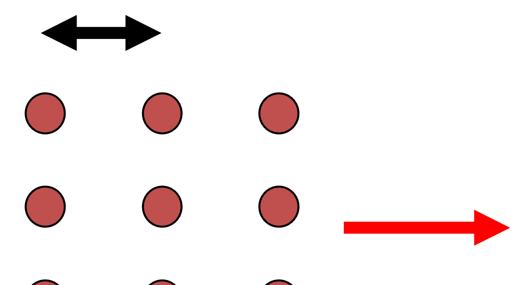
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

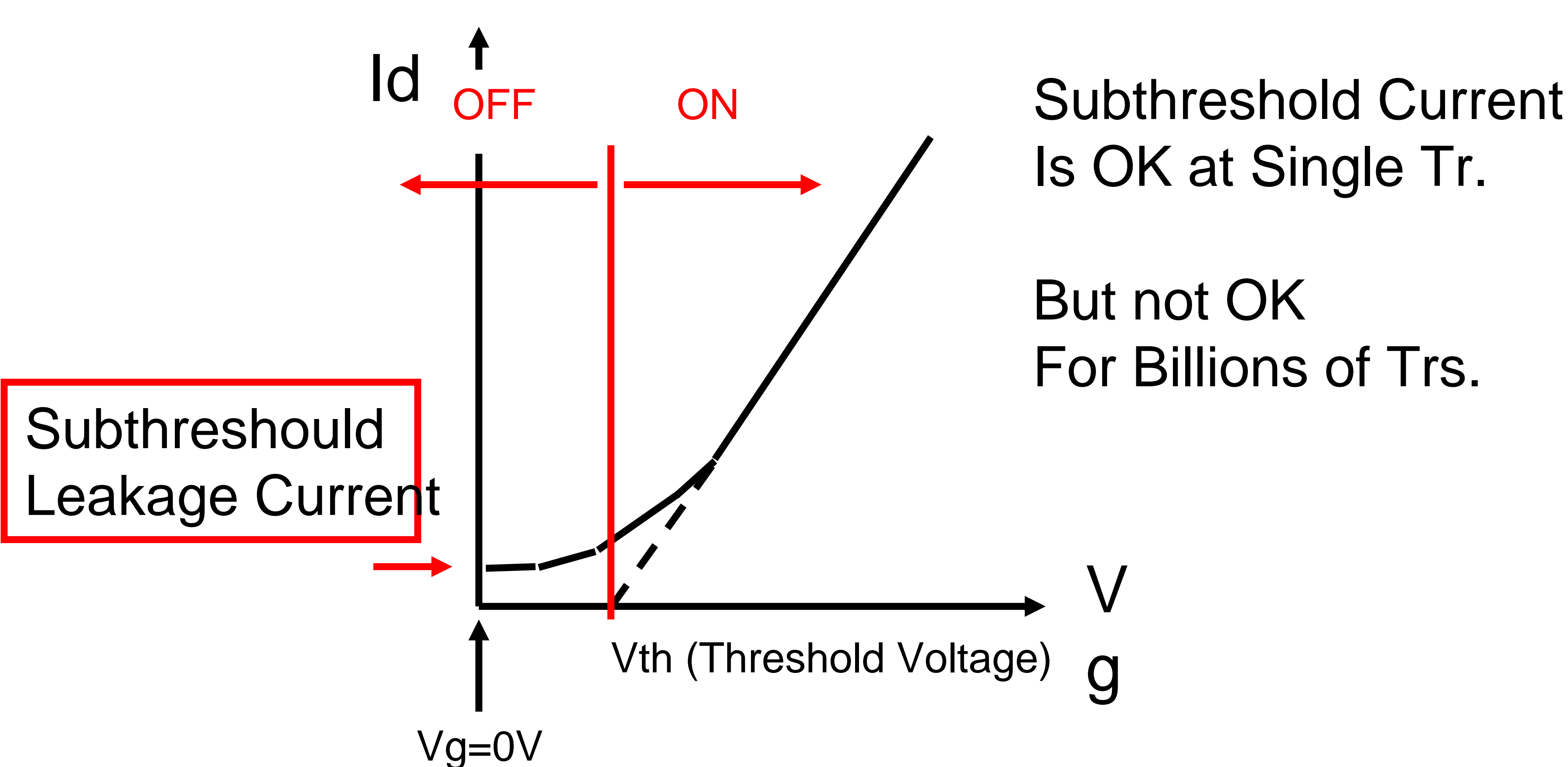
Lg = 2 ~ 1.5 nm?

Below this, no one knows future!

Maybe, practical limit around 5 nm.

When Gate length Smaller,

→ Subthrehold Leakage Current Larger



Subthreshold Current
Is OK at Single Tr.

But not OK
For Billions of Trs.

We have to reduce the Supply voltage.

Then Vth should be lowered.

Subthreshold leakage current increase

Log Id

10^{-6}A

10^{-7}A

10^{-8}A

10^{-9}A

10^{-10}A

Vth lowering

Vth ***Vth***

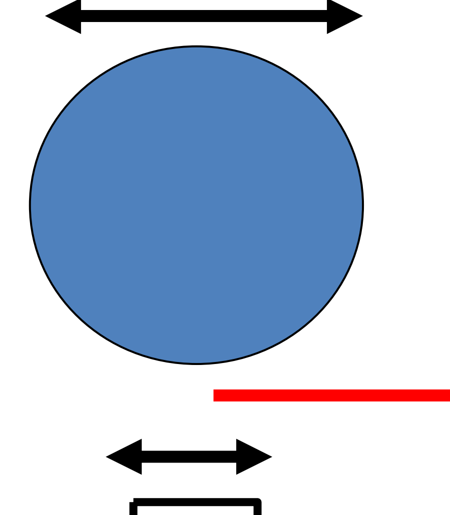
Vg = 0V

Vg (V)

Prediction now!

Electron wave length

10 nm



Tunneling distance

3 nm

Atom distance

0.3 nm

Practical limit for integration

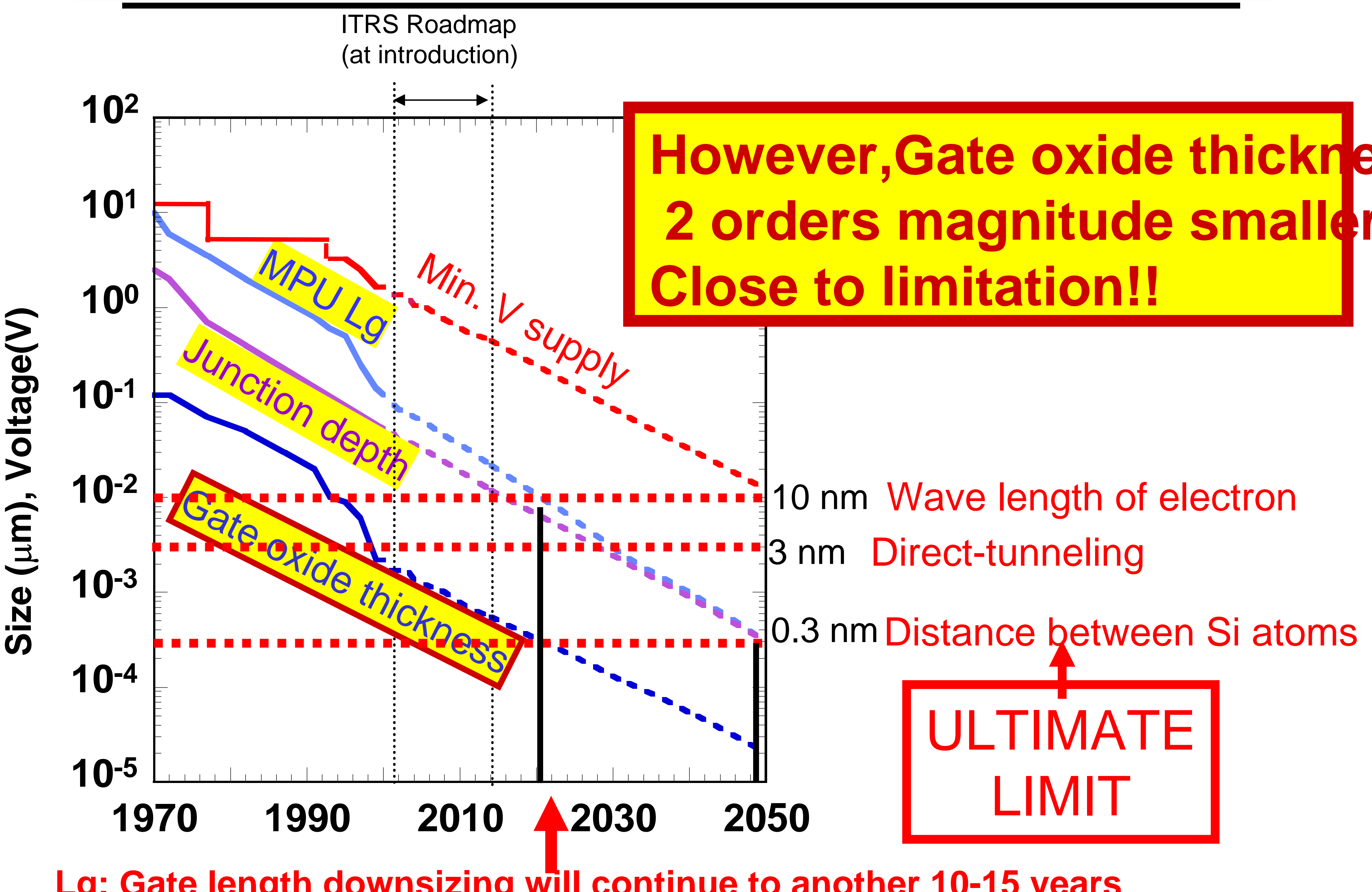
Lg = 5 nm?

MOSFET operation

Lg = 2 ~ 1.5 nm?

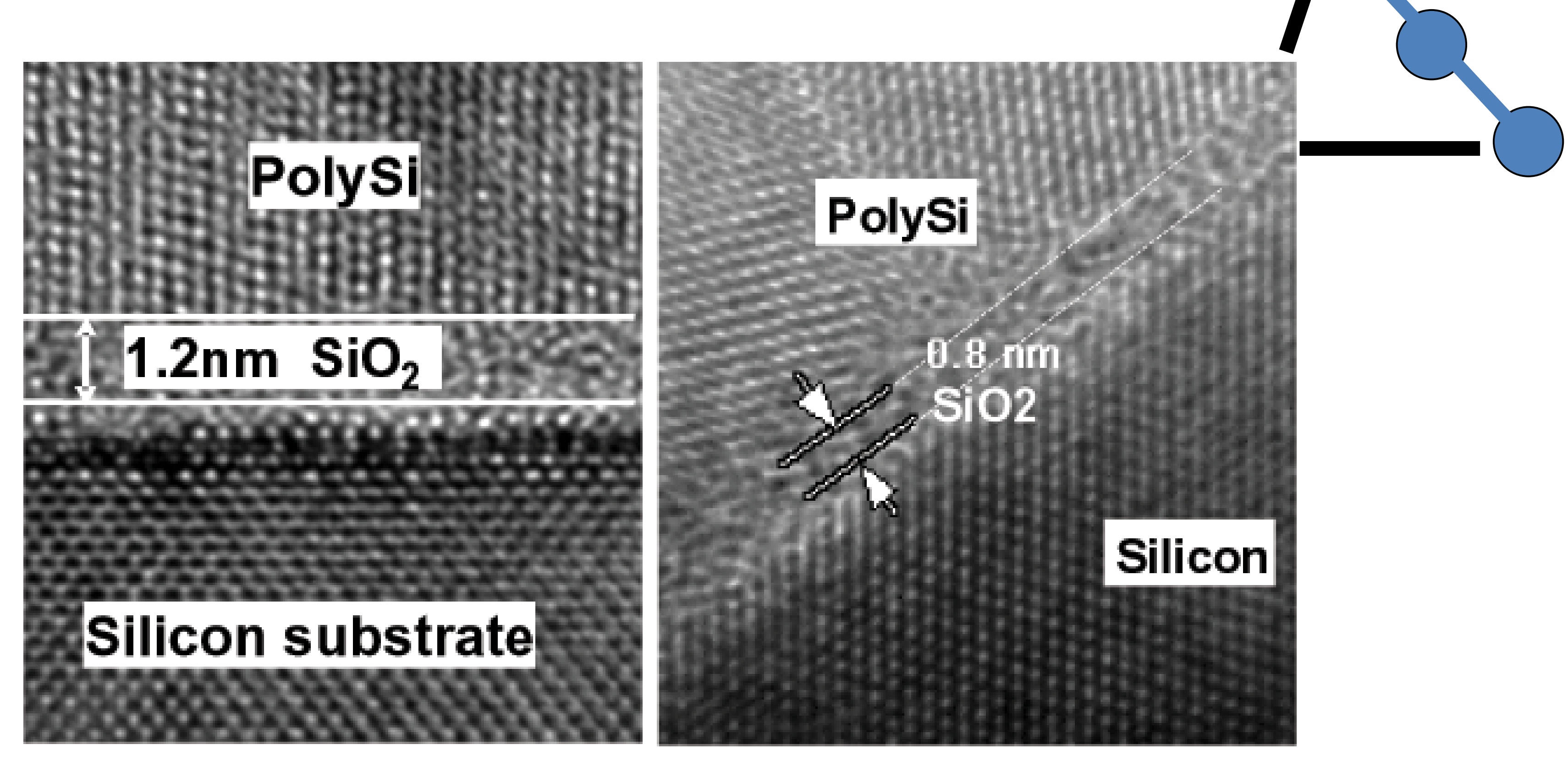
Below this, no one knows future!

Ultimate limitation



0.8 nm Gate Oxide Thickness MOSFETs operat

0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

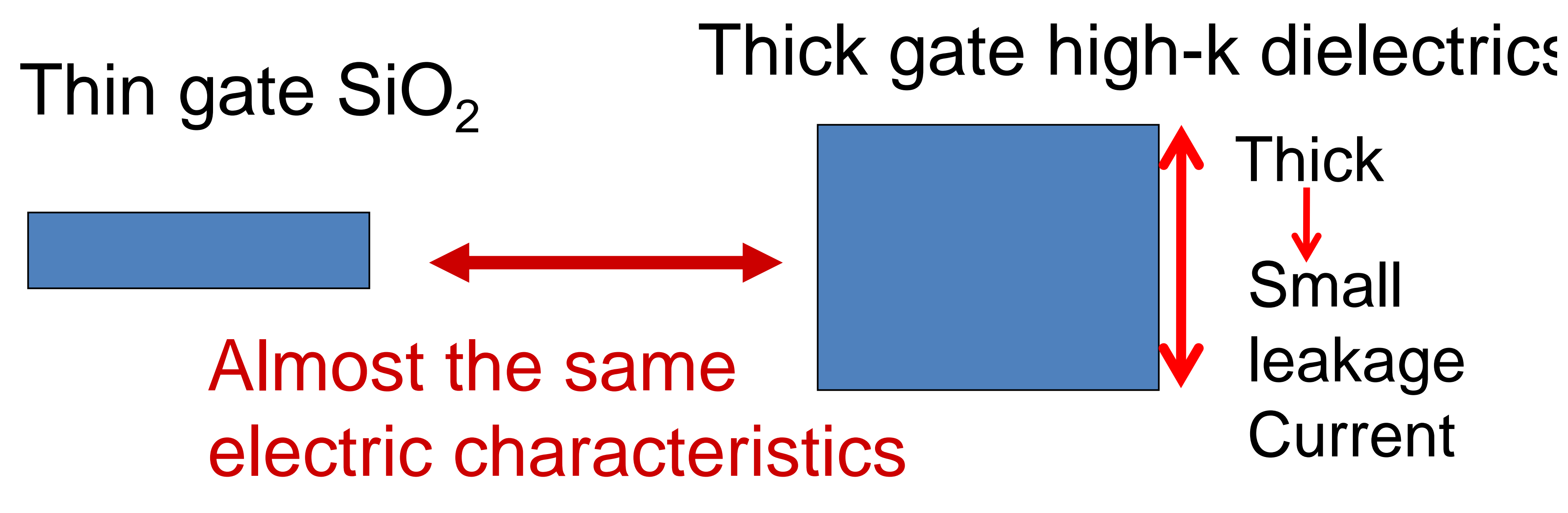
By Robert Chau, IWGI 200

So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constan

To use high-k dielectrics

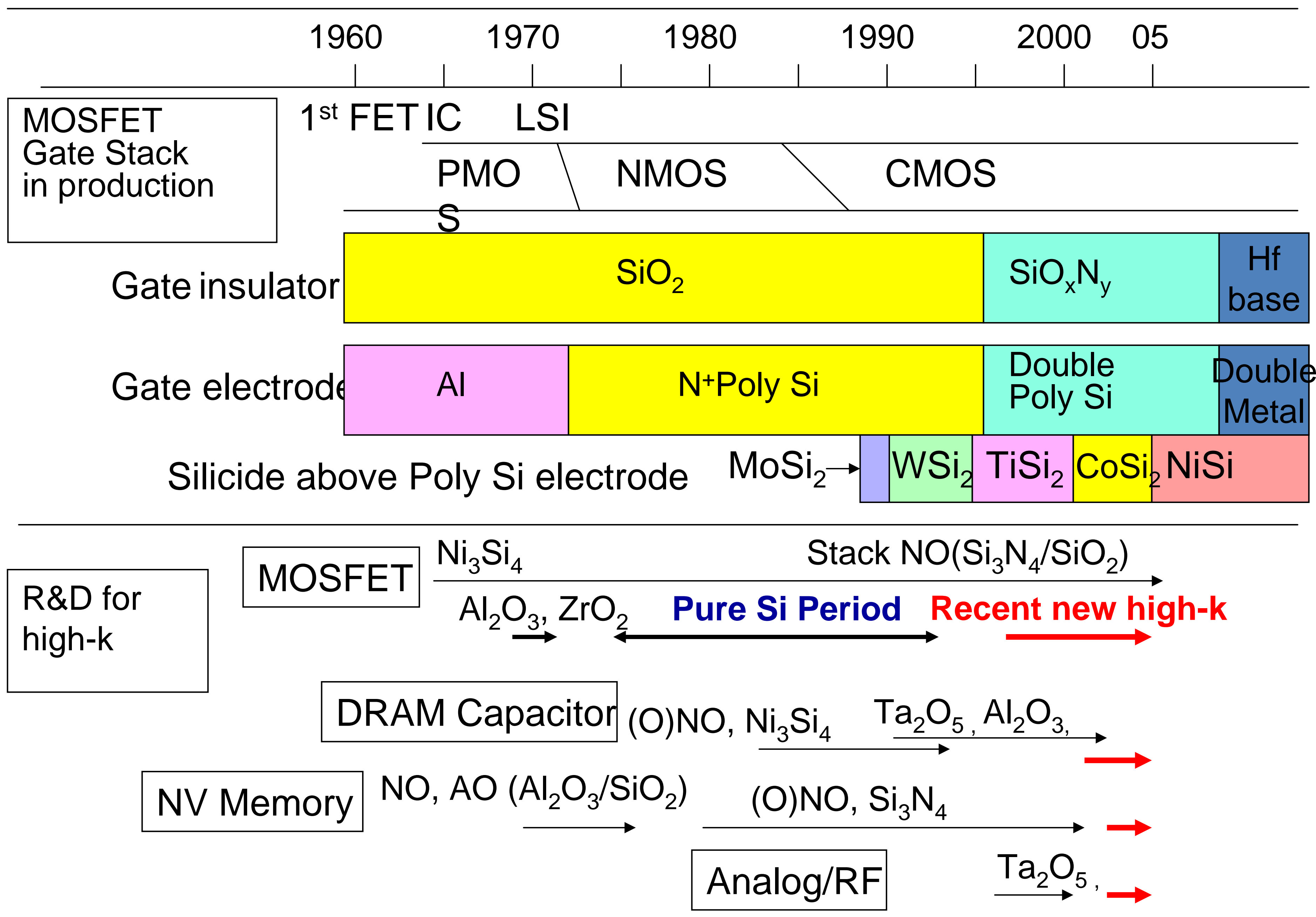


However, very difficult and big challenge!

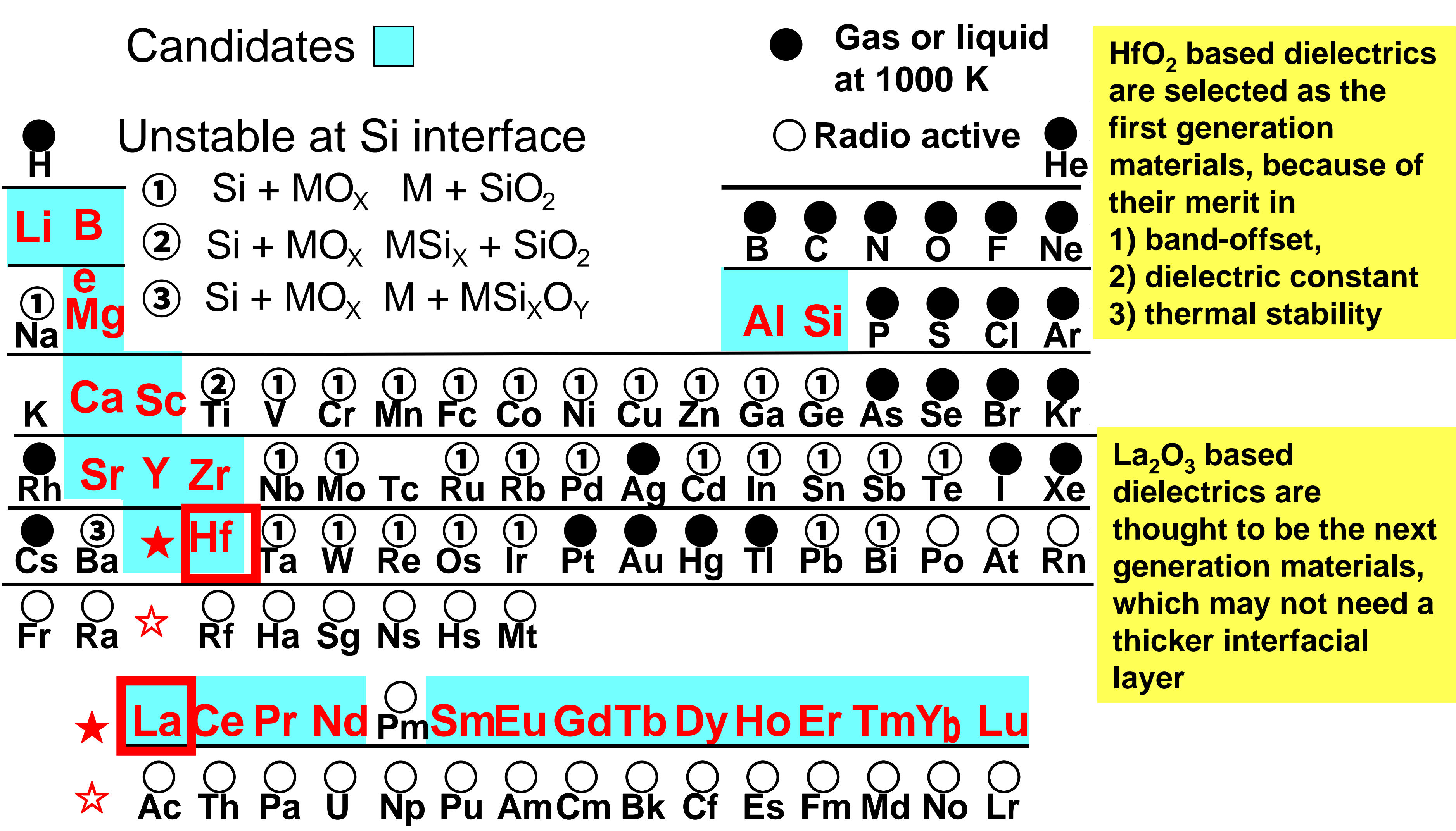
Remember MOSFET had not been realize

without Si/SiO_2!

Historical Trend of New Material for Gate Stack

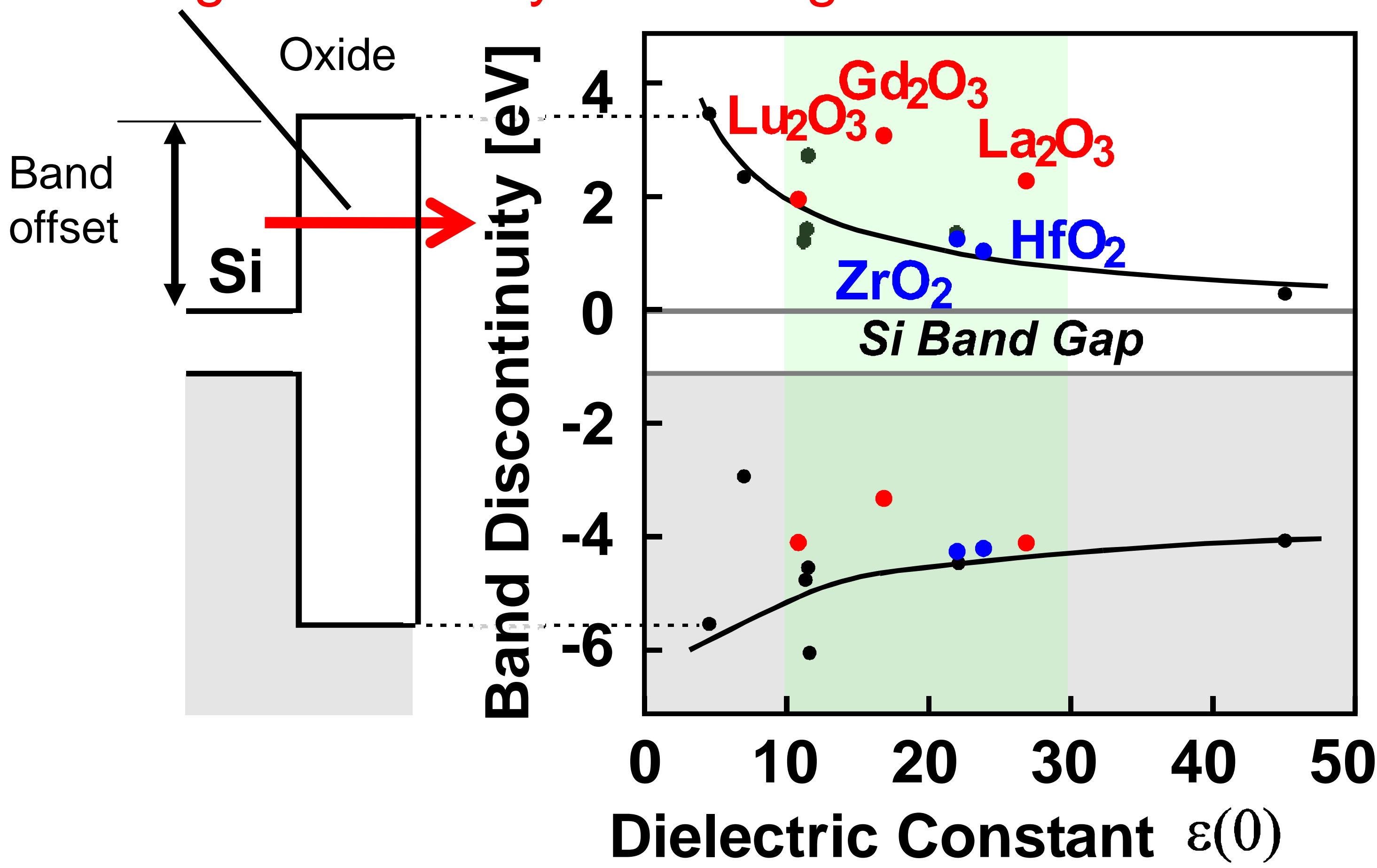


Choice of High-k elements for oxide



R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Conduction band offset vs. Dielectric Constan



XPS measurement by Prof. T. Hattori, INFOS 2003

Intel's announcement, January 26, 2007, and IEDM Dec 2007

Hafnium-based high-k material by ALD: EOT= 1nm
Specific gate metals (Intel's trade secret)
Different Metals for NMOS and PMOS
Use of 193nm dry lithography

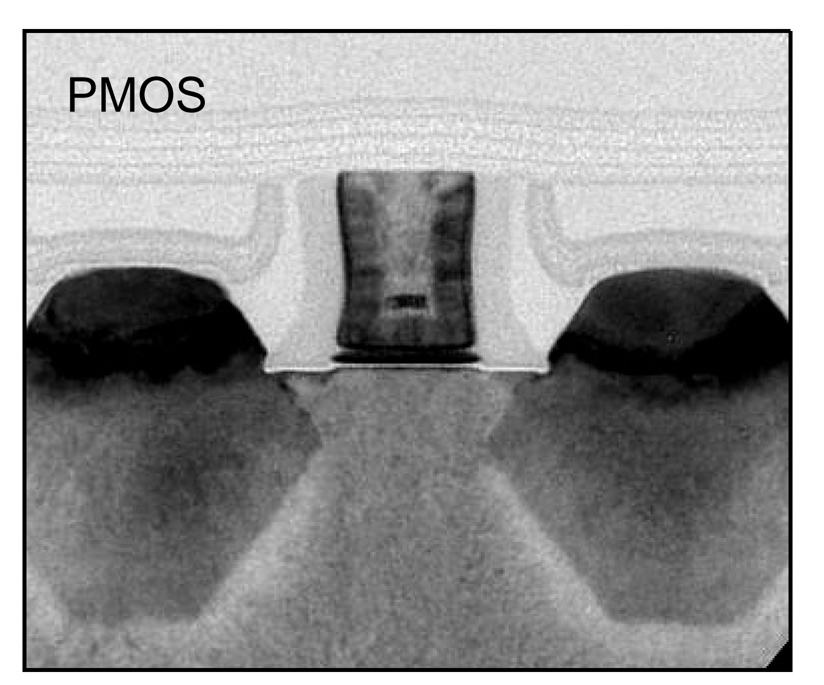
From 65 nm to 45 nm Tech.
Tr density: 2 times increase
Tr switching power: 30% reduction
Tr switching speed: 20% improvement
S-D leakage power: 5 times reduction
Gate oxide leakage: 10 times reduction

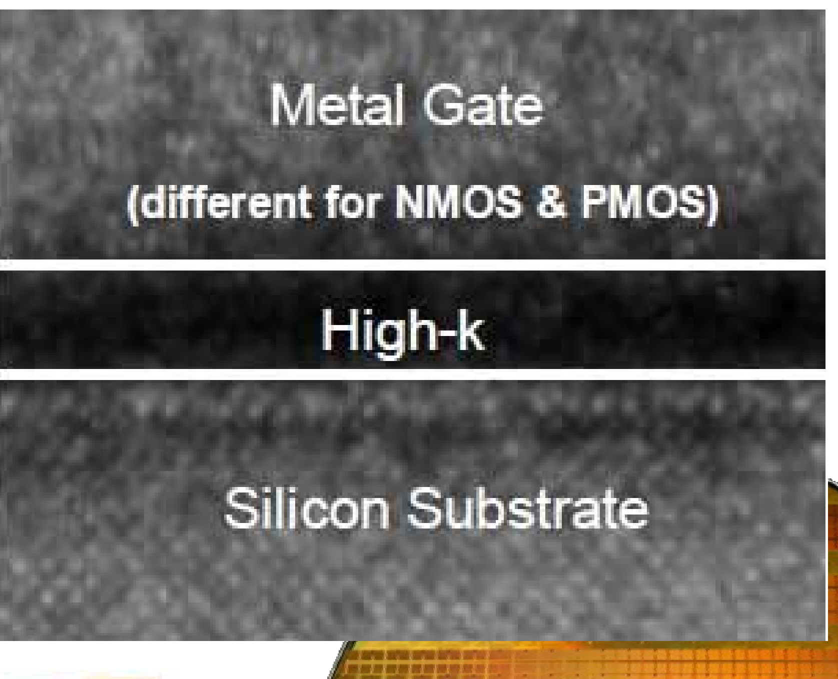
45nm processors (Core™2 family processors "Penryn") running Windows* Vista*, Linux* etc.

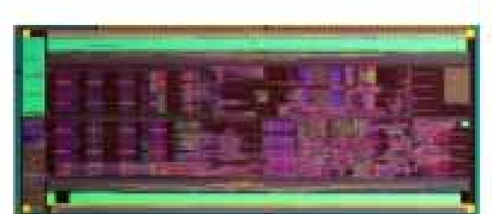
45nm production in the second half of 2007

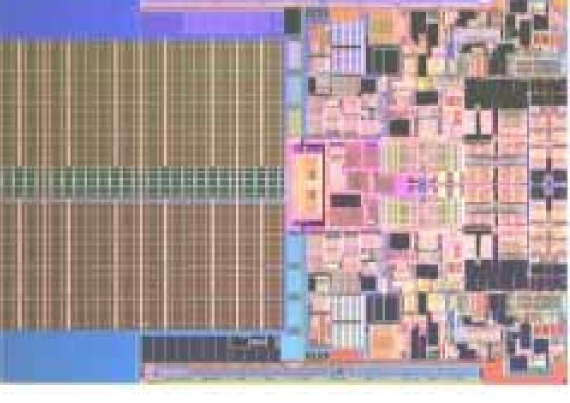
High-k gate insulator MOSFETs for Intel: EOT=1nm

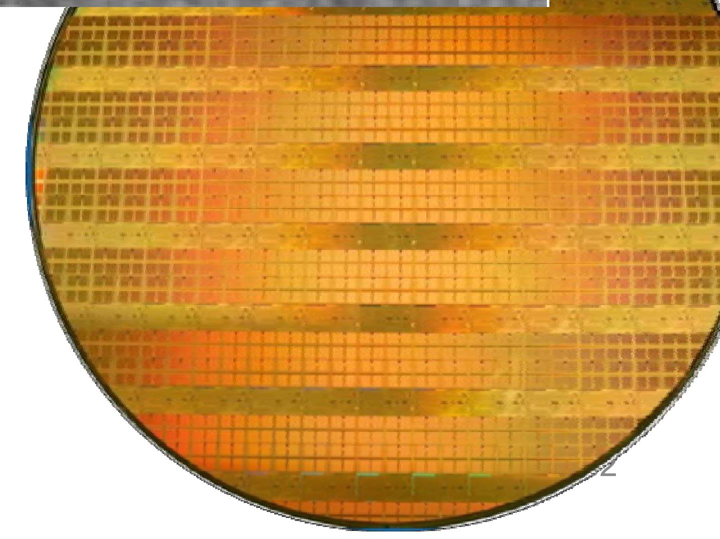
EOT: Equivalent Oxide Thickness











History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking!

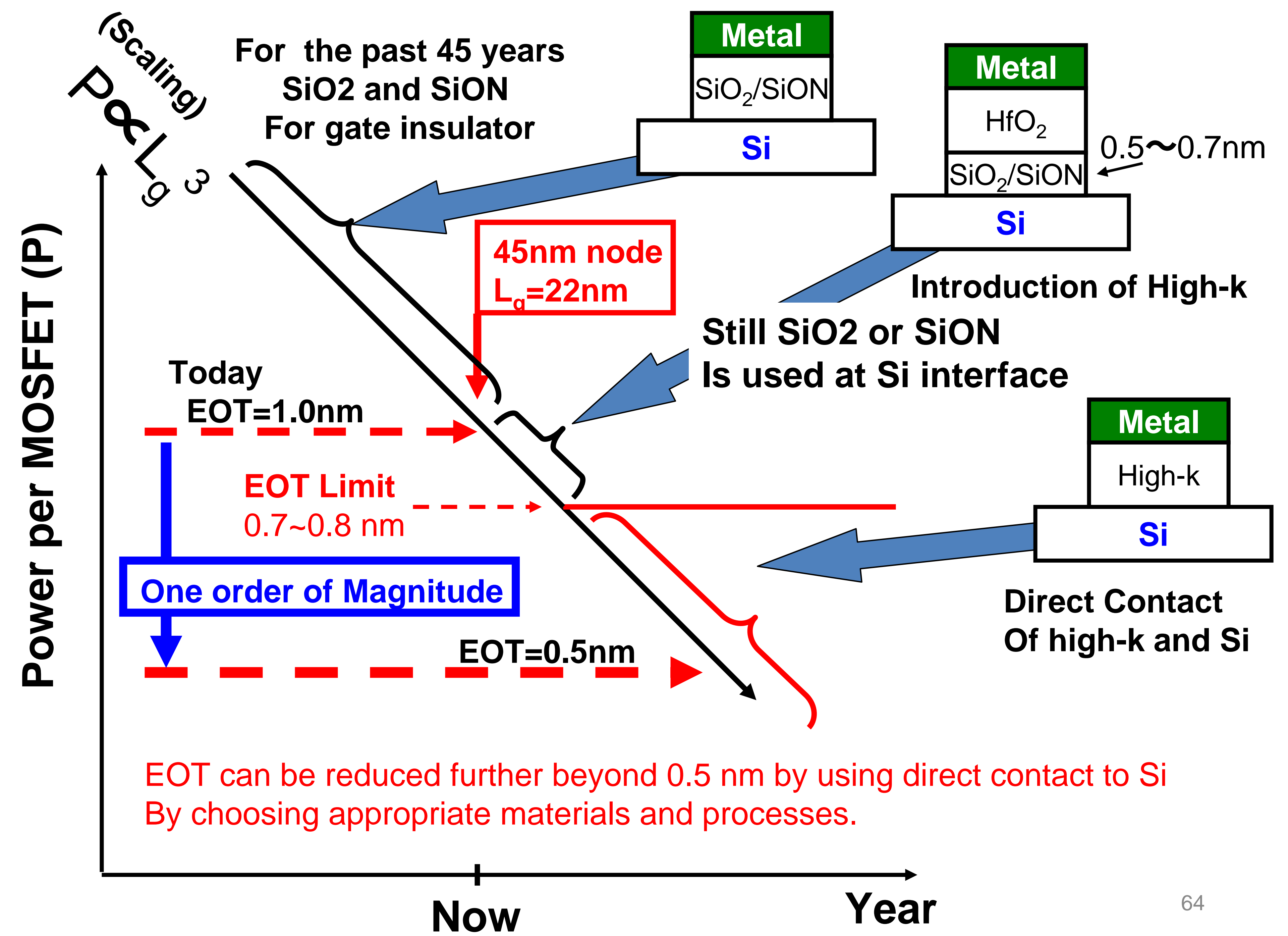
$C, V \propto L$ C: Capacitance V: Voltage

Switching speed CV/I → Decrease

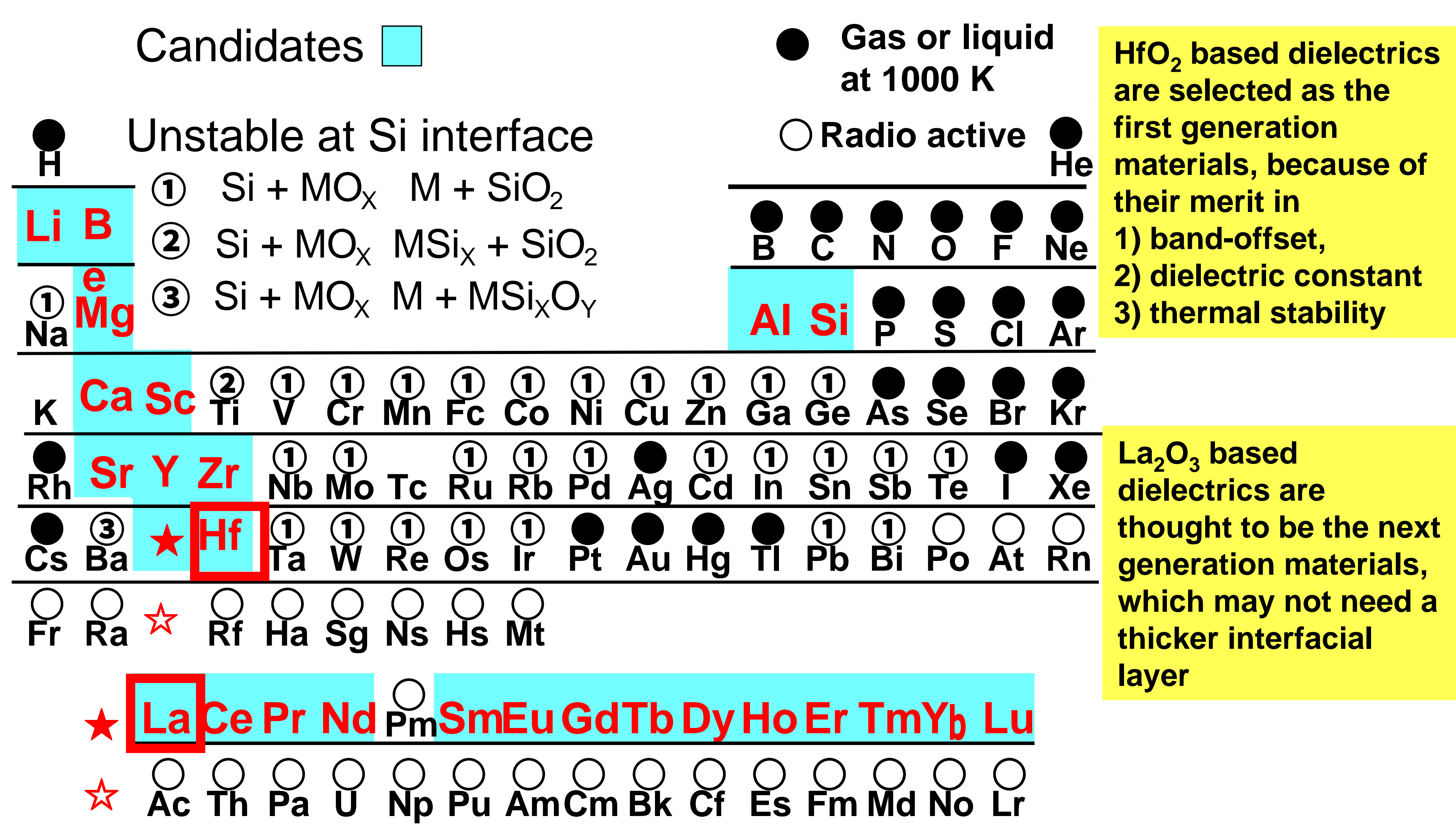
Power consumption $CV^2/2$ → Decrease

Integration density: $1/L^2$ → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm


(Scaling)
P ∝ Lg 3
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
0.5〜0.7nm
SiO2/SiON
Si
45nm node
Lg=22nm
Introduction of High-k
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
Metal
High-k
Si
EOT Limit
0.7~0.8 nm
One order of Magnitude
Direct Contact
Of high-k and Si
EOT=0.5nm
Power per MOSFET (P)
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.
Now
Year

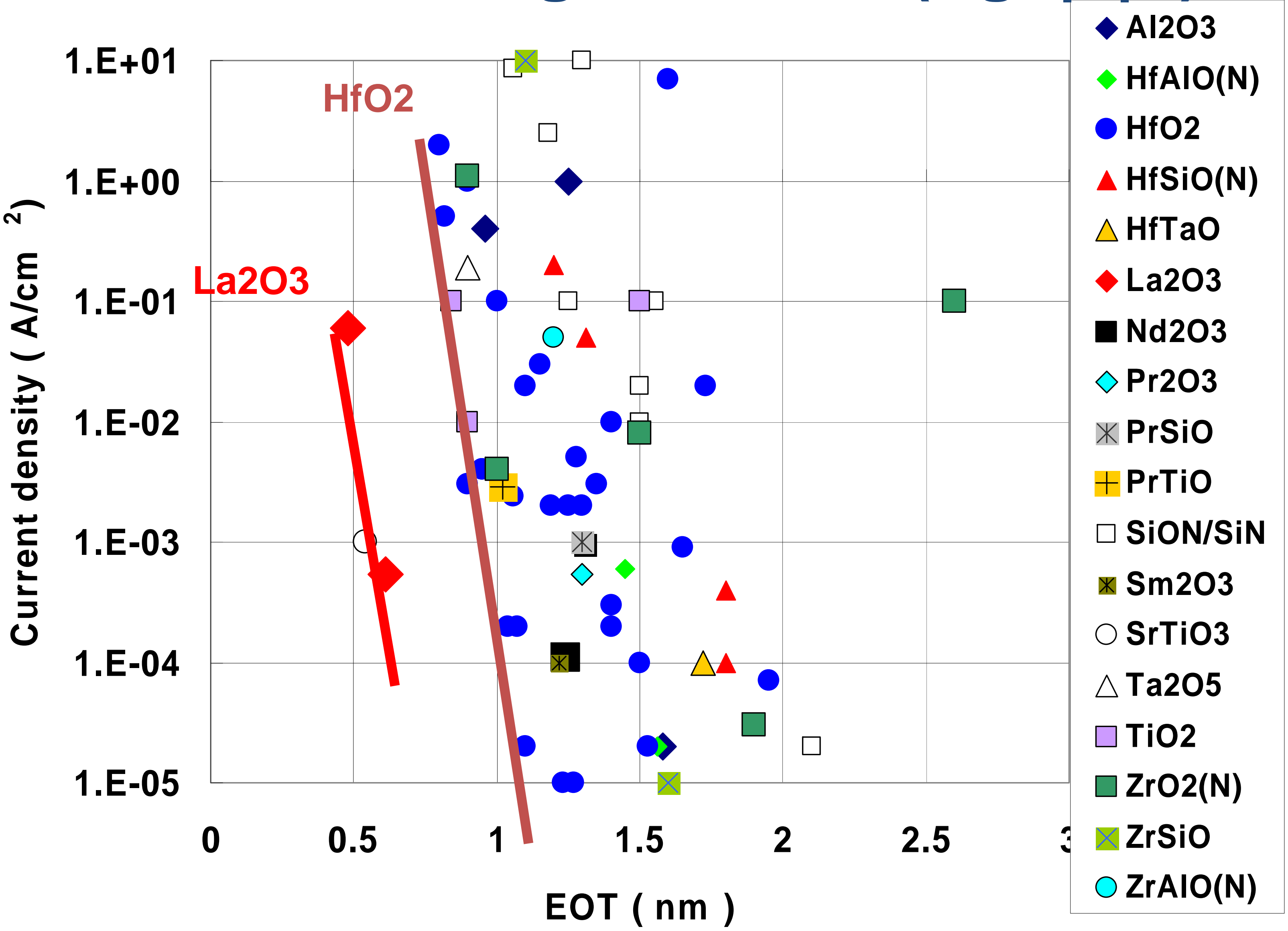
Choice of High-k elements for oxide



R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

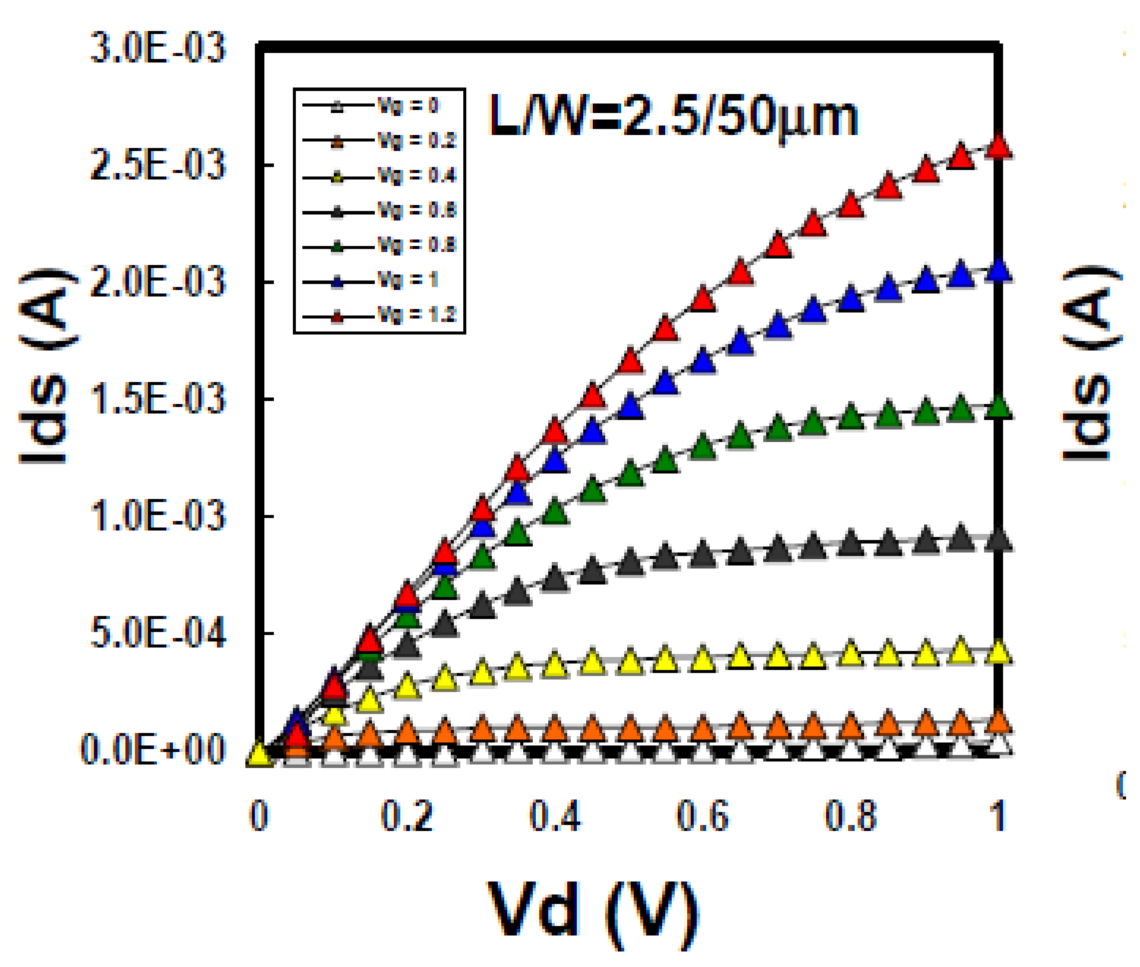
Gate Leakage vs EOT, (Vg=|1|V)



EOT = 0.48 nm

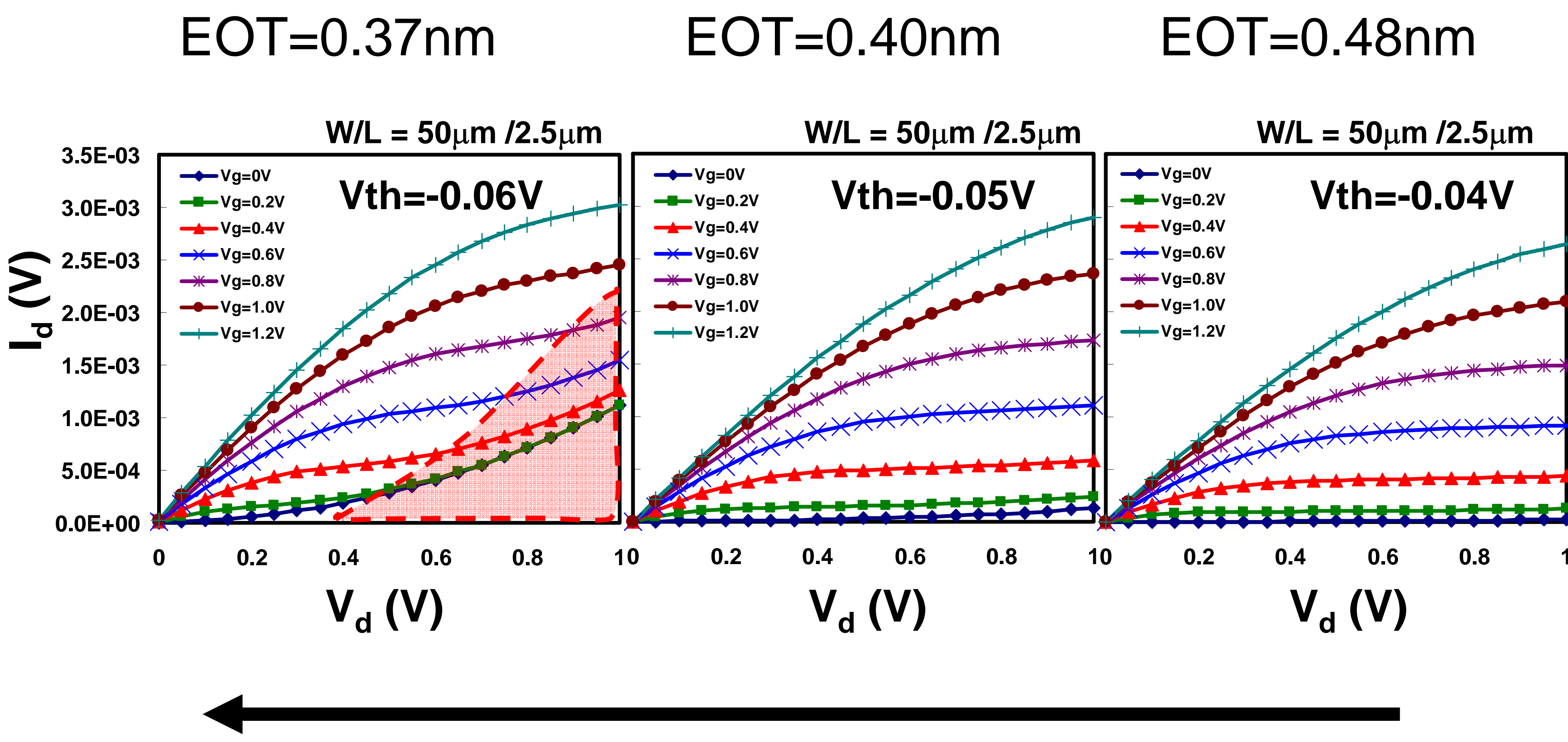
Our results

Transistor with La_2O_3 gate insulator



EOT=0.37nm

La2O3



0.48 →0.37nm Increase of Id at 30%

New material research will give us many future possibilities and the most important for Nano-CMOS!

Not only for high-k!

New material for Metal gate electrode

New material for High-k gate dielectric

New channel material

New material For Metal S/D

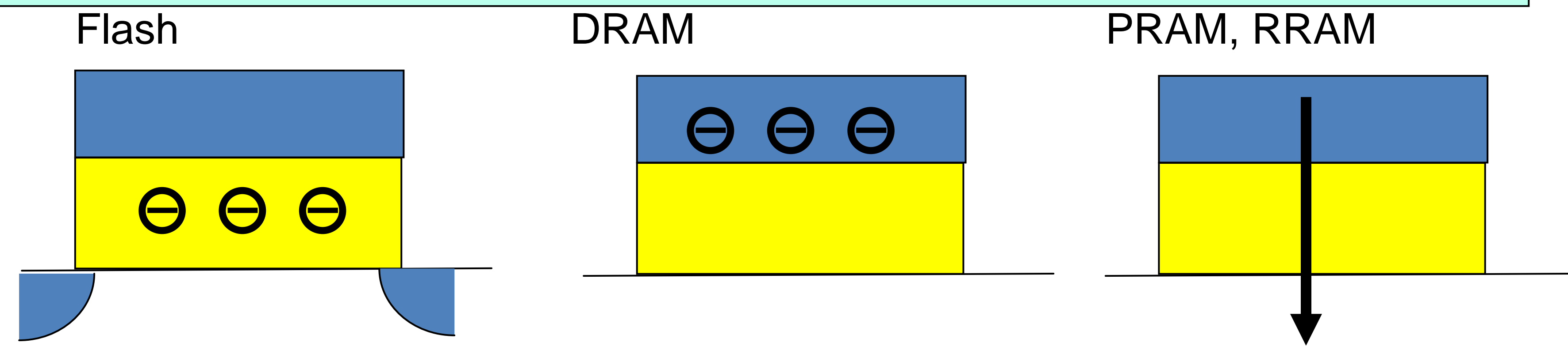
New materials are important for Not only nano-CMOS logic MOSFETs, But also for new memories!

Limit of high-density memories, such as flash, DRAM will be solved by new materials.

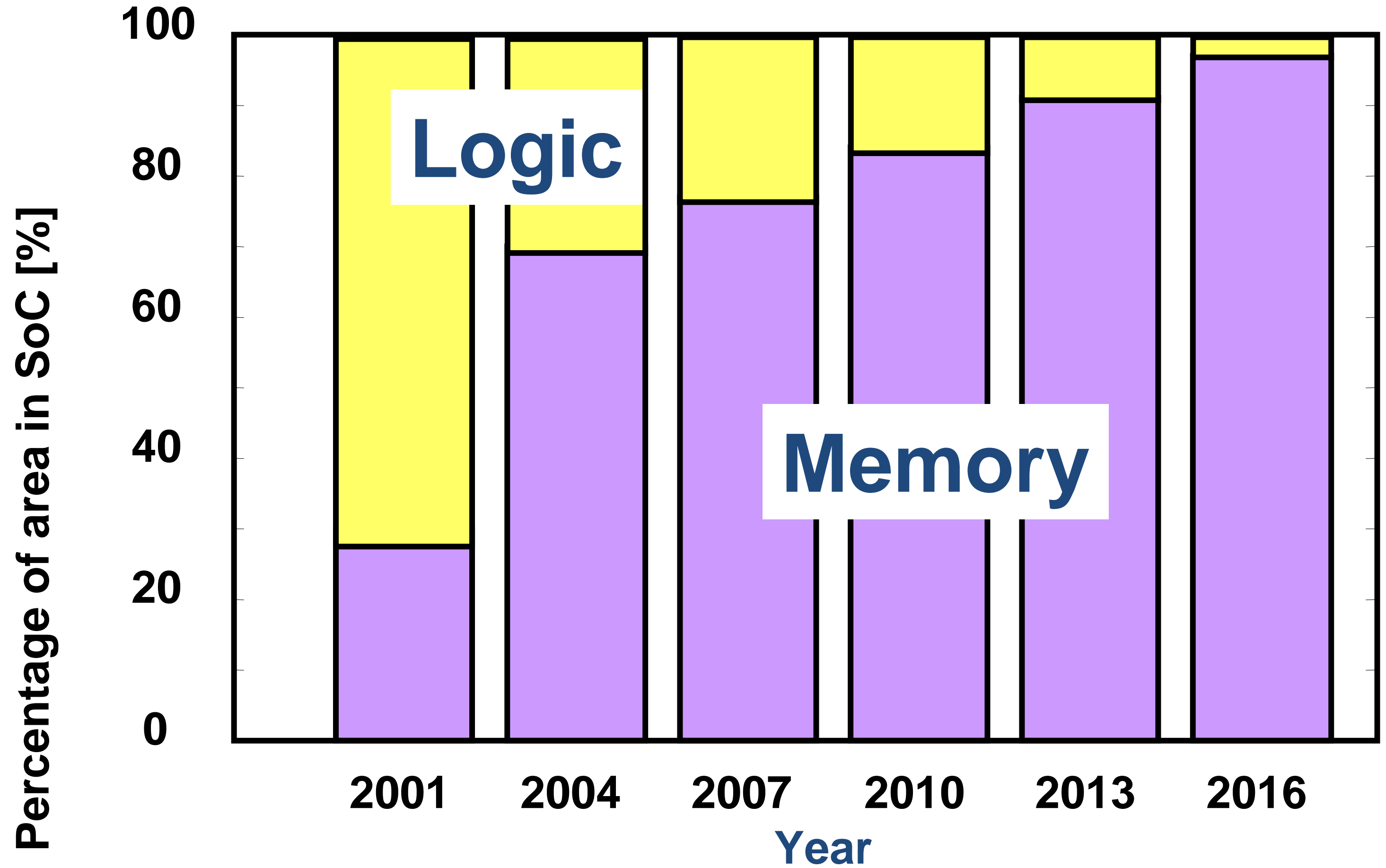
Flash: floating gate → gate insulator charge trap like SONOS, MNOS

DRAM → New high-k insulator

New memory → PRAM, RRAM



Memory area will increase

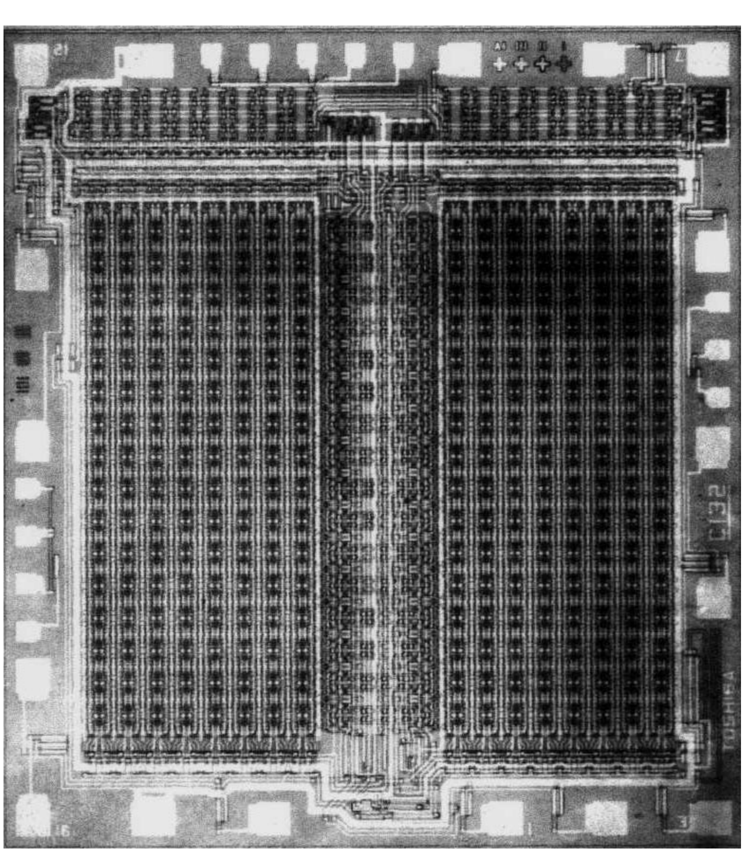


Due to design productivity, yield, and power

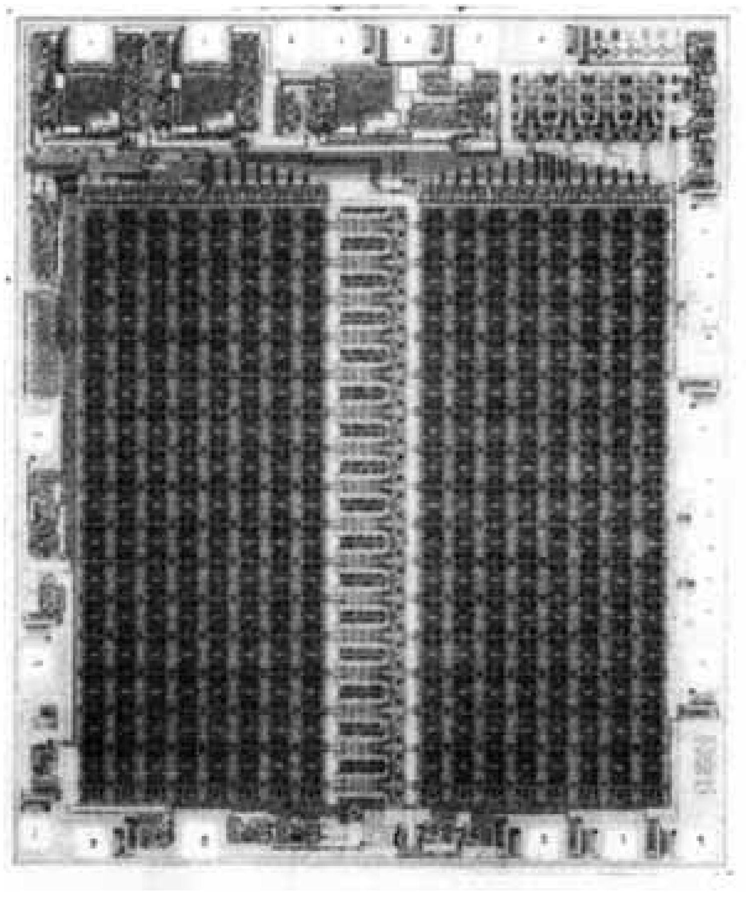
ITRS' 2000: Y, Nishi, Si Nano Workshop, 2006

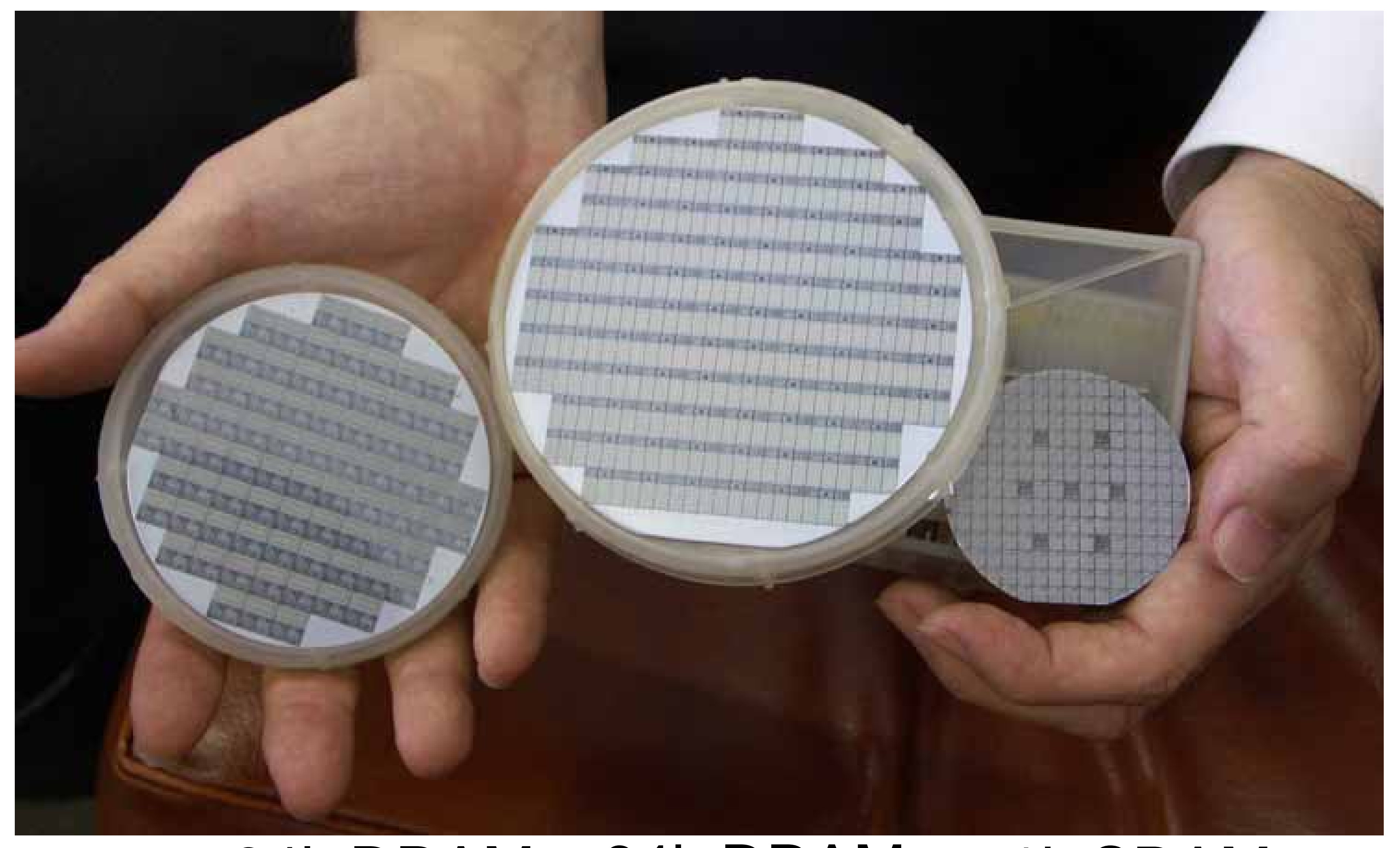
1970s: 10 years after single MOSFETs,

PMOS 1kbit DRAM Toshiba(1974)



NMOS 1k bit SRAM Toshiba (1974)





64k DRAM
3 inch
wafer

64k DRAM
4 inch wafer
1980

1k SRAM
2 inch wafer
1974

1970's

Toshiba Corporation

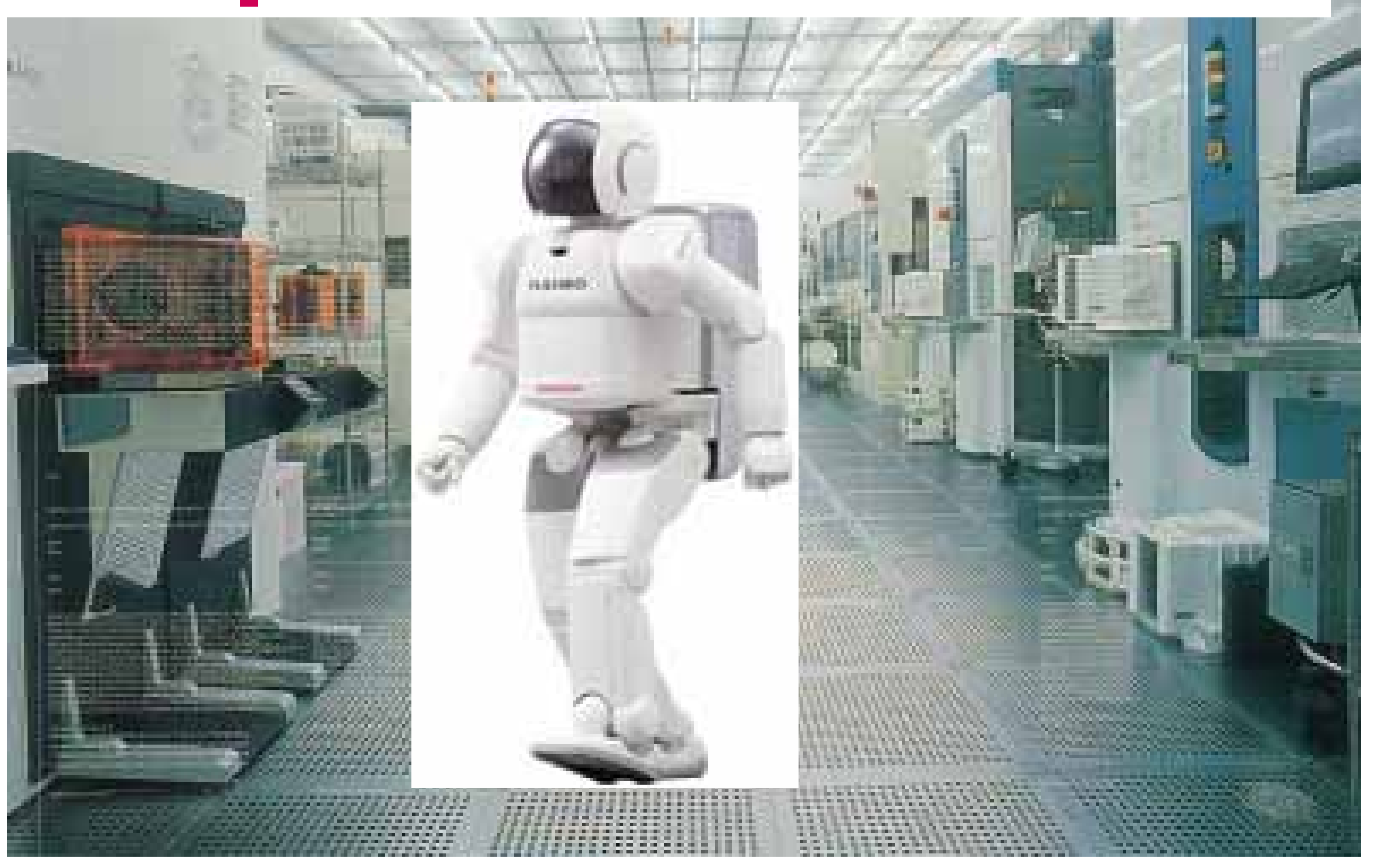
300 mm Fab TSMC

Now

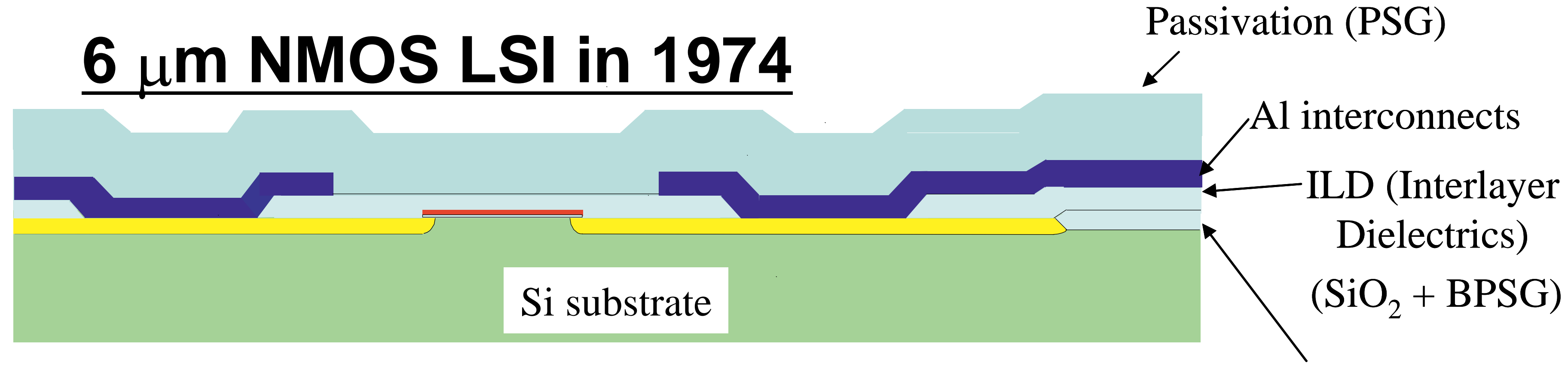
Toshiba Oita Works

300 mm Super clean room in Tsukuba,Selete

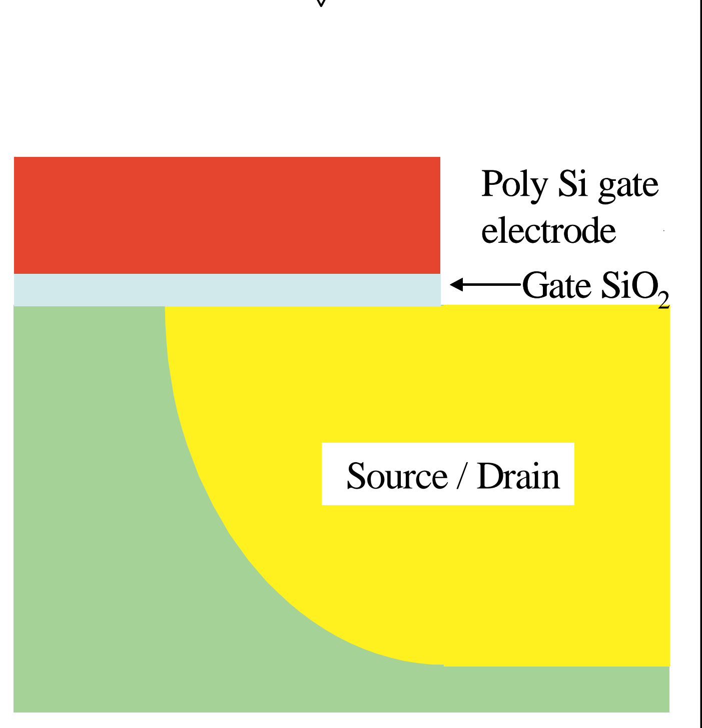
In a future
No person is necessary!



6 μm NMOS LSI in 1974



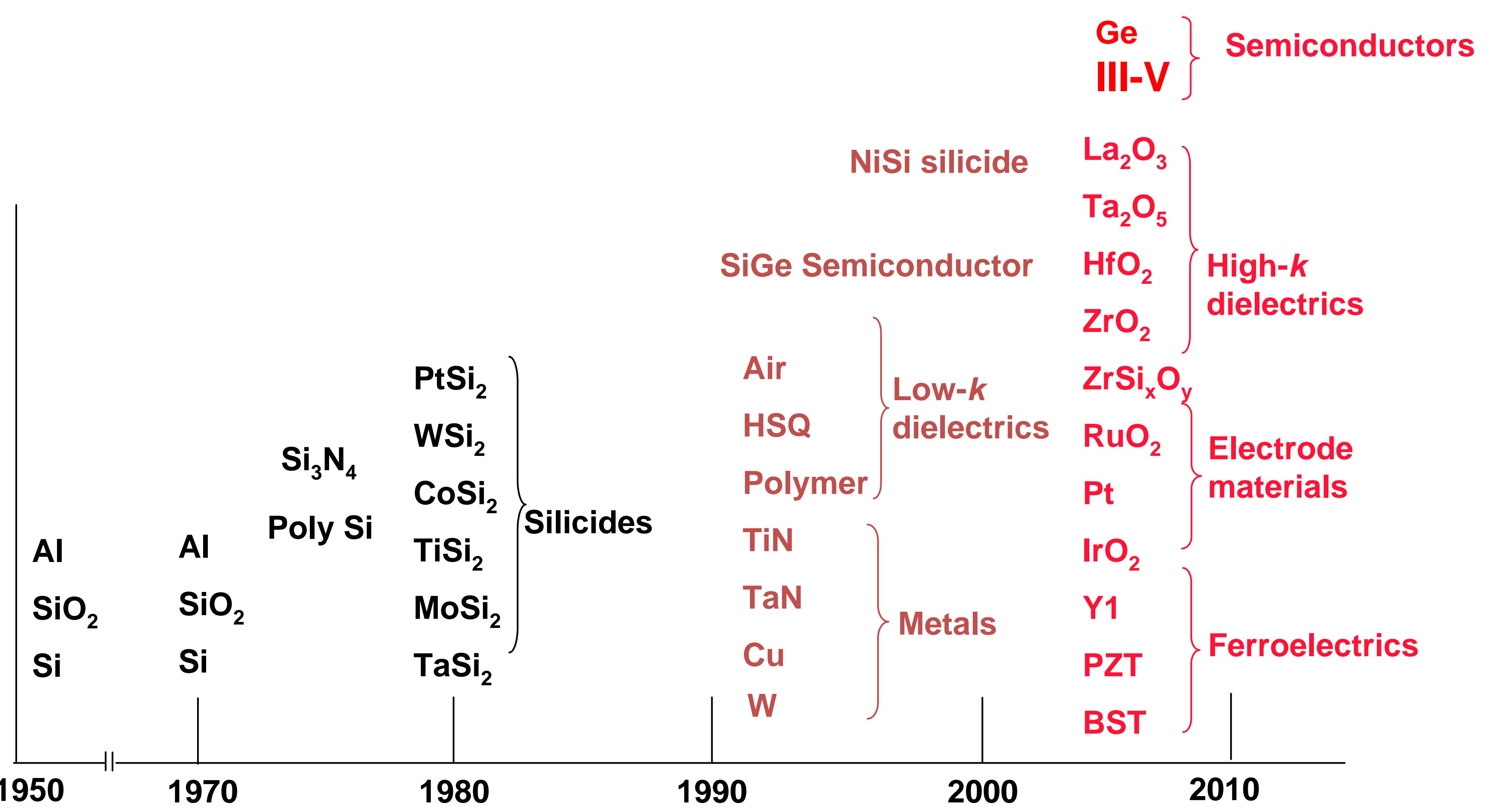
magnification



Layers	Materials	Atoms
1. Si substrate	1. Si	**1. Si**
2. Field oxide	2. SiO_2	**2. O**
3. Gate oxide	3. BPSG	**3. P**
4. Poly Si	4. Al	**4. B**
5. S/D	5. PSG	**5. Al**
6. Interlayer		**(H, N, Cl)**
7. Aluminum		
8. Passivation		

New materials

Just examples!
Many other candidates

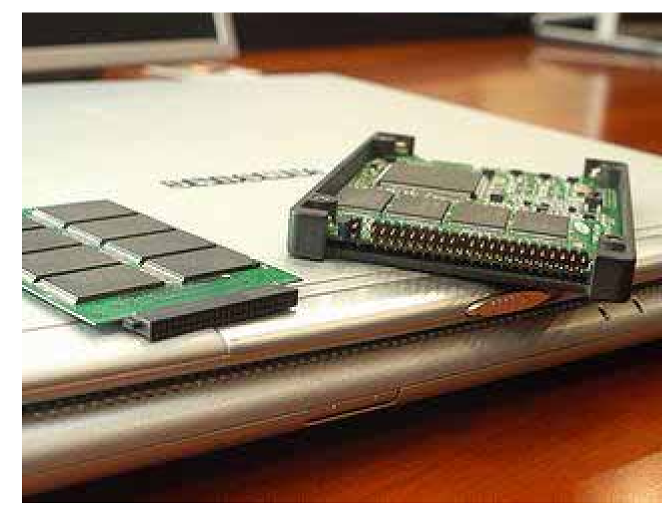


Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Now: After 45 Years from the 1st single MOSFE

32 Gb and 16Gb NAND, SAMSUNG



Samsung's NAND flash trend

Capacity	Node	1st Fabrication	Production
512Mbit	120nm	2000	2001
1Gbit	100nm	2001	2002
2Gbit	90nm	2002	2003
4Gbit	70nm	2003	2004
8Gbit	60nm	2004	2005
16Gbit	50nm	2005	2006
32Gbit	**40nm**		
256Gbit	**20nm**		

Even Tbit would be possible in future!

Already 32 Gbit:

larger than that of world population

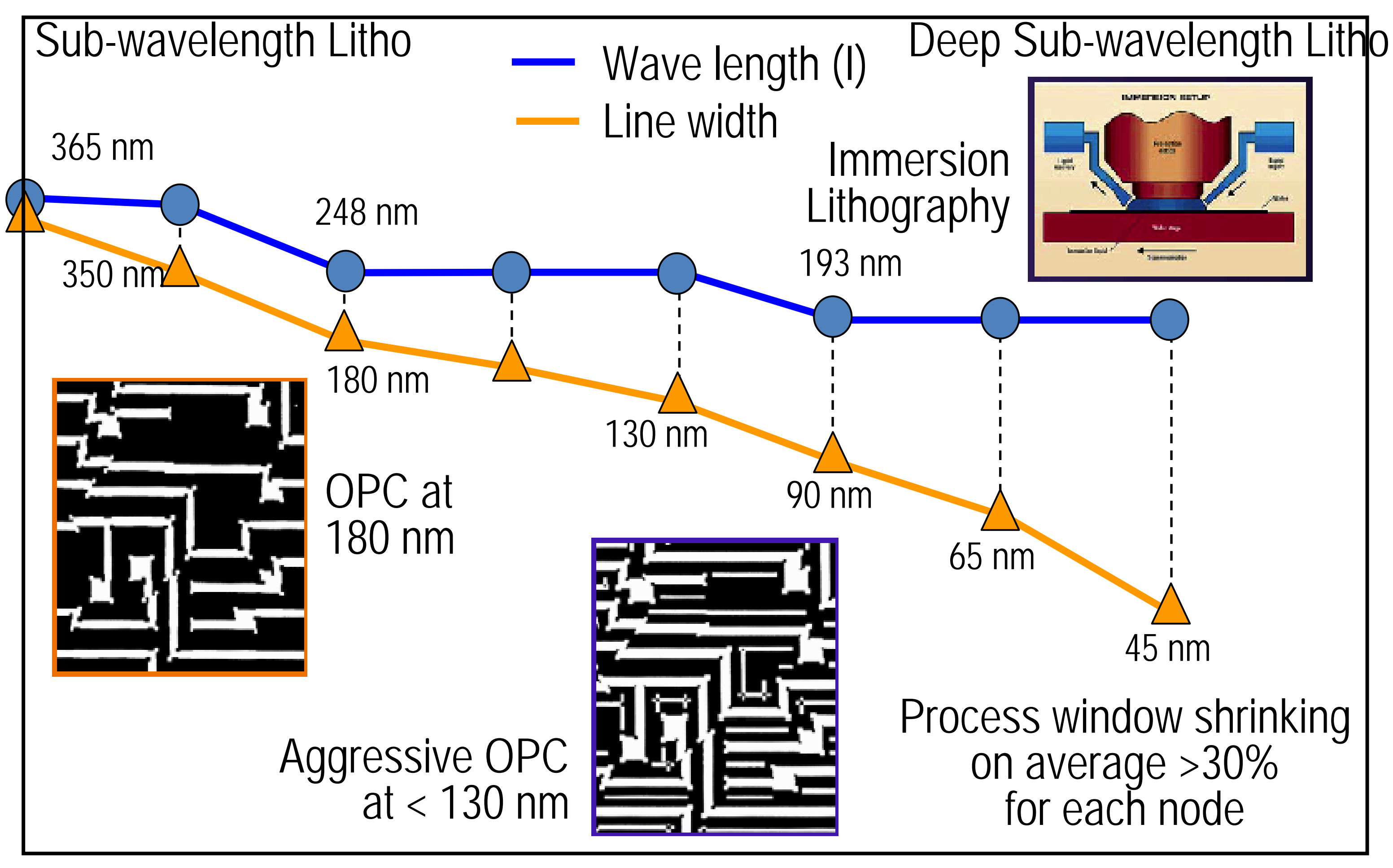
comparable for the numbers of neurons in human brain

Samsung announced 256 Gbit will be produced in 2010.

Only 4 years from now.

256Gbit: larger than those of # of stars in galaxies

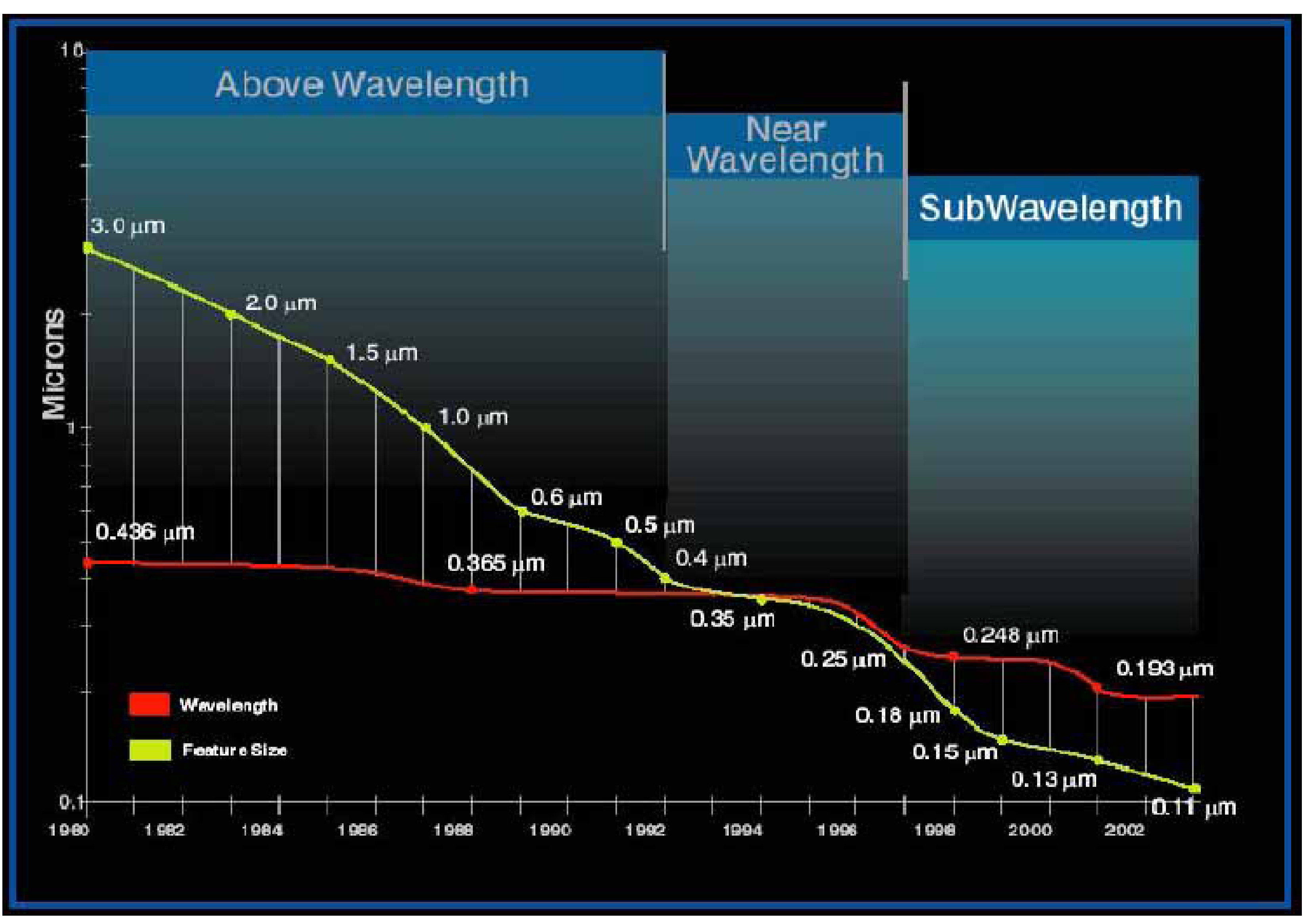
Example: Immersion lithography, plasma doping, laser annealing etc.



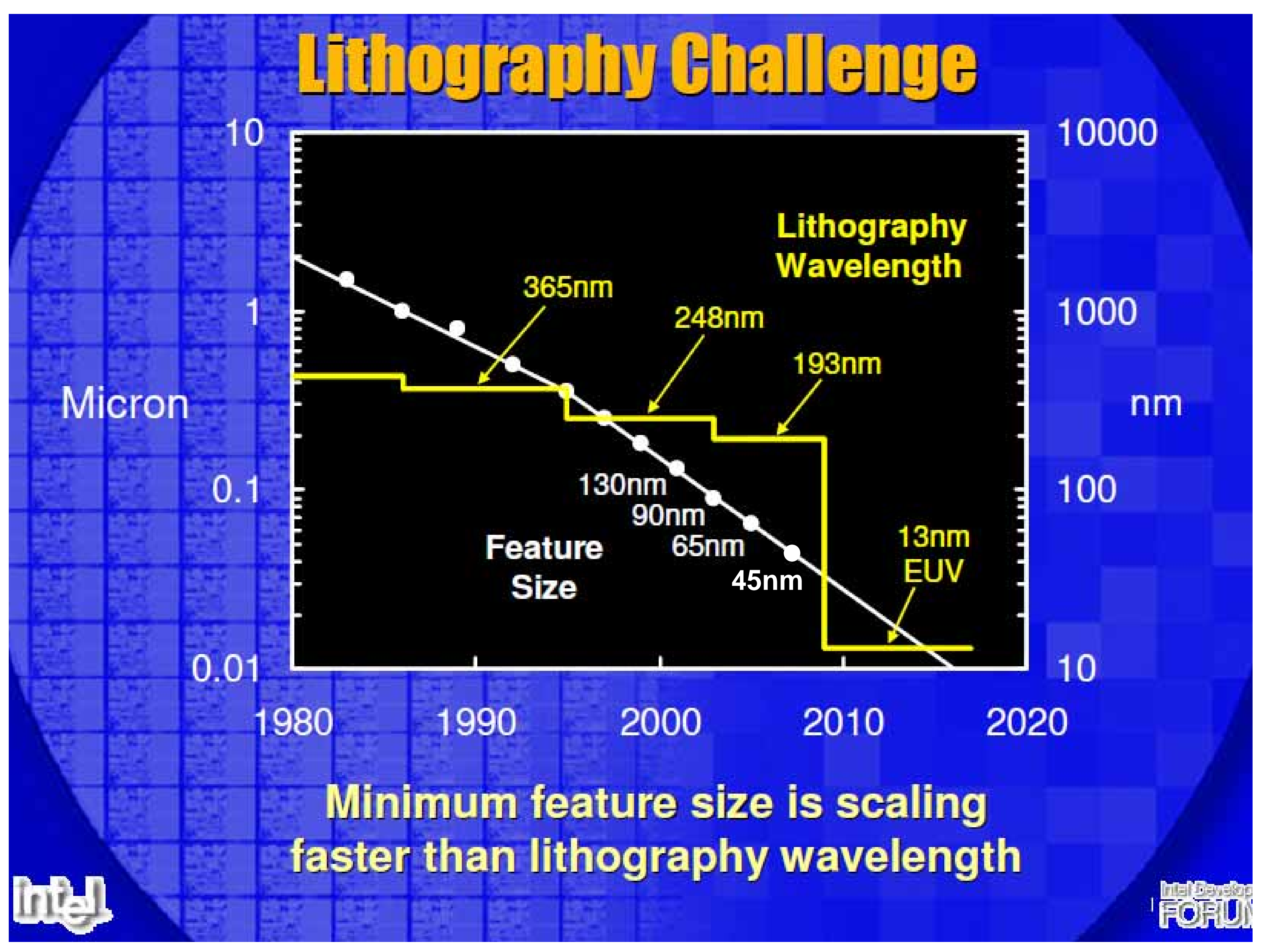
PROCESS CONTROL: THE INVESTMENT THAT YIELDS

Ref:KLA Tencor

Sub-Wavelength Scaling



Source: Numerical Technologies


Lithography Challenge
10
1
0.1
0.01
10000
1000
100
10
Micron
nm
Lithography
Wavelength
365nm
248nm
193nm
130nm
90nm
65nm
45nm
Feature
Size
13nm
EUV
1980
1990
2000
2010
2020
Minimum feature size is scaling
faster than lithography wavelength
intel
Intel Developer
FORUM

Light path in an EUV exposure tool

Reflective Mask

Collector Optics

Reflective Projection / Reduction Optics

EUV Light Source

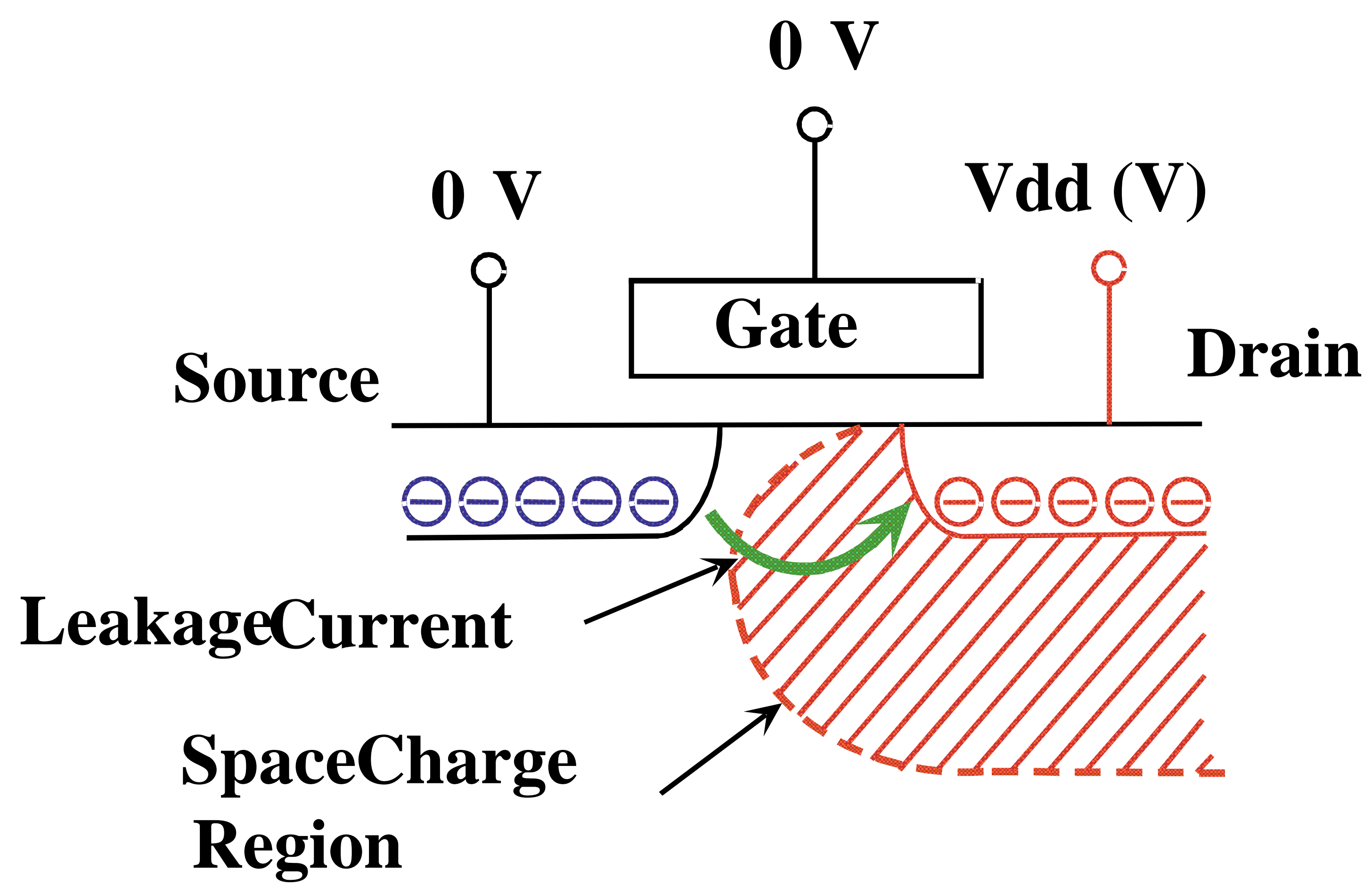
Condenser / Illuminator

Resist

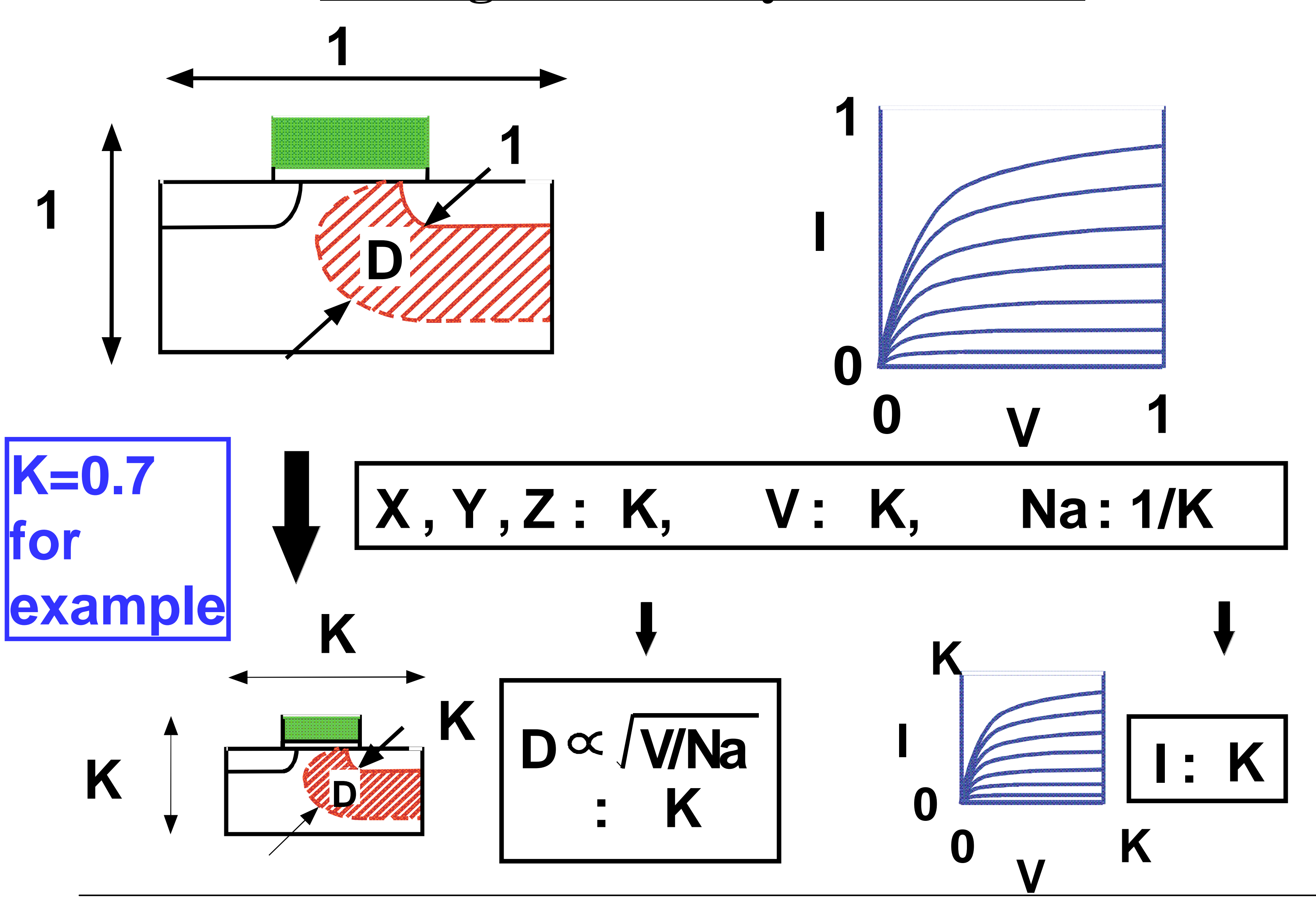
Wafer

intel

Short-channel effect at downsizing



Scaling Method: by R. Dennard



R. Dennard et al. , IEEE J. Solid State Circuits, vol.9. P.256, 1974

Downscaling merit

Geometry & Supply voltage	L_g, W_g T_{ox}, V_d	K	Scaling K : K=0.7 for example
Drive current in saturation	I_d	K	$I_d = v_{sat} W_g C_o (V_g - V_{th})$ C_o: gate C per unit area $\rightarrow W_g (t_{ox}^{-1})(V_g - V_{th}) = W_g t_{ox}^{-1} (V_g - V_{th}) = K K^{-1} K = K$
I_d per unit W_g	$I_d/\mu m$	1	I_d per unit $W_g = I_d / W_g = 1$
Gate capacitance	C_g	K	$C_g = \varepsilon_o \varepsilon_{ox} L_g W_g / t_{ox}$ $\rightarrow$ KK/K = K
Switching speed	τ	K	$\tau = C_g V_d / I_d$ $\rightarrow$ KK/K= K
Clock frequency	f	1/K	$f = 1/\tau = 1/K$
Chip area	A_{chip}	α	Scaling α
Integration (# of Tr)	N	α/K^2	N $\rightarrow$ α/K^2 1/K2 when $\alpha=1$
Power per chip	P	α	$fNCV^2/2 \rightarrow K^{-1}(\alpha K^{-2}) K (K^1)^2 = \alpha$ 1 when $\alpha=1$

What will be real Downscaling ?

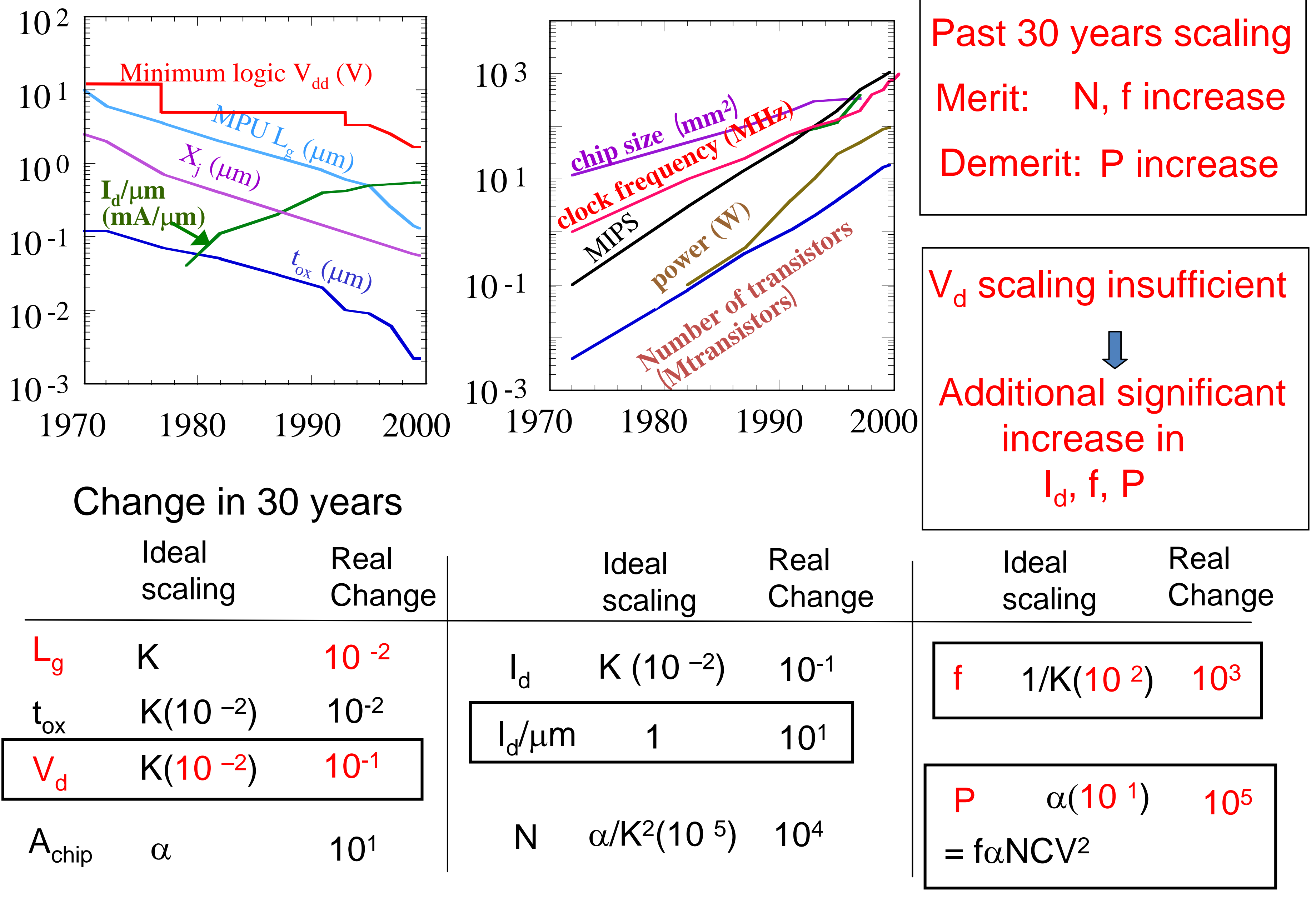
Is K the same for all the parameters?

L_g, W_g, t_{ox}, V_d $\longrightarrow$ K? $A_{chip} \longrightarrow \alpha$?

$I_d \longrightarrow$ K? $I_d/\mu m \longrightarrow$ 1? $f \longrightarrow 1/K$?

$C_g \longrightarrow$ K? $\tau \longrightarrow$ K? $N \longrightarrow \alpha/K^2$? $P \longrightarrow \alpha$?

Past downscaling trend



Change in 30 years

	Ideal scaling	Real Change
L_g	K	10^{-2}
t_{ox}	$K(10^{-2})$	10^{-2}
V_d	$K(10^{-2})$	10^{-1}
A_{chip}	α	10^{1}

	Ideal scaling	Real Change
I_d	$K(10^{-2})$	10^{-1}
$I_d/\mu m$	1	10^{1}
N	$\alpha/K^2(10^{5})$	10^{4}

	Ideal scaling	Real Change
f	$1/K(10^{2})$	10^{3}
P $= f\alpha NCV^2$	$\alpha(10^{1})$	10^{5}

Microprocessors Trend expected in 2001

Power Increase

Heat generation increase

Past: 1972 (Intel)	Today: 2002 (Intel)	2008 (Intel)
Lg 10,000 nm	Lg sub-70 nm	Lg sub-25 nm
Tox 1200 nm	Tox 1.4 nm	Tox 0.7 nm
f 0.00075 GHz	f 2.53 GHz	f 30 GHz
P a few 100 mW	P several 10 W	P 10 kW
N 2.25k	N 50 M	N 1.8B
		MIPS 1M MIPS (TIPS)

Cause

Tr. Number increase

Clock Frequency increase

↓

Solution:

Low supply Voltage

Heat Generation

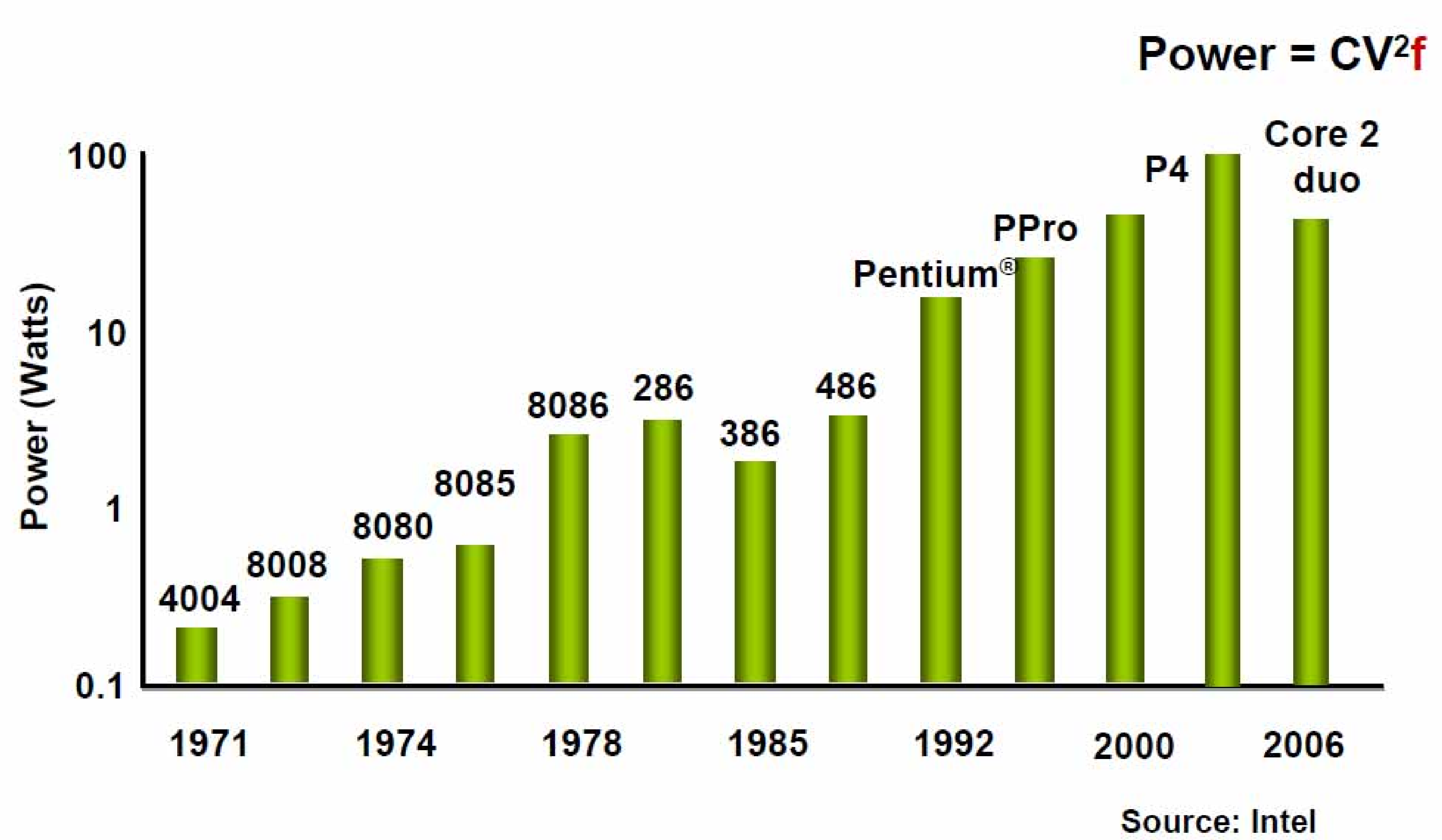
2002 10W/cm² Hot Plate

2006 100W/cm² Surface of Nuclear Reactor

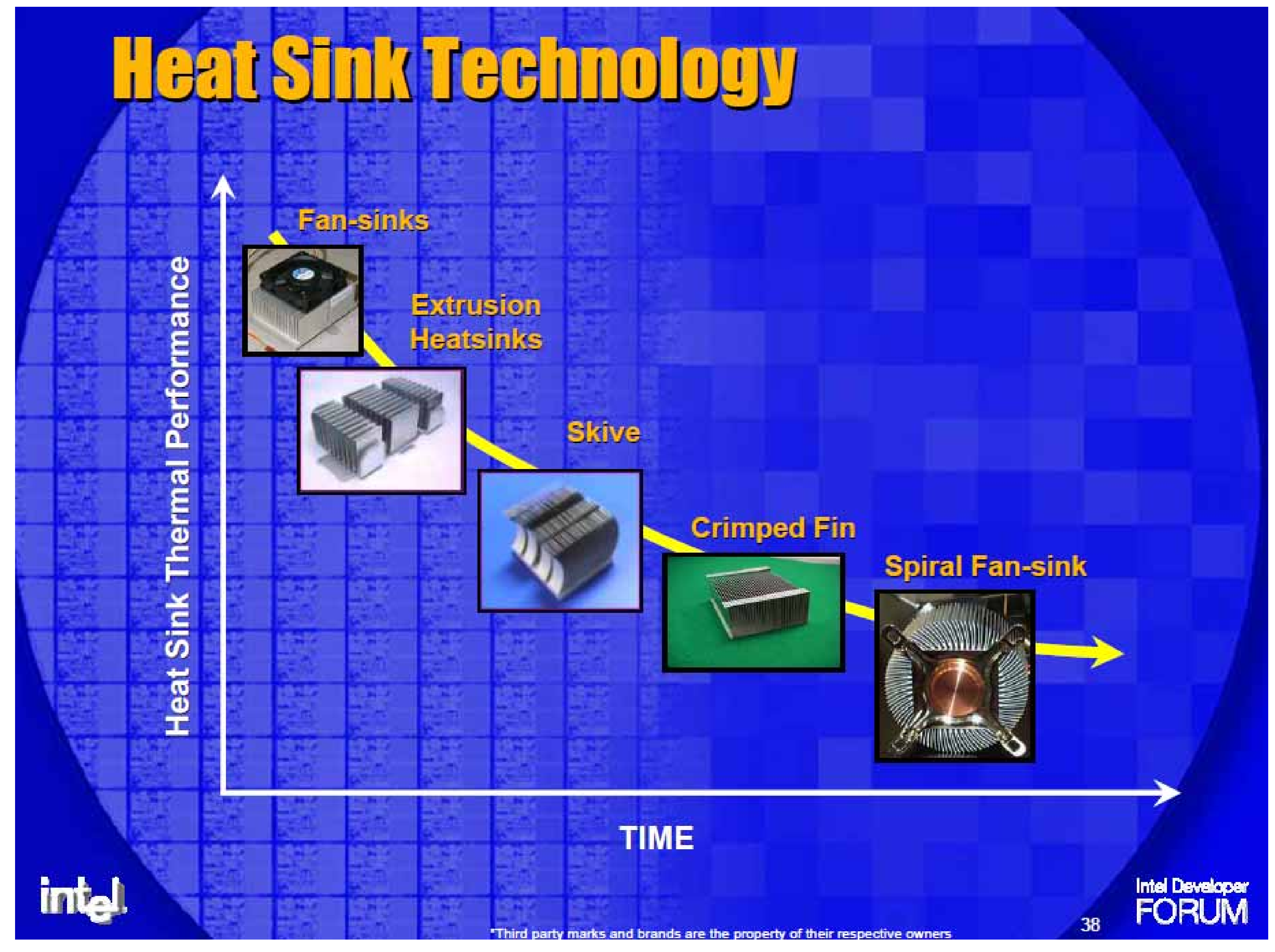
2010 1000W/cm² Rocket Nozzle

2016 10000W/cm² Sun Surface

P. P. Gelsinger, "Microprocessor for the New Millennium: Challenges, Opportunities, and New Frontiers," Dig. Tech. 2001 ISSCC, San Francisco, pp.22-23, February, 2001

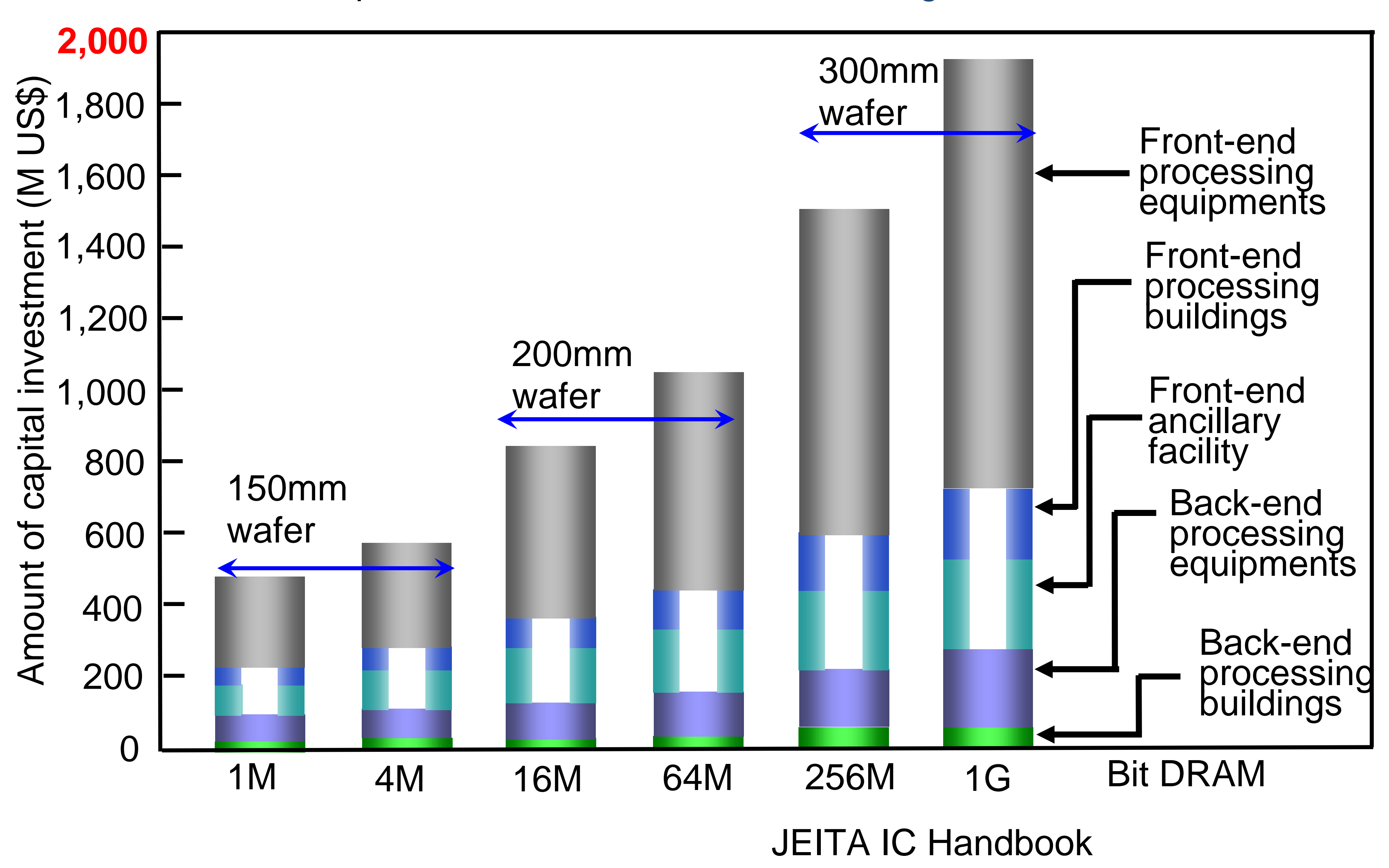


Paul Packan, Intel Corporation, IEDM Short Course 2007


Heat Sink Technology
Fan-sinks
Extrusion
Heatsinks
Skive
Crimped Fin
Spiral Fan-sink
Heat Sink Thermal Performance
TIME
intel
Intel Developer
FORUM
38
*Third party marks and brands are the property of their respective owners

Problem is the huge production cost and investme

Amount of capital investment on Each of DRAM generation



Examples of foundry facility: UMC

Fab 12A (Tainan, Taiwan)

- US$3 billion investment
- Production since 2001
- 38K wafers/month by E/06
- 90, 65nm in production

Fab 12i (Singapore)

- US$3.6 billion investment
- Production since 2004
- 25K wafers/month by E/06
- 130, 90nm in production
- Ready for 65nm pilot

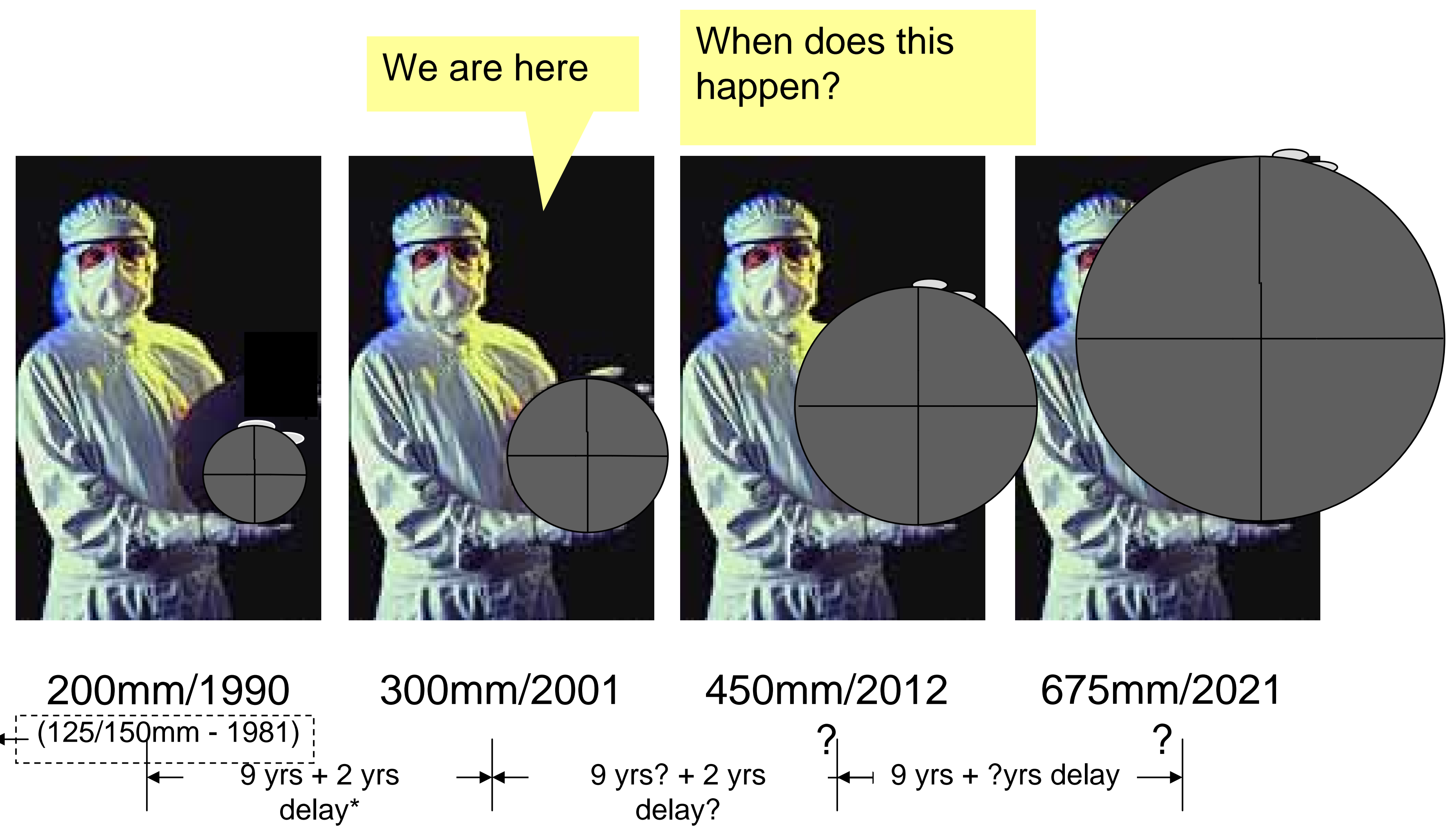
UMC

Volume production with lager wafer is a soluti

IC Fab Utility Usage : 12” vs. 8”

	12"-Fab	8"-Fab	12"/8" Usage ration	12"/8" Wafer size ratio
Power	1,100 KWH/Wafer	660 KWH/Wafer	1.7	2.25
Water	6.1 M3/Wafer	4.7 M3/Wafer	1.3	
Waste Water	3.8 M3/Wafer	2.9 M3/Wafer	1.3	
Waste Air	20,000 CMH/Wafer	13,000 CMH/Wafer	1.5	

When do we start planning for next wafer size transition?



Crystal pulling furnace becomes too huge
Si crystal height cannot be very long because of its weigh

Furnace

- Height: 12 m
- Weight: 36 ton
- Hot zone: 40 inch
- Cusp-type super conductive magnet

Crystal

- Diameter: 400 mm
- Weight: over 400 kg
- Body length: over 1m

Provided by Super Silicon Crystal Research Institute Corp.(SSi)

How about the integration of such small-geometry MOSFETs in a chip?

1)Integration of huge number of the ultra-small MOSFETs would consume too huge power and thus, creates too huge heat?

2)Integration of such ultra-small MOSFETs causes too huge variations in the transistor characteristics, which could make the circuit design impossible?

3)There are too many number of transistors in a chip for the circuit designers to manipulate? (design crisis),

4)There would be no merit of transistor downsizing in performance and power, because of RC (resistance capacitance product) of interconnect cannot be reduced aggressively any more?

5)Who will pay the huge development and production costs for the integration of such ultra-small MOSFETs? Note that the prices for the recent process equipments and the lithography mask became extremely high.

These concerns have been argued in the past 15 years at every new generation of the products, like the wolf boy.

Fortunately, the wolf has not come, and the concerns have not come true.

It is expected that we can go with several more generations for the integration.

There will be still a room for squeezing the technologies to obtain the merit of the scaling-down for integration.

The continuous progress of CMOS technologies for
- high-performance
- low power

is very important because of the 3 reasons:

1) Rapid progress of aging population and falling birth rate

1) Global warming

1) Semiconductor industry and world economy

1)Rapid progress of aging population and falling birth rate:

Replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example.

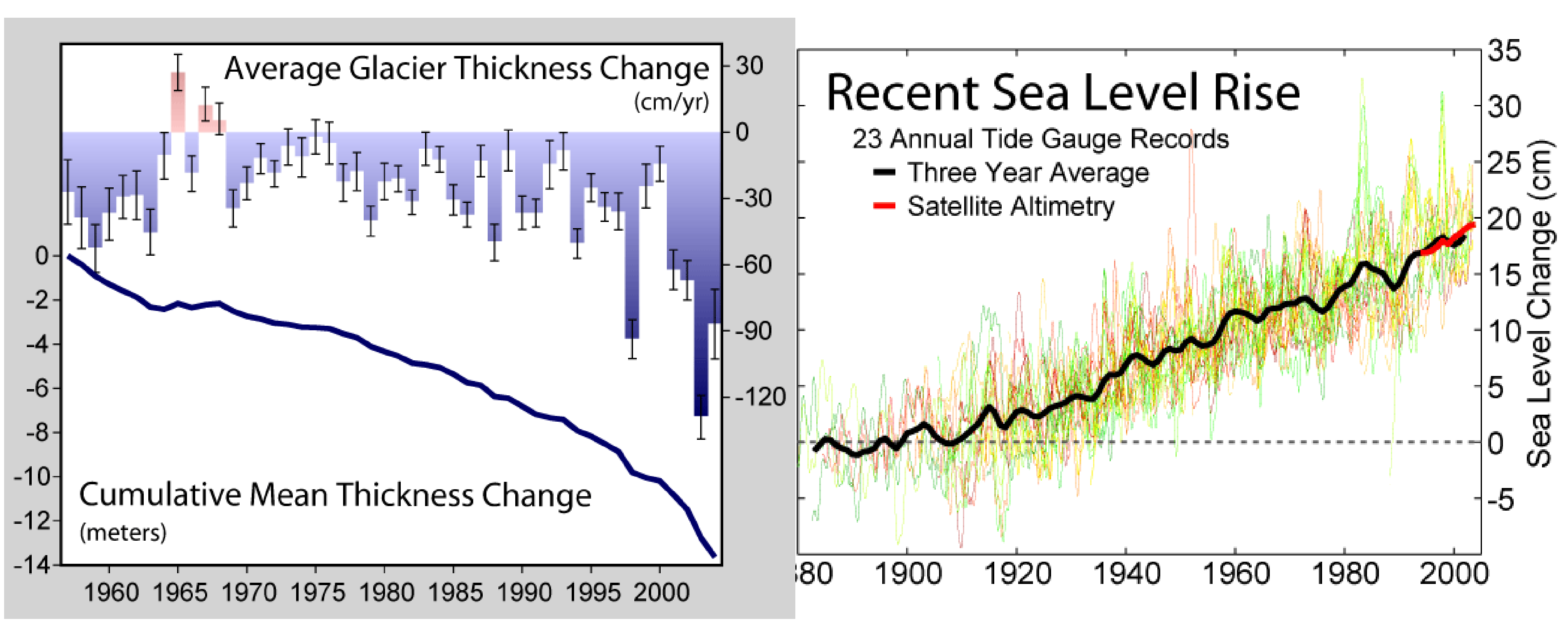
For, the daily family use, much higher intelligence and much lower power consumption than those of today are required.

Robot in 21c cannot made without integrated circuits

Robot (21C)

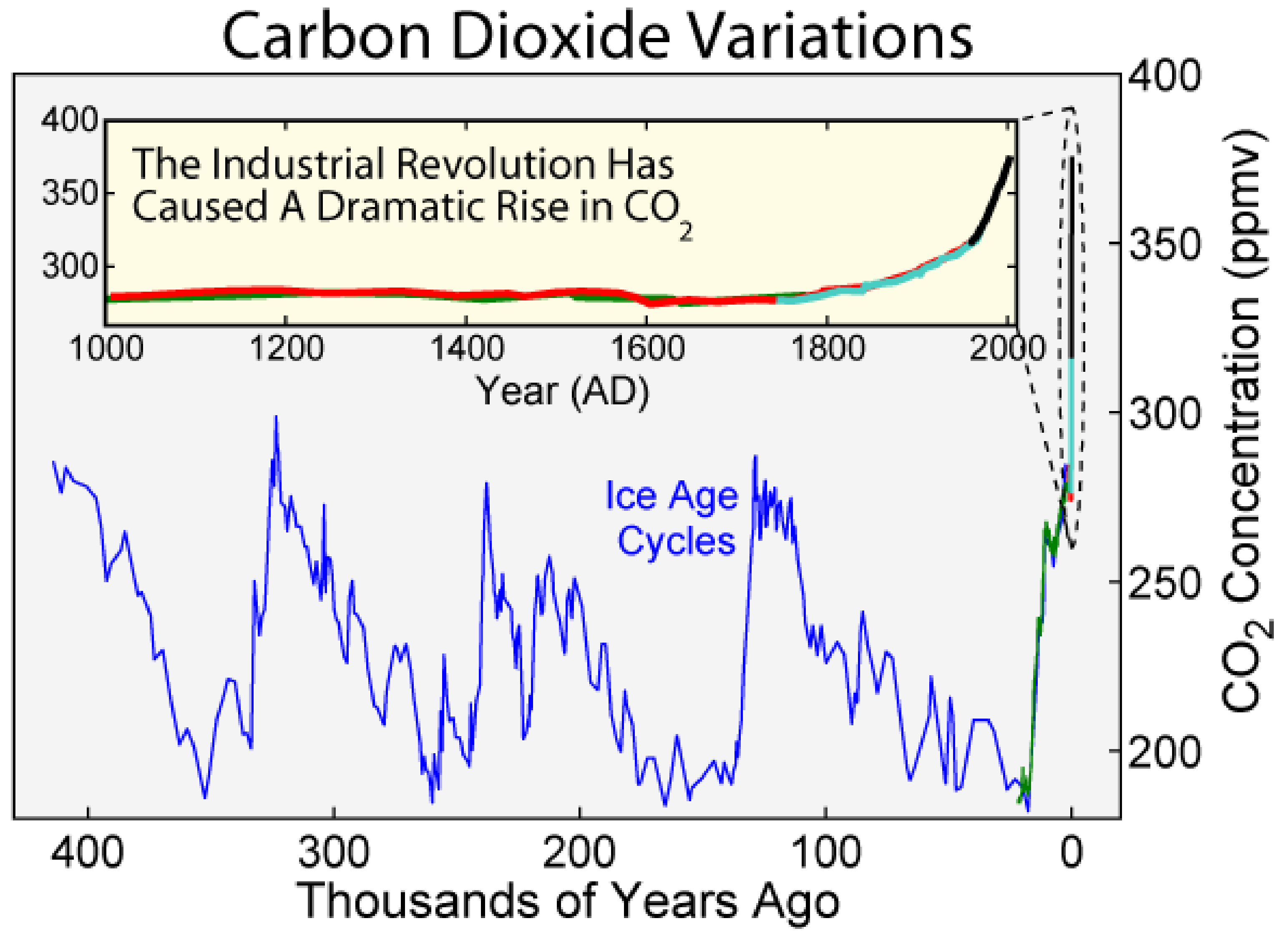
Karakuri (Windup Mechanical) do
(18C) in Japan

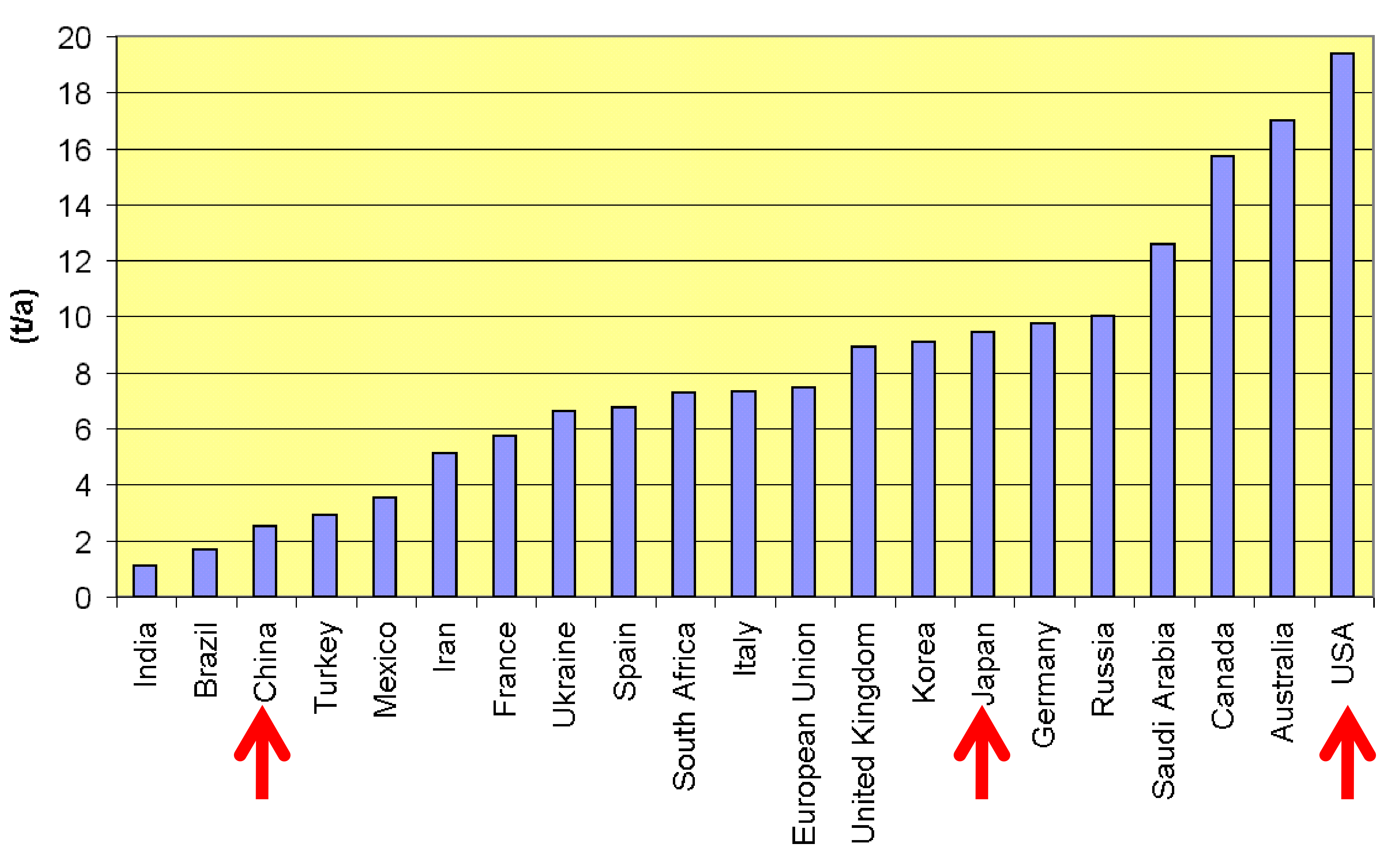
2) Recent Significant Global Warming



We need reduce CO2 generation!

→ Low power technology is urgent request




CO2 Emission per capita 2002
(t/a)
20
18
16
14
12
10
8
6
4
2
0
India
Brazil
China
Turkey
Mexico
Iran
France
Ukraine
Spain
South Africa
Italy
European Union
United Kingdom
Korea
Japan
Germany
Russia
Saudi Arabia
Canada
Australia
USA

3) Semiconductor industry, and world economy

If there is no more downsizing such as
45 → 32 nm Logic, 8 Gbit → 16 Gbit Memory

- LSIs will not be sold well, and semiconductor companies will face a disaster.

- Equipment and martial companies as well.

- There is no more R & D for semiconductors and many people will loose their jobs.

→ World economy crisis!

History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking

C, V $\propto$ L   C: Capacitance V: Voltage

Switching speed CV/I → Decrease

Power consumption $CV^2/2$ → Decrease

Integration density: $1/L^2$ → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm

<u>CMOS downsizing is critically important</u>

<u>However now, many people expect that we will reach limit in 2020.</u>

Totally, new paradigm after reaching
the downsizing limit.

What will be?

After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.

After 2020

4 reasons for no downsizing anymore
or No decrease in gate length

---

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.
   Ballistic ← No scattering of carriers in channel
   Thus, all the carrier from the source reach drain

2. Increase of Off-current (Subthreshold current)

3. No decrease of Gate capacitance by parasitic components

4. Increase in production cost.

After 2020

What will be the world with no gate length reduction?

More Moore and More than Moore

Moore's Law & More

More than Moore: Diversification

Analog/RF
Passives
HV Power
Sensors Actuators
Biochips

More Moore: Miniaturization

Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm
. . .
V

Interacting with people and environment

Non-digital content System-in-package (SiP)

Information Processing

Digital content System-on-chip (SoC)

Combining SoC and SiP: Higher Value Systems

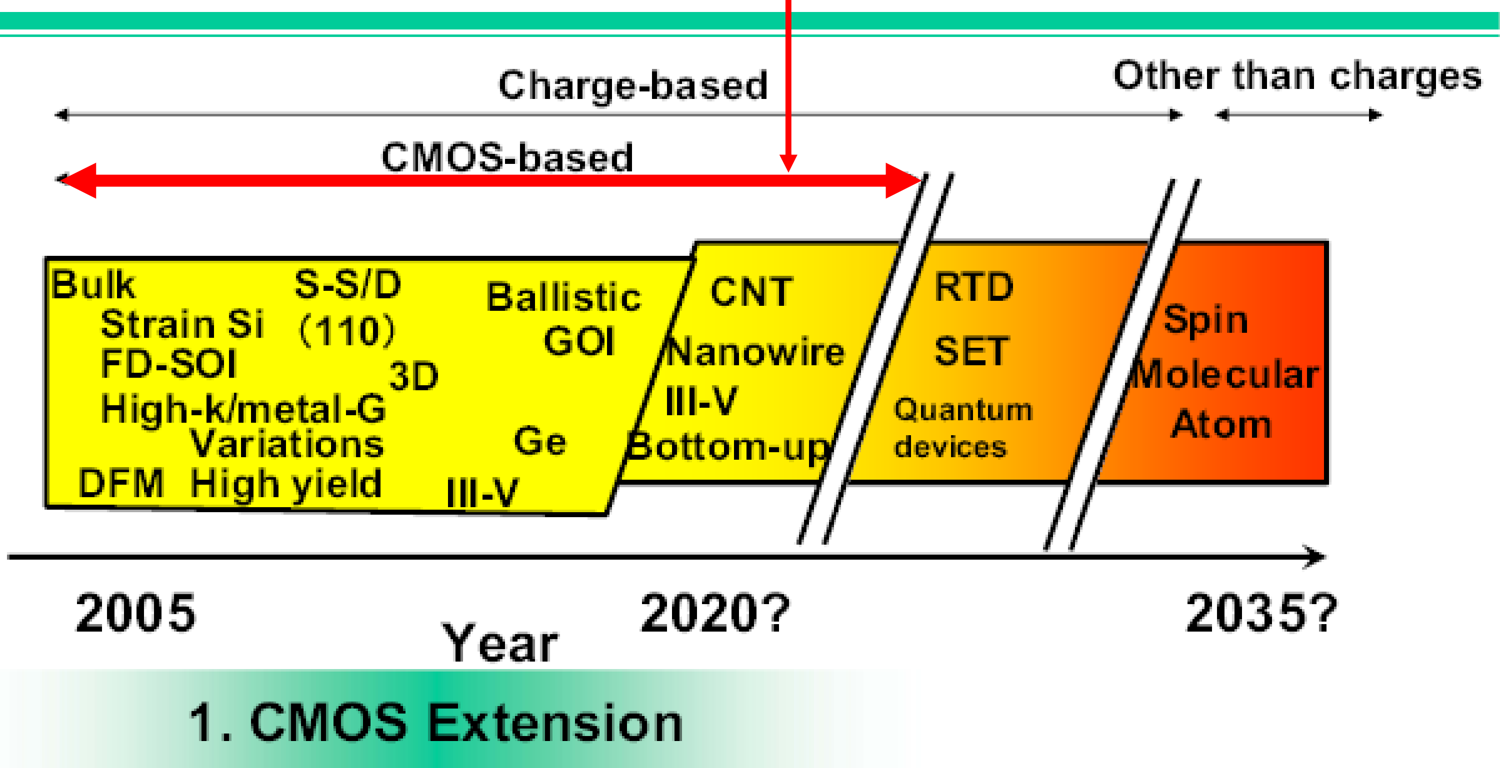
Beyond CMOS

Question what is the other side of the cloud?

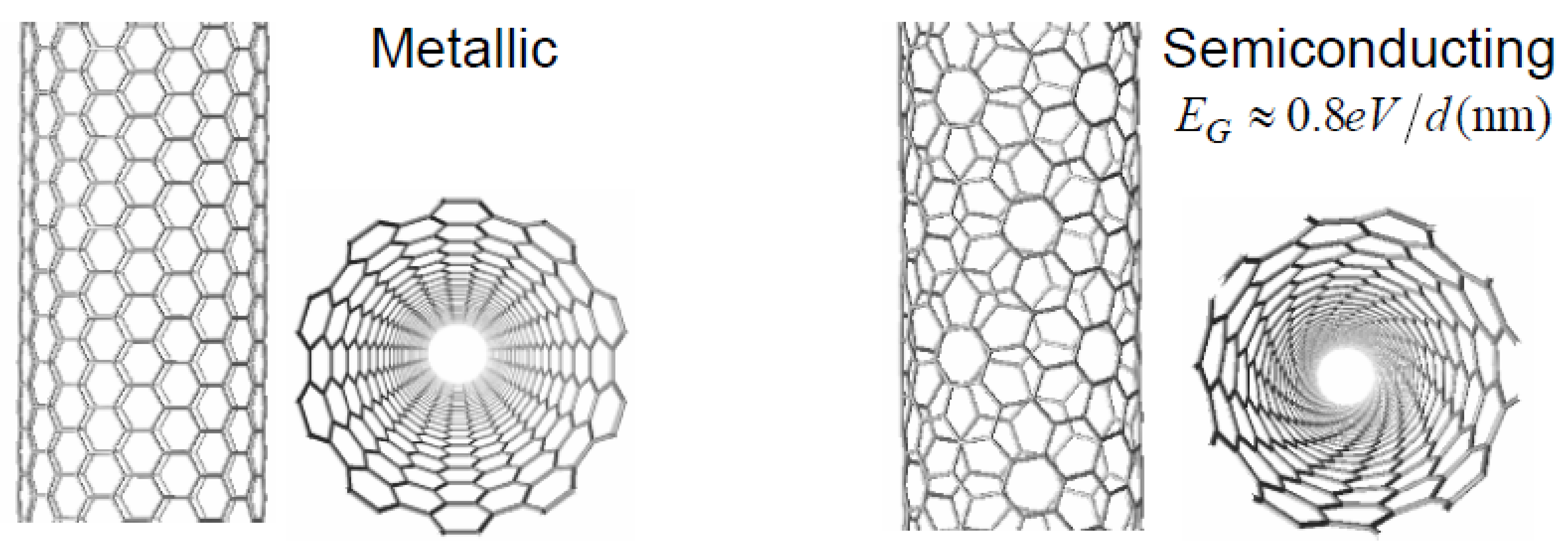
ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

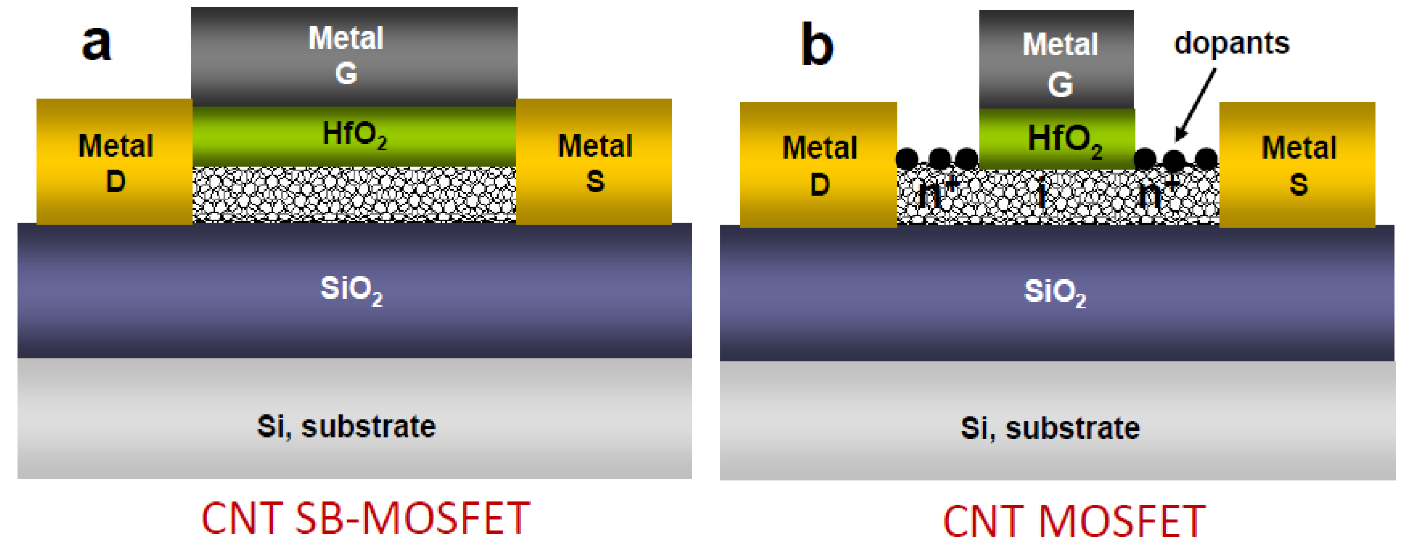
Question: Will CMOS end in 2020?



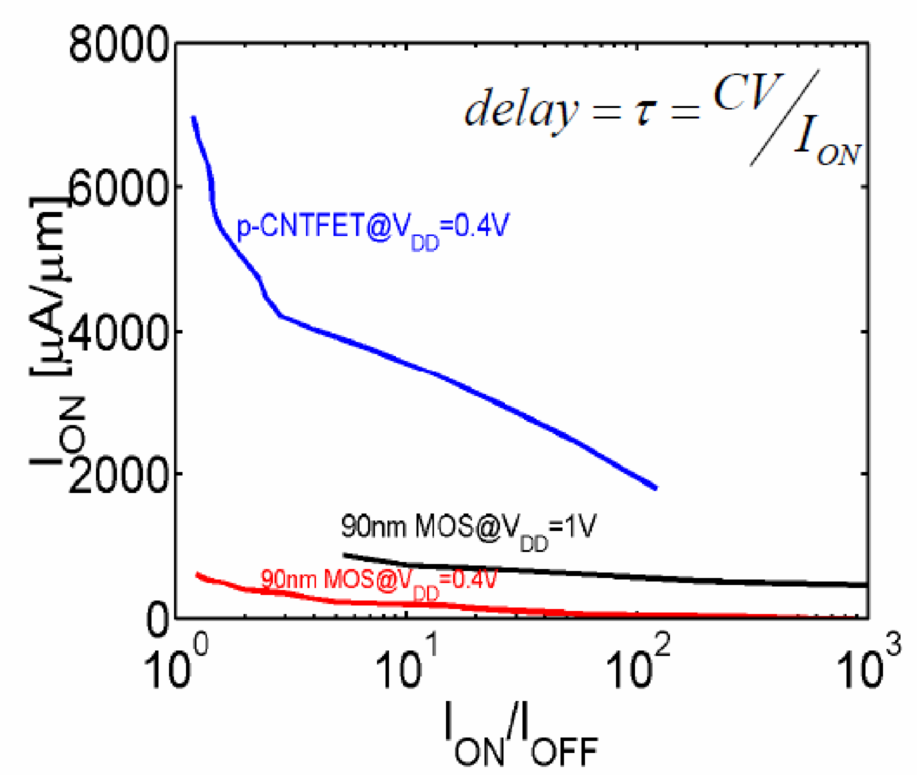
http://www.rcns.hiroshima-u.ac.jp/21coe/pdf/5th_WS/2-4-2_Hiramoto.pdf

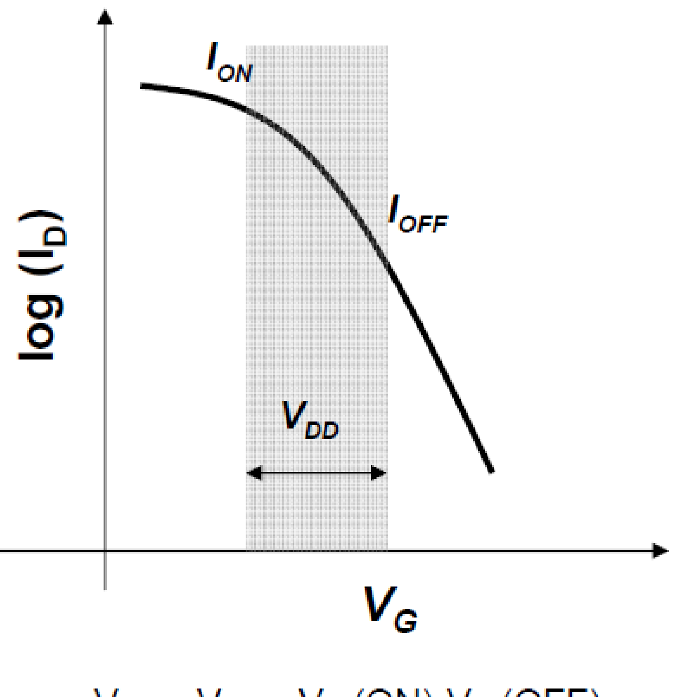


Diameter (d): ~ 0.5-5 nm, Length: ~ 10 nm - 10 cm



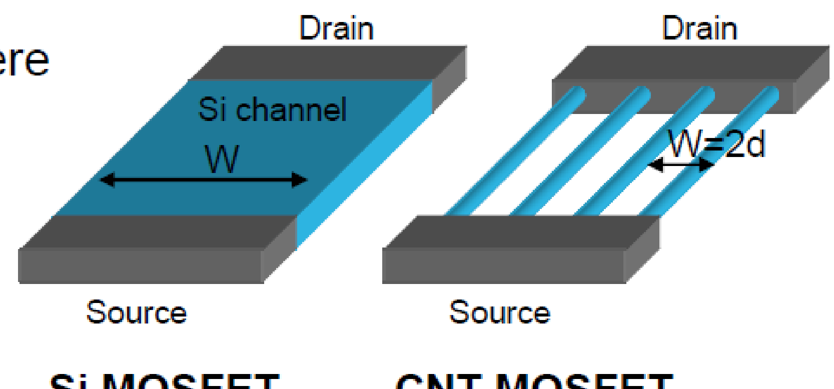
Charles M. Lieber, IEDM Short Course, 2008





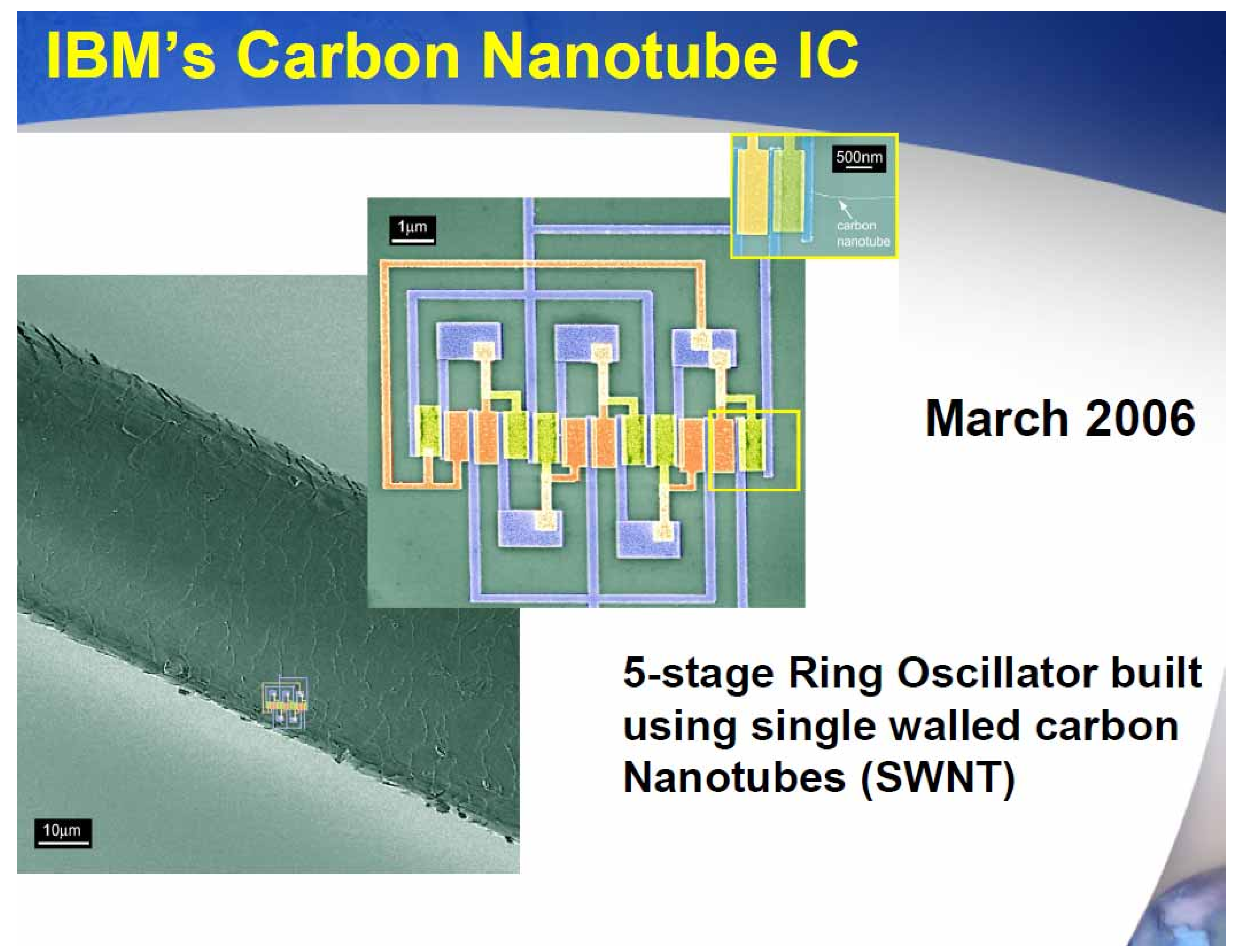
$V_{DD} = V_{DS} = V_G\,(ON) - V_G\,(OFF)$

The current density is normalized by 2*d*, where *d* is the nanotube diameter

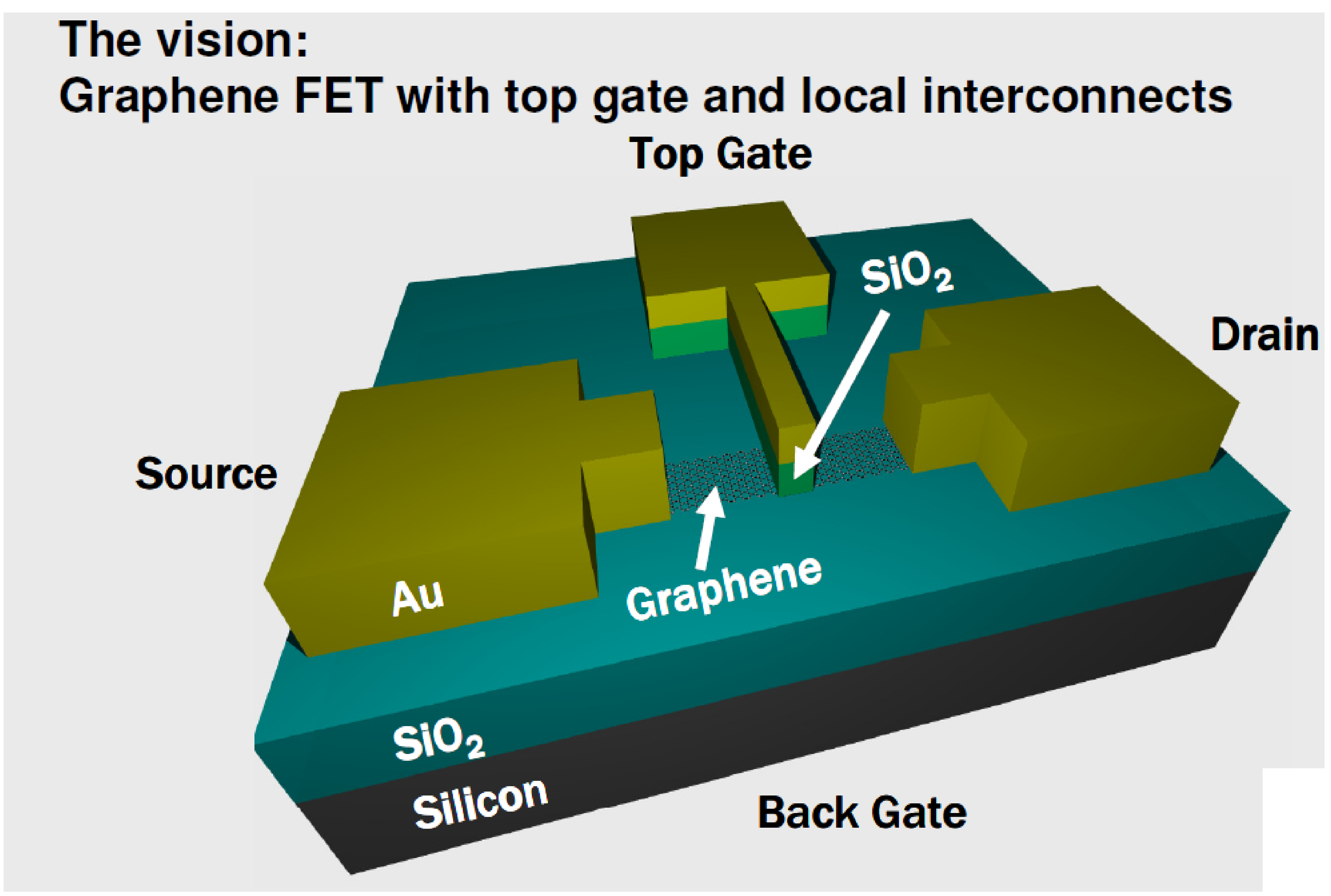


CNTFETs outperform Si MOSFETs

Charles M. Lieber, IEDM Short Course, 2008

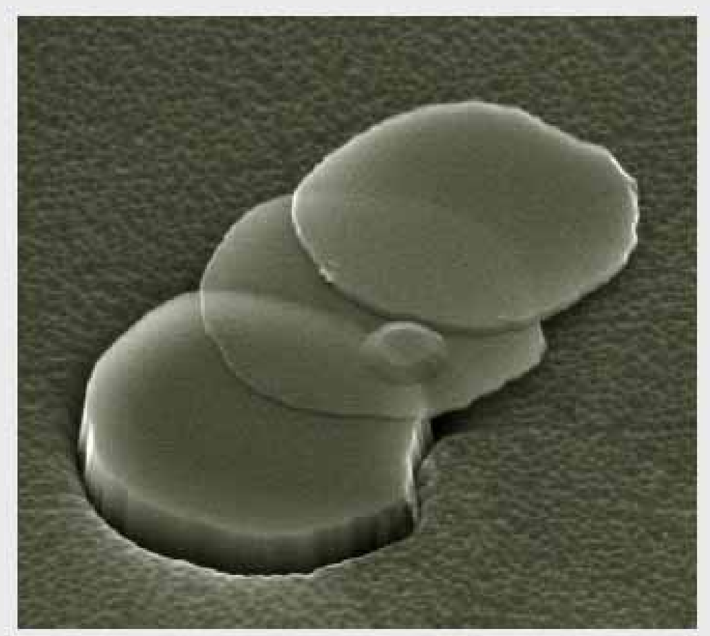


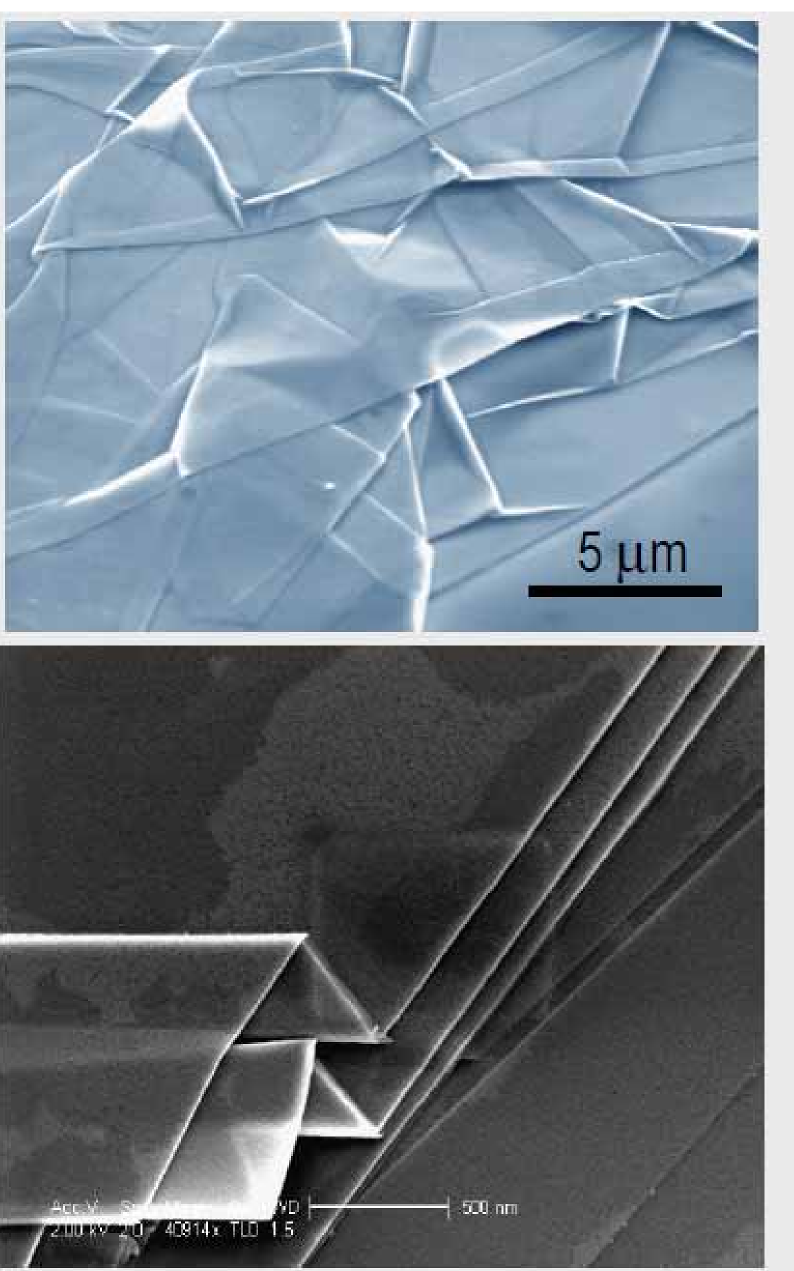
S.E Thompson, IEDM Short Course, 2008


The vision:
Graphene FET with top gate and local interconnects
Top Gate
SiO2
Drain
Source
Au
Graphene
SiO2
Silicon
Back Gate

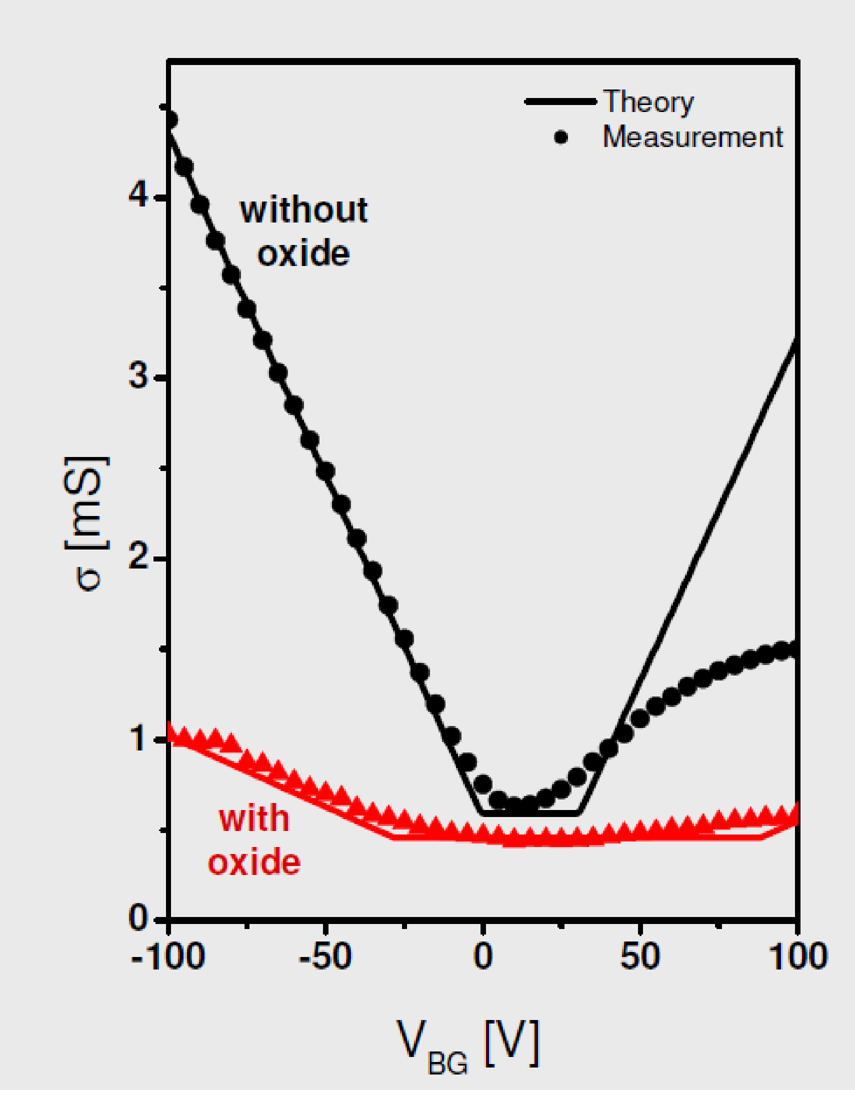
Graphene examples

Source: A. Geim





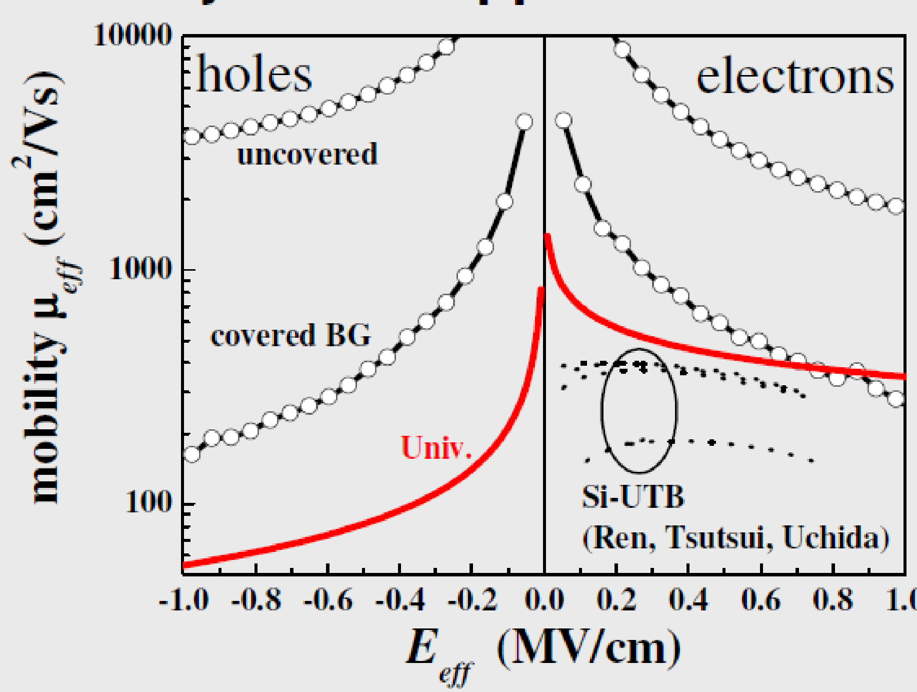
Graphene Field Effect Devices



- conductivity reduced by top gate oxide
- Model of Das Sarma:
  - Minimum conductivity and shift of Dirac Point caused by interface charges
  - without oxide: ~2 x 10^{12} cm^{-2}
  - with oxide: ~6 x 10^{12} cm^{-2}
- Charges are suspected to cause scattering

Graphene Field Effect Devices

Mobility: a first approximation



Approximation of μ (Drude modell):

$\mu = \boldsymbol{\sigma} / (n^* q)$

with

$\boldsymbol{\sigma} = J/E_{ds} = I/\text{width} * \text{length}/V_{ds}$

$n = \boldsymbol{\varepsilon} * E_{eff}/q$

- Mobility decreases (> 1/10) for graphene “sandwiched“ in SiO_2
  → dominant scattering mechanism seems to be substrate determined
- Yet higher values than silicon universal mobility and especially higher than Ultra Thin Body SOI MOSFETs

Lemme et al., tbp: SSE

3D Chip Stacking LSI

20 μm pitch

50 μm

10 μm

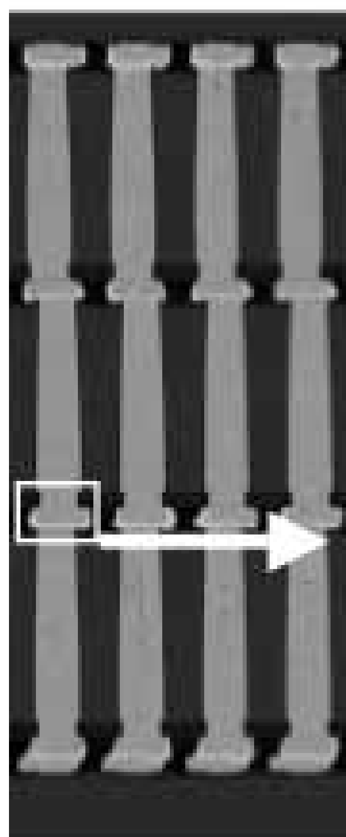
Encapsulate Resin

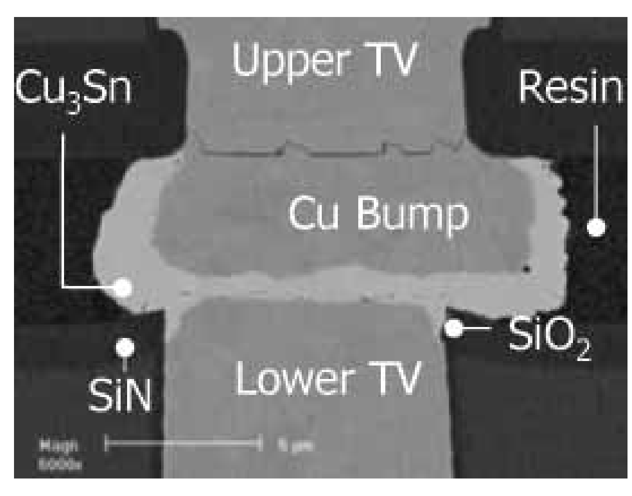
Si Die

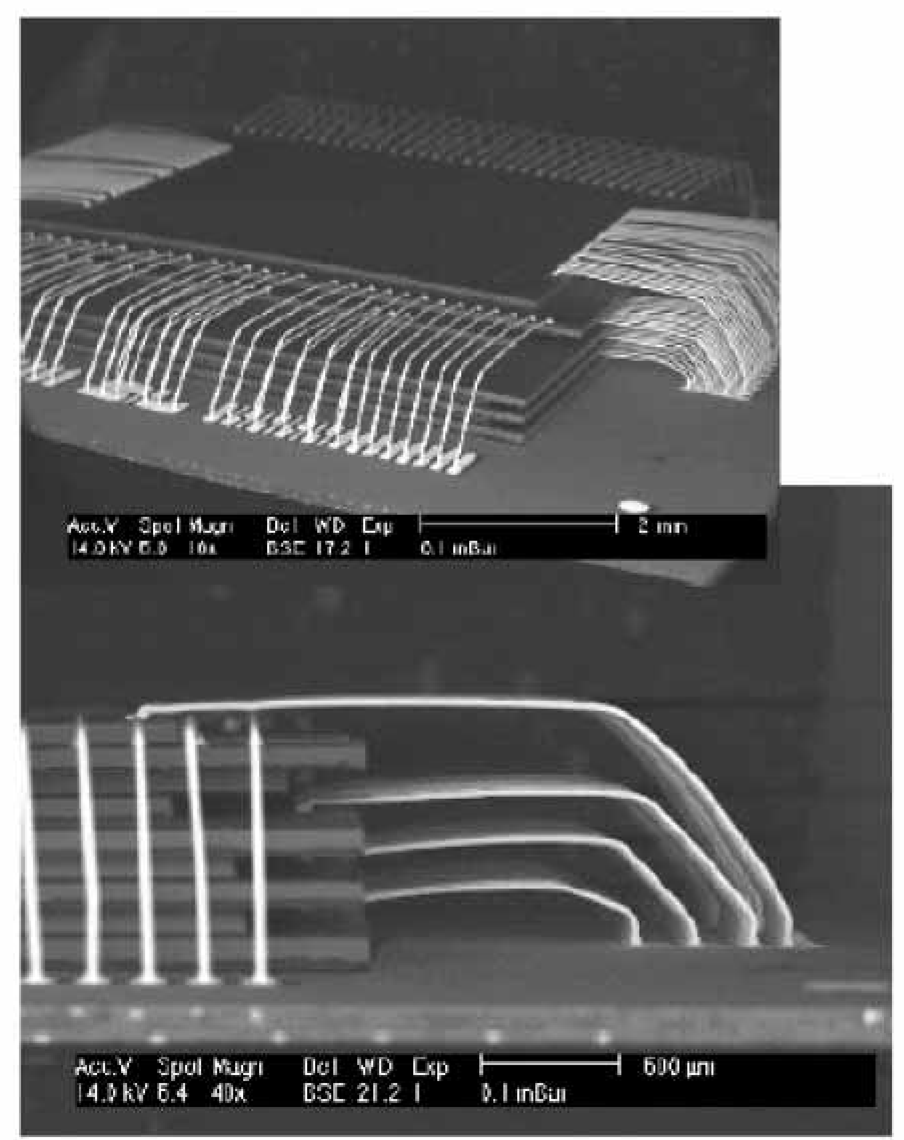
Si Interposer

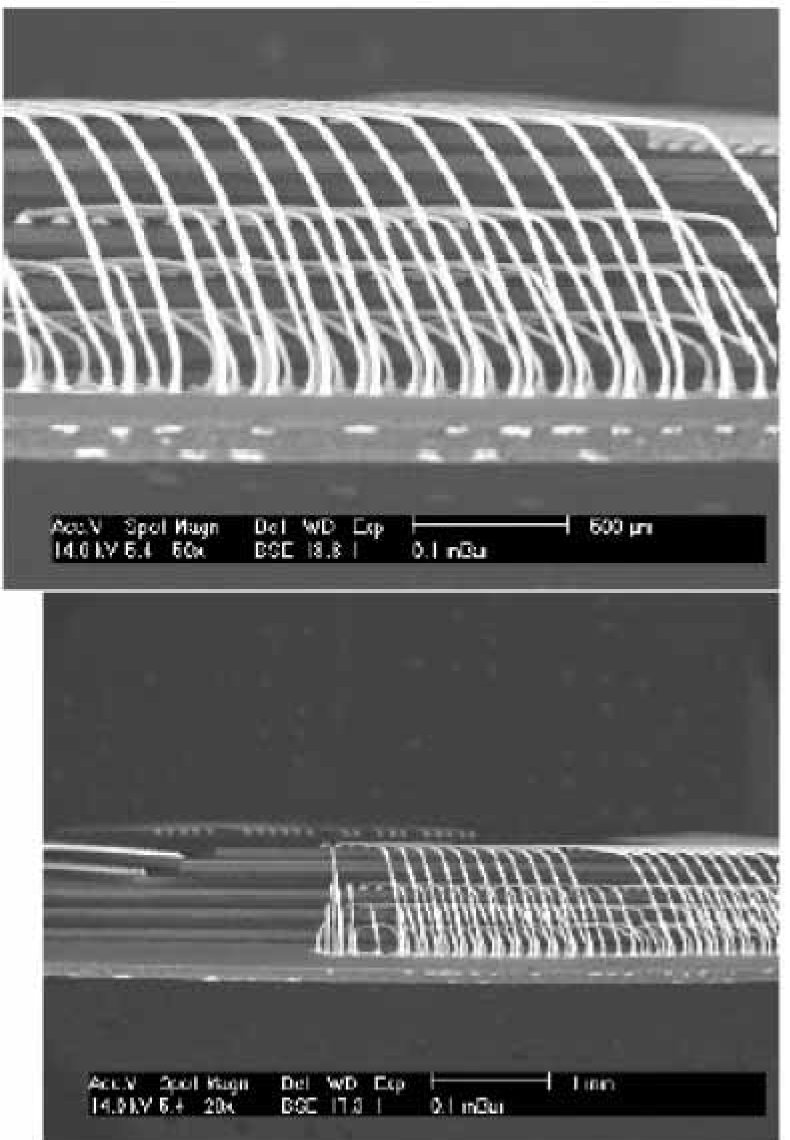
bonding with Cu/Sn alloy

ASET









Source: S. Maekawa, CAST2005

Charles Lee, IEDM 2005 Short Course

Victor V. Zhirnov and Ralph K. Cavin III, ECS 207
Washington DC

Device	*FET*	*RSFQ*	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*	*Spin transistor*
Cell Size	100 nm	0.3 µm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density *(cm^{-2})*	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4\times10^{-17}$	2×10^{-18}	$>2\times10^{-18}$	$>1.5\times10^{-17}$	1.3×10^{-16}	$>1\times10^{-18}$	2×10^{-18}
Binary Throughput, GBit/ns/cm^2	86	0.4	86	86	10	N/A	0.06	86

We HAVE IDENTIFIED NO VIABLE EMERGING LOGIC TECHNOLOGIES for Information Processing beyond CMOS

We could keep the Moore’s law after 2020
Without downswing the gate length

What is Moore’s law.

Keep increase of the number of components.
Cost per components decreases!

Gordon Moore

http://www.intel.com/technology/mooreslaw/index.htm

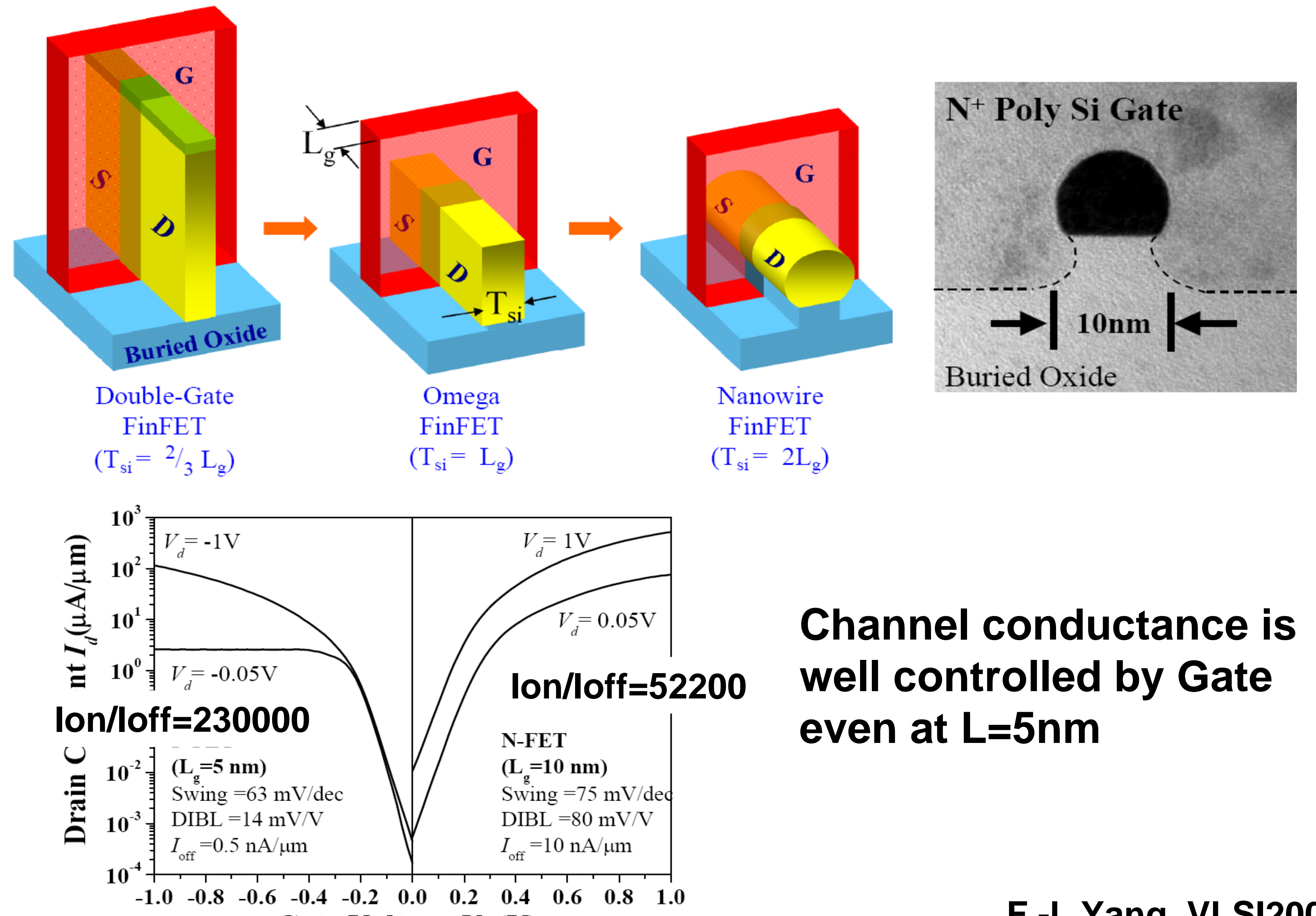
We could keep the Moore's law after 2020
Without downswing the gate length

What is Moore's law.
→ to increase the number (#) of Tr. In a chip

Now, # of Tr. in a chip is limited by power.
→ key issue is to reduce the power.
→ to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.

FinFET to Nanowire



F.-L.Yang, VLSI2004

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1. Use 1D ballistic conduction

M2. Increase number of quantum channel

M3. Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.

1D conduction per one quantum channel:

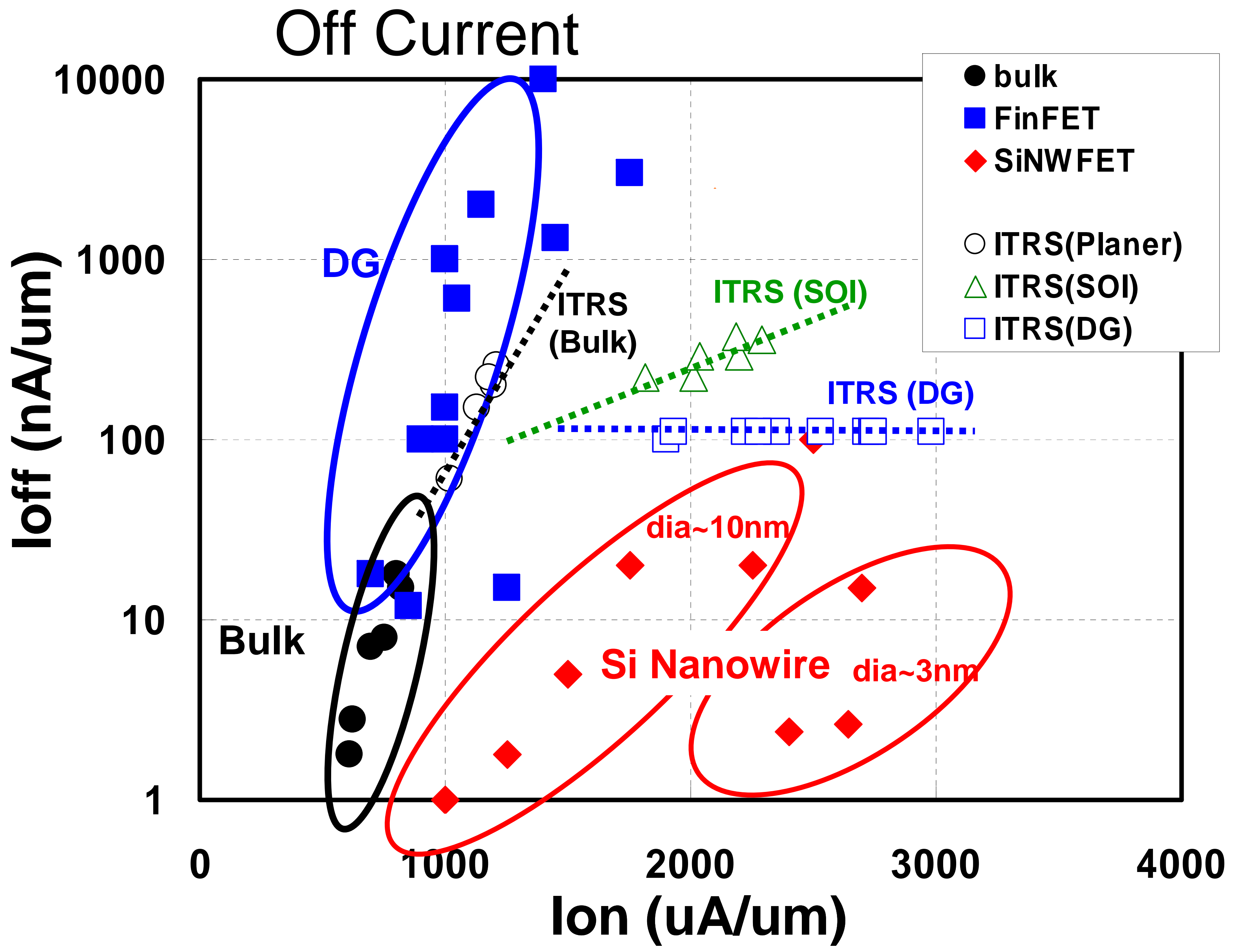
$G = 2e^2/h = 77.8\ \mu S$/wire or tube

regardless of gate length and channel material

That is 77.8 mA/wire at 1V supply

This an extremely high value

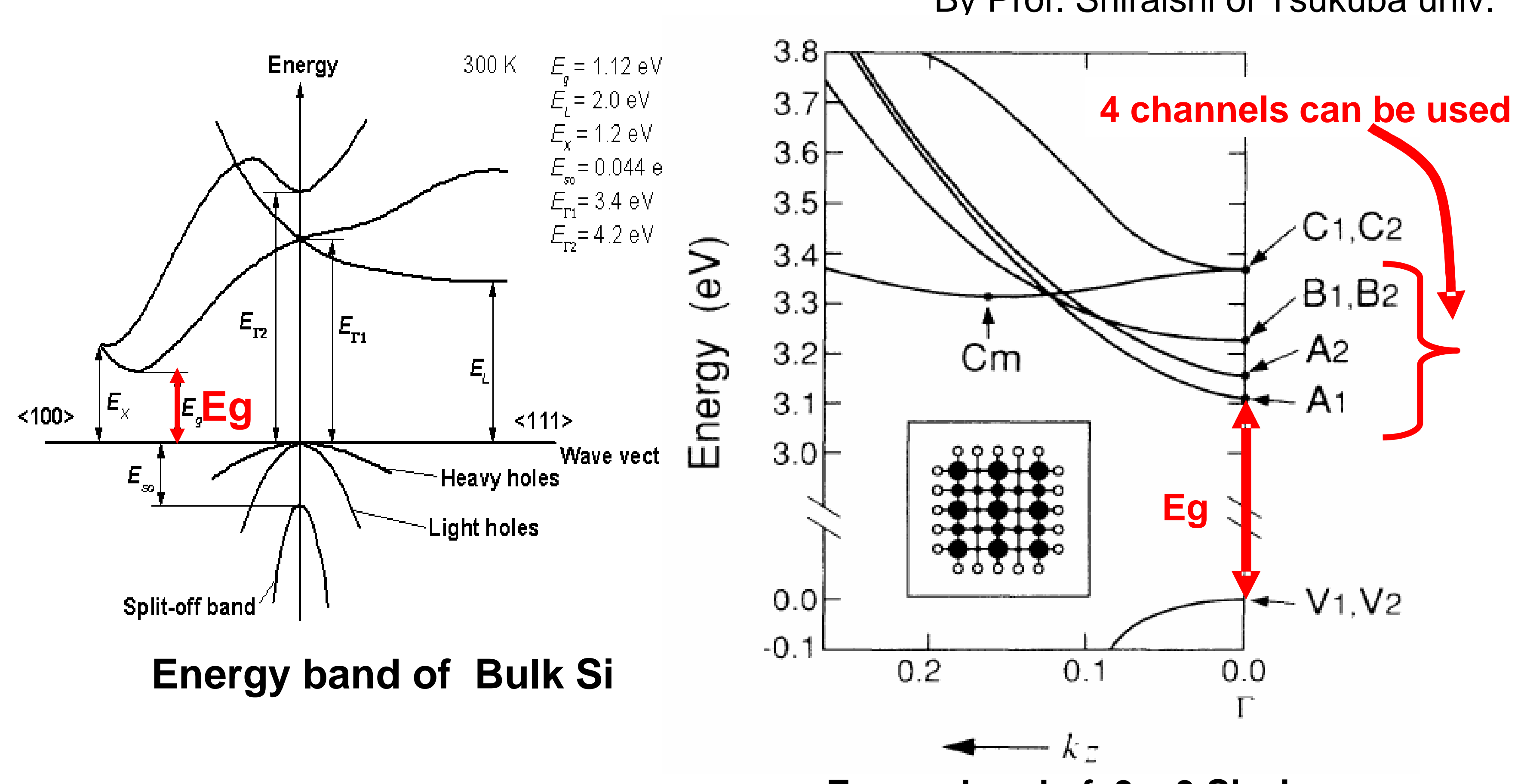
However, already 20mA/wire was obtained experimentaly by Samsung



Off Current
Ioff (nA/um)
Ion (uA/um)
10000
1000
100
10
1
0
1000
2000
3000
4000
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

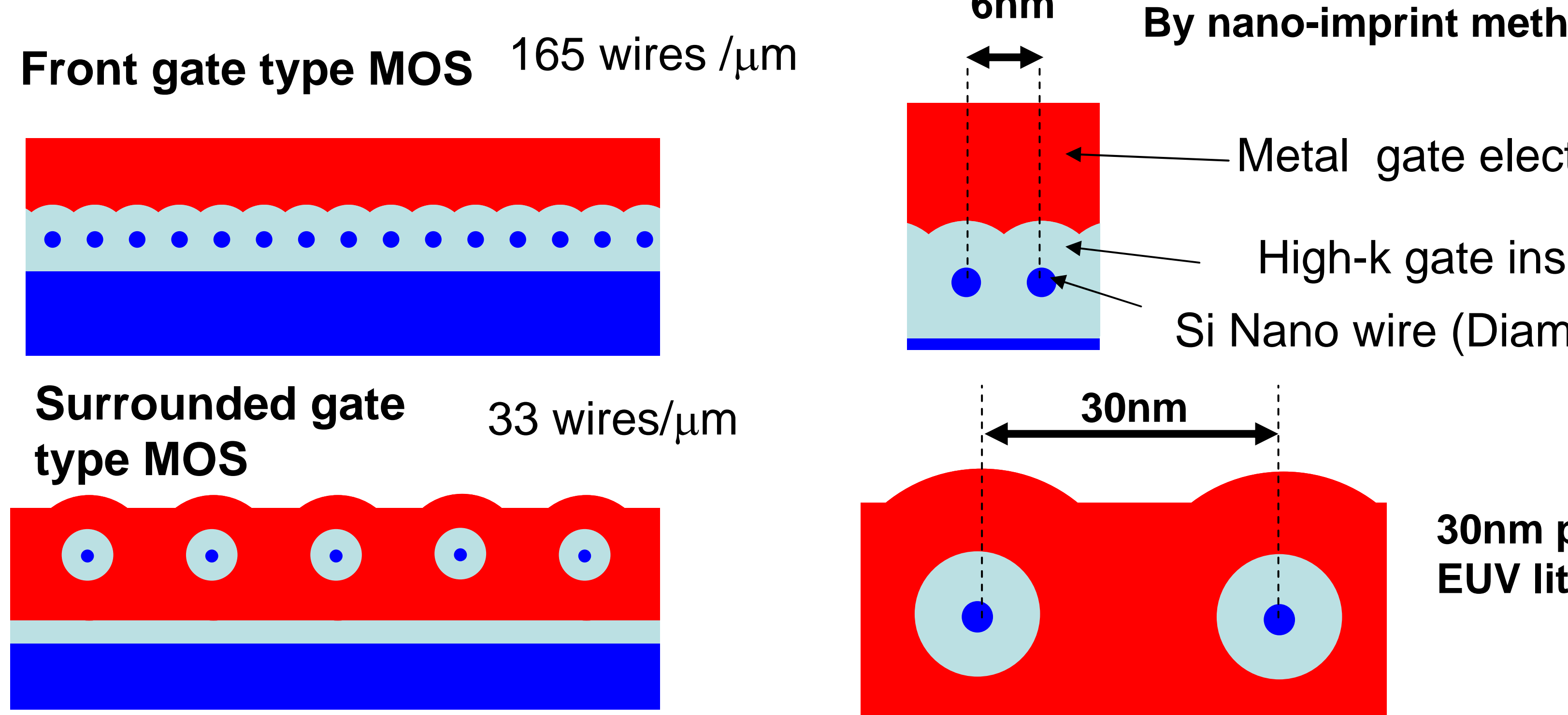
By Prof. Shiraishi of Tsukuba univ.

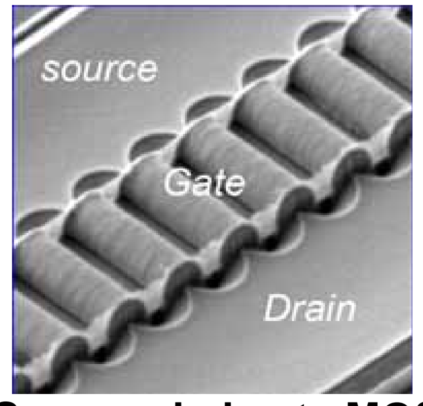


Energy band of Bulk Si

Energy band of 3 x 3 Si wire

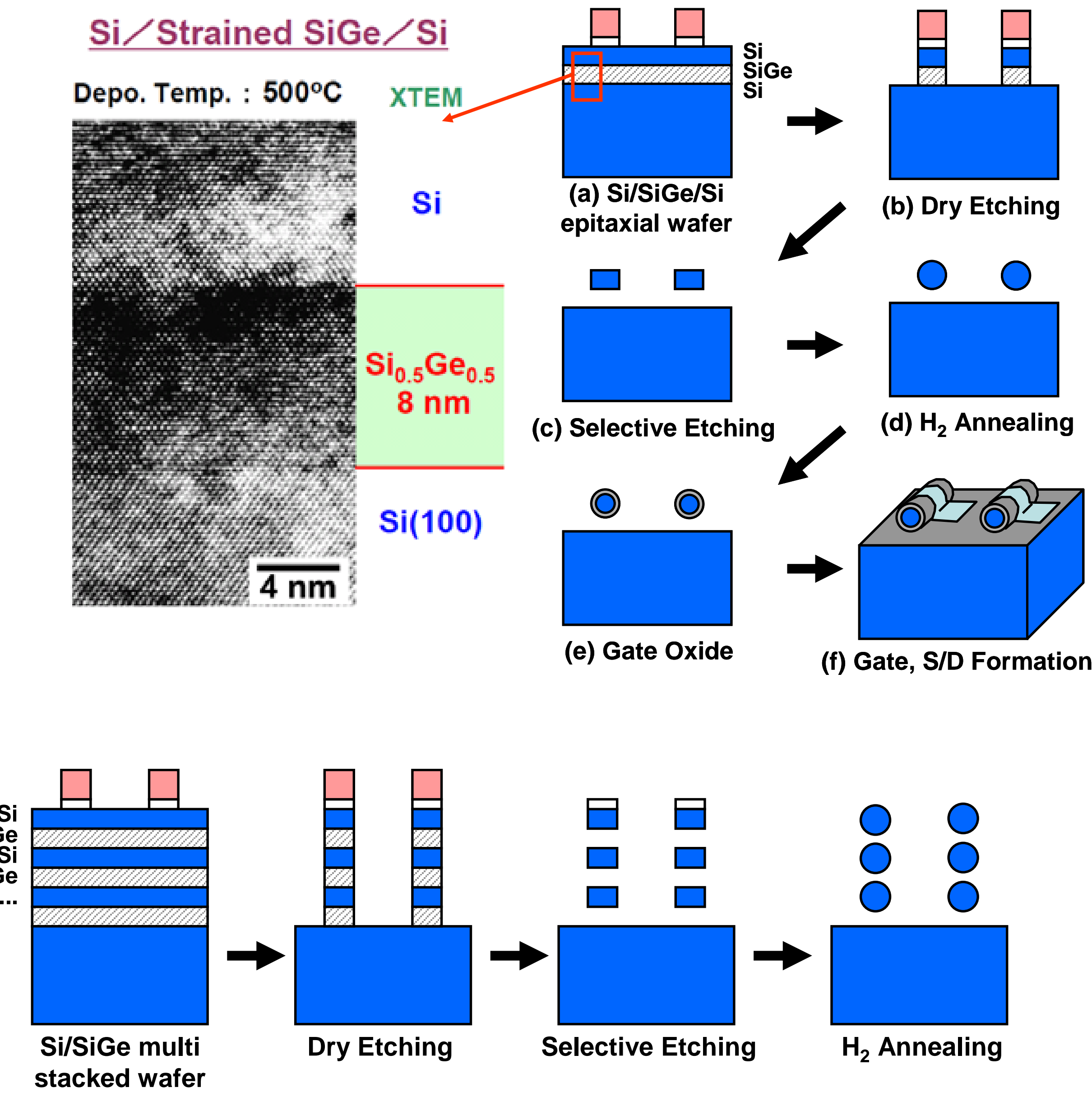
Maximum number of wires per 1 µm

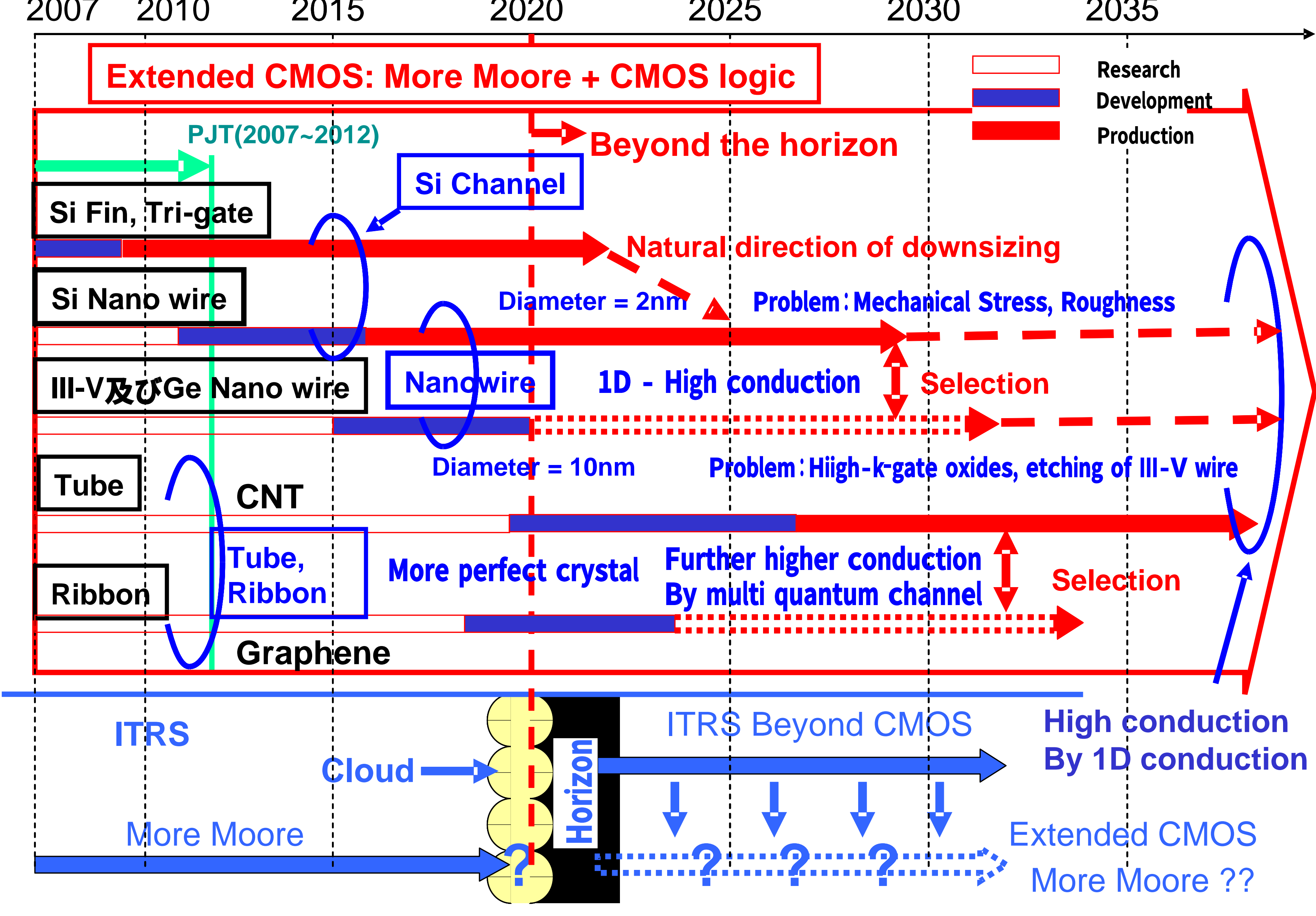


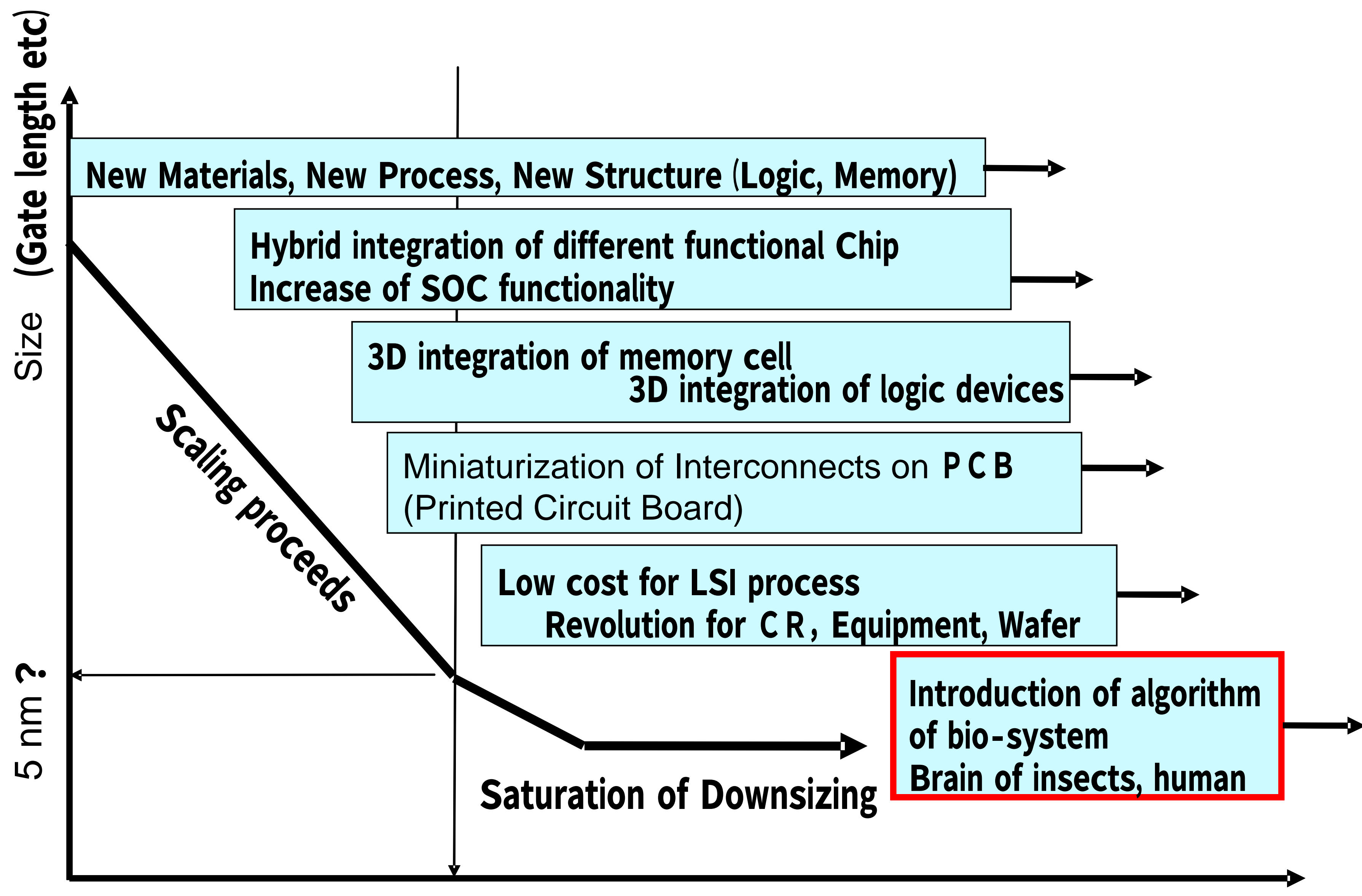


Surrounded gate MOS

Increase the number of wires towards vertical dimension




Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V及びGe Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Ribbon
Graphene
ITRS
ITRS Beyond CMOS
High conduction
By 1D conduction
Cloud
Horizon
More Moore
Extended CMOS
More Moore ??


Size (Gate length etc)
New Materials, New Process, New Structure (Logic, Memory)
Hybrid integration of different functional Chip
Increase of SOC functionality
3D integration of memory cell
3D integration of logic devices
Miniaturization of Interconnects on PCB
(Printed Circuit Board)
Low cost for LSI process
Revolution for CR, Equipment, Wafer
Introduction of algorithm
of bio-system
Brain of insects, human
Scaling proceeds
5 nm ?
Saturation of Downsizing
2020 ?

Brain

Ultra small volume

Small number of neuron cells

Extremely low power

Sensor

Infrared

Humidity

CO_2

Real time image processing

(Artificial) Intelligence

3D flight control

Mosquito

System and Algorism becomes more important !

But do not know how?

Dragonfly is further high performance

Thank you
for your attention!