シリコン集積回路の現状とその微細化終焉後の世界

平成20年度　飯綱・サイエンスサマー道場
―進化・発展するナノエレクトロニクス。その本命は?―

2008年8月19日
@長野県飯綱高原　「ホテルアルカディア」

東京工業大学
岩井　洋

言うまでもないが

Si集積回路とは、即ちCMOS 集積回路のことであり、
今や我々人類社会に必要不可欠なものとなっている

我々の社会はCMOS集積回路の補助無してはやっていけない

家庭、オフィス, 生産, 金融, 通信, 運輸, 医療, 教育, 娯楽等

仮に、CMOS集積回路が動かなければ

銀行のコンピュータが停止 → 世界経済が直ちに停止

携帯電話を含め世界の通信が停止
→ 情報が全く入らない状況

学生を含め世の中一般の人はSi集積回路と言っても良く理解できない人が大部分であると思うが、その重要性を改めて認識する必要がある。

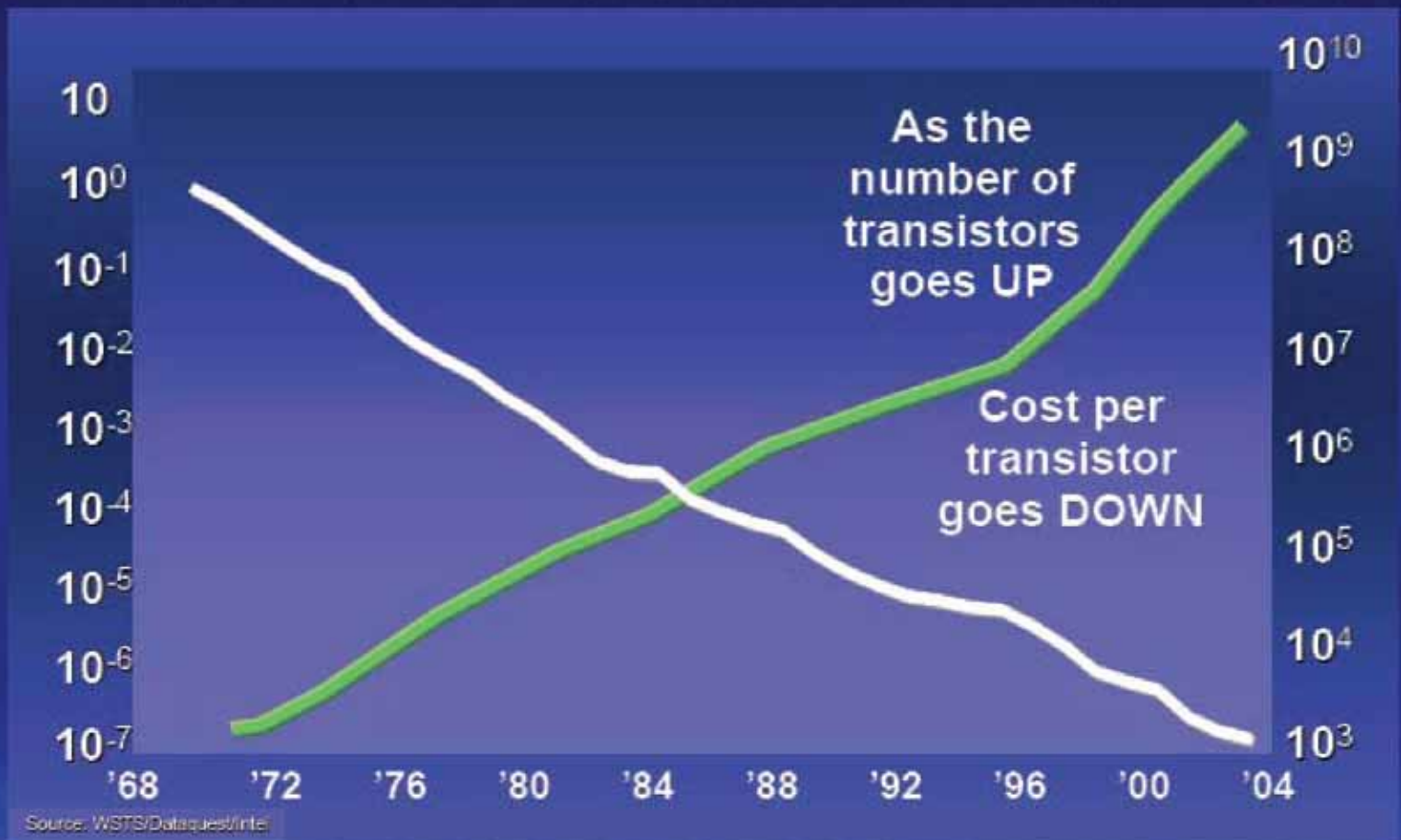
S集積回路は毎年のように集積度を上げてきた

年代	名称	トランジスタ数
1960年代	IC (Integrated Circuits)	~ 10
1970年代	LSI (Large Scale Integrated Circuit)	~1,000
1980年代	VLSI (Very Large Scale IC)	~10,000
1990年代	ULSI (Ultra Large Scale IC)	~1,000,000
2000年代	?LSI (? Large Scale IC)	~1000,000,000

これ以降は、10年毎に新たな名前を考え出すことは難しいので、世界で通じる名前は無い

Exponential Cost Reduction

Cost per Transistor



intel Leap ahead

SPIE Microlithography 2006, San Jose, Ca USA

6

微細化が集積回路発展の駆動力

	1900	1950	1960	1970	2000
	真空管	Transistor	IC	LSI	ULSI
寸法（ゲート長、フィラメント）	10 cm	cm	mm	10 μm	100 nm
	10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

過去100年足らずの間に百万分の一に縮小

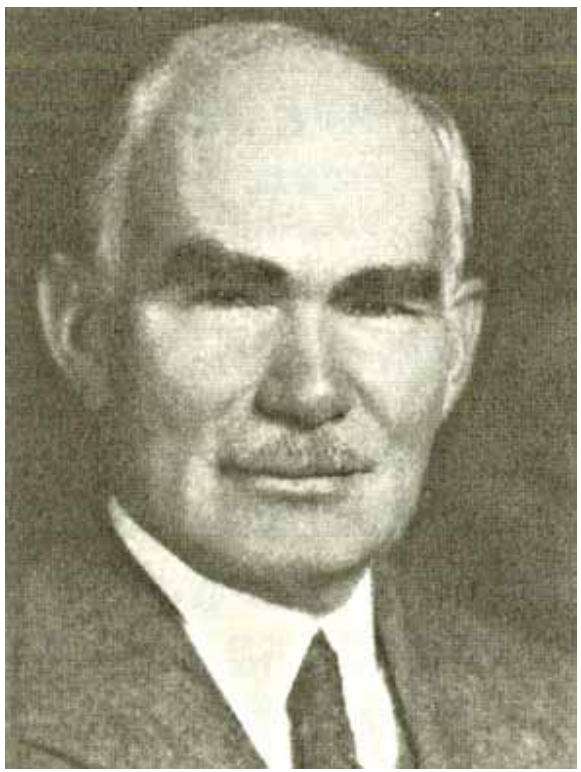
石器時代から人類は数々の道具を発明して来たが、このような急激な微細化は、人類史の中で空前絶後の出来事

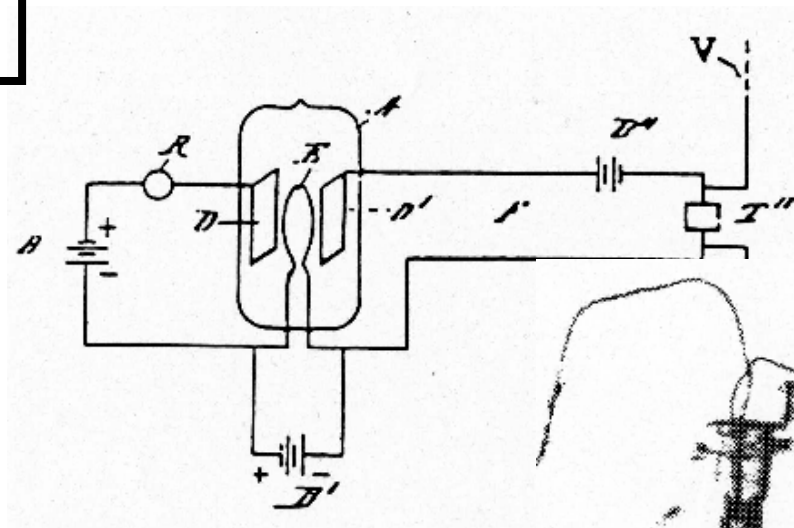
1906: 真空管：3極管

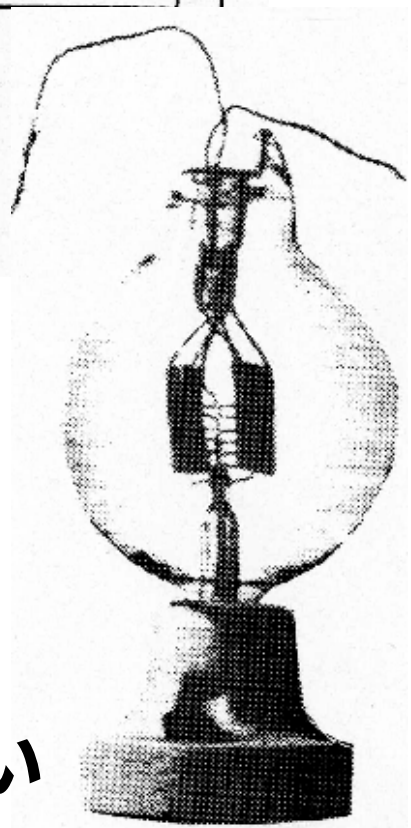
一昨年2006年はその100周年
この100年前後にされた発明の中でも最も重要なもの

1996年　コンピュータ50周年
1997年　電子発見　100周年
　　トランジスタ50周年
2005年　物理年　アインシュタイン

Lee De Forest (1873-1961)





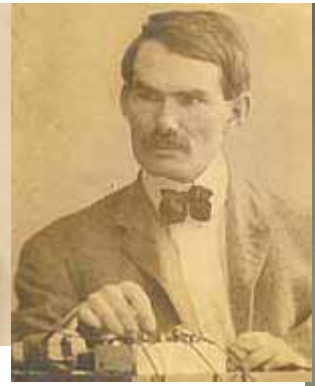


電子回路は3極管がその始まり

彼が生きていればノーベル賞を受賞するのに最も相応しい

Lee De Forestの4人の妻

1906 Lucille Sheardown
1907 Nora Blatch
1912 Mary Mayo, singer
1930 Marie Mosquini, silent film actress



Mary

Marie

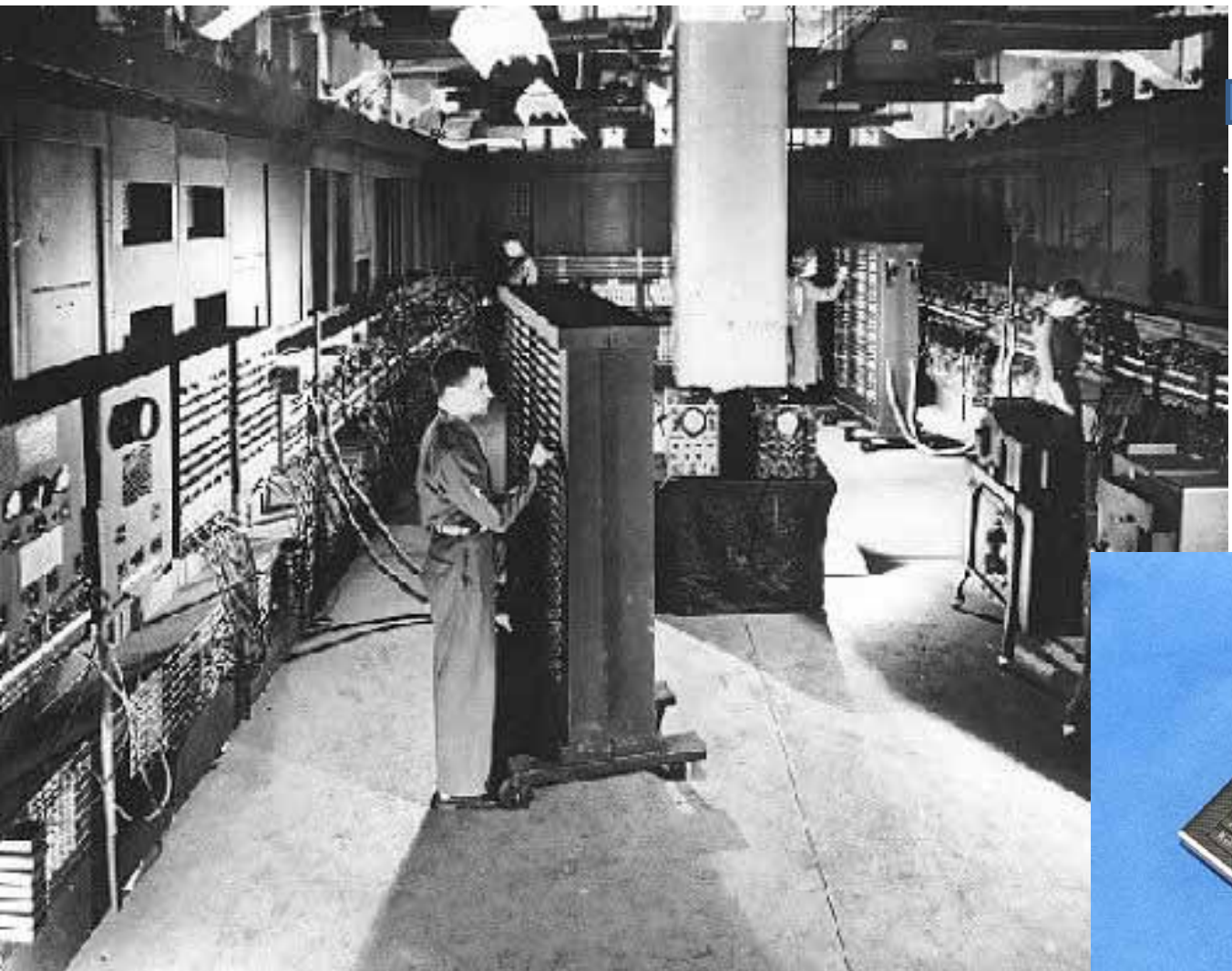
微細化

1. **素子のキャパシタンス (容量) の減少**
   → トランジスタのスイッチ時間の減少
   → 集積回路の高速動作

2. **集積回路中の素子数の増加**
   → 集積回路の多機能化
   → ジョブの並列処理化
   → 集積回路の高速動作

微細化は集積回路の高性能化に文字通り一石二鳥
→ 微細化は集積回路の発展にとって最も重要

世界最初の電算機 Eniac: 多くの真空管で形成 1946
重厚長大, 大消費電力, 真空管のフィラメントの寿命が短時間



今日のpocket PCは遥かに高性能で、尚且つ極めて低消費電力

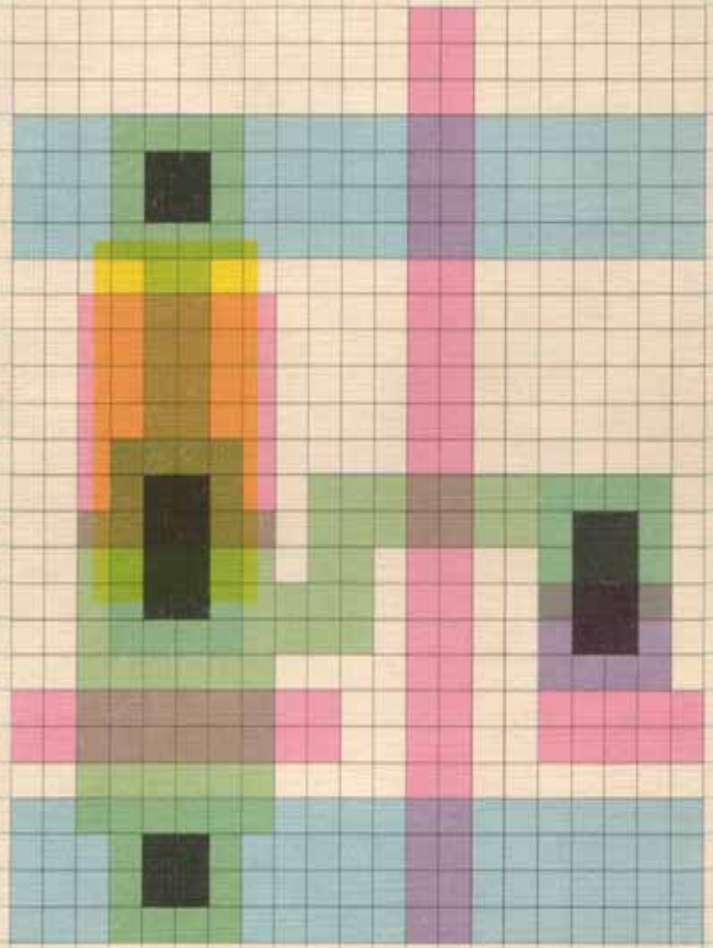
Many people wanted to say about the limit. Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

INTRODUCTION TO VLSI SYSTEMS

超LSI
システム入門

C.ミード・L.コンウェイ共著 東京大学教授 工博 菅野卓雄 東京大学助教授 工博 榊 裕之 監訳

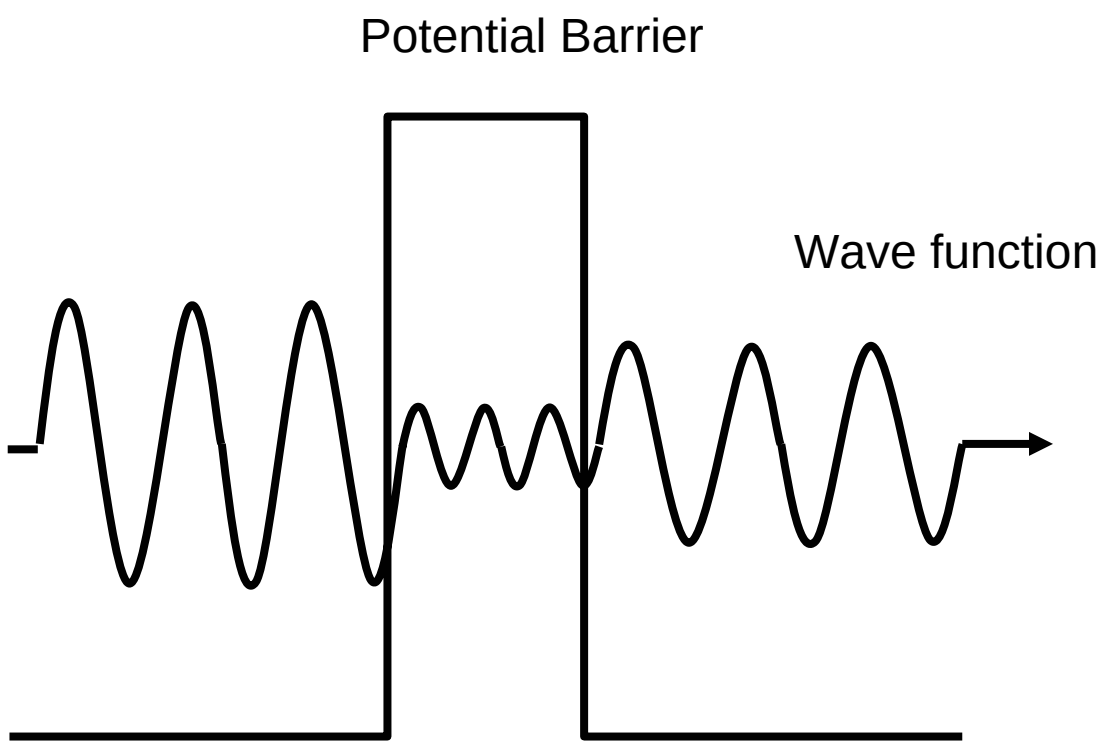


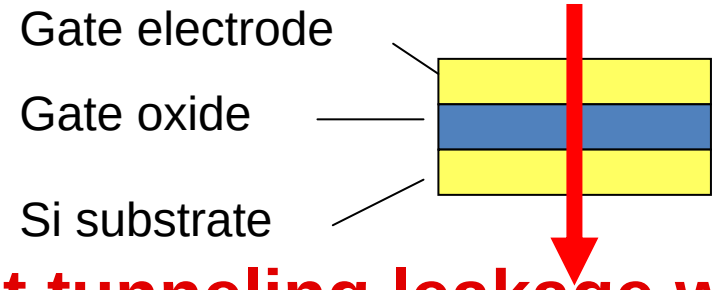
培風館

超LSI教科書

の理由により，できる限り低い供給電圧で動作するように最適設計を施した回路においても，電源電圧 VDD としてはほぼ 0.5 ボルトが必要となる。1978 年時点での素子は，VDD がほぼ 5 ボルトの状態で働いており，そのチャネル長は最小 6 ミクロン程度である。したがって，本書に記した種類の比例縮小法を用いれば，将来チャネル長が約 0.5 ミクロンで，(単位面積当りの)電流密度が現在のほぼ 10 倍であるような回路がもたらされるであろう。単位面積当りの消費電力は，その範囲では一定に保たれる。さらに小さな寸法の素子が作られるかも知れないが，それを使う際には電圧をさらに下げることを避けなければならない。その結果，単位面積当りの電力は上昇することになる。最終的には，チャネル長がほぼ 0.25 ミクロンの領域に素子の基本的限界が存在するように思われる。その領域では，ゲート酸化膜を通じてのトンネル効果や空乏層内の不純物の位置の統計的なバラつきの効果など，種々の物理現象の影響のために，微小寸法を持つ素子が動作不能となり始めるからである。

Direct-tunneling effect



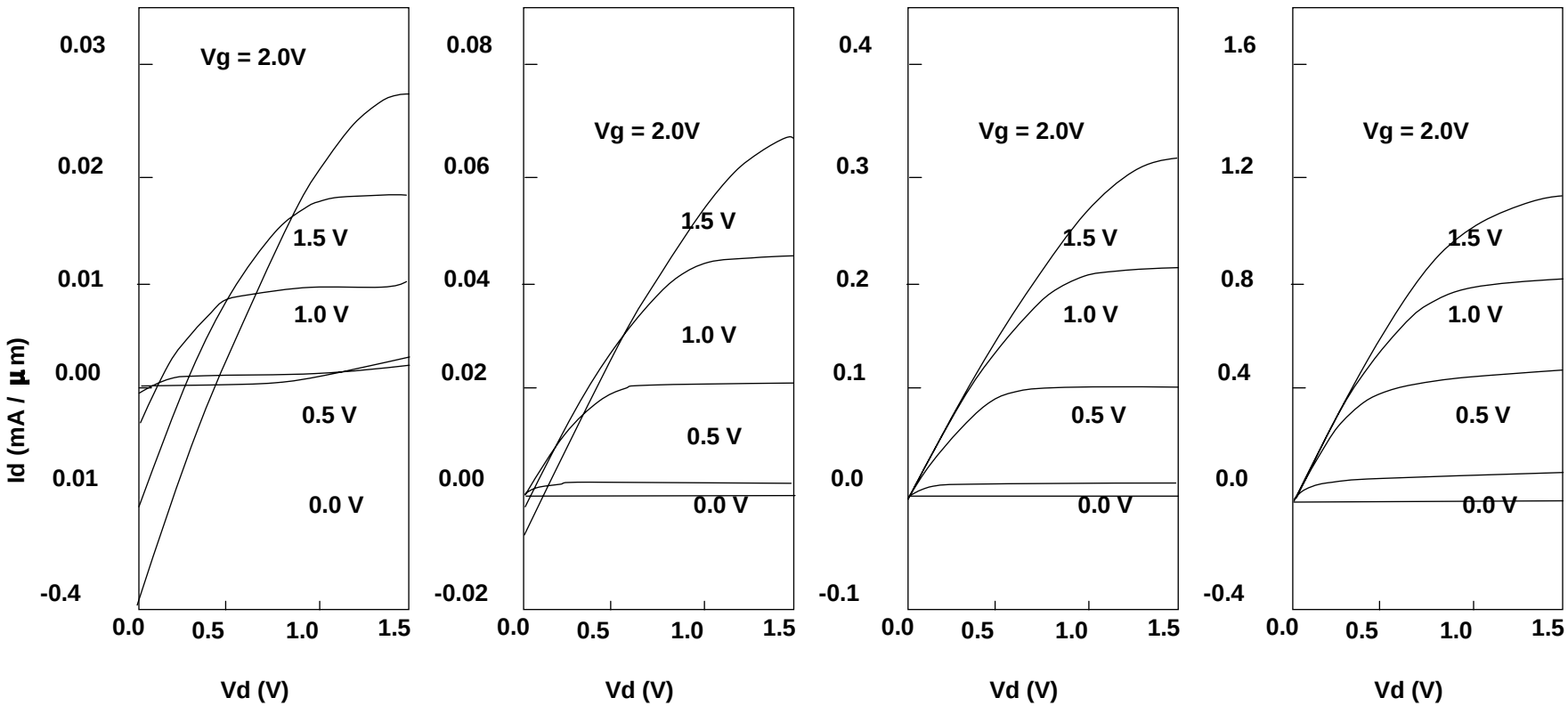


Direct tunneling leakage current start to flow when the thickness is 3 nm.

Direct tunneling leakage was found to be OK! In 1994

MOSFETs with 1.5 nm gate oxide

Lg = 10 μm | Lg = 5 μm | Lg = 1.0 μm | Lg = 0.1μm



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

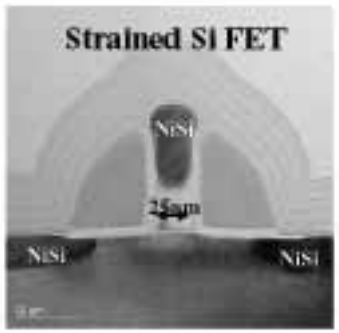
90nm node

Lg=50nm

65nm node

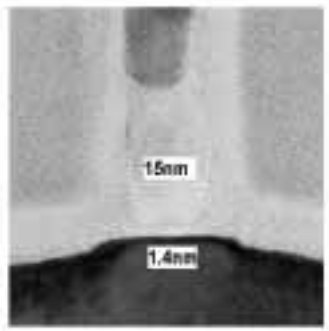
Lg=35nm

45nm node



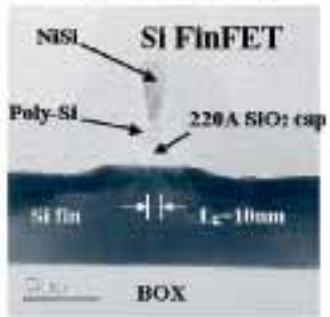
Lg=25nm

32nm node

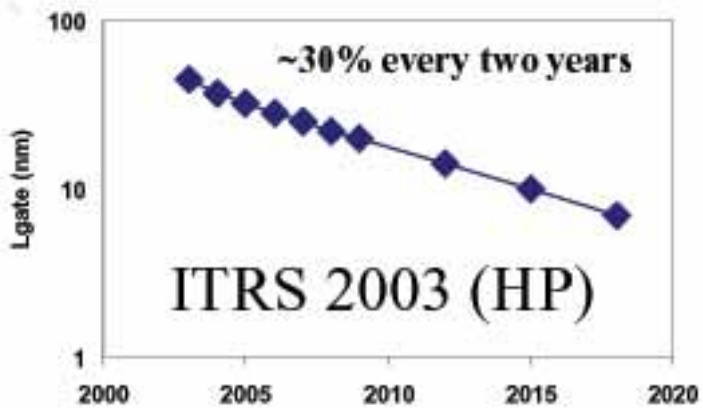


Lg=15nm

22nm node



Lg=10nm



Qi Xinag, ECS 2004, AM

1992年のロードマップ　米国半導体協会

NTRS (National Technology Roadmap for Semiconductors)

	1992年	2007年予想
ゲート長	0.5 μm	0.1 μm
ゲート絶縁膜厚	12 nm	4 nm
動作周波数	120 MHz	1 GHz

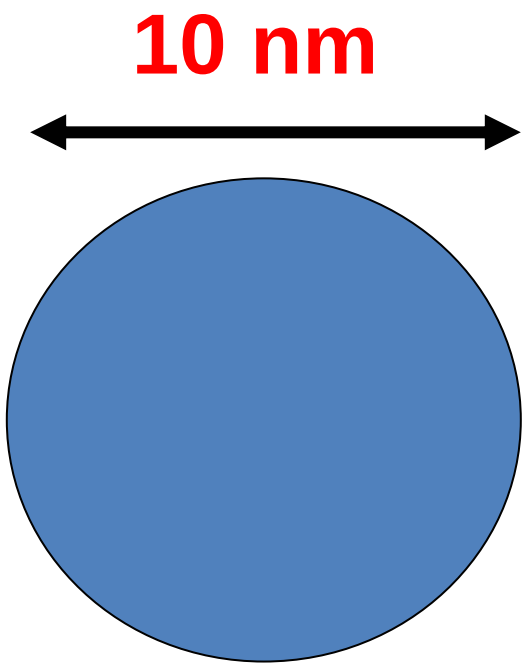
2007年製品実績
高速ロジックデバイス

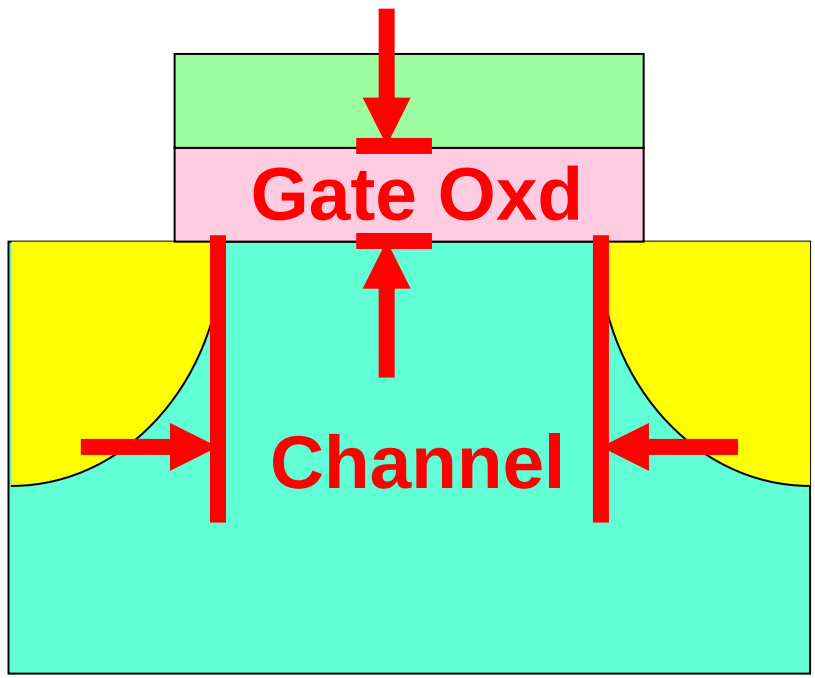
2007年実績
40 ～ 30 nm
1.5 ～ 1 nm
2 ～ 3 GHz

Downsizing limit?

Channel length?

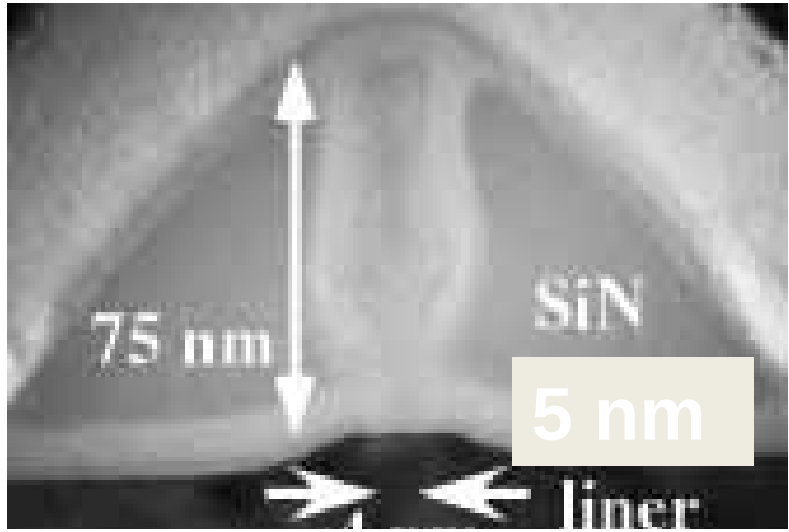
Electron wave length



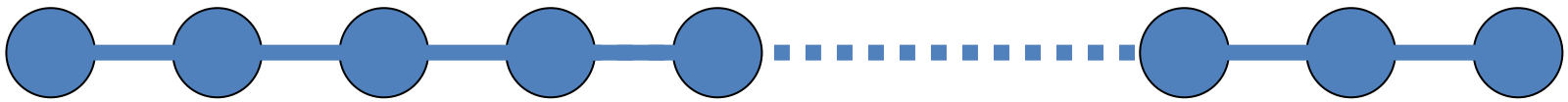


5 nm gate length CMOS

Is a Real Nano Device!!

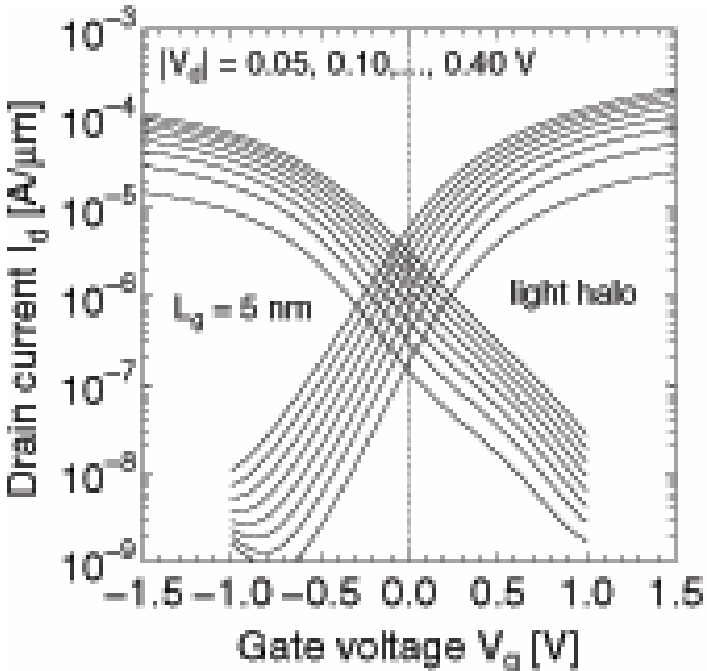


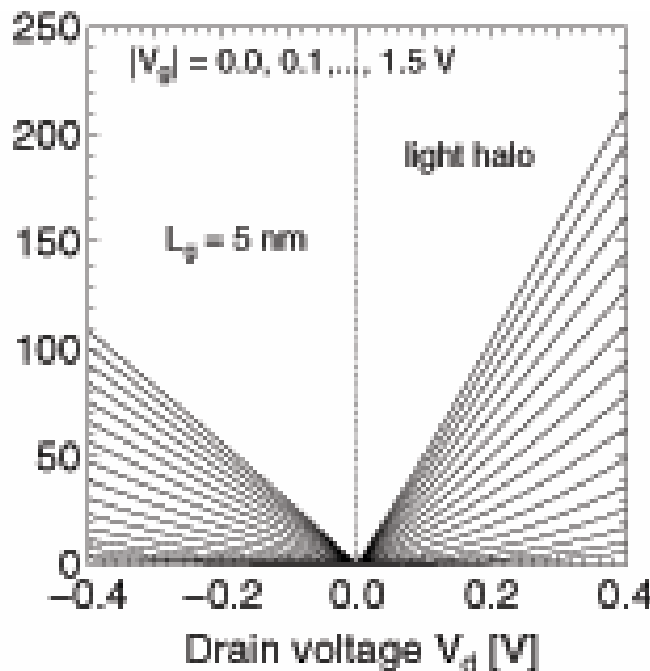
Length of 18 Si atoms



H. Wakabayashi et.al, NEC

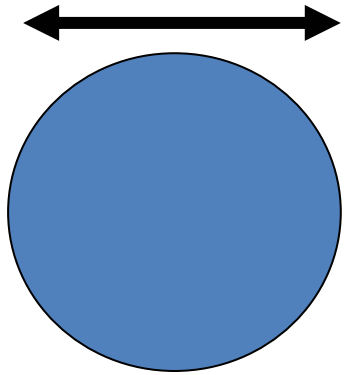
IEDM, 2003





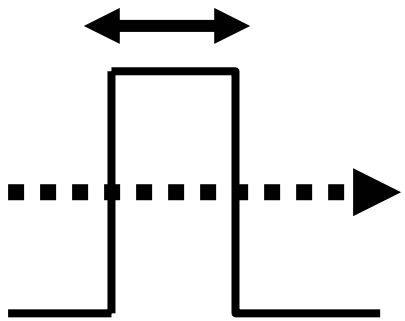
Electron wave length

10 nm



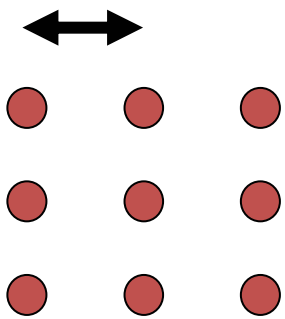
Tunneling distance

3 nm



Atom distance

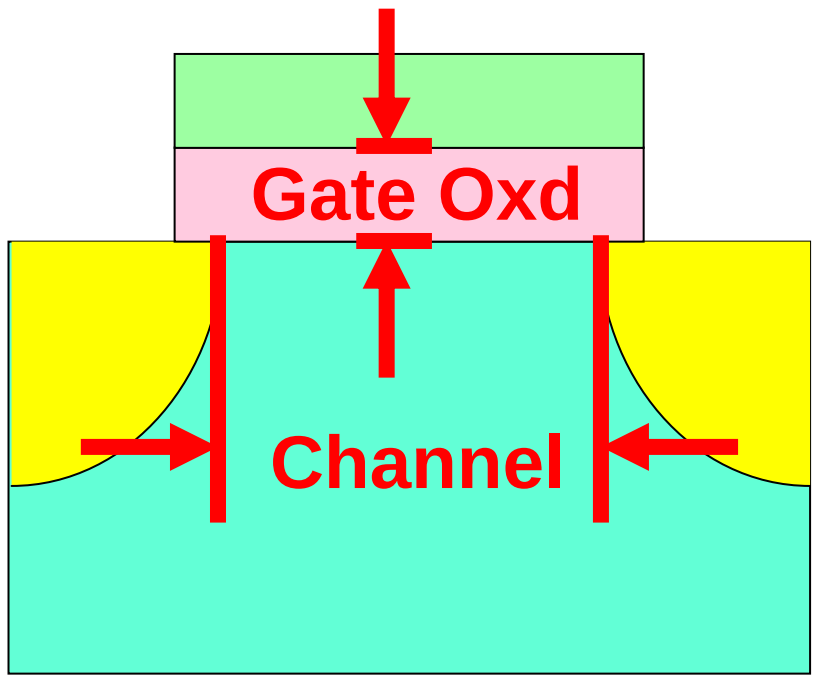
0.3 nm



Downsizing limit!

Channel length

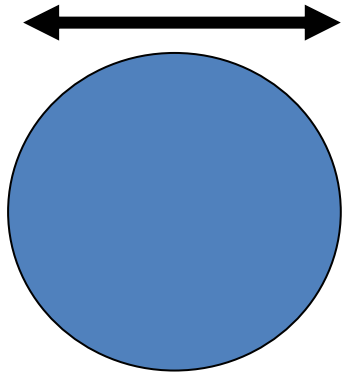
Gate oxide thickness



Prediction now!

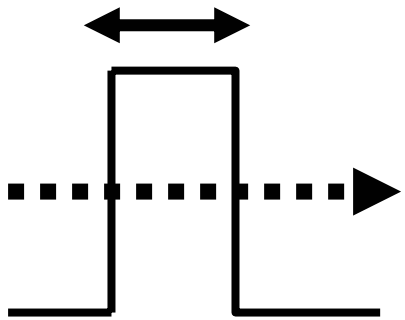
Electron wave length

10 nm



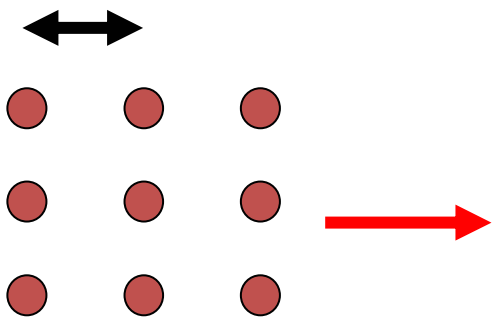
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

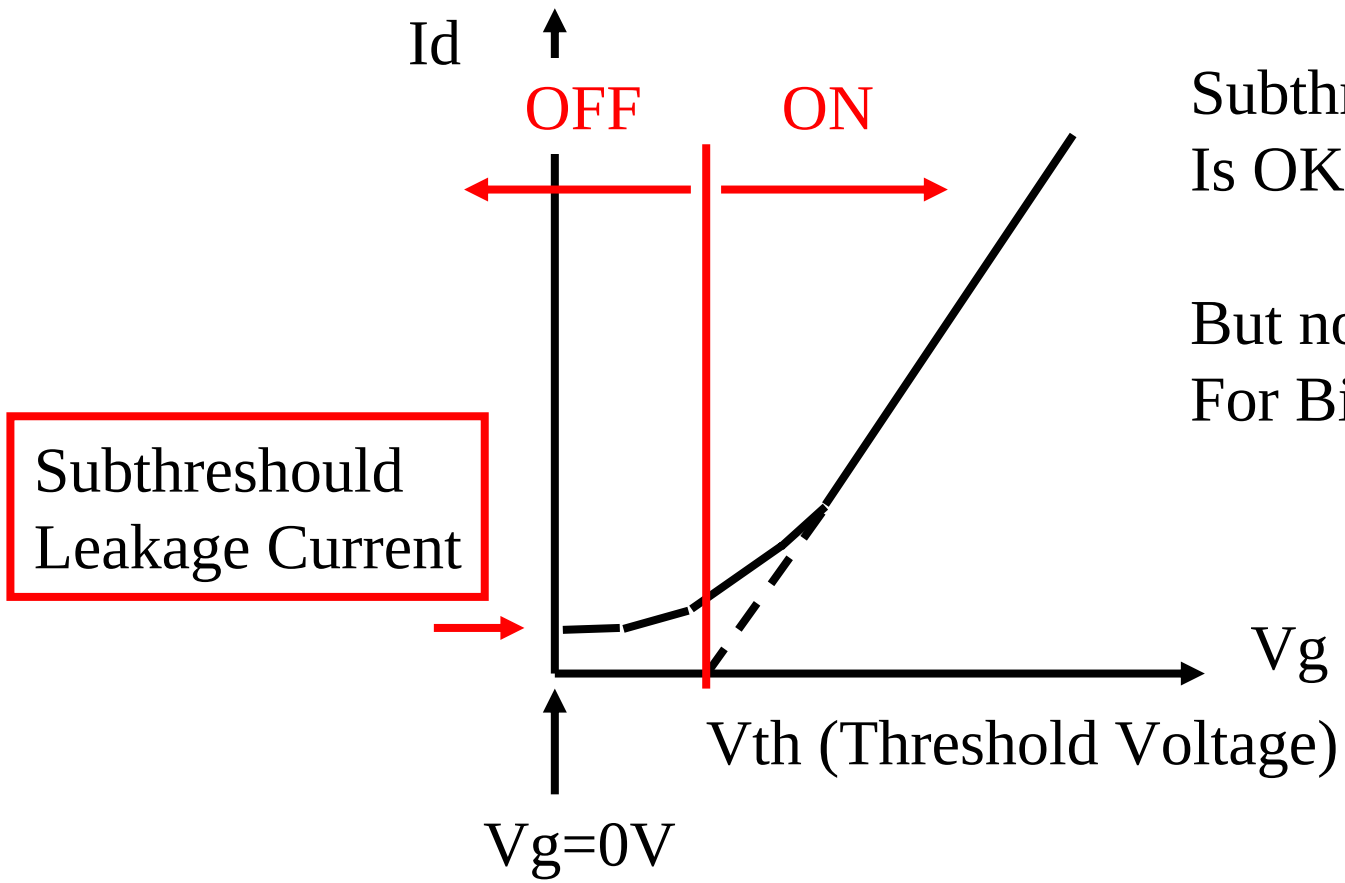
Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Maybe, practical limit around 5 nm or so.

When Gate length Smaller,

→ Subthrehold Leakage Current Larger

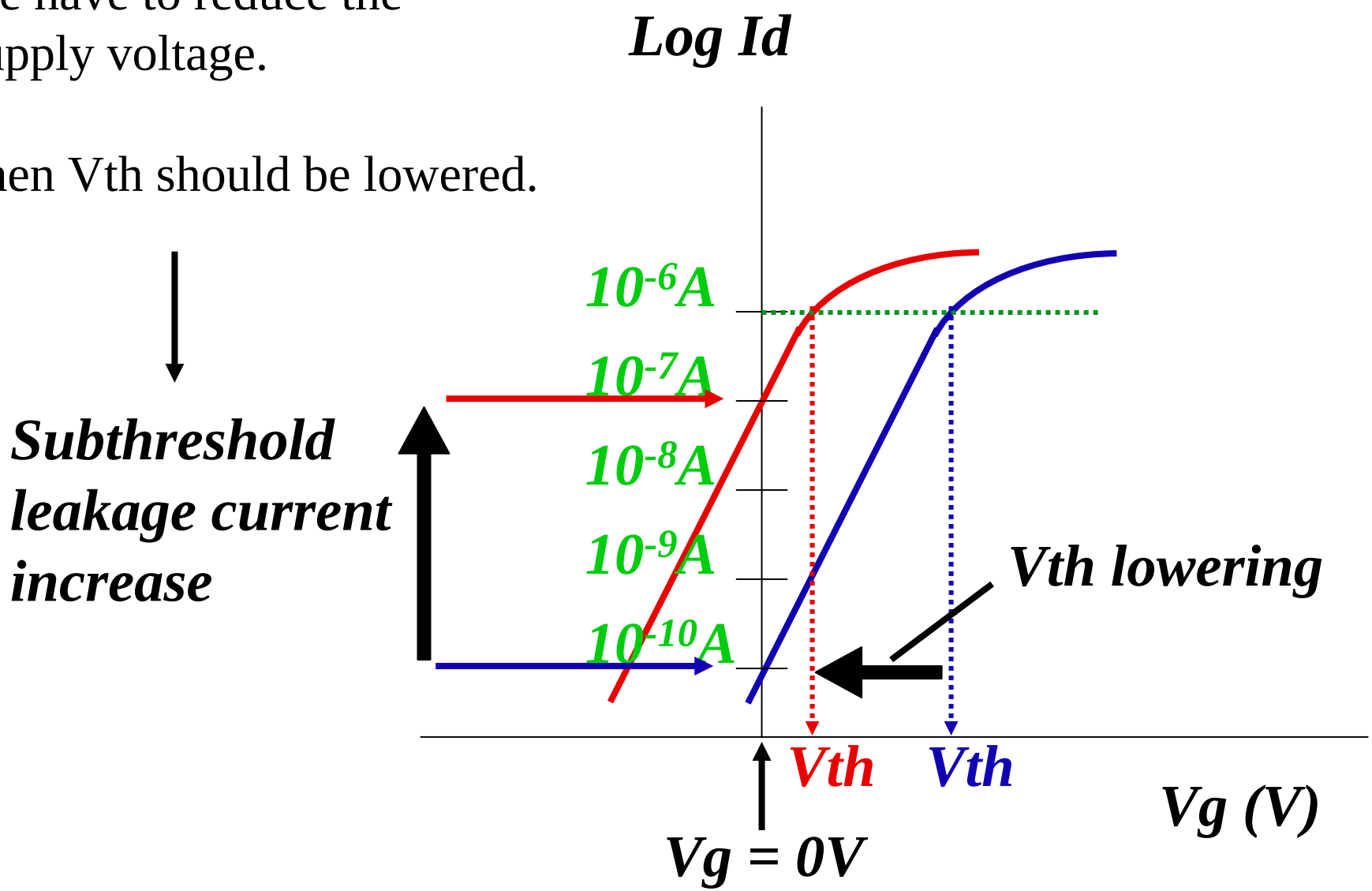


Subthreshold Current
Is OK at Single Tr.

But not OK
For Billions of Trs.

We have to reduce the Supply voltage.

Then Vth should be lowered.



微細化を阻む低電圧化の問題（今後はここを重点的に対処する必要あり）

1．Vd**低電圧化** → Vth**低電圧化をせざるを得ない**
→ Subthreshold**リーク電流の増大**
→ **消費電力の大半が**Subthreshold**リーク電流**

解決策：基板バイアス制御、FinFET**や**Nanowire FET**などの導入、、、、**

2．Vd**低電圧化** → **電源電圧変換ロスの急激な増大**
→ **消費電力の大半が電圧変換ロスに**

解決策：電圧変換回路のチップ内分散化、素子インピーダンスの低下（低抵抗化）、、、

半導体デバイスの消費電力化は$P=CV^2/2$（**即ちスケールファクターの3乗で減少**）

低電圧への変換ロスが$PLOSS=RI^2(=R/V^2)$（**スケールファクターのマイナス3乗で増加**）**で増加（チップ供給電力を一定としたとき）**

How about the integration of such small-geometry MOSFETs in a chip?

1)Integration of huge number of the ultra-small MOSFETs would consume too huge power and thus, creates too huge heat?

2)Integration of such ultra-small MOSFETs causes too huge variations in the transistor characteristics, which could make the circuit design impossible?

3)There are too many number of transistors in a chip for the circuit designers to manipulate? (design crisis),

4)There would be no merit of transistor downsizing in performance and power, because of RC (resistance capacitance product) of interconnect cannot be reduced aggressively any more?

5)Who will pay the huge development and production costs for the integration of such ultra-small MOSFETs? Note that the prices for the recent process equipments and the lithography mask became extremely high.

These concerns have been argued in the past 15 years at every new generation of the products, like the wolf boy.

Fortunately, the wolf has not come, and the concerns have not come true.

It is expected that we can go with several more generations for the integration.

There will be still a room for squeezing the technologies to obtain the merit of the scaling-down for integration.

The continuous progress of CMOS technologies for
- high-performance
- low power

is very important because of the 3 reasons:

1) Rapid progress of aging population and falling birth rate

1) Global warming

1) Semiconductor industry and world economy

1)Rapid progress of aging population and falling birth rate:

Replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example.

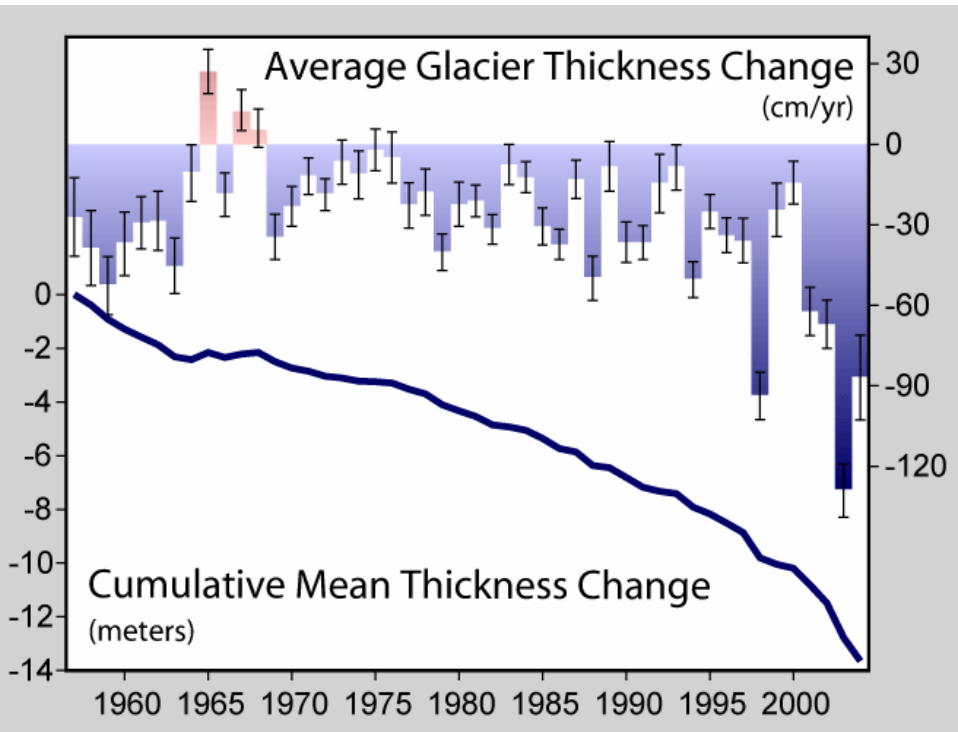
For, the daily family use, much higher intelligence and much lower power consumption than those of today are required.

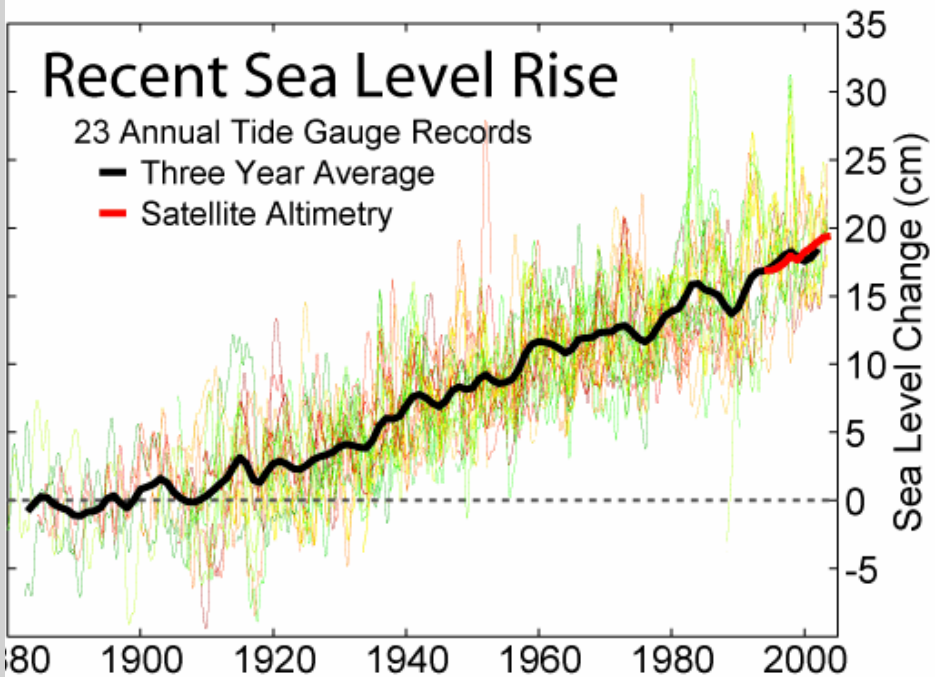
Robot in 21c cannot made without integrated circuits

Robot (21C)

Karakuri (Windup Mechanical) doll (18C) in Japan

2) Recent Significant Global Warming

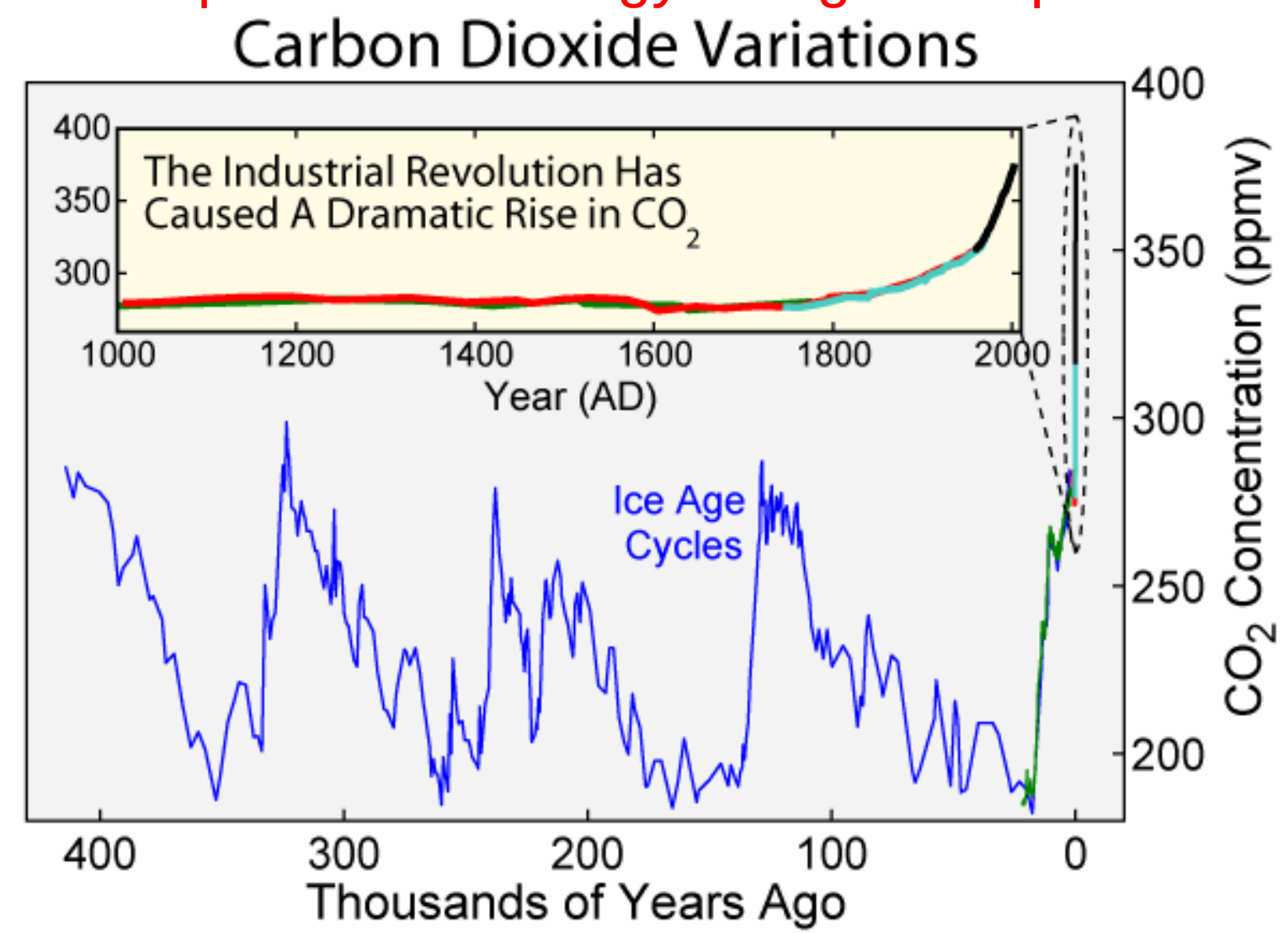




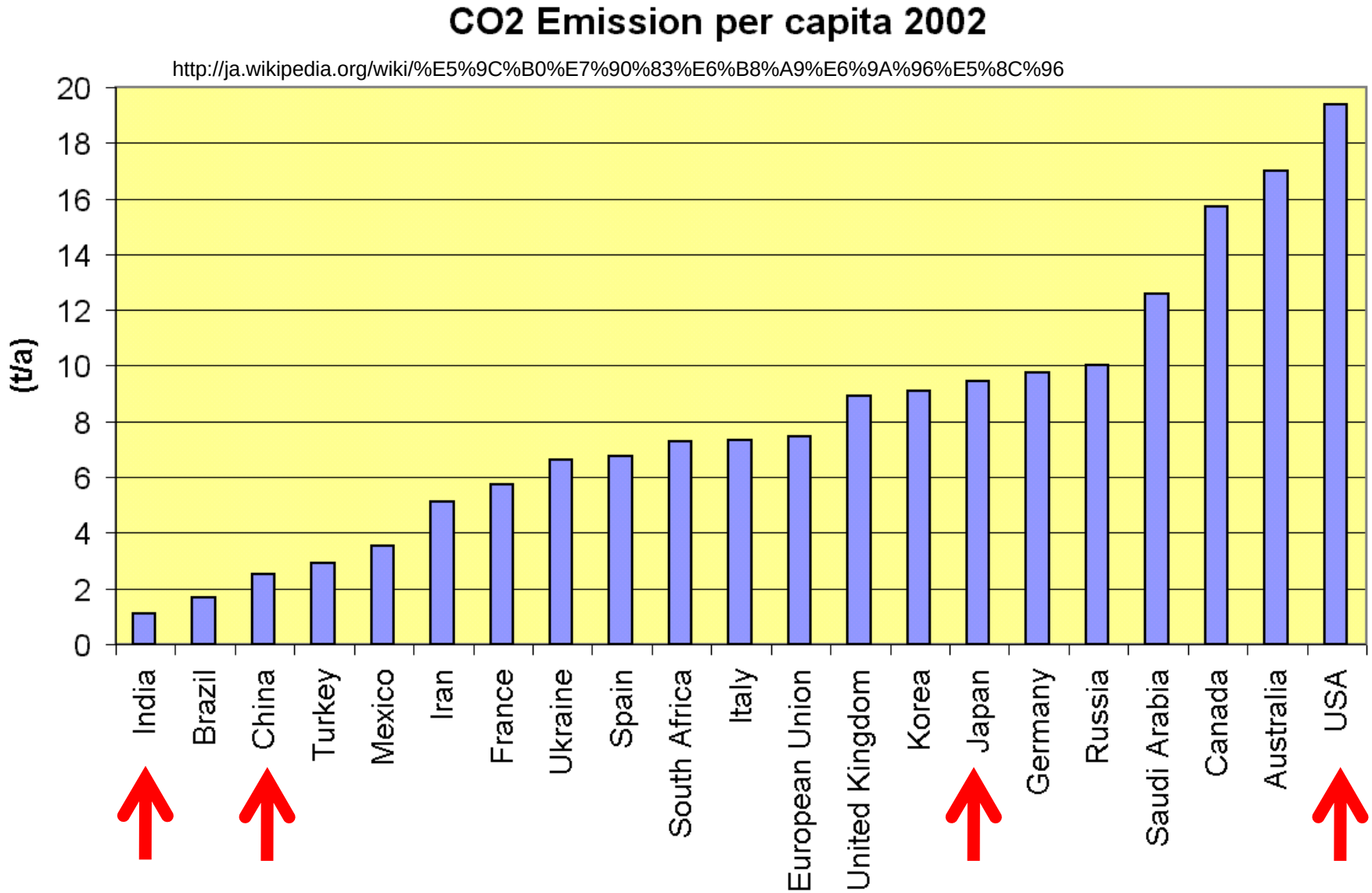
http://ja.wikipedia.org/wiki/%E5%9C%B0%E7%90%83%E6%B8%A9%E6%9A%96%E5%8C%96

We need to reduce CO_2 generation!

→ Low power technology is urgent request



http://ja.wikipedia.org/wiki/%E5%9C%B0%E7%90%83%E6%B8%A9%E6%9A%96%E5%8C%96



ＣＯ２ガス排出削減の緊急度やその効果に関しては色々と議論はあるが、人類の活動により地球の環境をこれ以上悪化させてはならないことと、化石燃料には限りがあるという観点から、早晩着手をしなければならない事柄である。

3) Semiconductor industry, and world economy

If there is no more downsizing such as
45 → 32 nm Logic, 8 Gbit → 16 Gbit Memory

- LSIs will not be sold well, and semiconductor companies will face a disaster.

- Equipment and martial companies as well.

-There is no more R & D for semiconductors and many people will loose their jobs.

→ World economy crisis!

History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking!

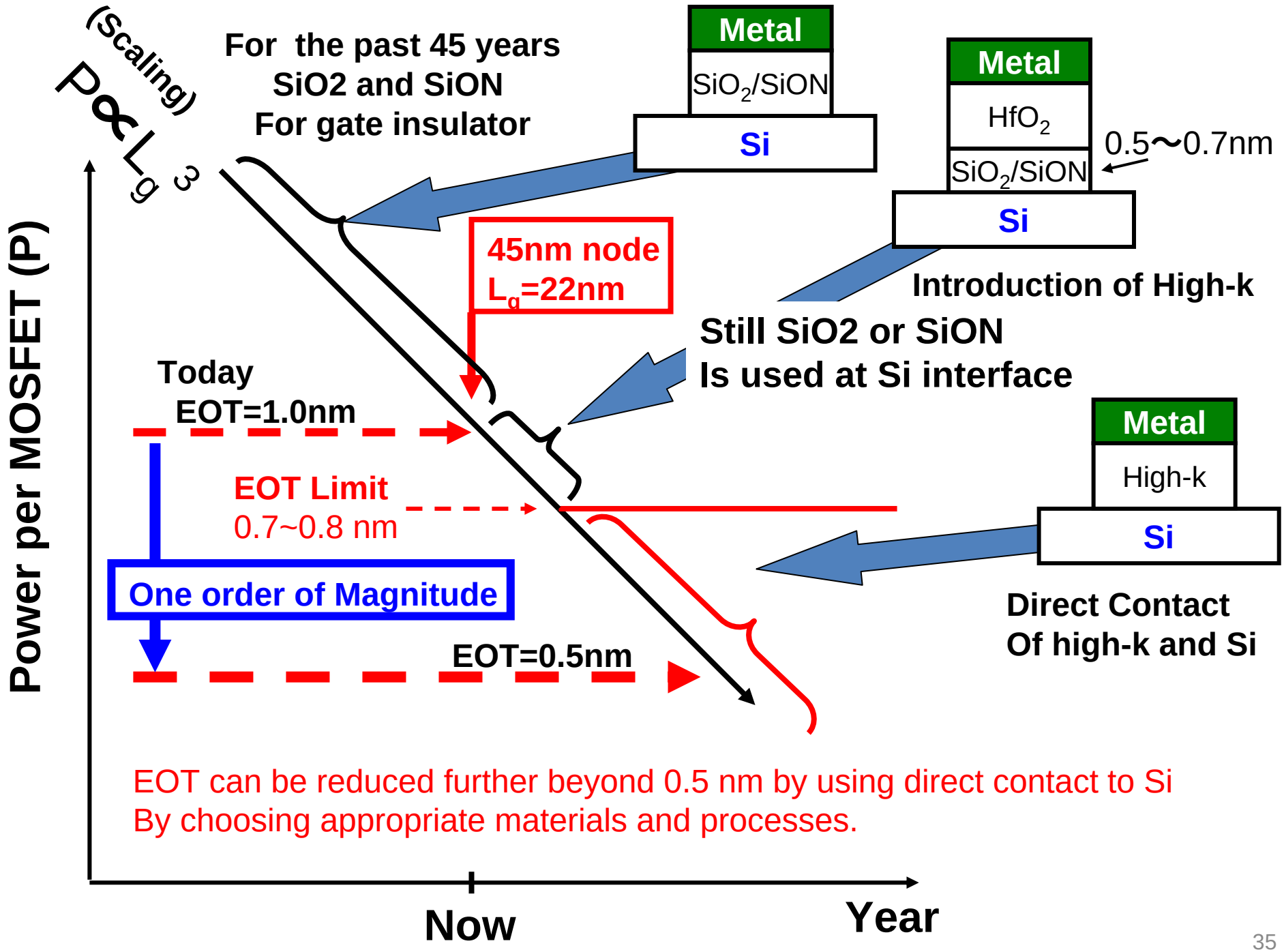
C, V $\propto$ L C: Capacitance V: Voltage

Switching speed CV/I → Decrease

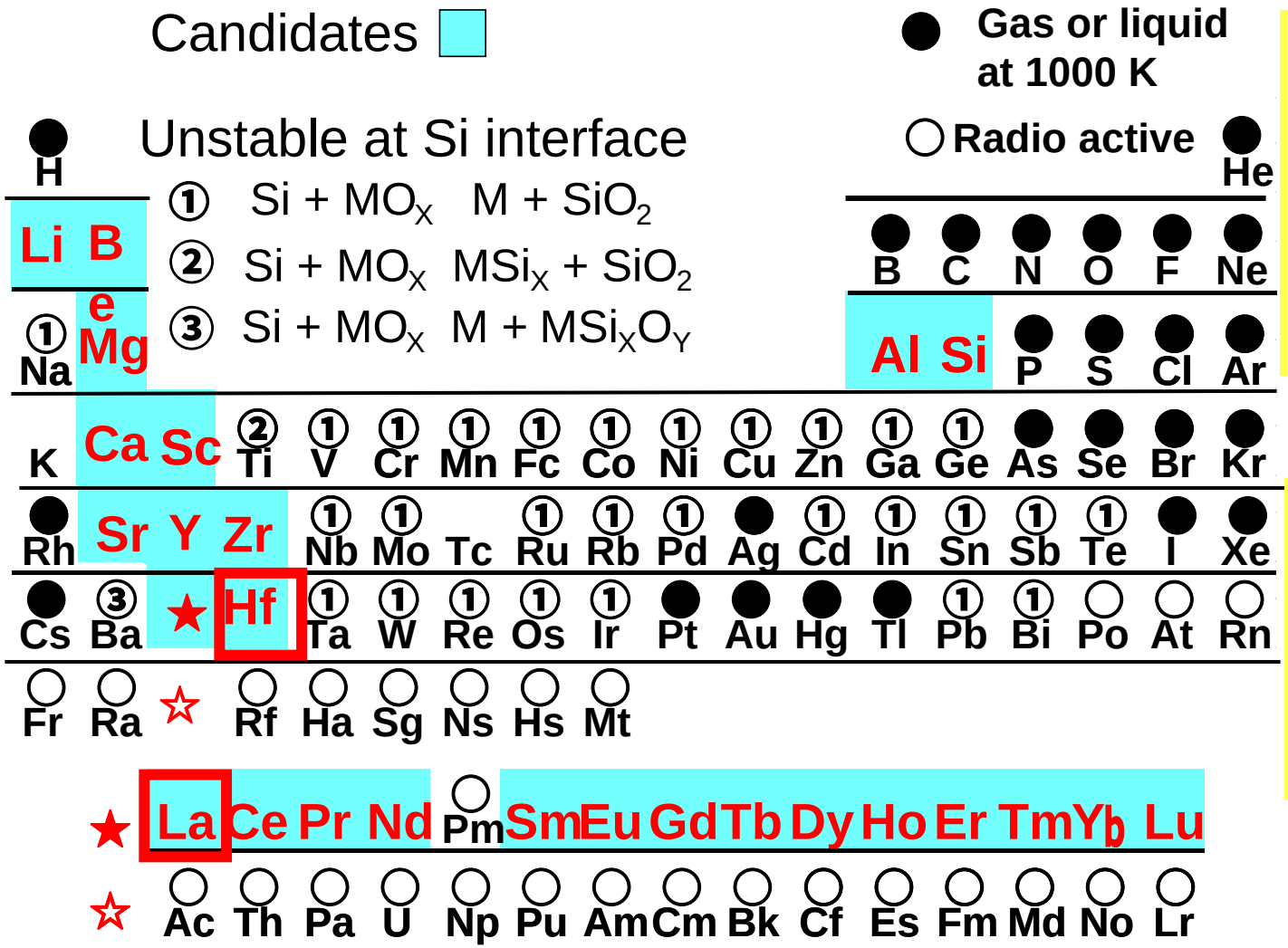
Power consumption $CV^2/2$ → Decrease

Integration density: $1/L^2$ → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm


(scaling)
P∝Lg 3
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
SiO2/SiON
Si
0.5~0.7nm
45nm node
Lg=22nm
Introduction of High-k
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
One order of Magnitude
EOT=0.5nm
Metal
High-k
Si
Direct Contact
Of high-k and Si
Power per MOSFET (P)
Now
Year
EOT can be reduced further beyond 0.5 nm by using direct contact to Si
By choosing appropriate materials and processes.

Choice of High-k elements for oxide



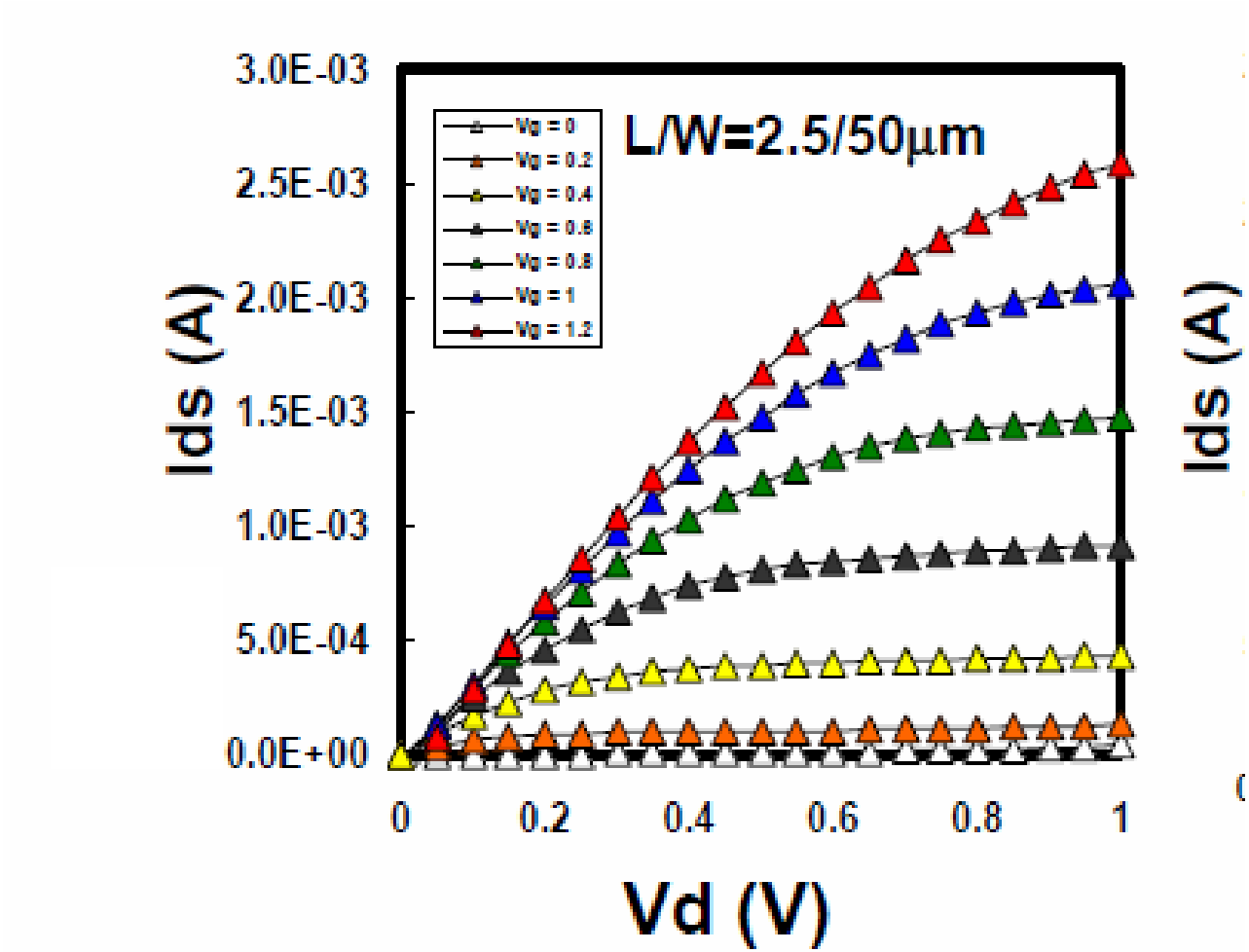
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

EOT = 0.48 nm Our results

Transistor with La2O3 gate insulator



CMOS downsizing is critically important

However now, many people expect that we will reach limit in 2020.

Totally, new paradigm after reaching the downsizing limit.

What will be?

After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.

After 2020

4 reasons for no downsizing anymore
or No decrease in gate length

---

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.
   Ballistic ← No scattering of carriers in channel
   Thus, all the carrier from the source reach drain

2. Increase of Off-current (Subthreshold current)

3. No decrease of Gate capacitance by parasitic components

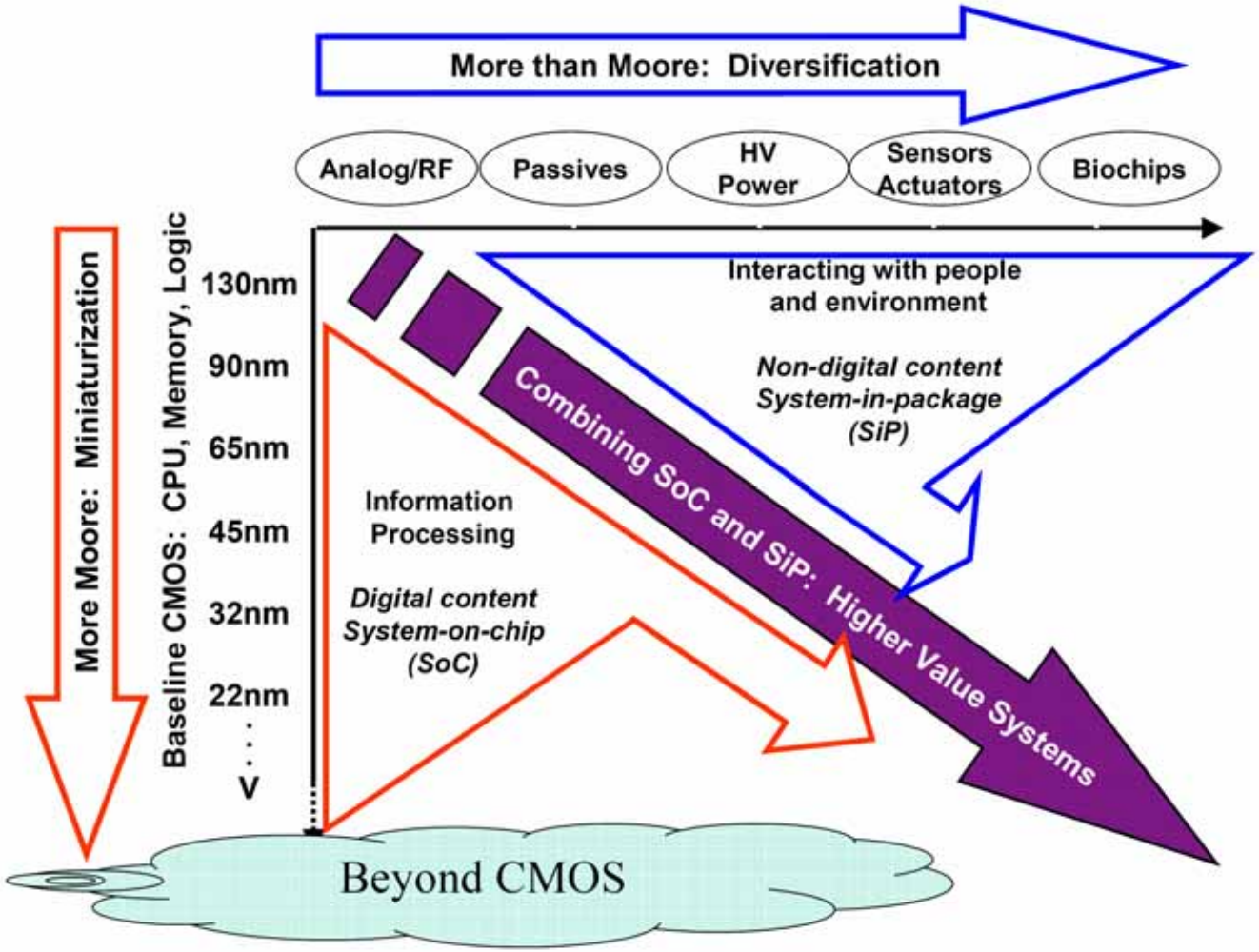
4. Increase in production cost.

After 2020

What will be the world with no gate length reduction?

More Moore and More than Moore

Moore's Law & More

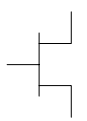
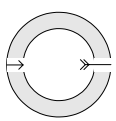
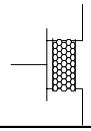
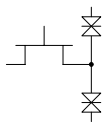
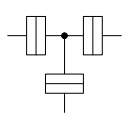
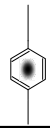
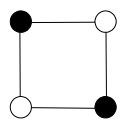
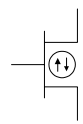


Question what is the other side of the cloud?

ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

Victor V. Zhirnov and Ralph K. Cavin III, ECS 207
Washington DC

Device								
	FET	*RSFQ*	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*	*Spin transistor*
Cell Size	100 nm	0.3 μm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density (cm^{-2})	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4\times10^{-17}$	2×10^{-18}	$>2\times10^{-18}$	$>1.5\times10^{-17}$	1.3×10^{-16}	$>1\times10^{-18}$	2×10^{-18}
Binary Throughput, GBit/ns/cm^2	86	0.4	86	86	10	N/A	0.06	86

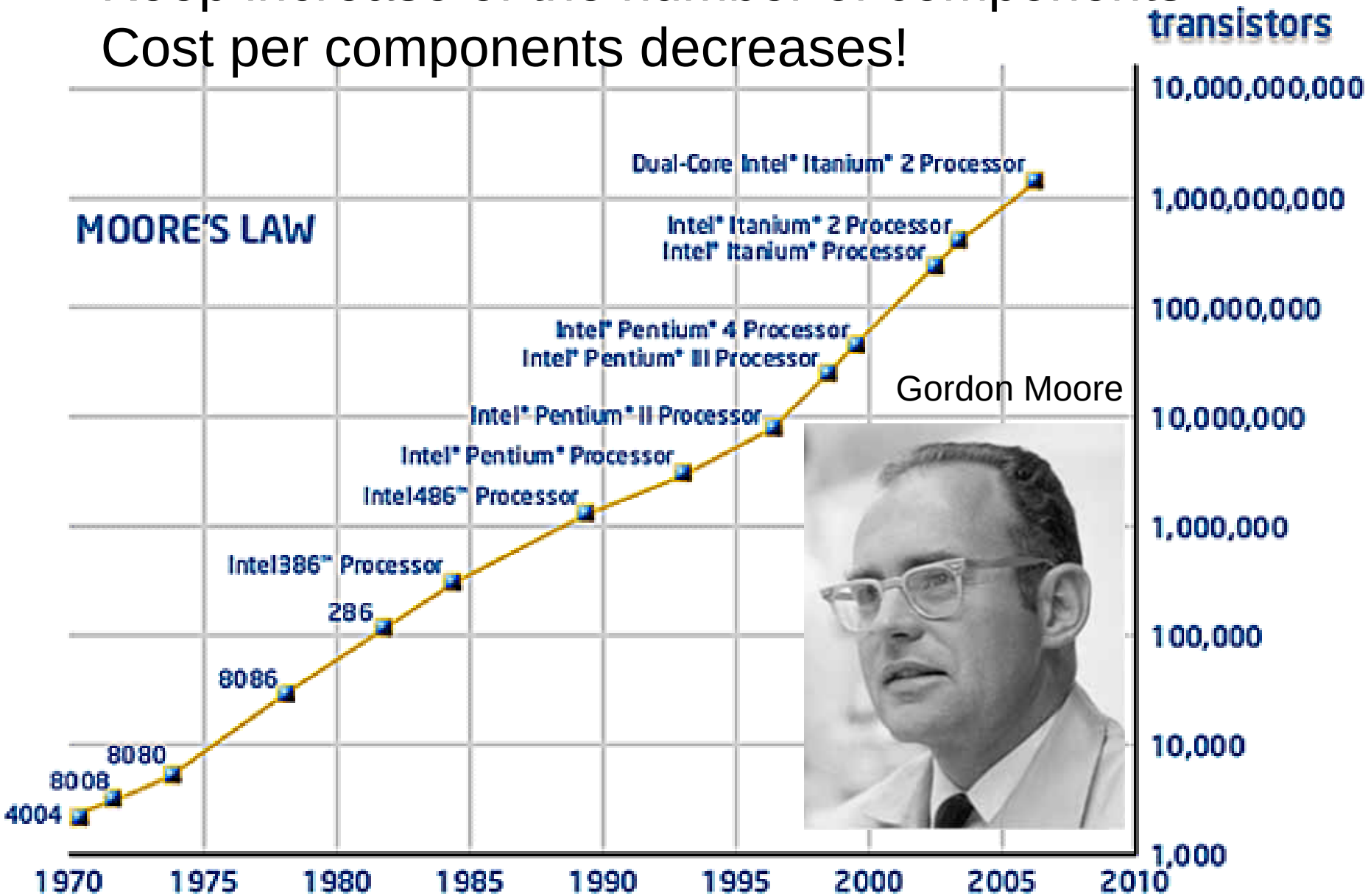
We HAVE IDENTIFIED NO VIABLE EMERGING LOGIC TECHNOLOGIES for Information Processing beyond CMOS

43

We could keep the Moore’s law after 2020
Without downswing the gate length

What is Moore’s law.

Keep increase of the number of components.
Cost per components decreases!



http://www.intel.com/technology/mooreslaw/index.htm

We could keep the Moore's law after 2020
Without downswing the gate length

What is Moore's law.

→ to increase the number (#) of Tr. In a chip

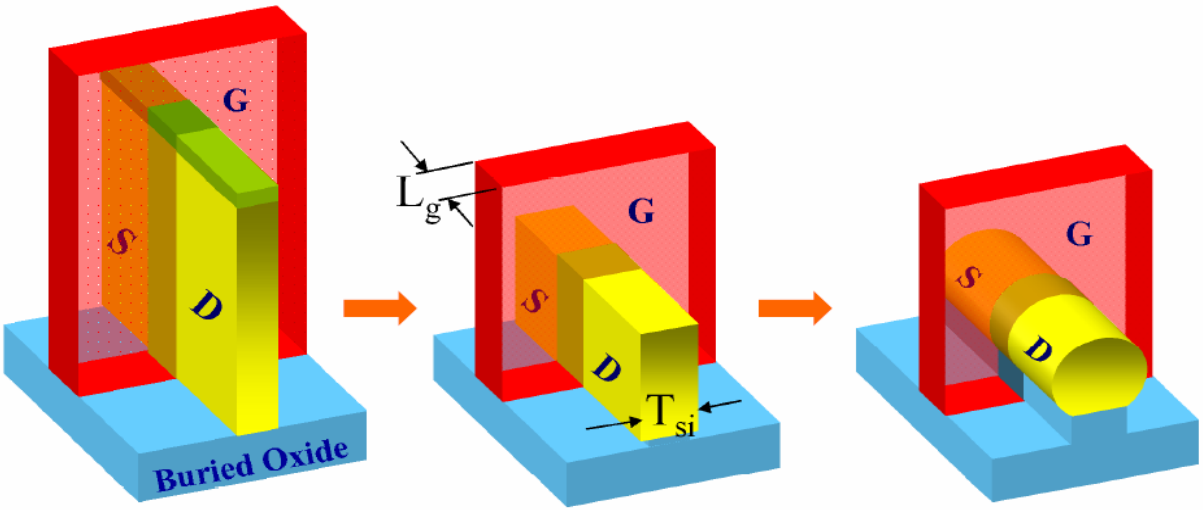
Now, # of Tr. in a chip is limited by power.

→ key issue is to reduce the power.

→ to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.

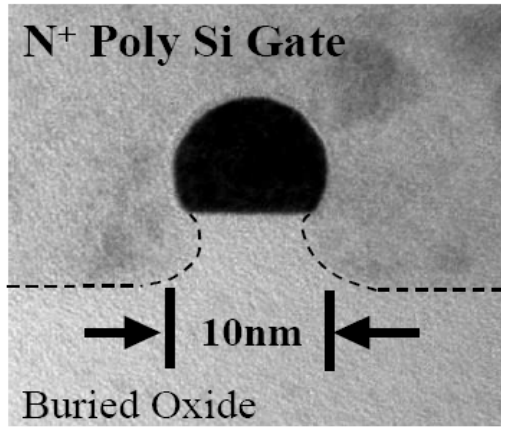
FinFET to Nanowire

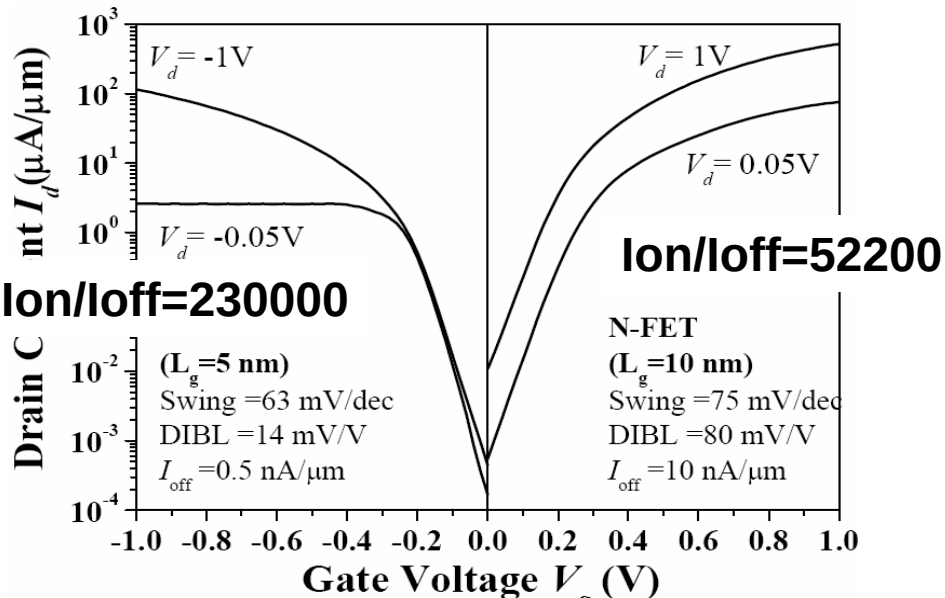


Double-Gate FinFET ($T_{si} = {}^{2}/_{3}\, L_g$)

Omega FinFET ($T_{si} = L_g$)

Nanowire FinFET ($T_{si} = 2L_g$)





Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1. Use 1D ballistic conduction

M2. Increase number of quantum channel

M3. Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.

1D conduction per one quantum channel:

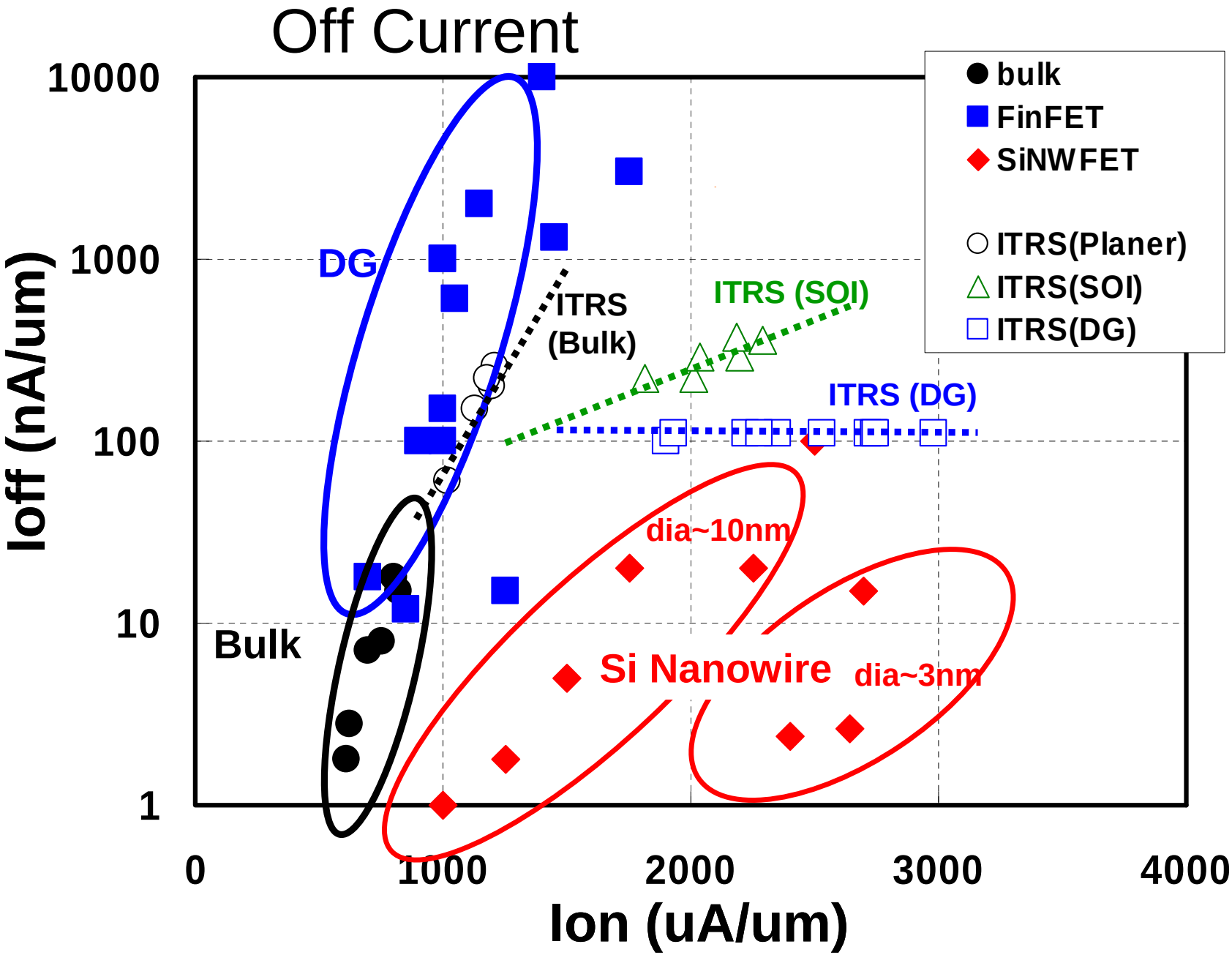
$G = 2e^2/h = 78\ \mu S$/wire or tube

regardless of gate length and channel material

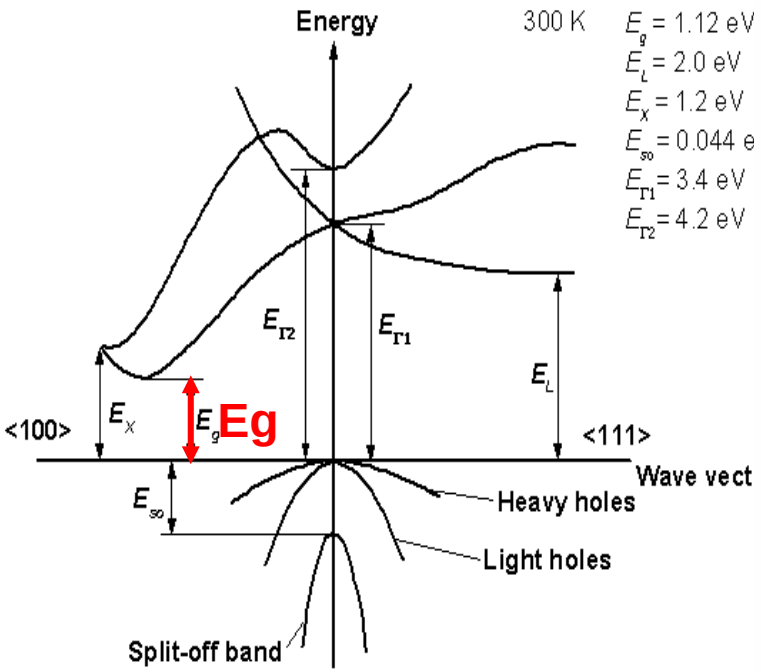
That is 78 μA/wire at 1V supply

This an extremely high value

However, already 20mA/wire was obtained experimentaly by Samsung

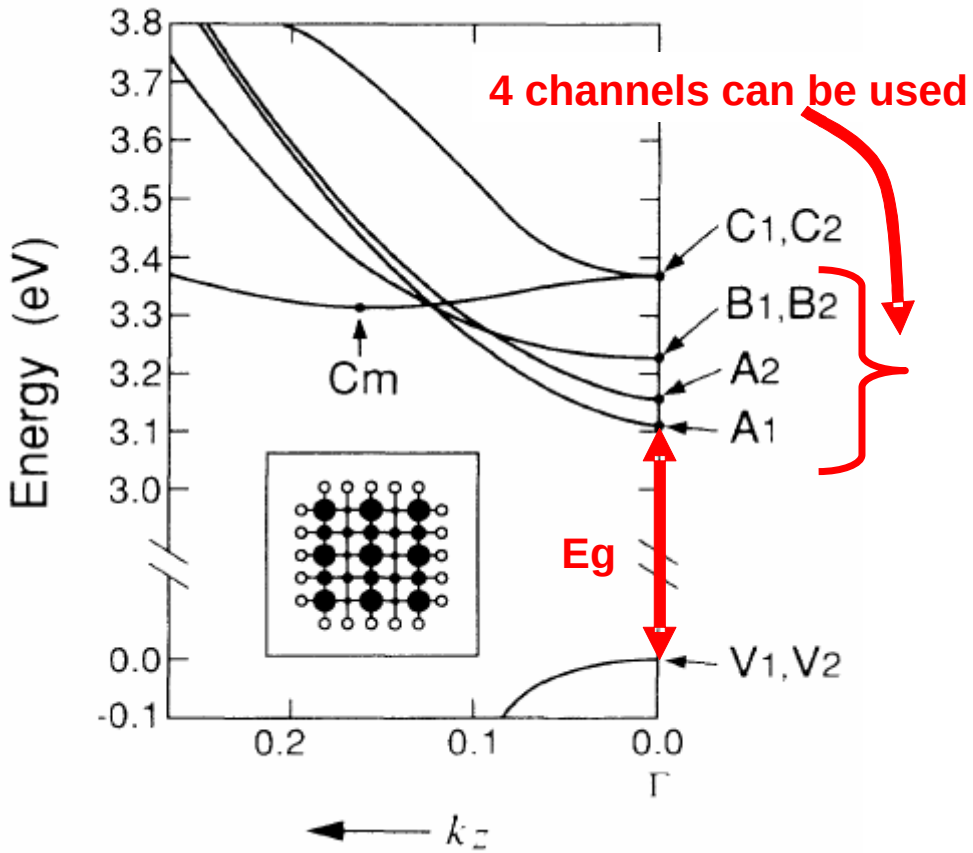

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels



Energy band of Bulk Si

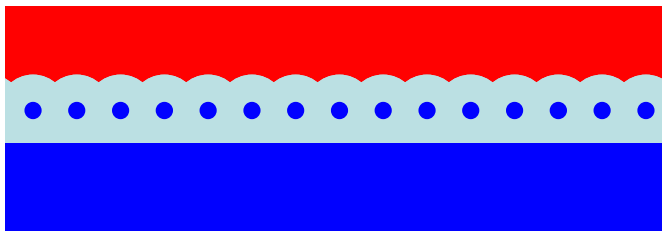
By Prof. Shiraishi of Tsukuba univ.



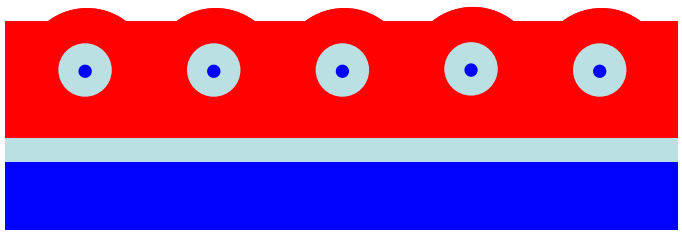
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

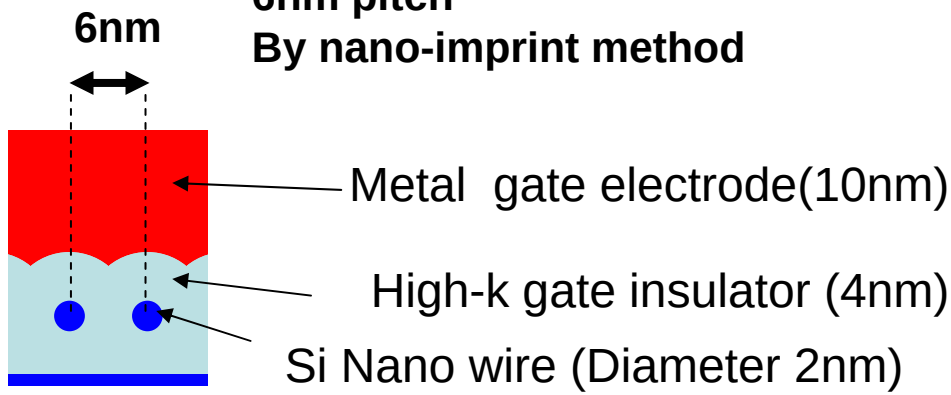
Front gate type MOS 165 wires /μm

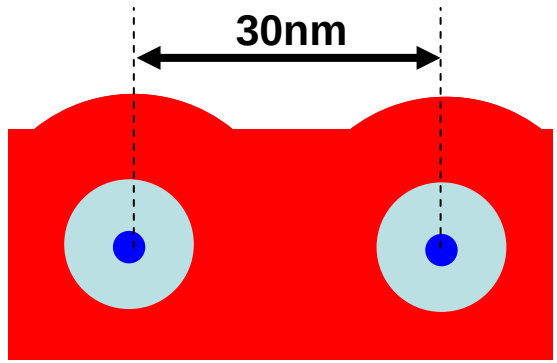


Surrounded gate type MOS 33 wires/μm

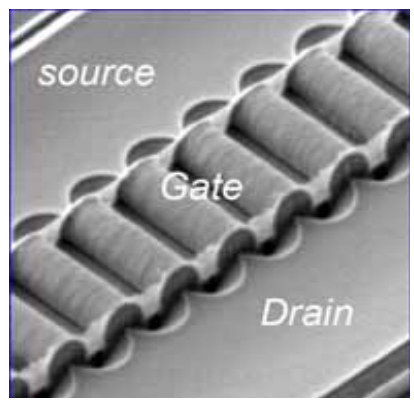


6nm pitch
By nano-imprint method



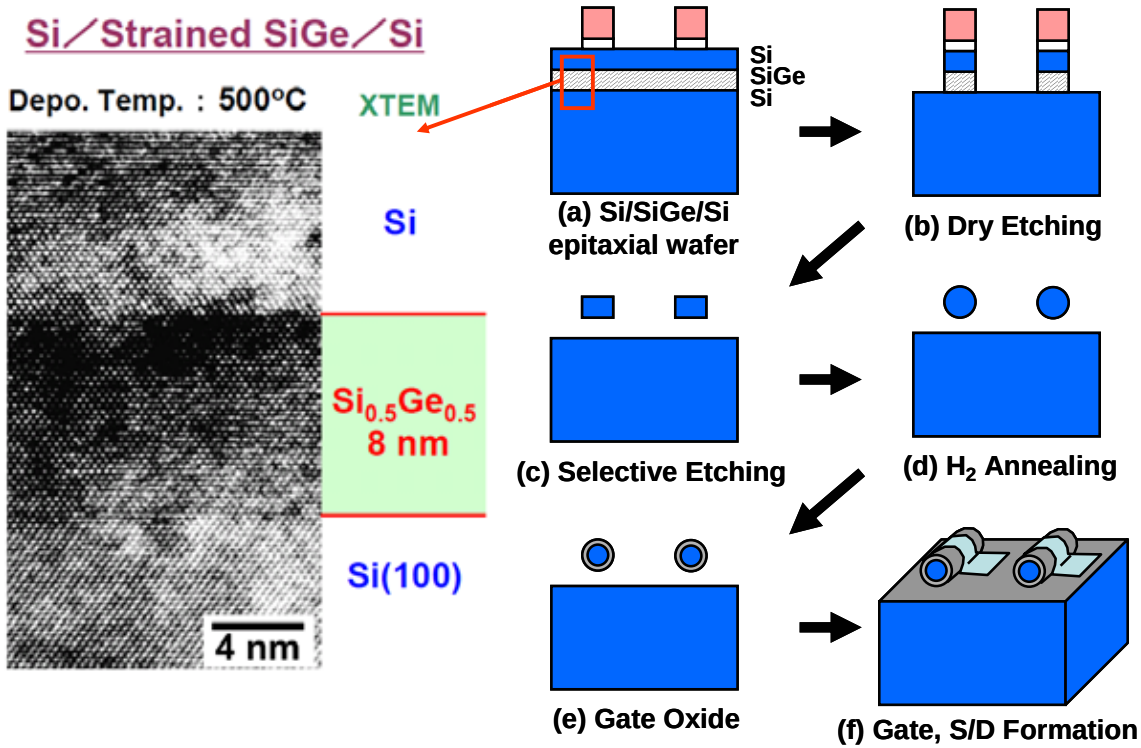


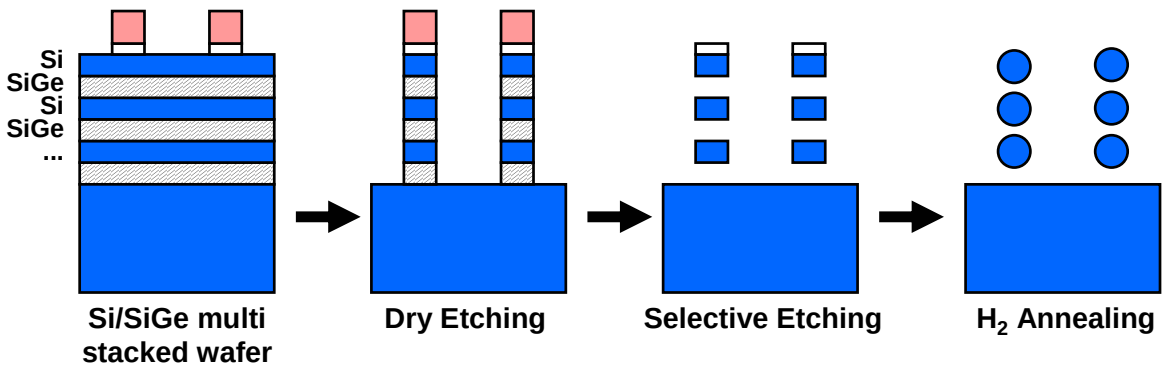
30nm pitch:
EUV lithograpy

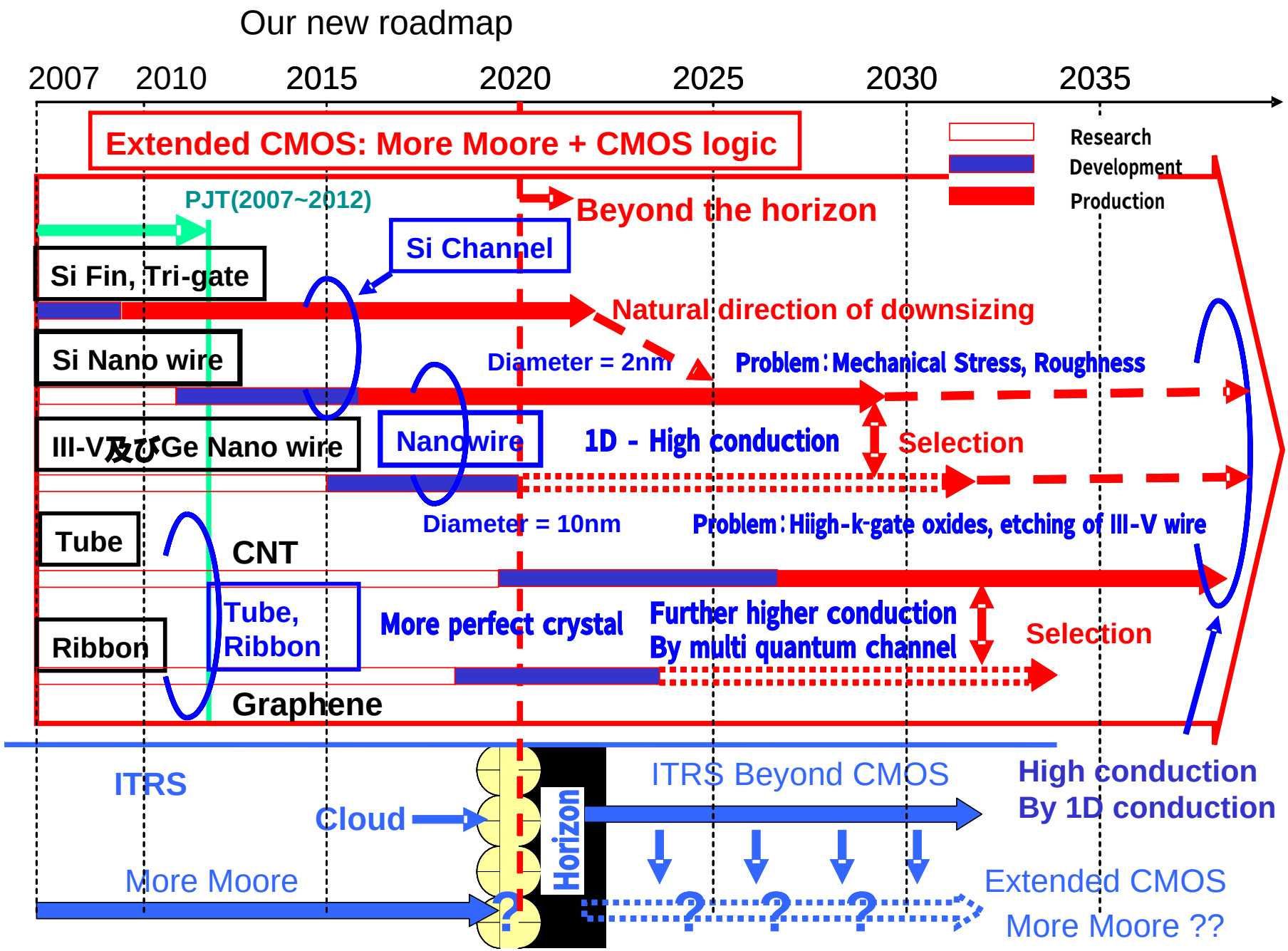


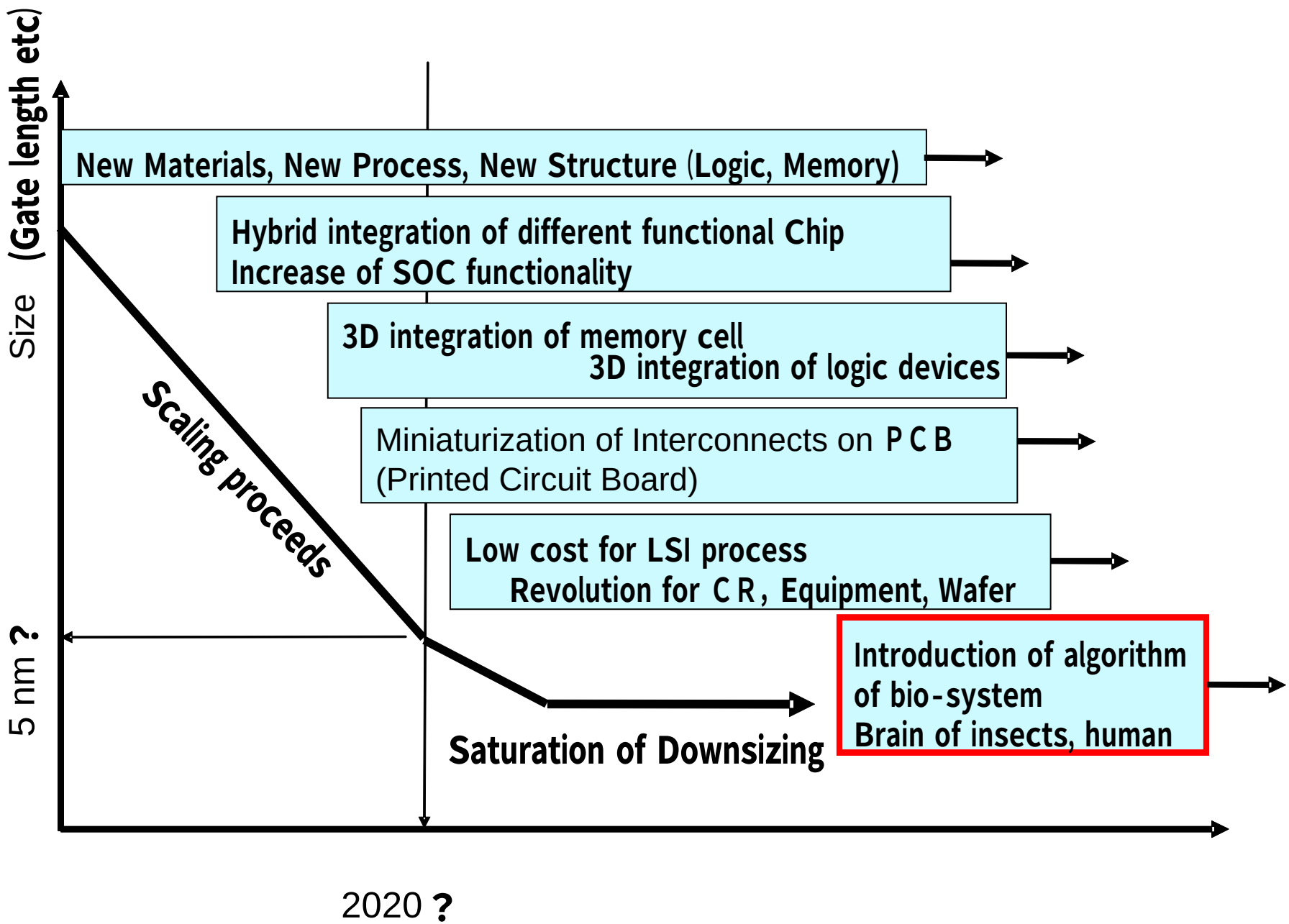
Surrounded gate MOS

Increase the number of wires towards vertical dimension






Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V及びGe Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Graphene
ITRS
Cloud
More Moore
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
Extended CMOS
More Moore ??


Size (Gate length etc)
New Materials, New Process, New Structure (Logic, Memory)
Hybrid integration of different functional Chip
Increase of SOC functionality
3D integration of memory cell
3D integration of logic devices
Miniaturization of Interconnects on P C B
(Printed Circuit Board)
Low cost for LSI process
Revolution for C R, Equipment, Wafer
Introduction of algorithm
of bio-system
Brain of insects, human
Scaling proceeds
Saturation of Downsizing
5 nm ?
2020 ?

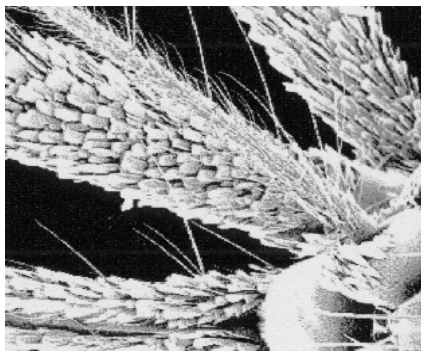
Brain

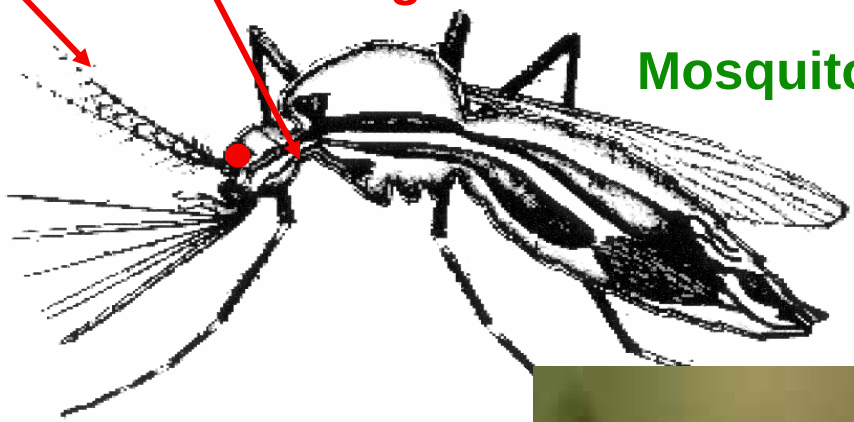
Ultra small volume
Small number of neuron cells
Extremely low power

Sensor

Infrared
Humidity
CO_2

Real time image processing
(Artificial) Intelligence
3D flight control





Mosquito

System and Algorism becomes more important!

But do not know how?

Dragonfly is further high performance

今後の取り組むべき姿

1. 2020年まではMore Mooreを徹底的に追究
   徹底的によるメリットを搾り出す
   → 未だ未だ材料選択,構造設計で微細化のメリットを引きだすことが可能
   → 未だに微細化を制するものは世界を制す

   低電圧化の諸問題が微細化の鍵を握る

2. More than Moore（多チップや素子のハイブリッド集積化）は当然重要

3. その後の対策としては、ワイヤ系、チューブ系ＦＥＴの検討が重要

4. いわゆるBeyond ＣＭＯＳ素子に関しては、個別の技術研究も価値はあるが、
   原理的にＣＭＯＳに打ち勝つことができるのか、またその為には何が必要か
   を可視化、明確化することが重要

5. 昆虫の脳など、現在のＣＭＯＳロジックと比べ何桁も高性能、低消費
   エネルギーシステムの構造解析、アルゴリズム解析が今後の重要な課題

御清聴有難う御座居ました