

# **Past and future for micro- and nano-electronics, focusing on Si integrated circuits technology**

**June 4, 2008**

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Needless to say, but....

CMOS Technology:

Indispensable for our human society

All the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and  
world economical activities immediately stop.

Cellarer phone dose not exists

# CMOS experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
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1960s	IC (Integrated Circuits)	~ 10
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1970s	LSI (Large Scale Integrated Circuit)	~1,000
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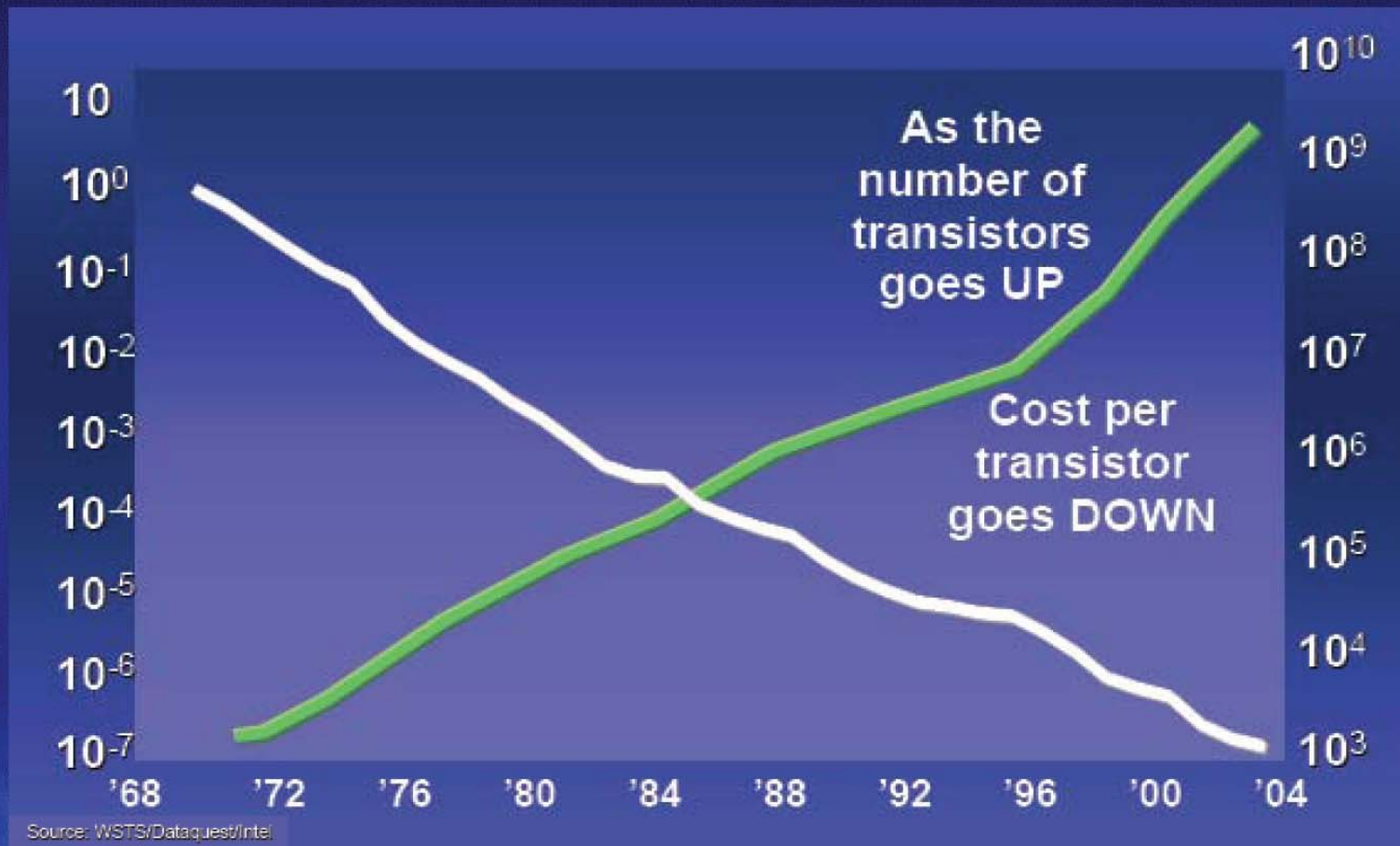
1980s	VLSI (Very Large Scale IC)	~10,000
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1990s	ULSI (Ultra Large Scale IC)	~1,000,000
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2000s	?LSI (? Large Scale IC)	~1000,000,000
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# Exponential Cost Reduction

## Cost per Transistor



# Downsizing of the components has been the driving force for circuit evolution



1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 $\mu\text{m}$	100 nm
$10^{-1}\text{m}$	$10^{-2}\text{m}$	$10^{-3}\text{m}$	$10^{-5}\text{m}$	$10^{-7}\text{m}$

In 100 years, the size reduced by one million times.  
There have been many devices from stone age.

**We have never experienced such a tremendous reduction of devices in human history.**

# Downsizing

## **1. Reduce Capacitance**

**→ Reduce switching time of MOSFETs**

Reduce power consumption

## **2. Increase number of Transistors**

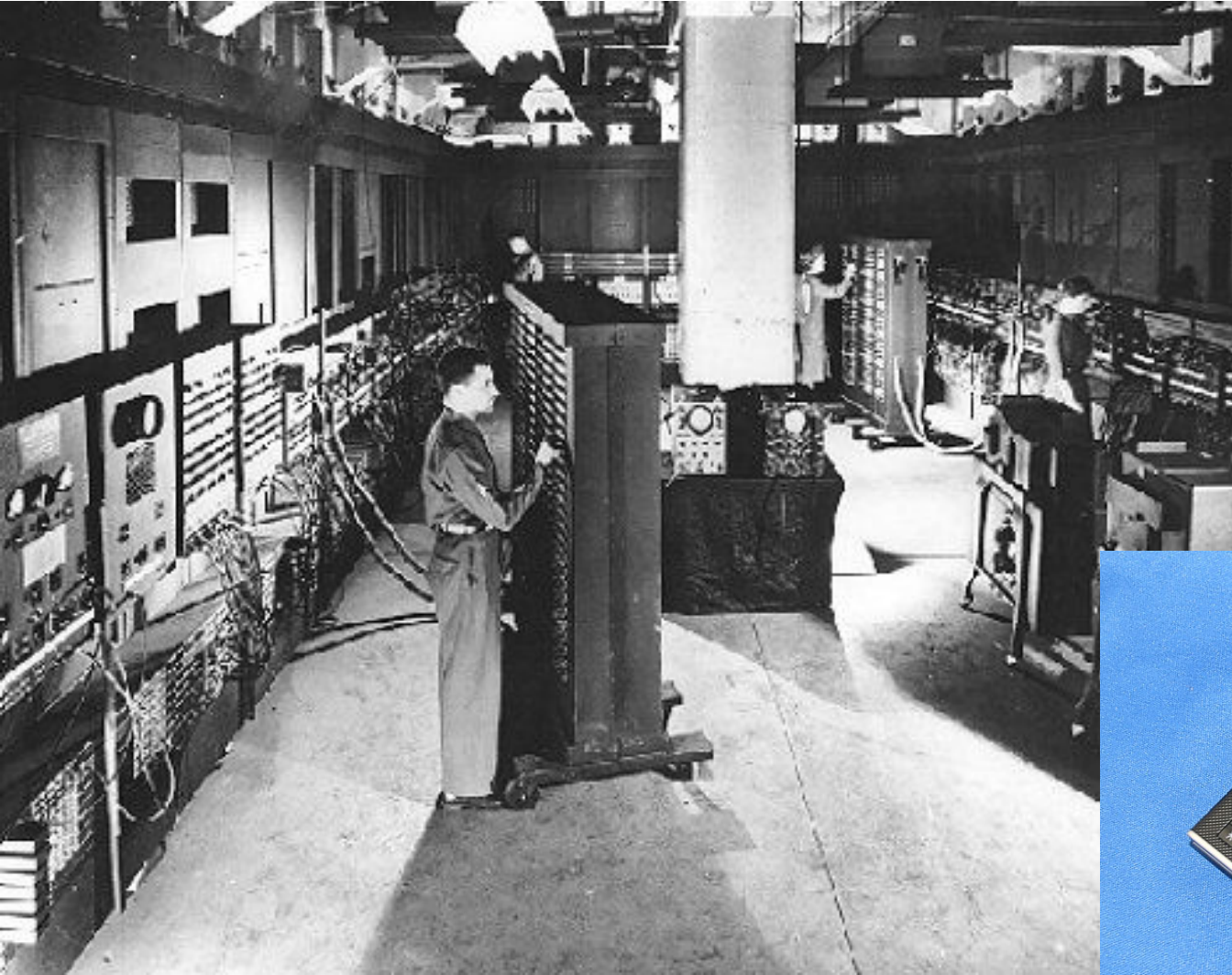
Increase functionality

**→ Parallel processing**

**→ Increase circuit operation speed**

Thus, downsizing of Si devices is the most important and critical issue.

First Computer Eniac: made of huge number of vacuum tubes 1946  
Big size, huge power, short life time filament



Today's pocket PC  
has much higher  
performance with  
extremely low  
power consumption



# Many people wanted to say about the limit. Past predictions were not correct!!

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Period	Expected limit(size)	Cause
Late 1970's	1 $\mu$ m:	SCE
Early 1980's	0.5 $\mu$ m:	S/D resistance
Early 1980's	0.25 $\mu$ m:	Direct-tunneling of gate SiO <sub>2</sub>
Late 1980's	0.1 $\mu$ m:	'0.1 $\mu$ m brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

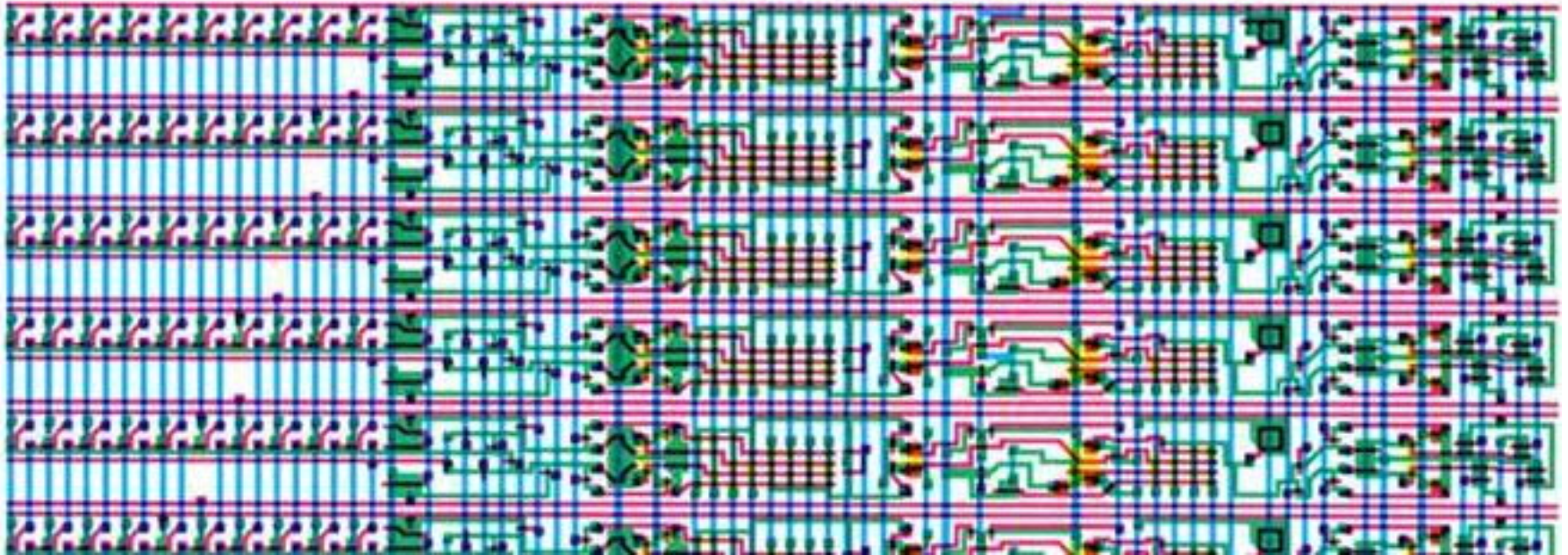


Historically, many predictions of the limit of downsizing.

**VLSI text book written 1979 predict that 0.25 micrometer would be the limit because of direct-tunneling current through the very thin-gate oxide.**

# INTRODUCTION TO **VLSI** SYSTEMS

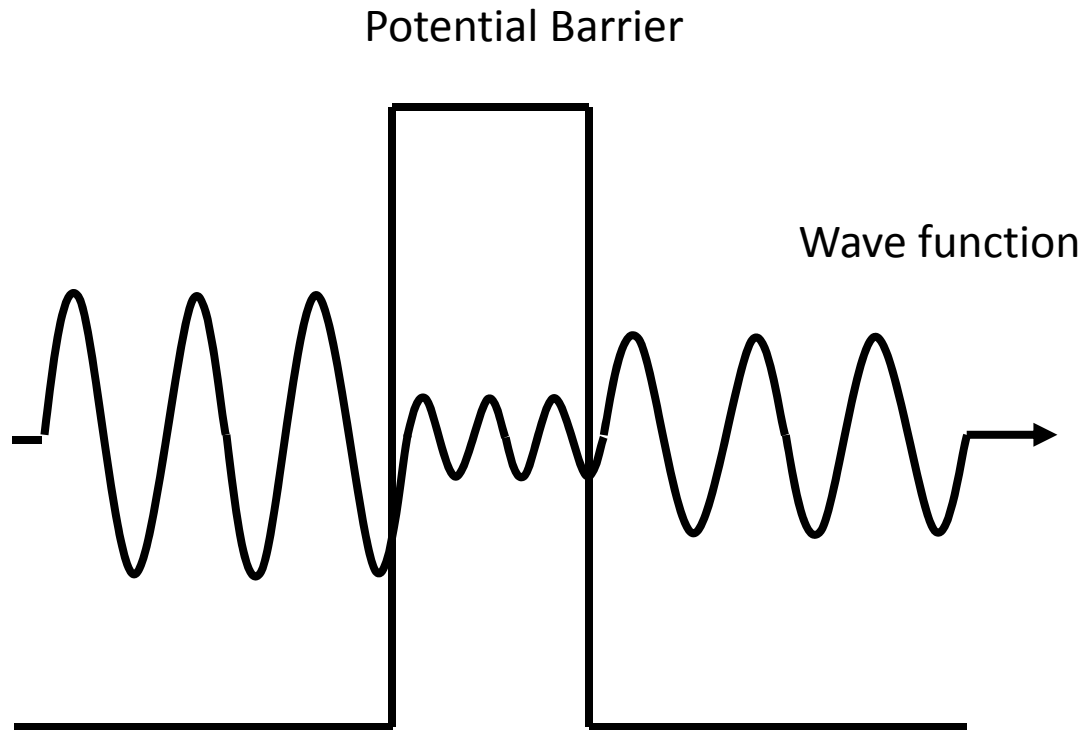
CARVER MEAD • LYNN CONWAY



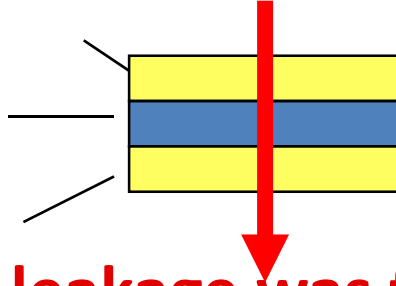
# VLSI textbook

**Finally, there appears to be a fundamental limit <sup>10</sup> of approximately quarter micron channel length, where certain physical effects such as the **tunneling through the gate oxide** and **fluctuations in the positions of impurities** in the depletion layers begin to make the devices of smaller dimension unworkable.**

# Direct-tunneling effect



Gate electrode  
Gate oxide  
Si substrate



Direct tunneling leakage current start to flow when the thickness is 3 nm.

**Direct tunneling leakage was found to be OK! In 1994!**

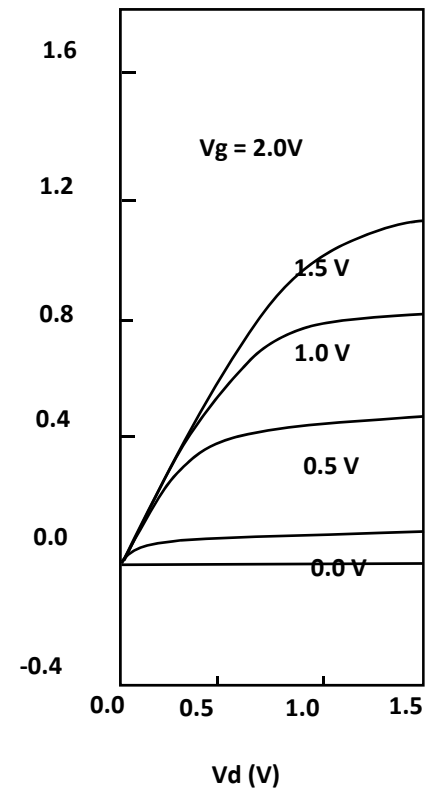
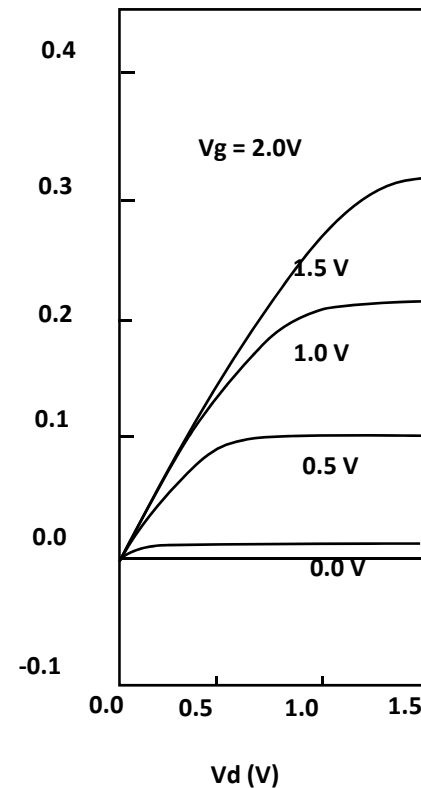
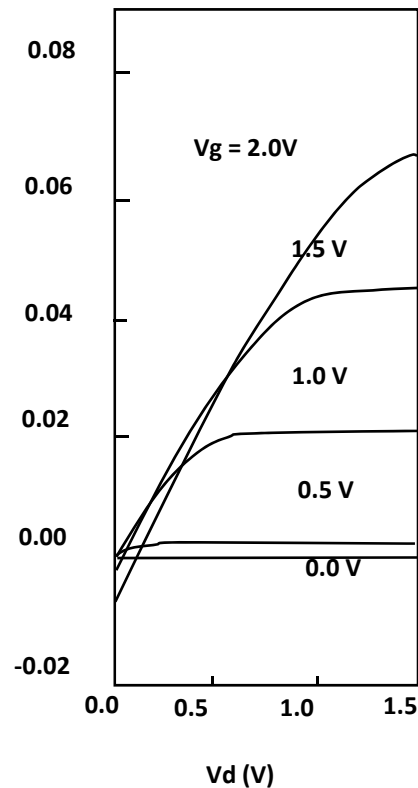
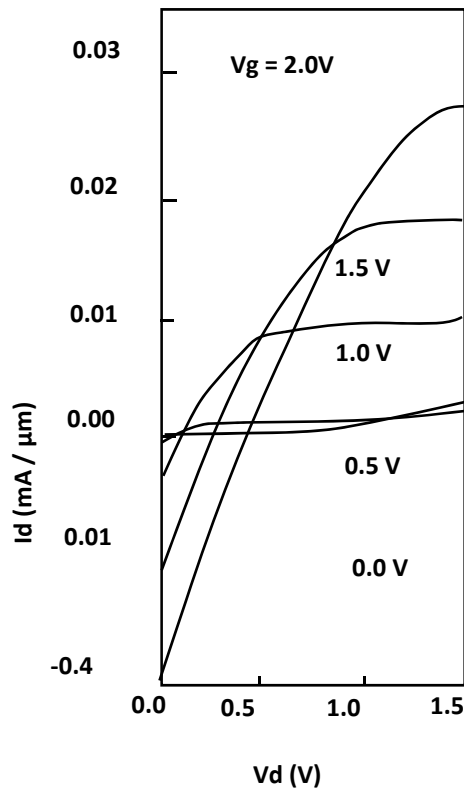
MOSFETs with 1.5 nm gate oxide

$L_g = 10 \mu\text{m}$

$L_g = 5 \mu\text{m}$

$L_g = 1.0 \mu\text{m}$

$L_g = 0.1 \mu\text{m}$



**Do not believe a text book statement, blindly!**

**Never Give Up!**

**No one knows future!**

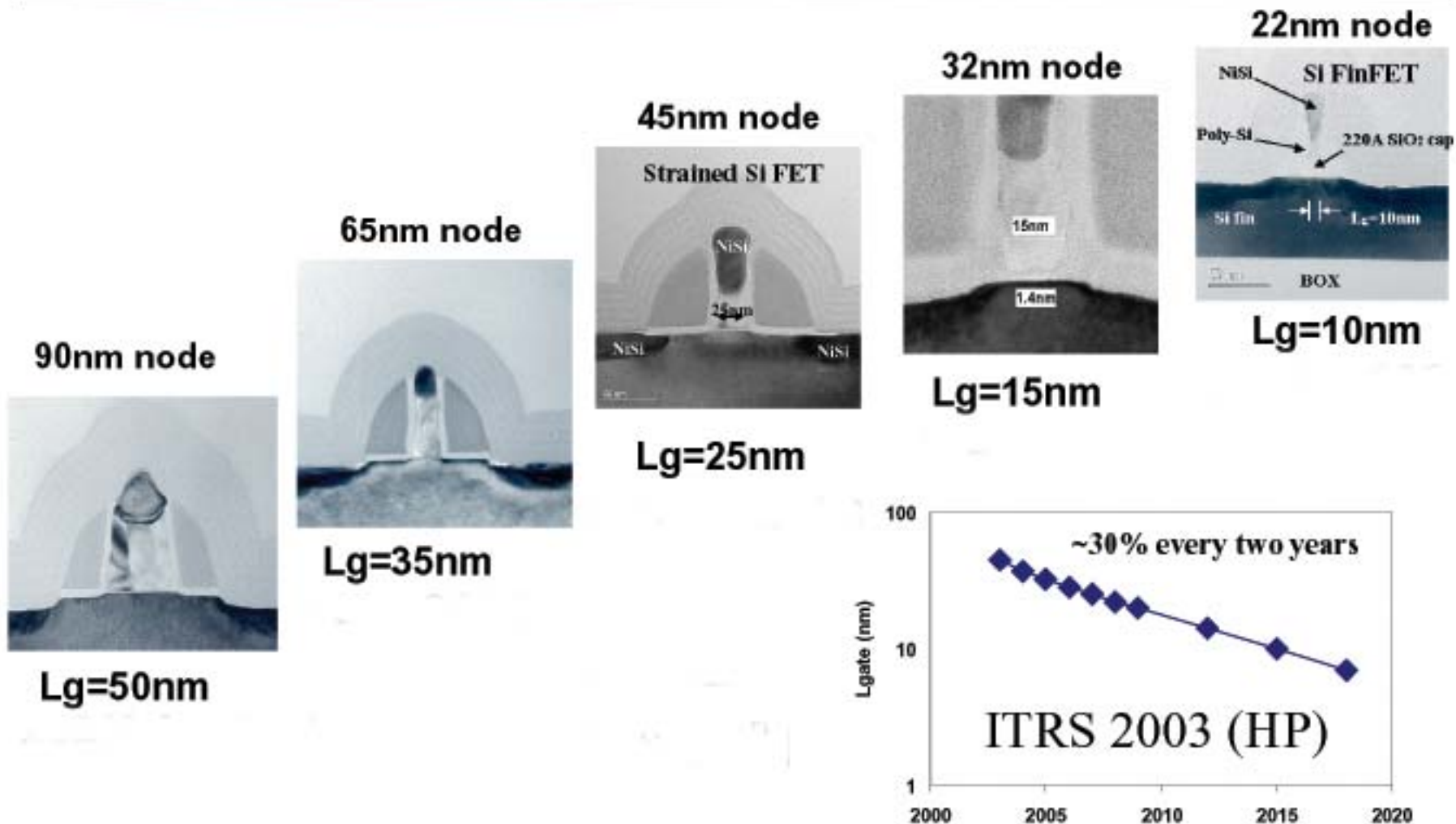
**There would be a solution!**

**Think, Think, and Think!**

**Or, Wait the time!**

**Some one will think for you**

# Transistor Scaling Continues

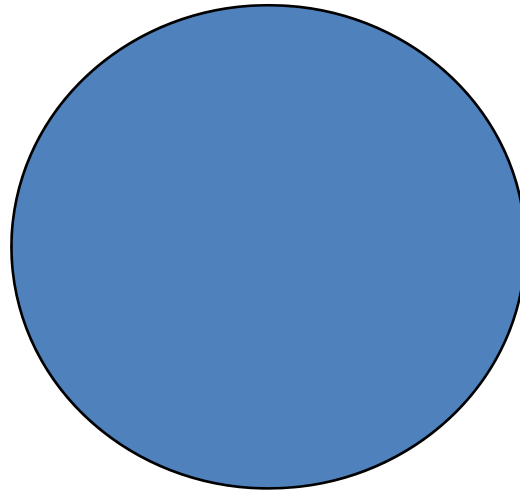


# Downsizing limit?

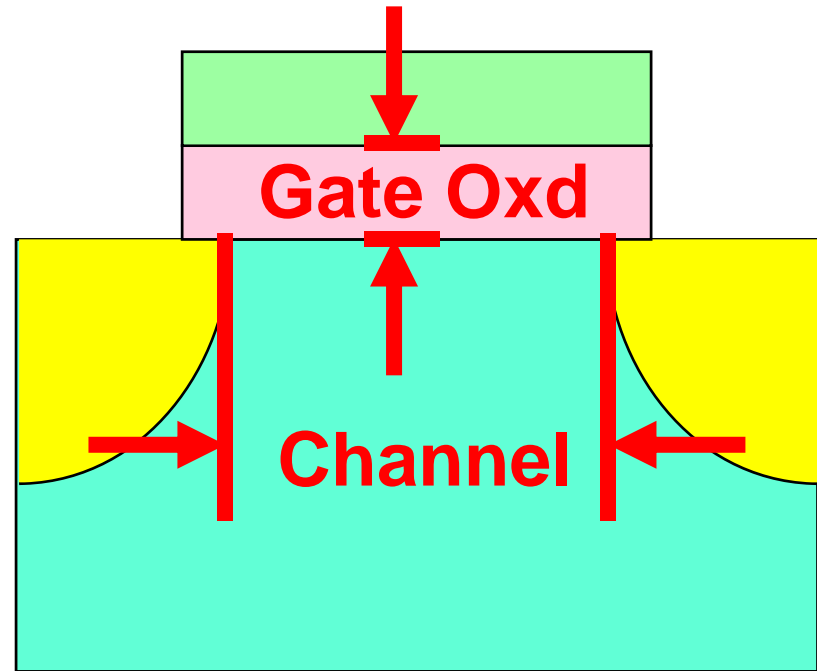
**10 nm**



Electron  
wave  
length

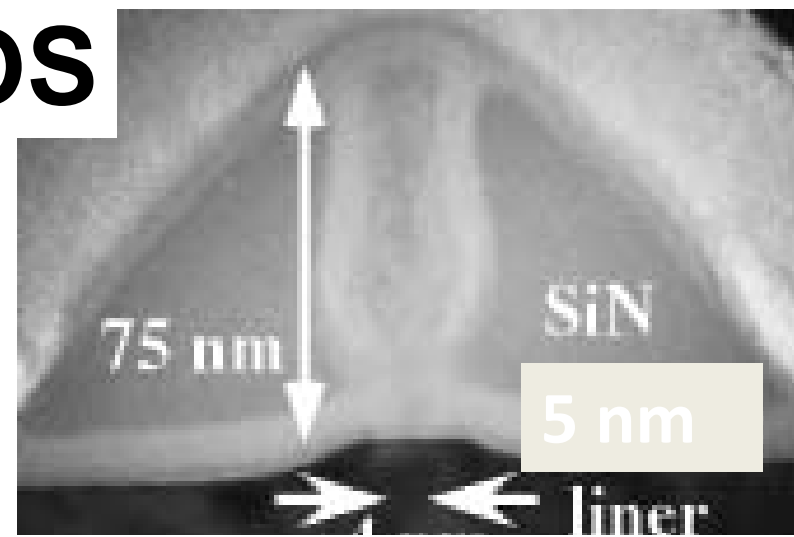


# Channel length?

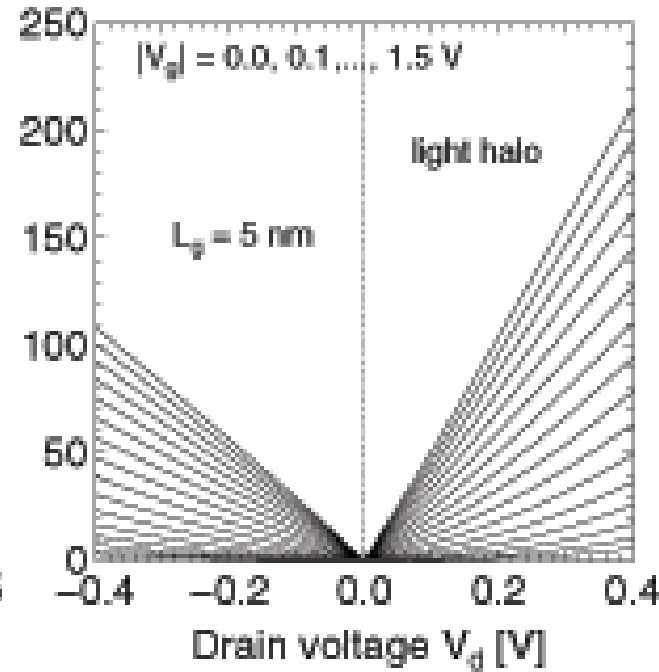
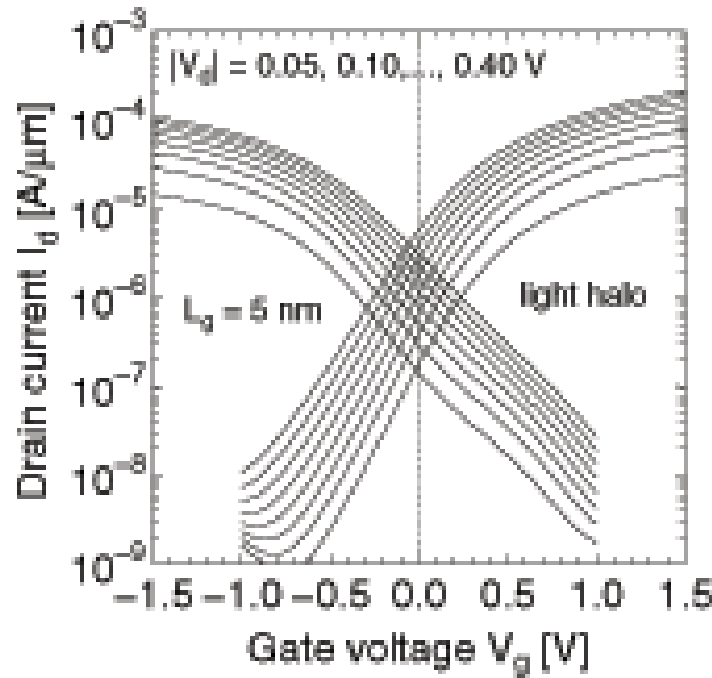
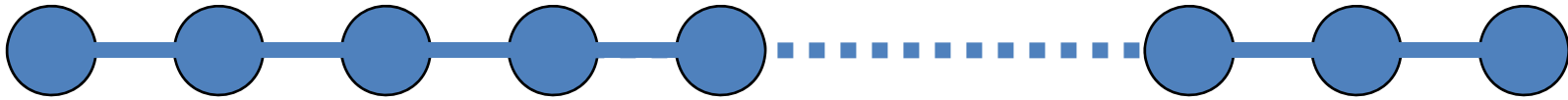


# 5 nm gate length CMOS

## Is a Real Nano Device!!



*Length of 18 Si atoms*



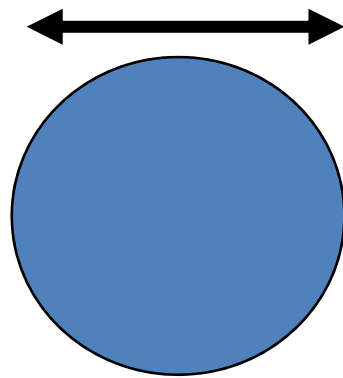
H. Wakabayashi  
et.al, NEC

IEDM, 2003



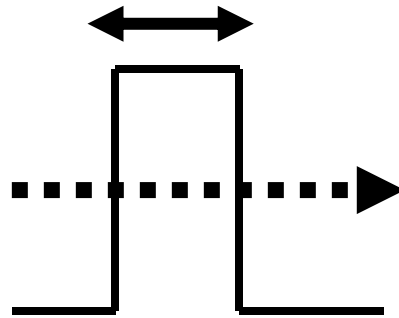
Electron  
wave  
length

**10 nm**



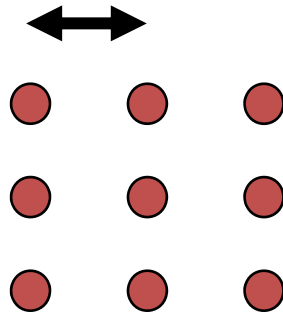
Tunneling  
distance

**3 nm**



Atom  
distance

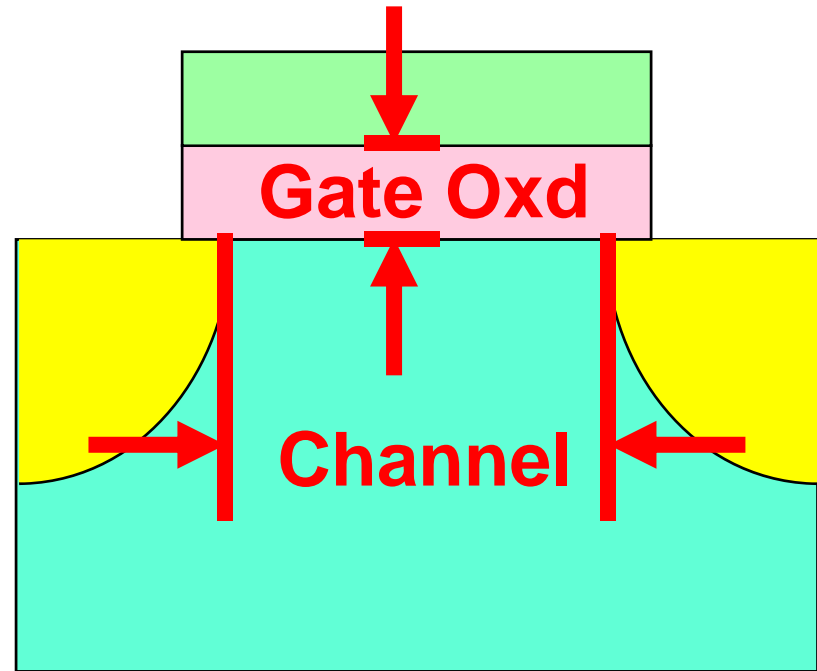
**0.3 nm**



Downsizing limit!

Channel length

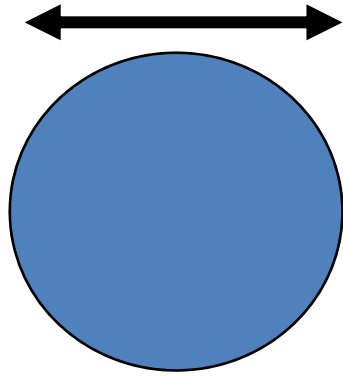
Gate oxide thickness



**Prediction now!**

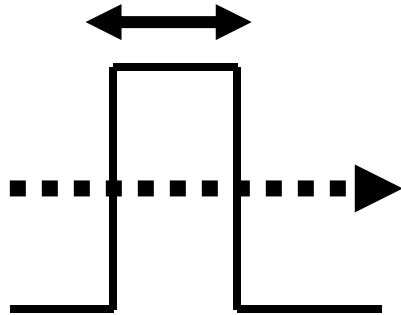
Electron  
wave  
length

**10 nm**



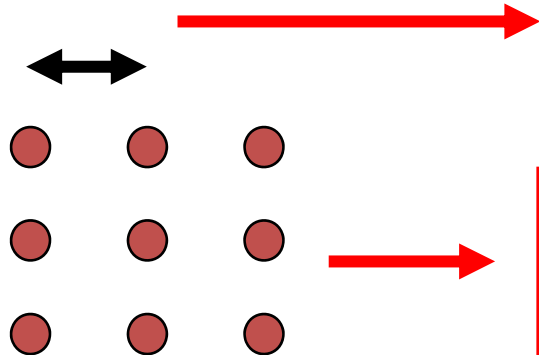
Tunneling  
distance

**3 nm**



Atom  
distance

**0.3 nm**



MOSFET operation

**$L_g = 2 \sim 1.5 \text{ nm?}$**

**Below this,  
no one knows future!**

## How about the integration of such small-geometry MOSFETs in a chip?

- 1) Integration of huge number of the ultra-small MOSFETs would consume too huge power and thus, creates too huge heat?
- 2) Integration of such ultra-small MOSFETs causes too huge variations in the transistor characteristics, which could make the circuit design impossible?
- 3) There are too many number of transistors in a chip for the circuit designers to manipulate? (design crisis),
- 4) There would be no merit of transistor downsizing in performance and power, because of RC (resistance capacitance product) of interconnect cannot be reduced aggressively any more?
- 5) Who will pay the huge development and production costs for the integration of such ultra-small MOSFETs? Note that the prices for the recent process equipments and the lithography mask became extremely high.

These concerns have been argued in the past 15 years at every new generation of the products, **like the wolf boy.**

Fortunately, **the wolf has not come**, and the concerns have not come true.

It is expected that we can go with several more generations for the integration.

There will be still a room for squeezing the technologies to obtain the merit of the scaling-down for integration.

The continuous progress of CMOS technologies for

- high-performance

- low power

is very important because of the 3 reasons:

1) Rapid progress of aging population and falling birth rate

1) Global warming

1) Semiconductor industry and world economy

# 1) Rapid progress of aging population and falling birth rate:

Replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example.

For, the daily family use, much higher intelligence and much lower power consumption than those of today are required.

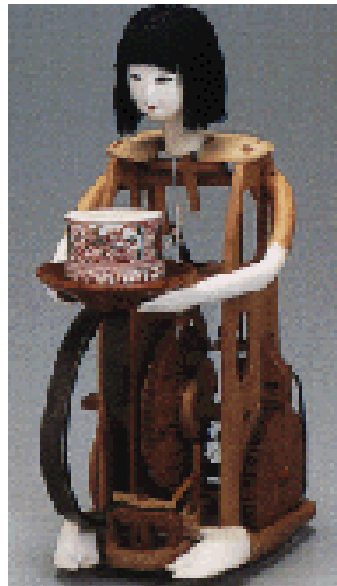


# Robot in 21c cannot be made without integrated circuits

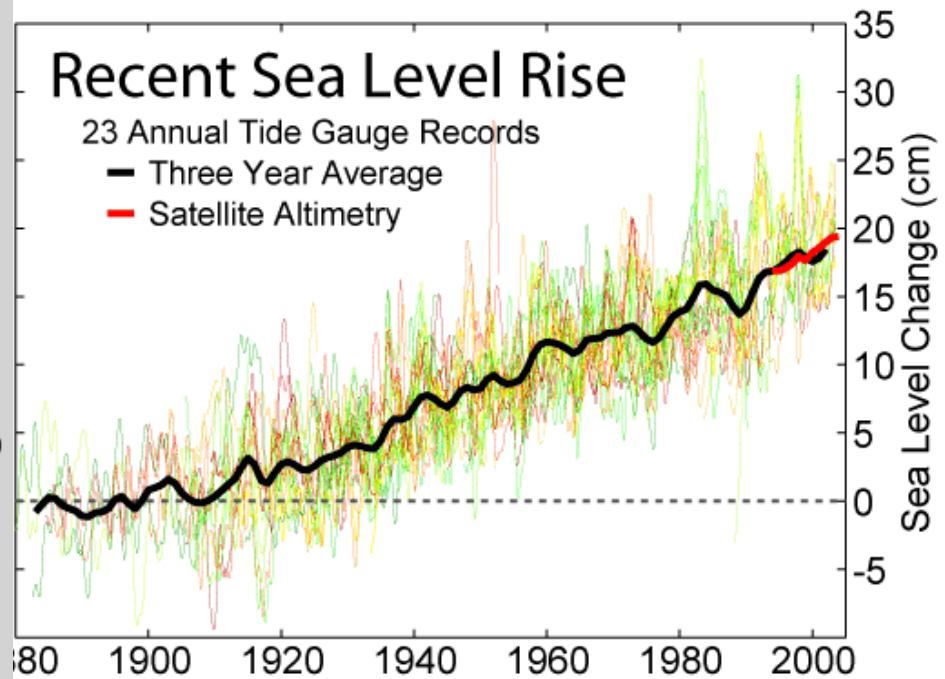
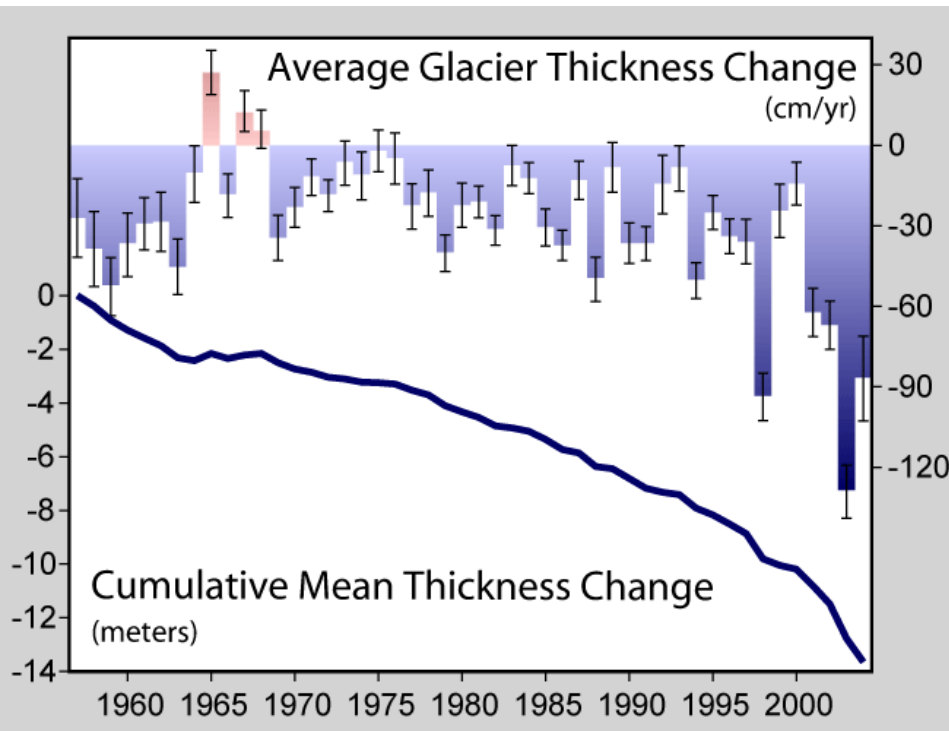
Robot (21C)



Karakuri (Windup Mechanical) doll (18C) in Japan



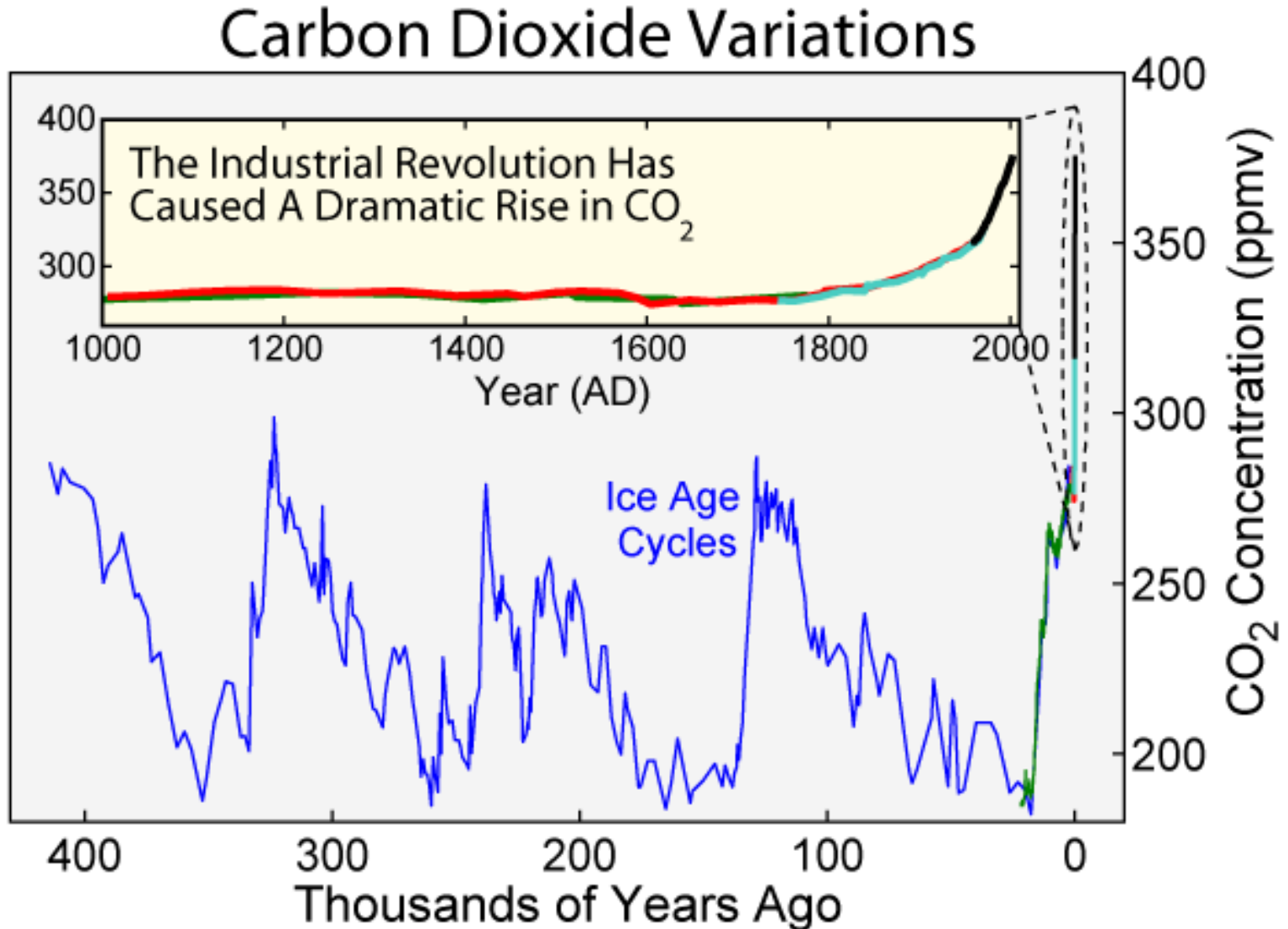
## 2) Recent Significant Global Warming



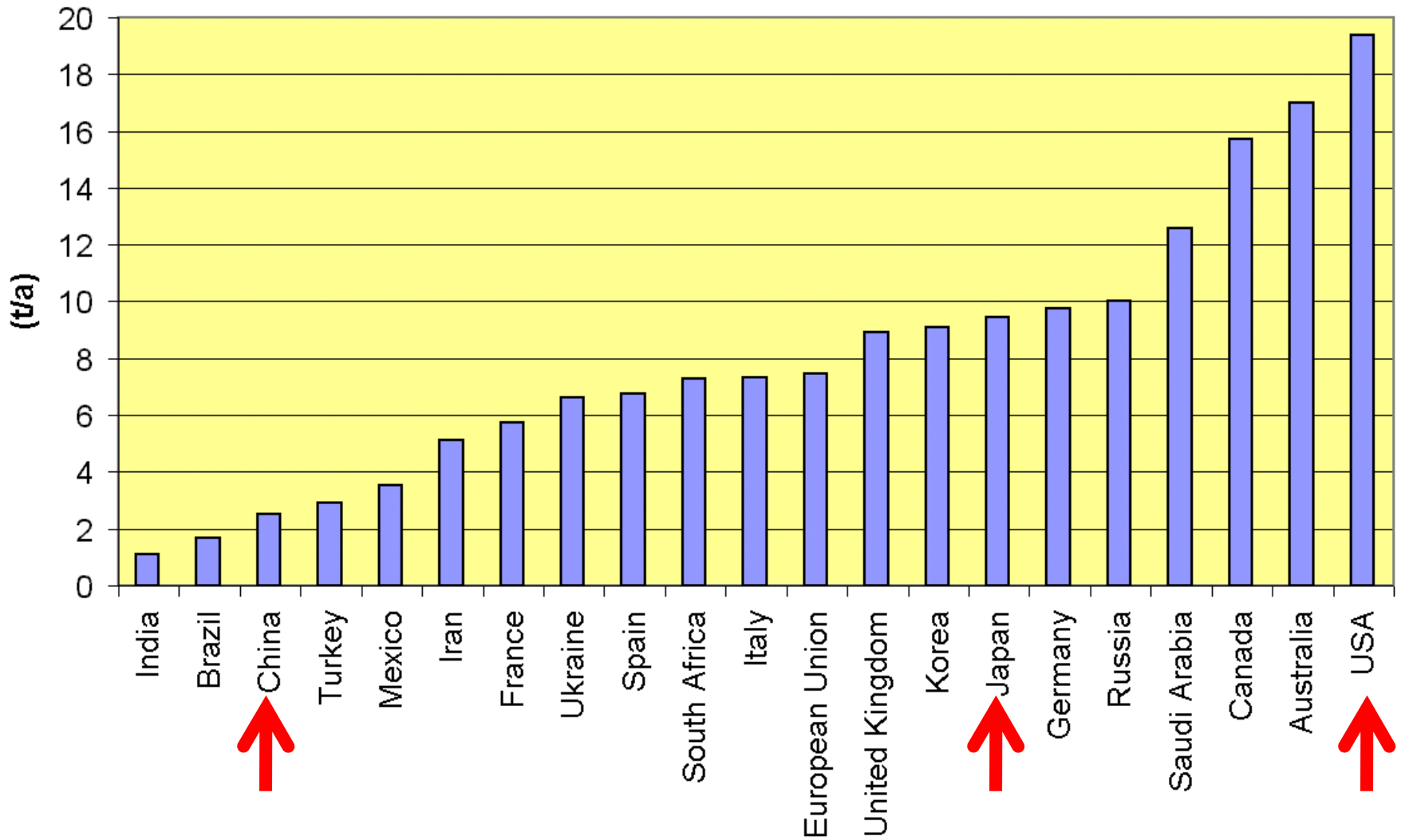


We need reduce CO<sub>2</sub> generation!

→ Low power technology is urgent request



# CO2 Emission per capita 2002



### 3) Semiconductor industry, and world economy

If there is no more downsizing such as

45 → 32 nm Logic, 8 Gbit → 16 Gbit Memory

- LSIs will not be sold well, and semiconductor companies will face a disaster.
- Equipment and material companies as well.
- There is no more R & D for semiconductors and many people will lose their jobs.  
→ World economy crisis!

# History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking!

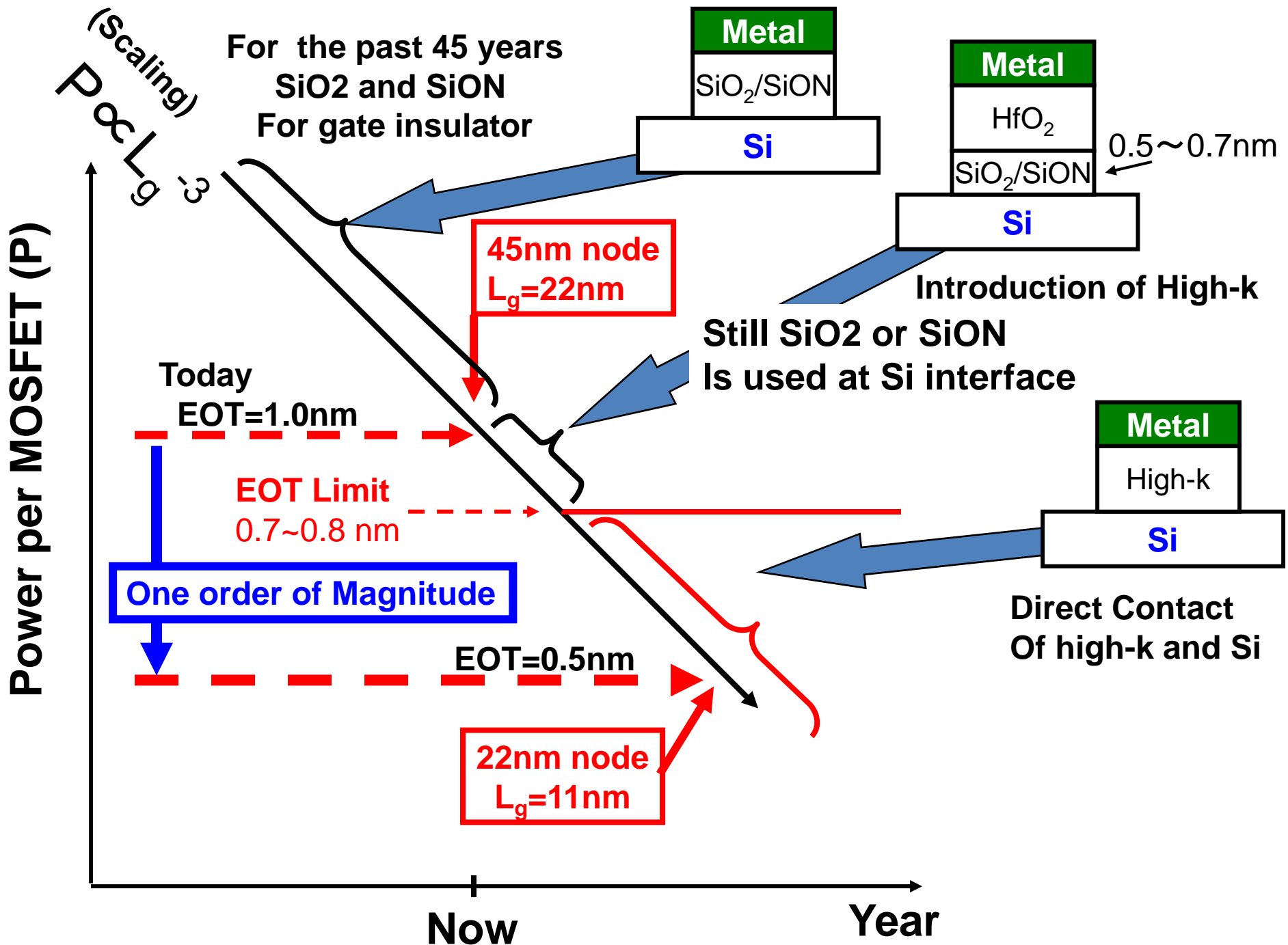
$C, V \propto L$       C: Capacitance    V: Voltage

Switching speed  $CV/I$       → Decrease

Power consumption  $CV^2/2$       → Decrease

Integration density:  $1/L^2$       → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm



# Choice of High-k elements for oxide

## Candidates

● Unstable at Si interface

- ①  $\text{Si} + \text{MO}_x \rightarrow \text{M} + \text{SiO}_2$
- ②  $\text{Si} + \text{MO}_x \rightarrow \text{MSi}_x + \text{SiO}_2$
- ③  $\text{Si} + \text{MO}_x \rightarrow \text{M} + \text{MSi}_x\text{O}_y$

● Gas or liquid at 1000 K

○ Radio active

**HfO<sub>2</sub> based dielectrics are selected as the first generation materials, because of their merit in**

- 1) band-offset,
- 2) dielectric constant
- 3) thermal stability

● H																	● He						
● Li	● Be																	● B	● C	● N	● O	● F	● Ne
① Na	● Mg																	● Al	● Si	● P	● S	● Cl	● Ar
K	● Ca	● Sc	② Ti	① V	① Cr	① Mn	① Fe	① Co	① Ni	① Cu	① Zn	① Ga	① Ge	● As	● Se	● Br	● Kr						
● Rh	● Sr	● Y	● Zr	① Nb	① Mo	Tc	① Ru	① Rb	① Pd	● Ag	① Cd	① In	① Sn	① Sb	① Te	● I	● Xe						
● Cs	③ Ba	★	● Hf	① Ta	① W	① Re	① Os	① Ir	● Pt	● Au	● Hg	● Tl	① Pb	① Bi	○ Po	○ At	○ Rn						
○ Fr	○ Ra	★	○ Rf	○ Ha	○ Sg	○ Ns	○ Hs	○ Mt															
★	● La	● Ce	● Pr	● Nd	○ Pm	● Sm	● Eu	● Gd	● Tb	● Dy	● Ho	● Er	● Tm	● Yb	● Lu								
★	○ Ac	○ Th	○ Pa	○ U	○ Np	○ Pu	○ Am	○ Cm	○ Bk	○ Cf	○ Es	○ Fm	○ Md	○ No	○ Lr								

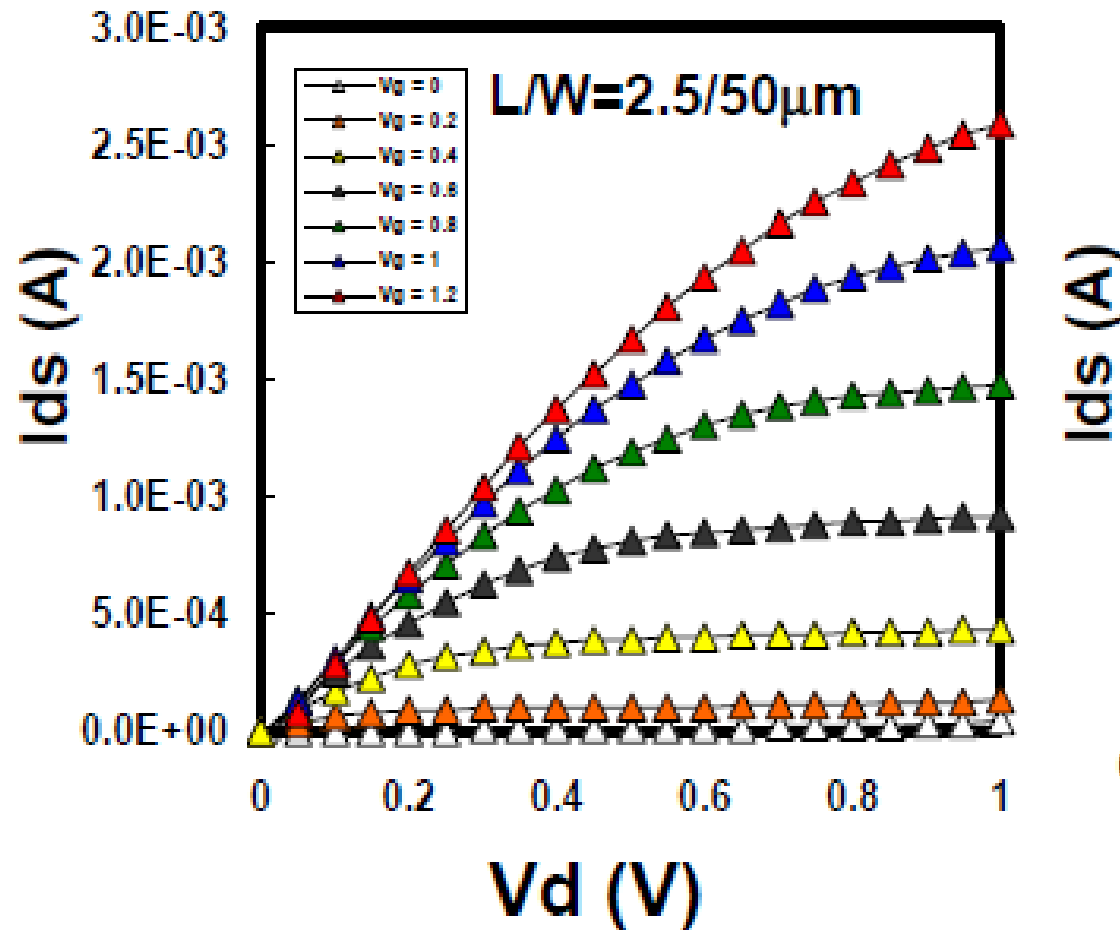
R. Hauser, IEDM Short Course, 1999

Hubbard and Schlom, J Mater Res 11 2757 (1996)

EOT = 0.48 nm

Our results

Transistor with La2O3 gate insulator



**CMOS downsizing is critically important**

**However now, many people expect that we will reach limit in 2020.**

Totally, new paradigm after reaching the downsizing limit.

What will be?



After 2020

There is no decrease in gate length  
around at 10 ~ 5 nm.

4 reasons.

# After 2020

4 reasons for no downsizing anymore  
or No decrease in gate length

---

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.

**Ballistic ← No scattering of carriers in channel**

Thus, all the carrier from the source reach drain

2. Increase of Off-current (Subthreshold current)

3. No decrease of Gate capacitance by parasitic components

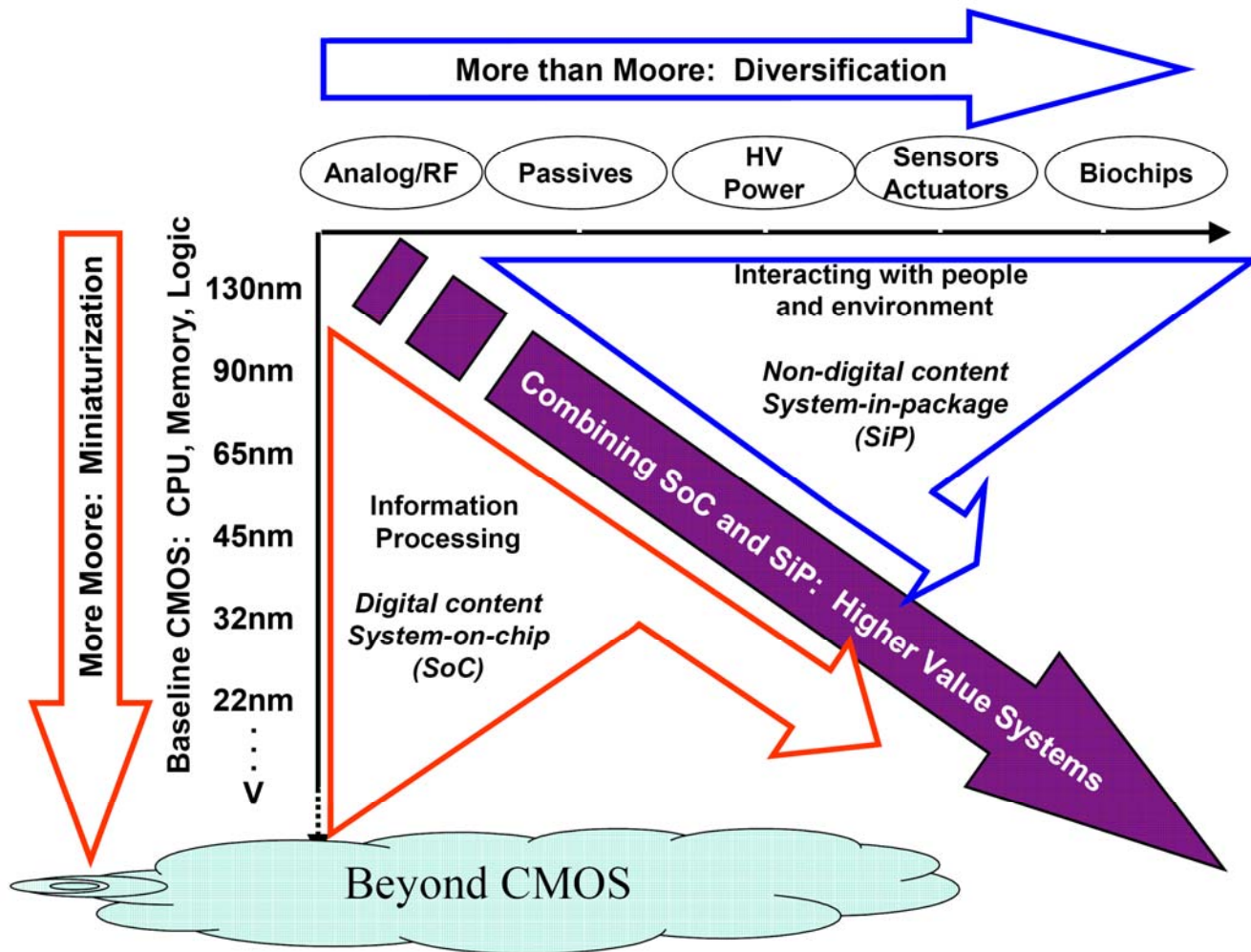
4. Increase in production cost.

After 2020

What will be the world with no gate length reduction?

# More Moore and More than Moore

## Moore's Law & More

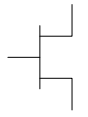
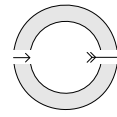
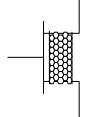
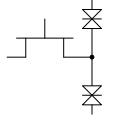
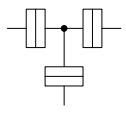

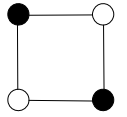
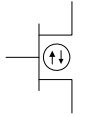


Question what is the other side of the cloud?

ITRS 2005 Edition

[http://strj-jeita.elisasp.net/pdf\\_ws\\_2005nendo/9A\\_WS2005IRC\\_Ishiuchi.pdf](http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf)

Victor V. Zhirnov and Ralph K. Cavin III, ECS 207 Washington DC

<i>Device</i>								
	<i>FET</i>	<i>RSFQ</i>	<i>1D structures</i>	<i>Resonant Tunneling Devices</i>	<i>SET</i>	<i>Molecular</i>	<i>QCA</i>	<i>Spin transistor</i>
<i>Cell Size</i>	100 nm	0.3 μm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
<i>Density (cm<sup>-2</sup>)</i>	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
<i>Switch Speed</i>	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
<i>Circuit Speed</i>	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
<i>Switching Energy, J</i>	2×10 <sup>-18</sup>	>1.4×10 <sup>-17</sup>	2×10 <sup>-18</sup>	>2×10 <sup>-18</sup>	>1.5×10 <sup>-17</sup>	1.3×10 <sup>-16</sup>	>1×10 <sup>-18</sup>	2×10 <sup>-18</sup>
<i>Binary Throughput, GBit/ns/cm<sup>2</sup></i>	86	0.4	86	86	10	N/A	0.06	86

We HAVE IDENTIFIED NO VIABLE EMERGING LOGIC TECHNOLOGIES for Information Processing beyond CMOS

We could keep the Moore's law after 2020  
Without downswing the gate length

What is Moore's law.

Keep increase of the number of components.  
Cost per components decreases!

## MOORE'S LAW

transistors

10,000,000,000

1,000,000,000

100,000,000

10,000,000

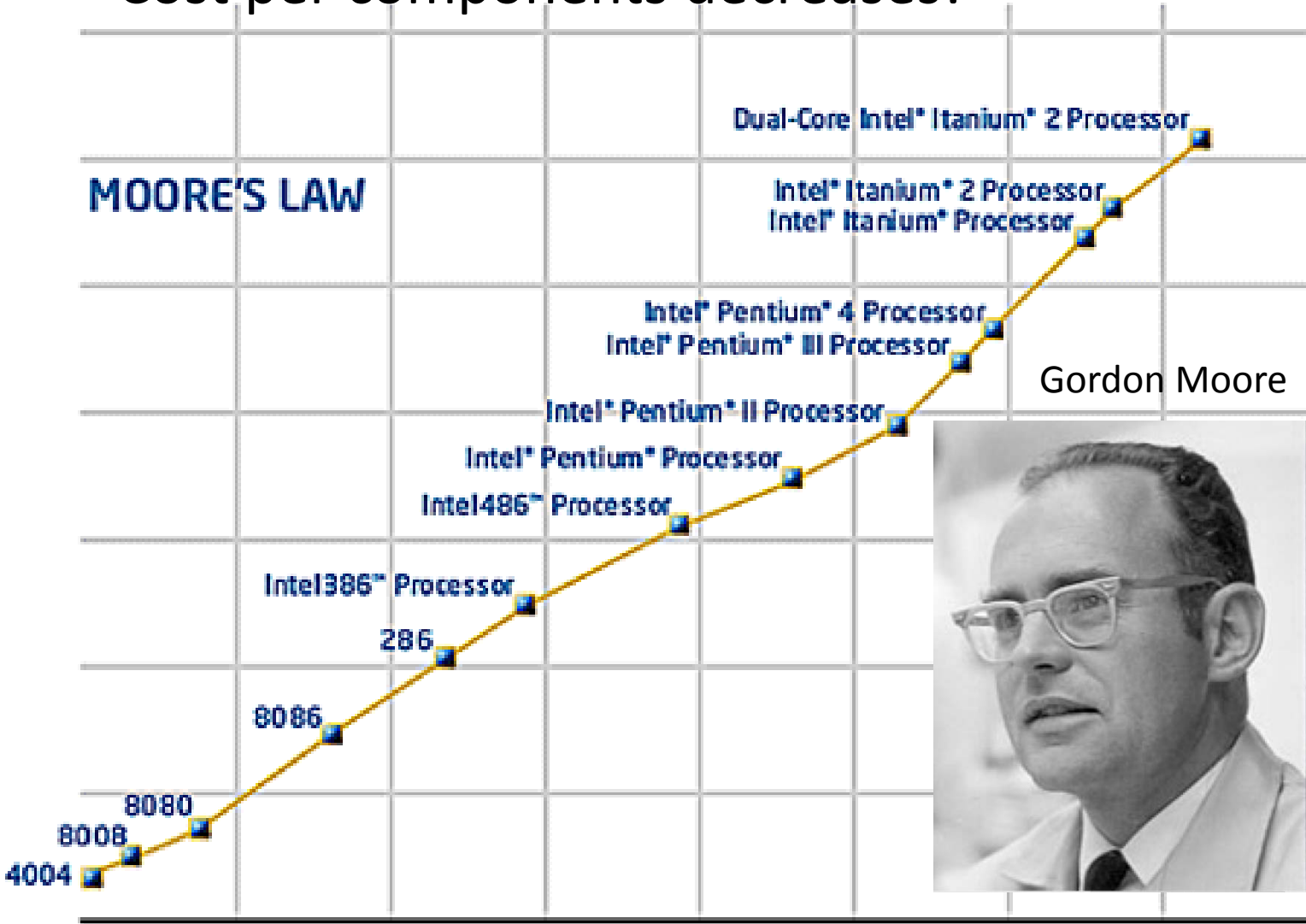
1,000,000

100,000

10,000

1,000

1970 1975 1980 1985 1990 1995 2000 2005 2010



Gordon Moore



We could keep the Moore's law after 2020  
Without downswing the gate length

What is Moore's law.

→ to increase the number (#) of Tr. In a chip

Now, # of Tr. in a chip is limited by power.

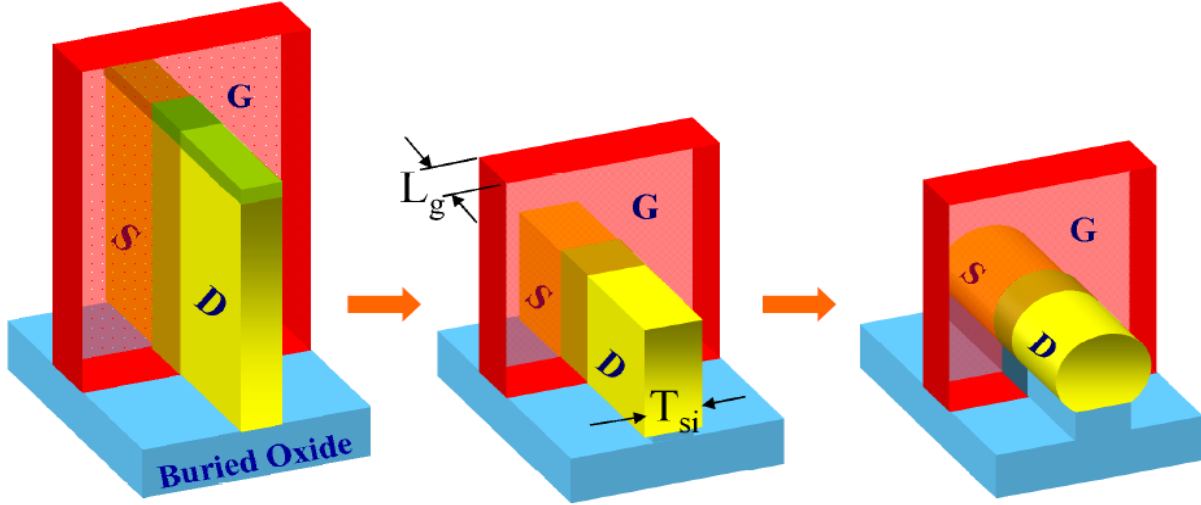
→ key issue is to reduce the power.

→ to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.



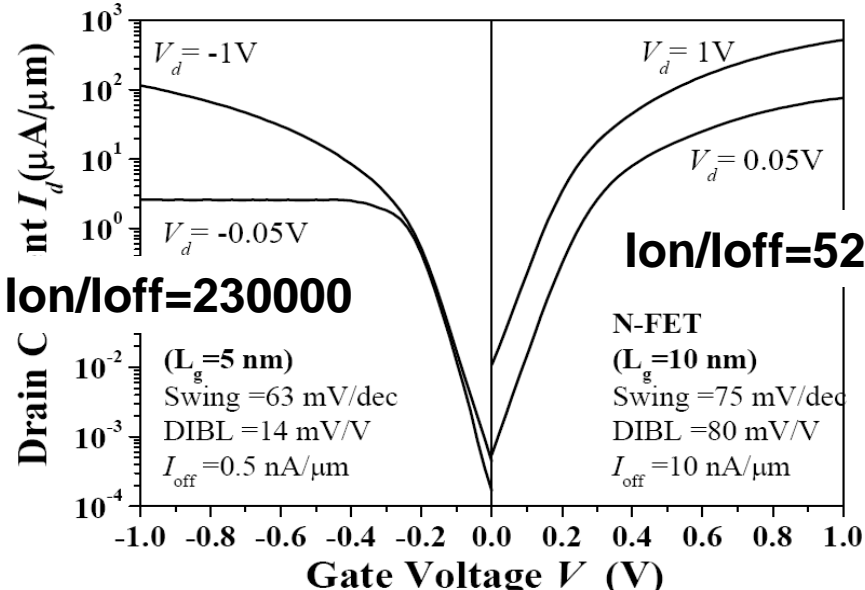
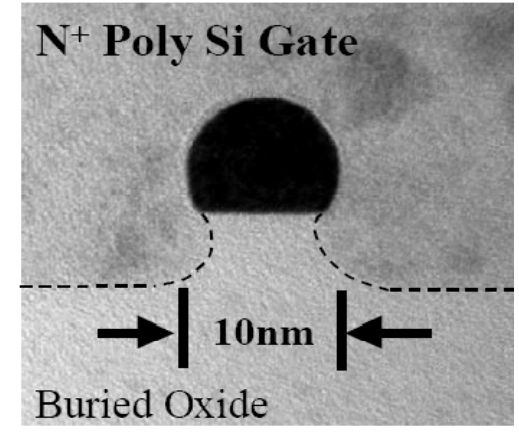
# FinFET to Nanowire



Double-Gate FinFET  
( $T_{si} = \frac{2}{3} L_g$ )

Omega FinFET  
( $T_{si} = L_g$ )

Nanowire FinFET  
( $T_{si} = 2L_g$ )



**Channel conductance is well controlled by Gate even at  $L=5\text{nm}$**

Selection of MOSFET structure for high conduction:  
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1. Use 1D ballistic conduction

M2. Increase number of quantum channel

M3. Increase the number of wire or tube per area  
3D integration of wire and tubes

For suppression of  $I_{off}$ , the Nanowire/tube is also good.

1D conduction per one quantum channel:

$$G = 2e^2/h = 77.5 \mu\text{S/wire or tube}$$

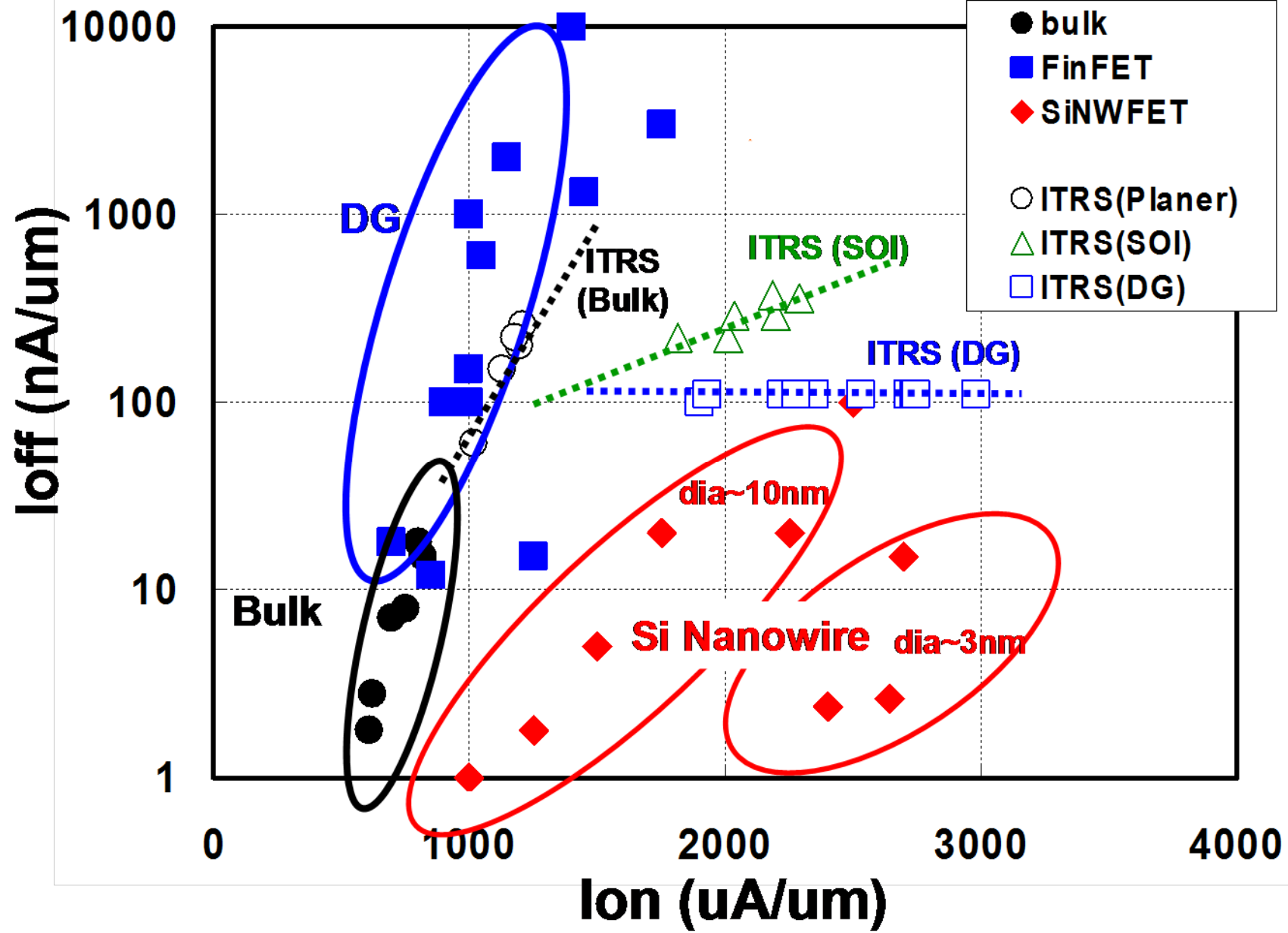
regardless of gate length and channel material

That is 77.5 mA/wire at 1V supply

This an extremely high value

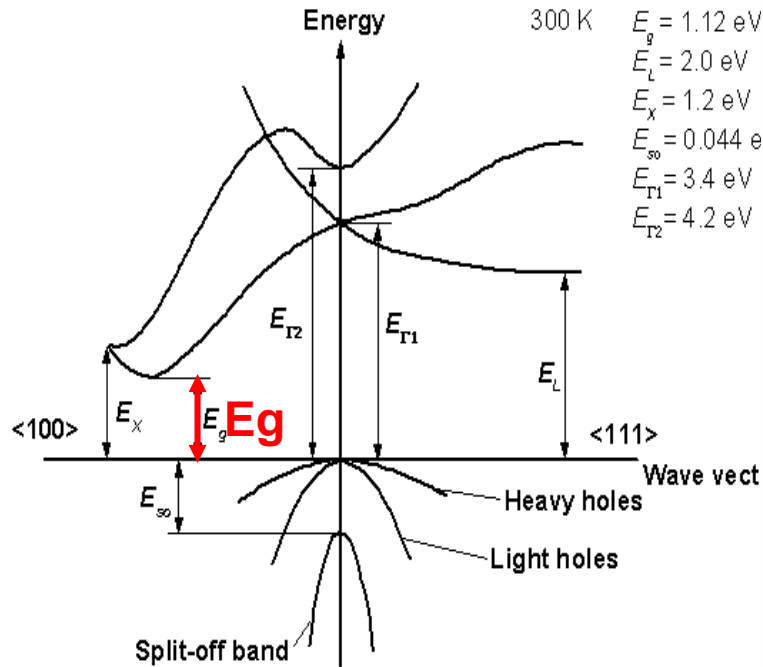
However, already 20mA/wire was obtained experimentally  
by Samsung

# Off Current

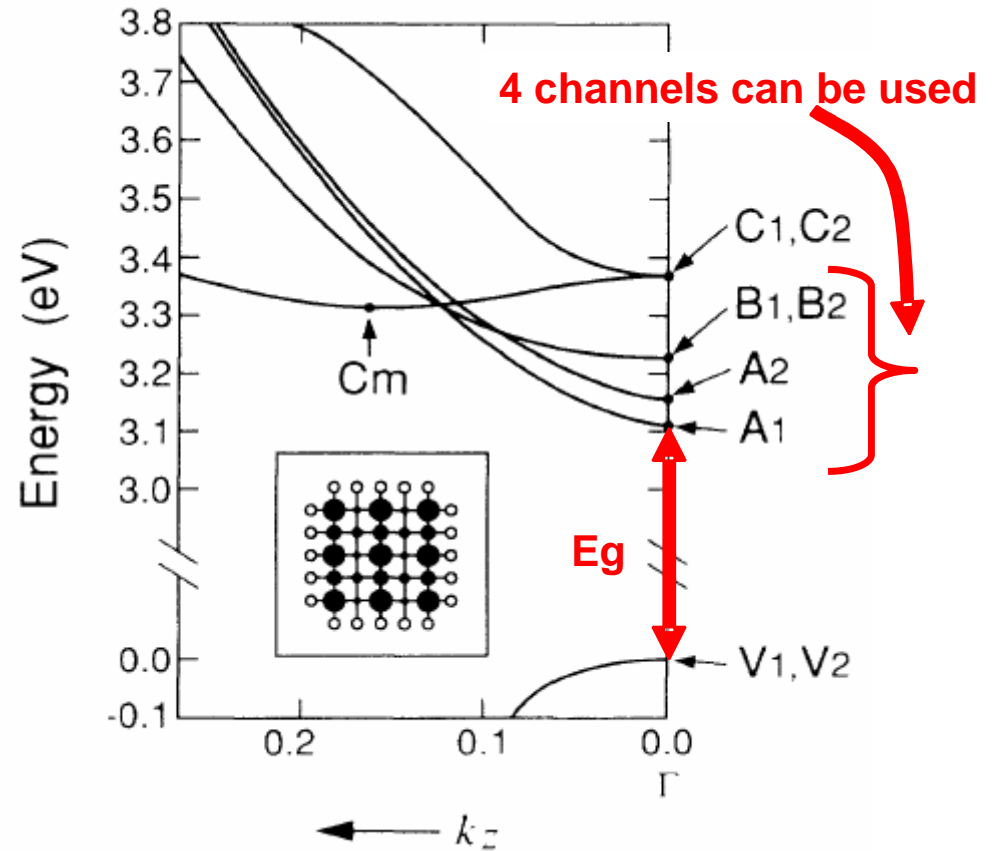


# Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



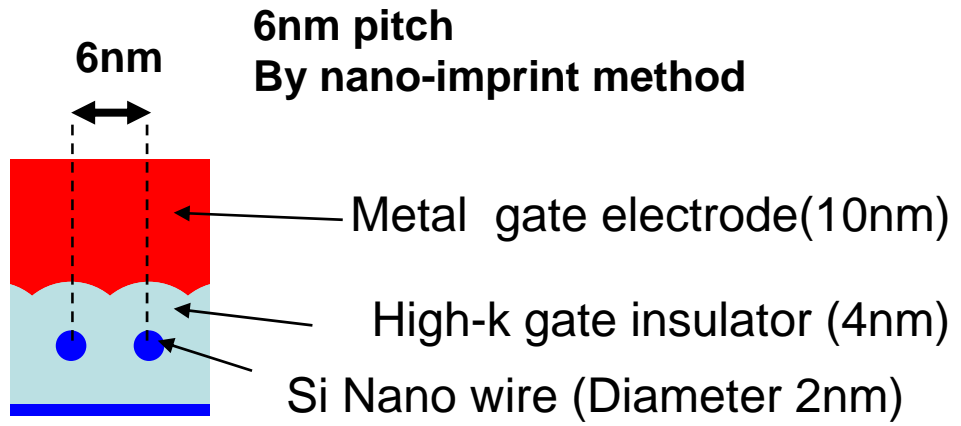
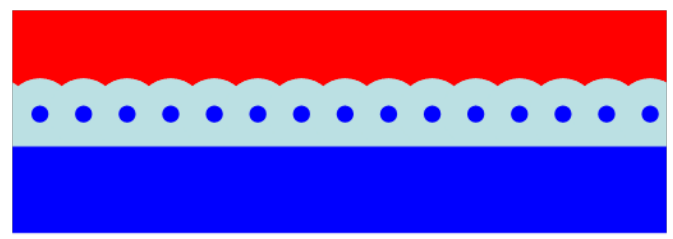
Energy band of Bulk Si



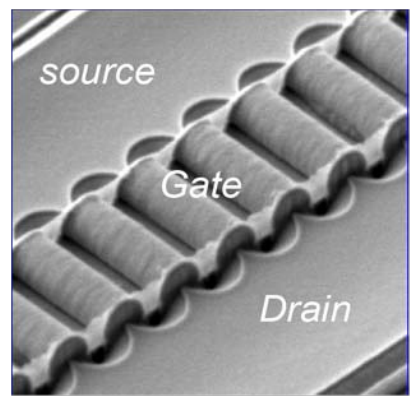
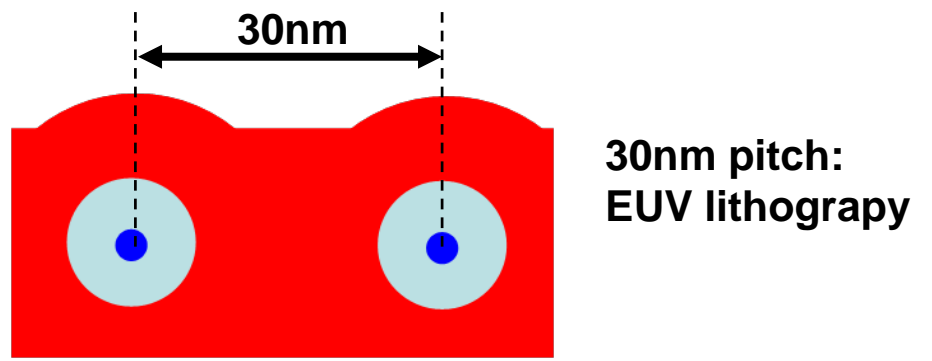
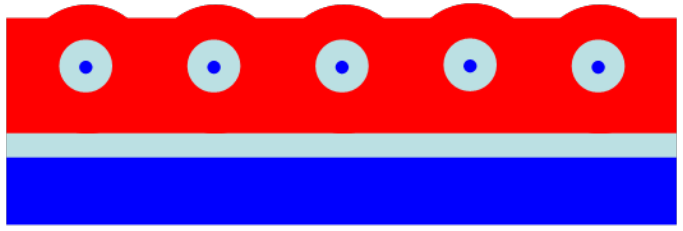
Energy band of 3 x 3 Si wire

# Maximum number of wires per 1 $\mu\text{m}$

**Front gate type MOS** 165 wires /  $\mu\text{m}$

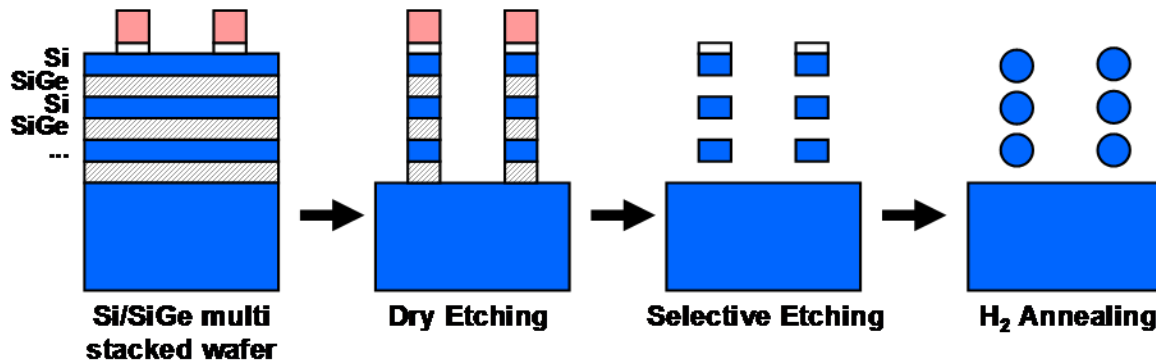
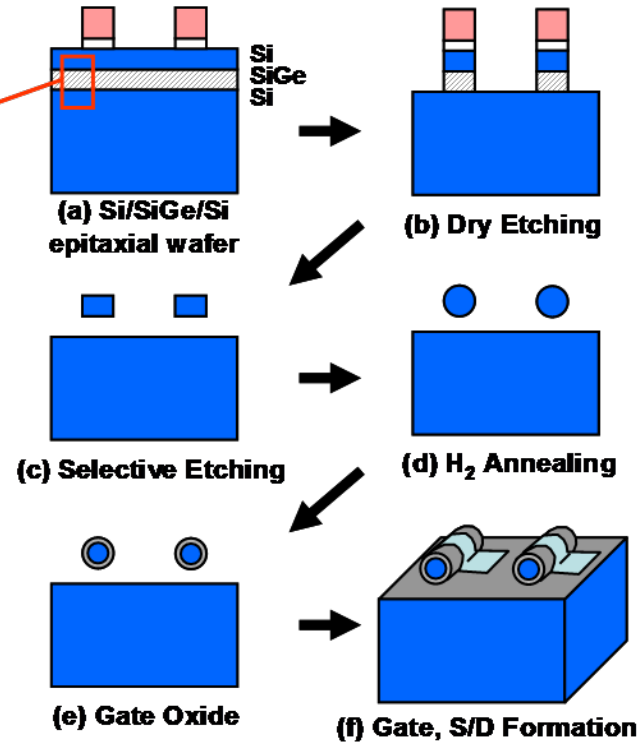
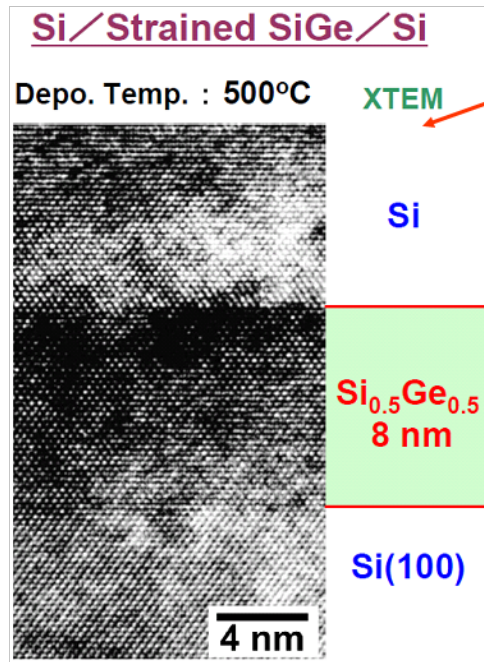


**Surrounded gate type MOS** 33 wires /  $\mu\text{m}$

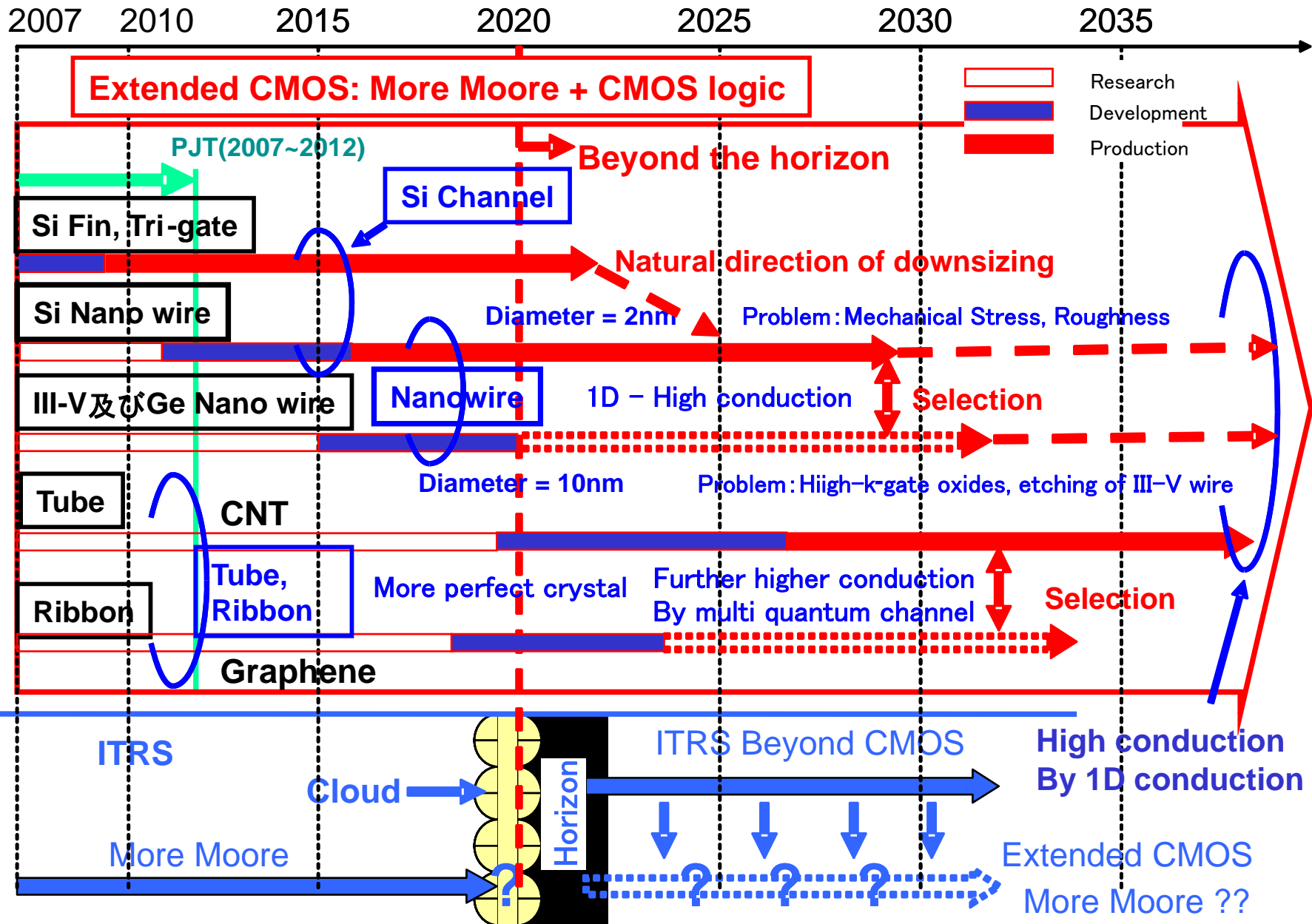


**Surrounded gate MOS**

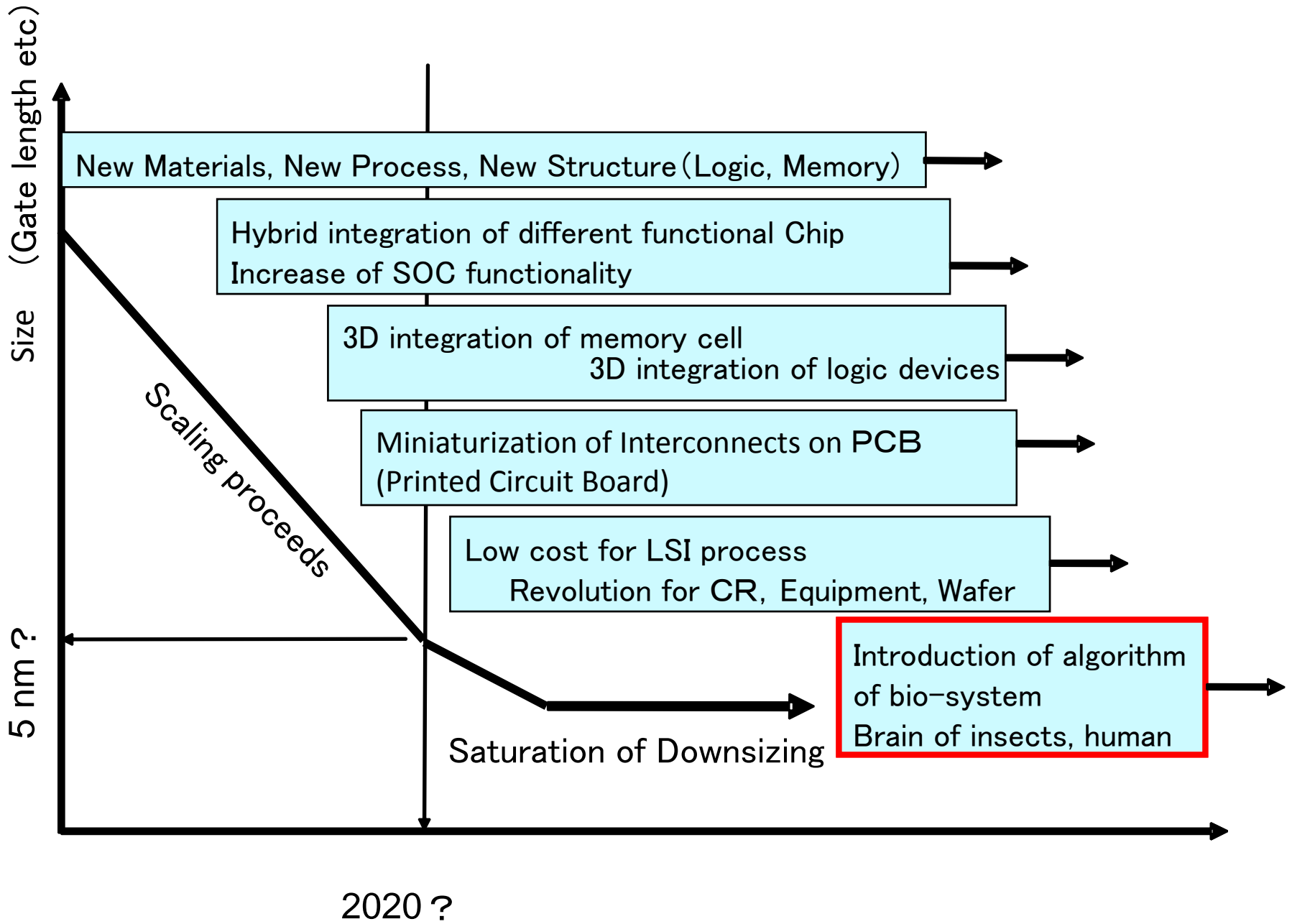
# Increase the number of wires towards vertical dimension



# Our new roadmap







Sensor

Brain

Ultra small volume  
Small number of neuron cells  
Extremely low power

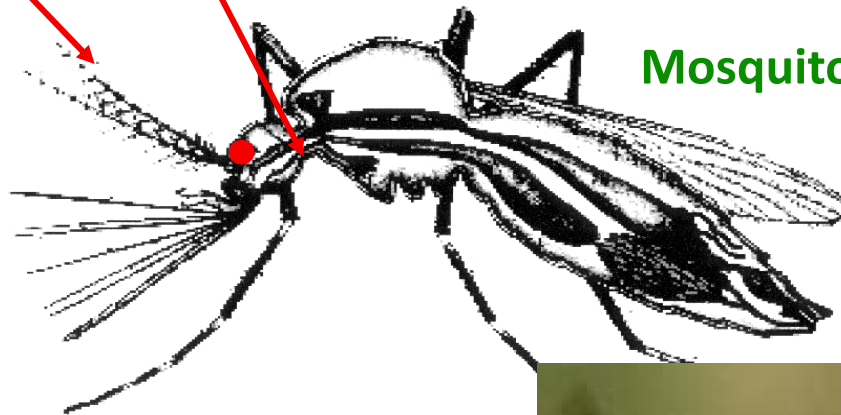
Real time image processing  
(Artificial) Intelligence  
3D flight control

Mosquito

**System and  
Algorithm  
becomes  
more  
important!**

**But do not  
know how?**

Infrared  
Humidity  
CO<sub>2</sub>



Dragonfly is further high performance



Thank you  
for your attention!