Past and future for micro- and nano-electronics, focusing on Si integrated circuits technology

June 2, 2008

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Toyo Institute of Technology

Needless to say, but….

CMOS Technology:

Indispensible for our human society

Al the human activities are controlled by CMOS

living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc.

Without CMOS:

There is no computer in banks, and

world economical activities immediately stop.

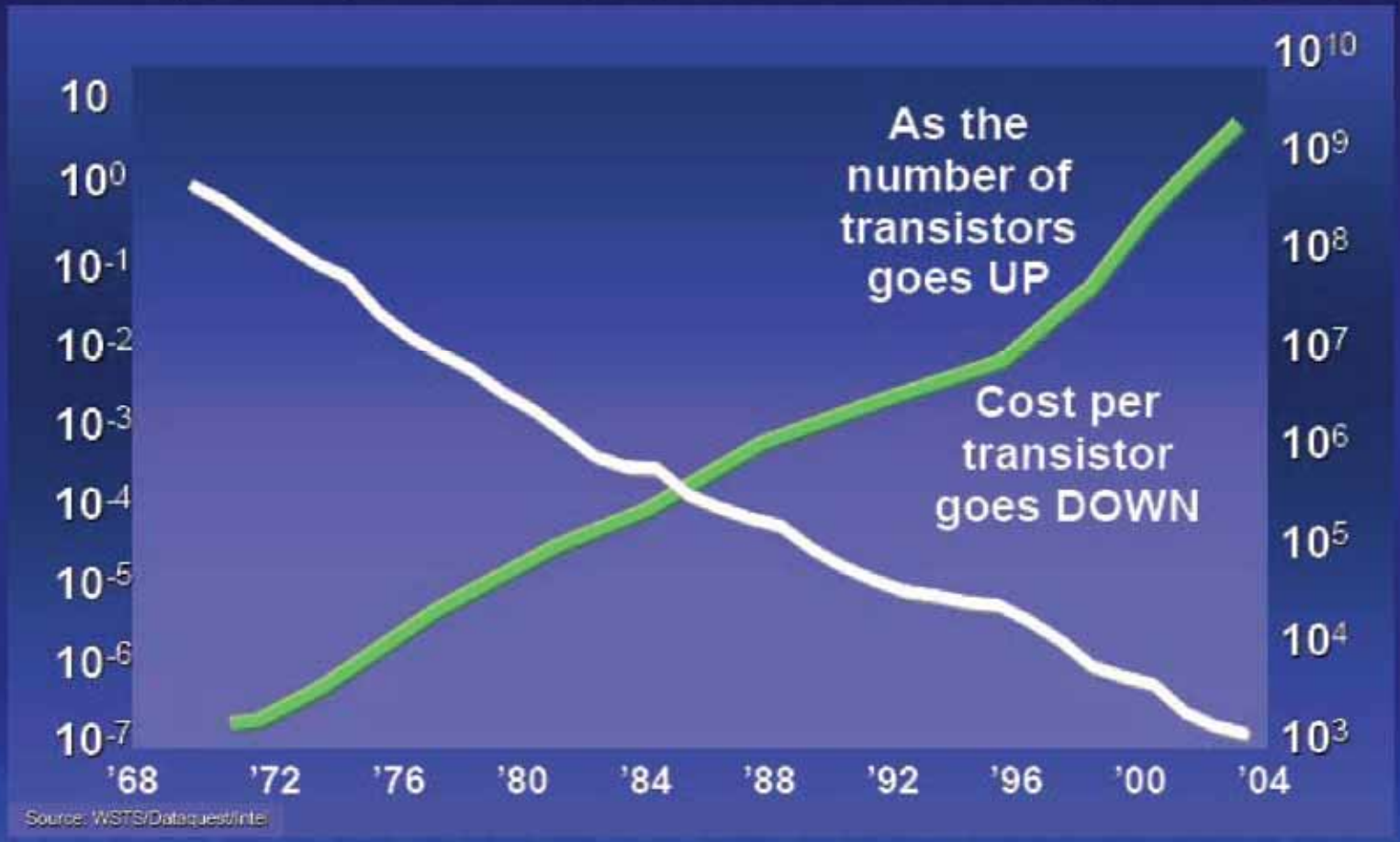
Cellarer phone dose not exists

CMOS experienced continuous progress for many years

	Name of Integrated Circuits	Number of Transistors
1960s	IC (Integrated Circuits)	~
1970s	LSI (Large Scale Integrated Circuit)	~1,0
1980s	VLSI (Very Large Scale IC)	~10,0
1990s	ULSI (Ultra Large Scale IC)	~1,000,0
2000s	?LSI (? Large Scale IC)	~1000,000

Exponential Cost Reduction

Cost per Transistor



Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the size reduced by one million times.
There have been many devices from stone age.
We have never experienced such a tremendous reduction of devices in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFE**

Reduce power consumption

2. **Increase number of Transistors**

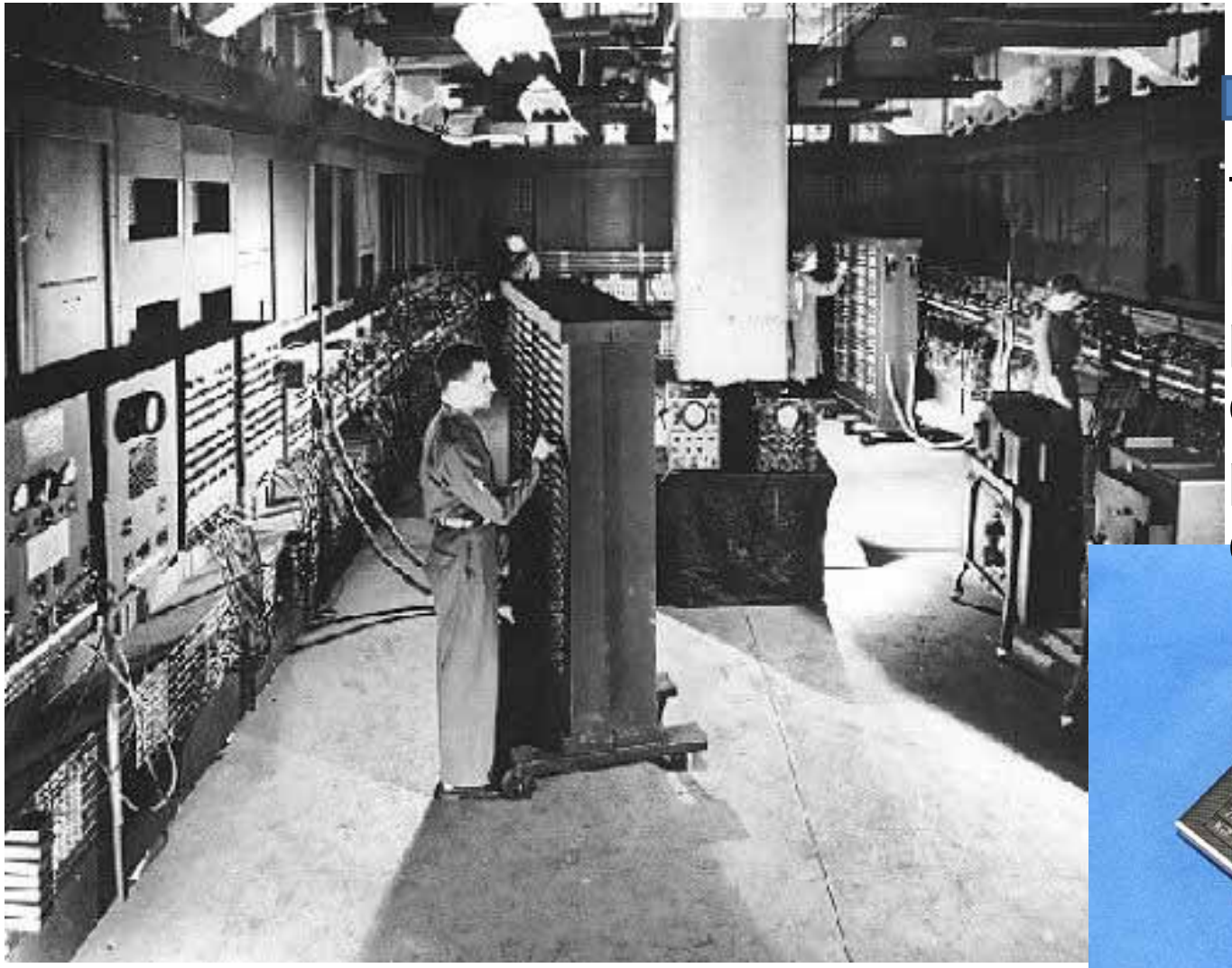
Increase functionality

→ **Parallel processing**

→ **Increase circuit operation sp**

Thus, downsizing of Si devices is the most important and critical issue.

First Computer Eniac: made of huge number of vacuum tubes 19
Big size, huge power, short life time filament



Today's pocket PC has much higher performance with extremely low power consumption

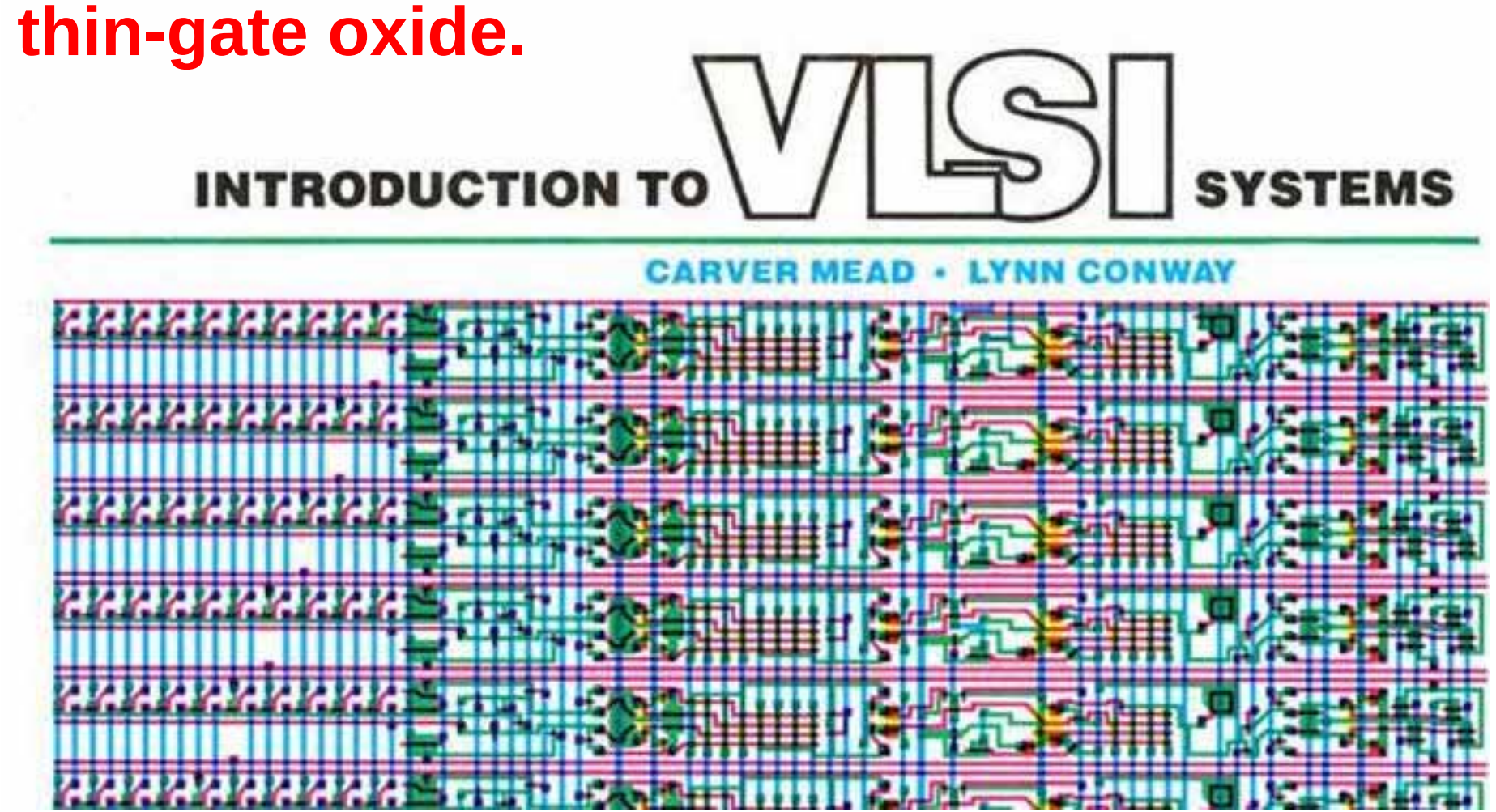
Many people wanted to say about the limit.

Past predictions were not correct!!

Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall' (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing

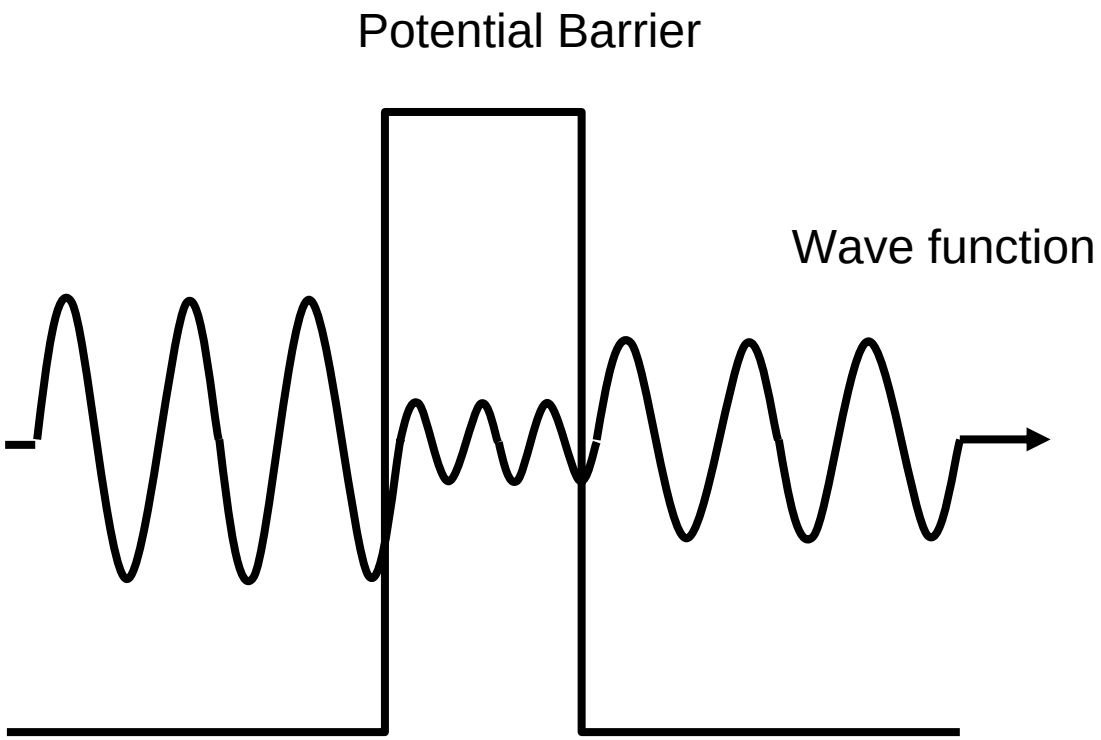
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.

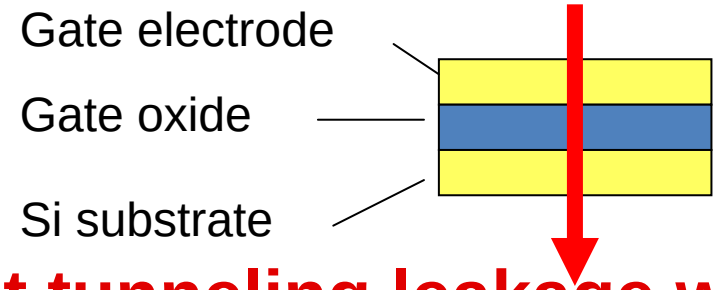


VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

Direct-tunneling effect



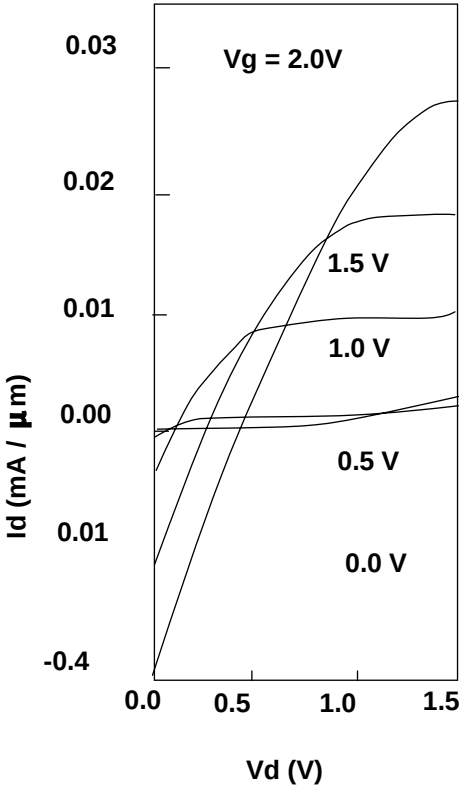


Direct tunneling leakage current start to flow when the thickness is 3 nm.

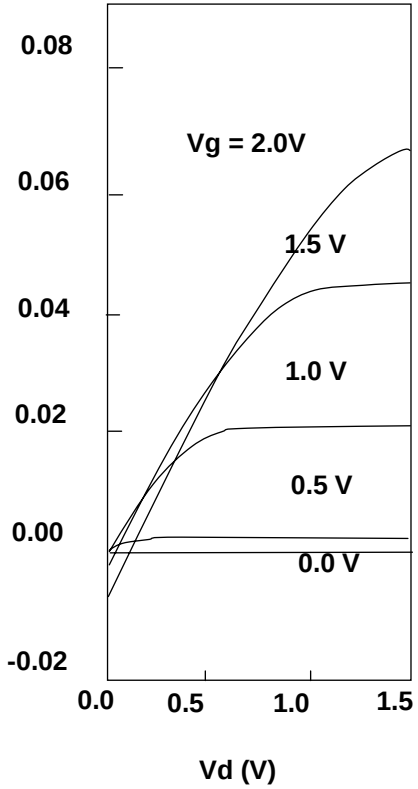
Direct tunneling leakage was found to be OK! In 1994

MOSFETs with 1.5 nm gate oxide

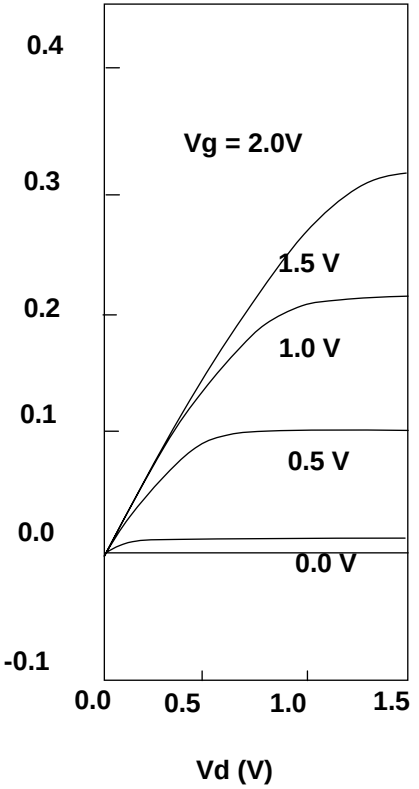
Lg = 10 μm



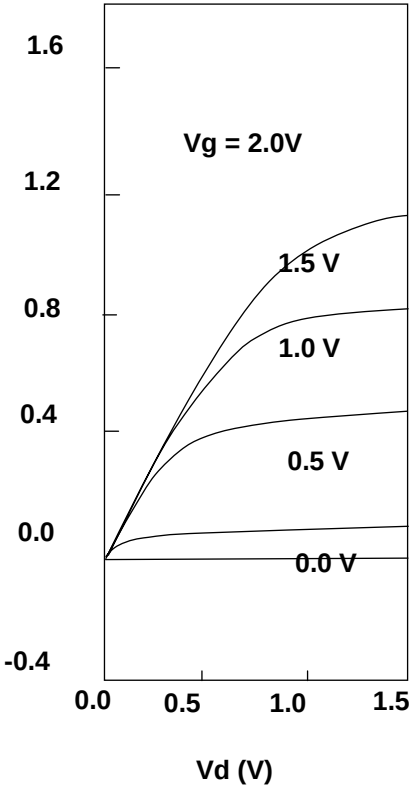
Lg = 5 μm



Lg = 1.0 μm



Lg = 0.1μm



Do not believe a text book statement, blindly!

Never Give Up!

No one knows future!

There would be a solution!

Think, Think, and Think!

Or, Wait the time!
Some one will think for you

Transistor Scaling Continues

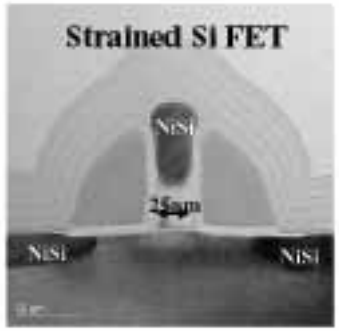
90nm node

Lg=50nm

65nm node

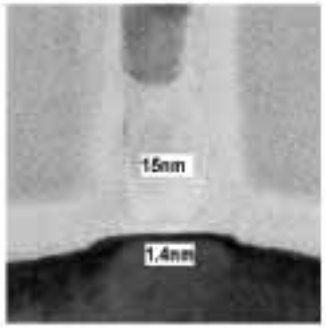
Lg=35nm

45nm node



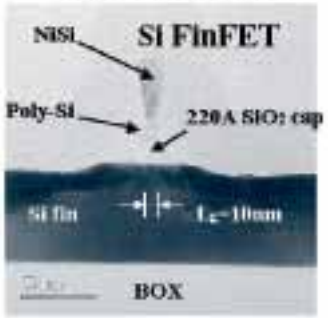
Lg=25nm

32nm node

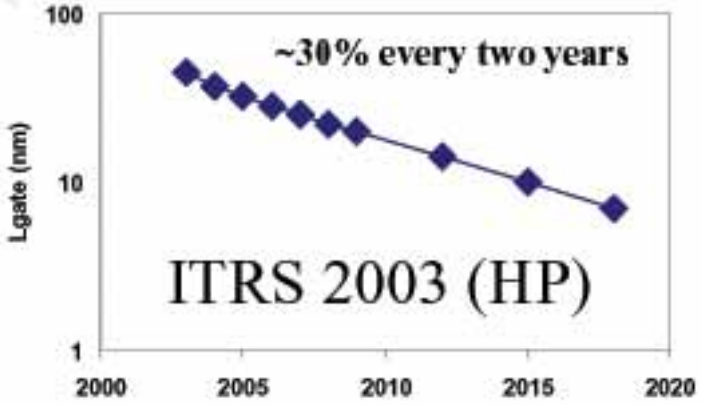


Lg=15nm

22nm node



Lg=10nm

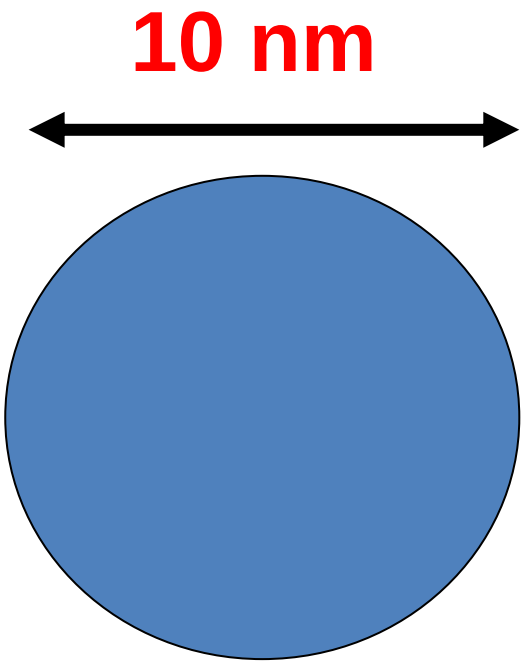


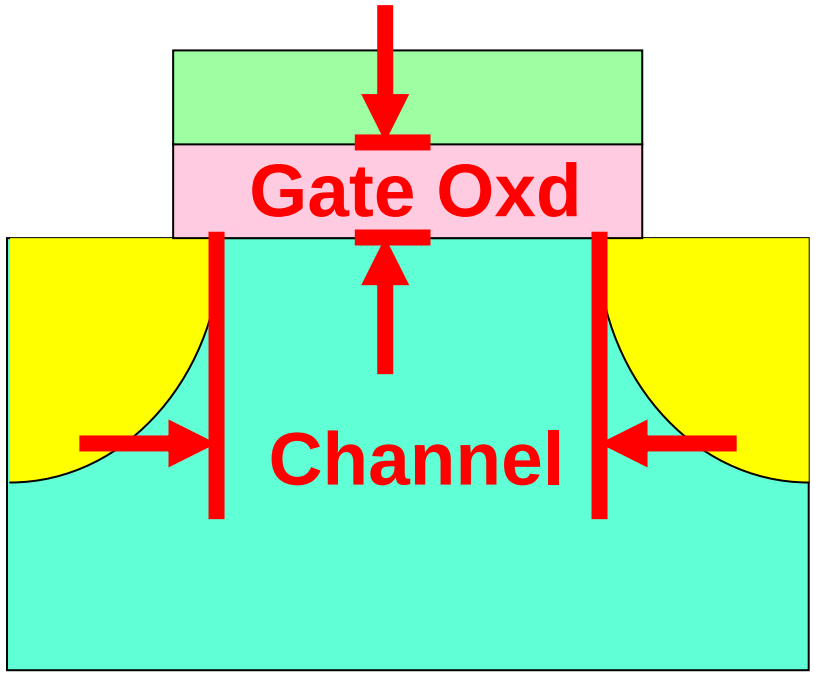
Qi Xinag, ECS 2004, AMI

Downsizing limit?

Channel length?

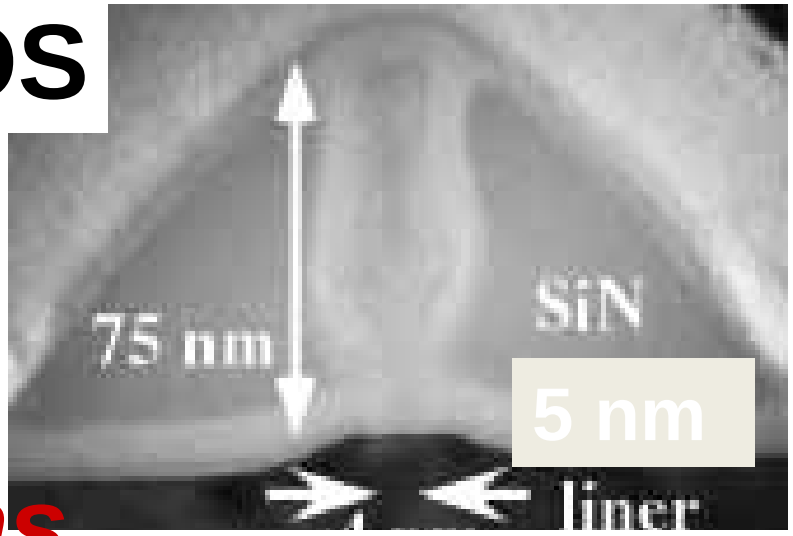
Electron wave length



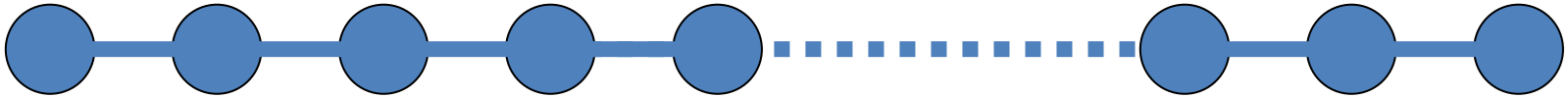


5 nm gate length CMOS

Is a Real Nano Device!!

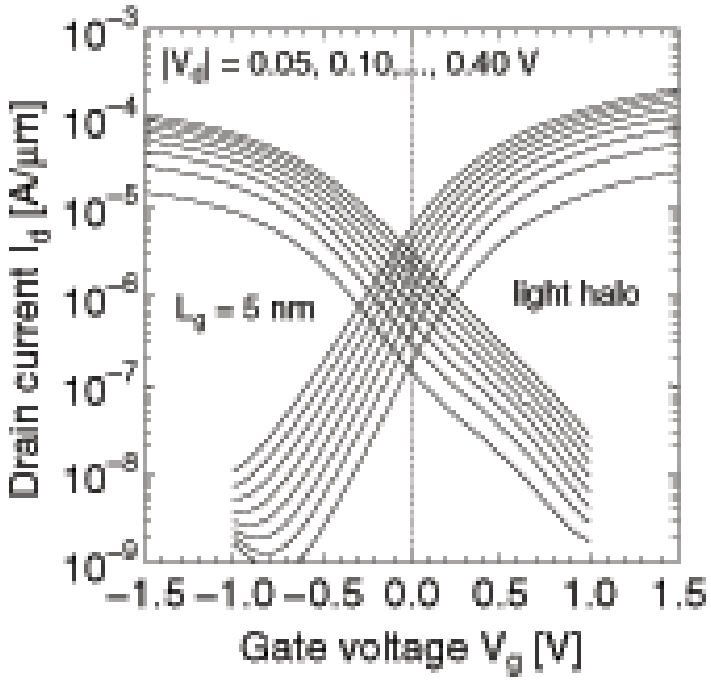


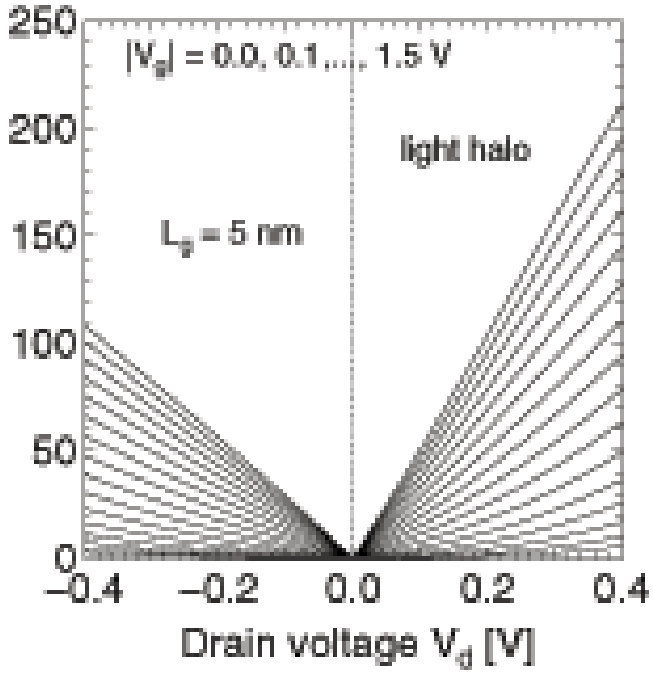
Length of 18 Si atoms



H. Wakabayashi
et.al, NEC

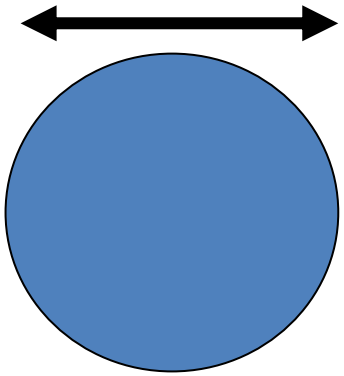
IEDM, 2003





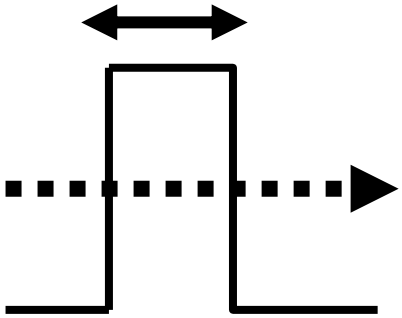
Electron wave length

10 nm



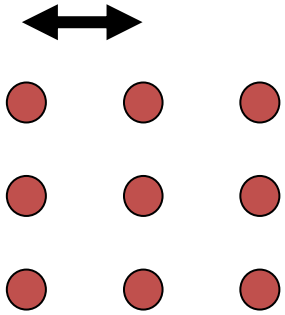
Tunneling distance

3 nm



Atom distance

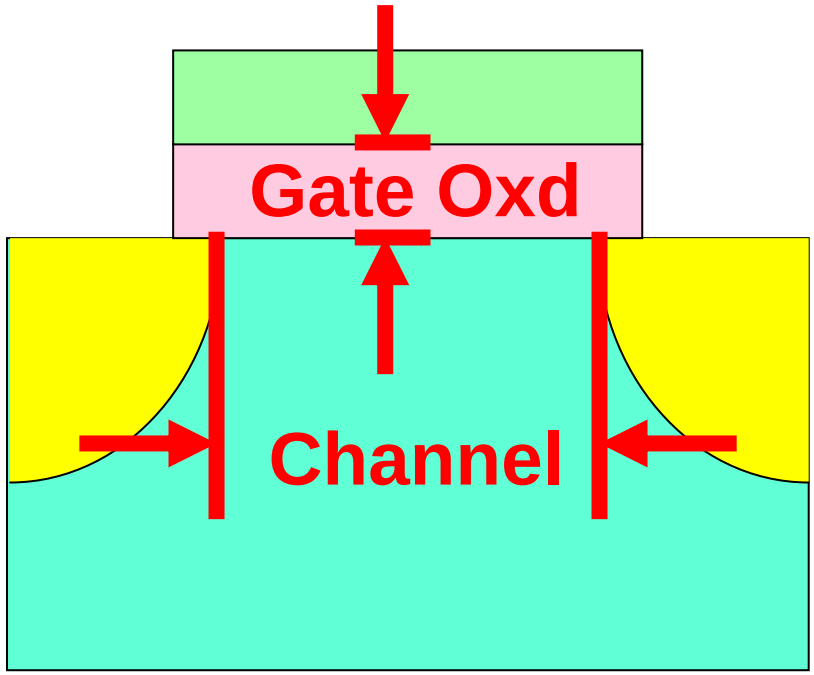
0.3 nm



Downsizing limit!

Channel length

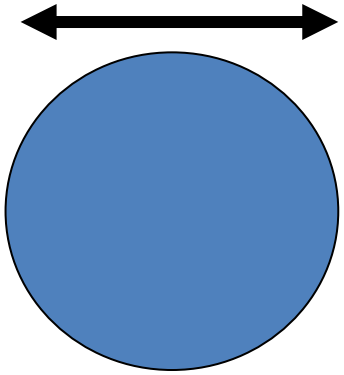
Gate oxide thickness



Prediction now!

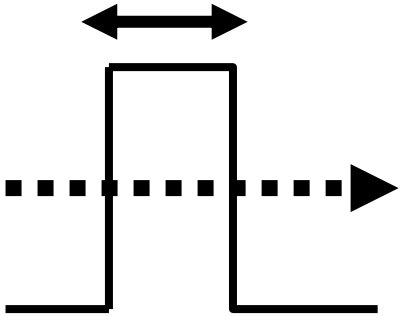
Electron wave length

10 nm



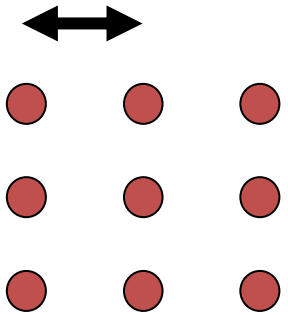
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

How about the integration of such small-geometry MOSFETs in a chip?

1)Integration of huge number of the ultra-small MOSFETs would consume too huge power and thus, creates too huge heat?

2)Integration of such ultra-small MOSFETs causes too huge variations in the transistor characteristics, which could make the circuit design impossible?

3)There are too many number of transistors in a chip for the circuit designers to manipulate? (design crisis),

4)There would be no merit of transistor downsizing in performance and power, because of RC (resistance capacitance product) of interconnect cannot be reduced aggressively any more?

5)Who will pay the huge development and production costs for the integration of such ultra-small MOSFETs? Note that the prices for the recent process equipments and the lithography mask became extremely high.

These concerns have been argued in the past 15 years at every new generation of the products, like the wolf boy.

Fortunately, the wolf has not come, and the concerns have not come true.

It is expected that we can go with several more generations for the integration.

There will be still a room for squeezing the technologies to obtain the merit of the scaling-down for integration.

The continuous progress of CMOS technologies for
- high-performance
- low power

is very important because of the 3 reasons:

1) Rapid progress of aging population and falling birth rate

1) Global warming

1) Semiconductor industry and world economy

1)Rapid progress of aging population and falling birth rate:

Replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example.

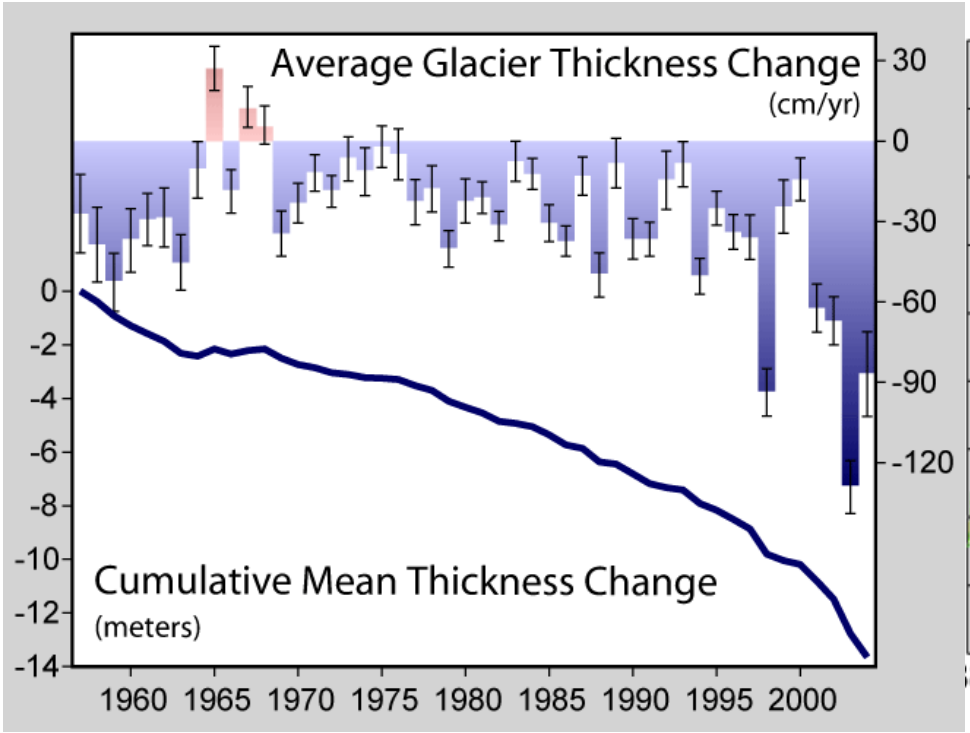
For, the daily family use, much higher intelligence and much lower power consumption than those of today are required.

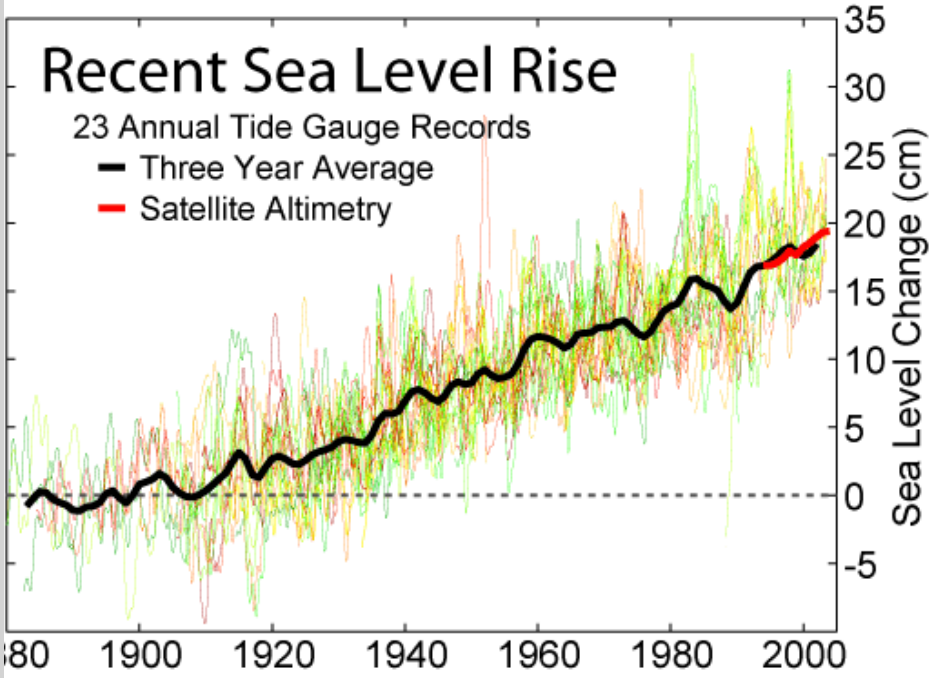
Robot in 21c cannot made without integrated circuits

Robot (21C)

Karakuri (Windup Mechanical) do
(18C) in Japan

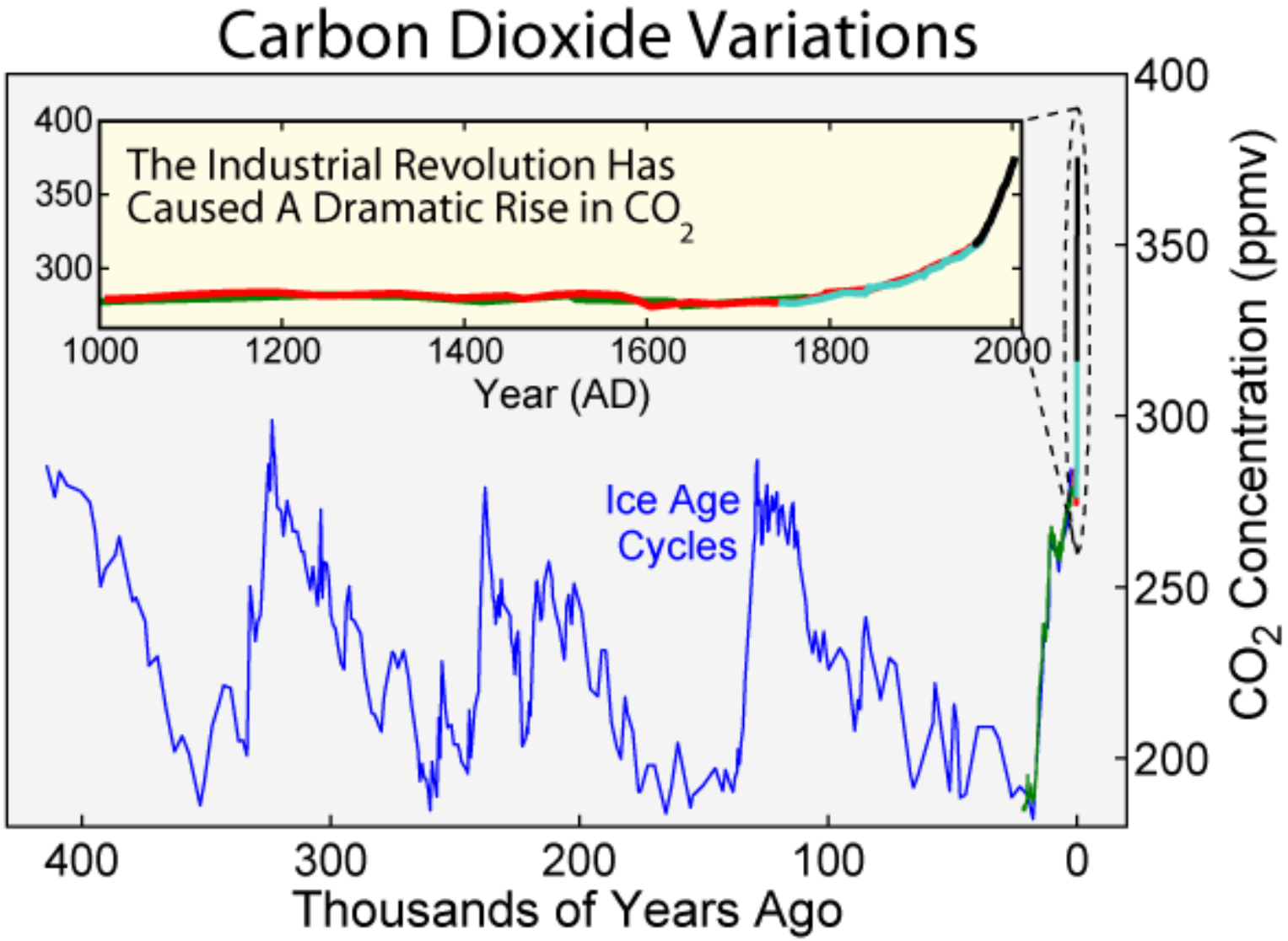
2) Recent Significant Global Warming

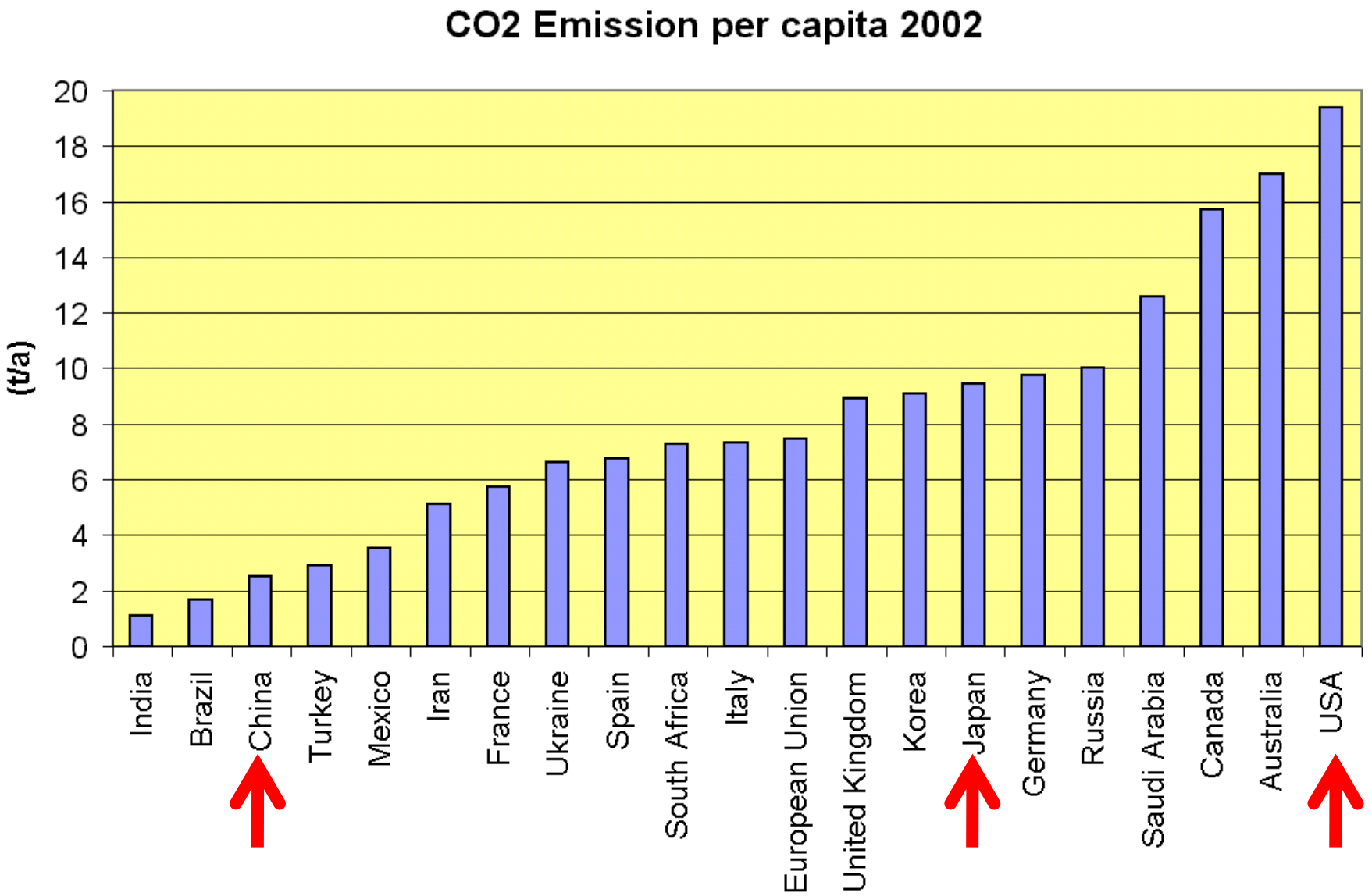




We need reduce CO2 generation!

→ Low power technology is urgent request




CO2 Emission per capita 2002
(t/a)
0
2
4
6
8
10
12
14
16
18
20
India
Brazil
China
Turkey
Mexico
Iran
France
Ukraine
Spain
South Africa
Italy
European Union
United Kingdom
Korea
Japan
Germany
Russia
Saudi Arabia
Canada
Australia
USA

3) Semiconductor industry, and world economy

If there is no more downsizing such as

45 → 32 nm Logic, 8 Gbit → 16 Gbit Memory

- LSIs will not be sold well, and semiconductor companies will face a disaster.

- Equipment and martial companies as well.

-There is no more R & D for semiconductors and many people will loose their jobs.

→ World economy crisis!

History and future of Transistor

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking

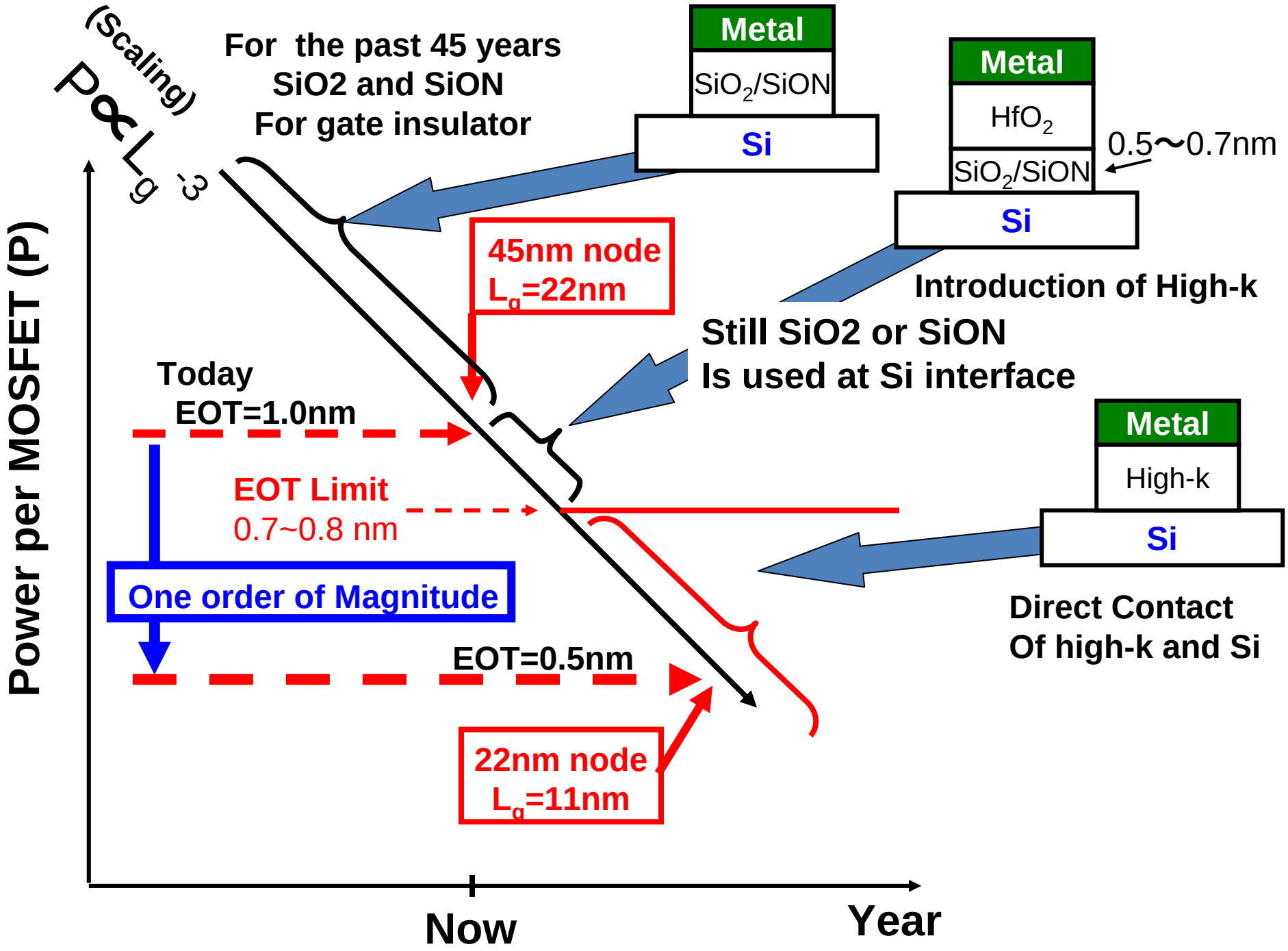
C, V $\propto$ L C: Capacitance V: Voltage

Switching speed CV/I → Decrease

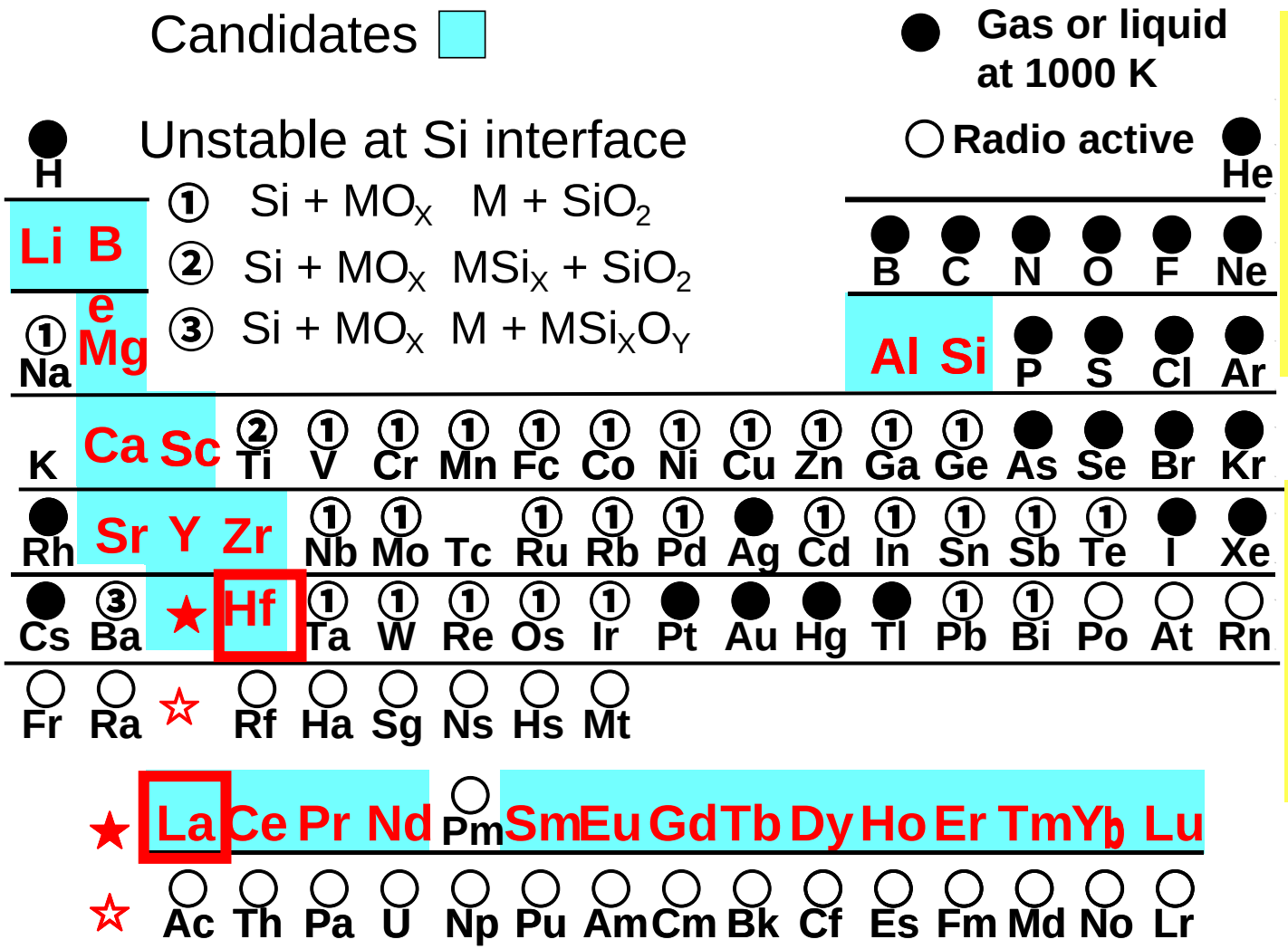
Power consumption $CV^2/2$ → Decrease

Integration density: $1/L^2$ → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm


(scaling)
P∝Lg -3
Power per MOSFET (P)
For the past 45 years
SiO2 and SiON
For gate insulator
Metal
SiO2/SiON
Si
Metal
HfO2
SiO2/SiON
Si
0.5~0.7nm
45nm node
Lg=22nm
Introduction of High-k
Still SiO2 or SiON
Is used at Si interface
Today
EOT=1.0nm
EOT Limit
0.7~0.8 nm
Metal
High-k
Si
One order of Magnitude
Direct Contact
Of high-k and Si
EOT=0.5nm
22nm node
Lg=11nm
Now
Year

Choice of High-k elements for oxide



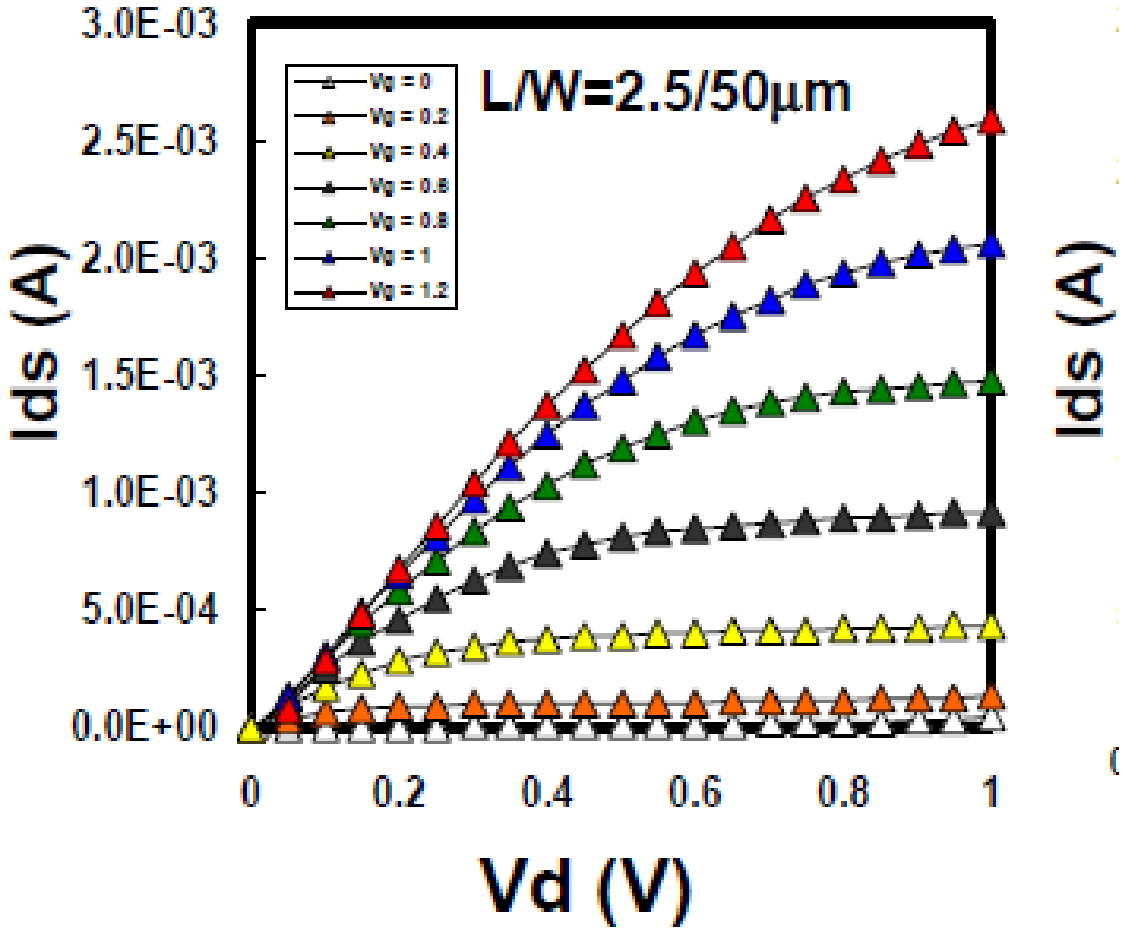
HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

EOT = 0.48 nm Our results

Transistor with La2O3 gate insulator



CMOS downsizing is critically important

However now, many people expect that we will reach limit in 2020.

Totally, new paradigm after reaching
the downsizing limit.

What will be?

After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.

After 2020

4 reasons for no downsizing anymore
or No decrease in gate length

---

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.
   Ballistic ← No scattering of carriers in channel
   Thus, all the carrier from the source reach drain

2. Increase of Off-current (Subthreshold current)

3. No decrease of Gate capacitance by parasitic components

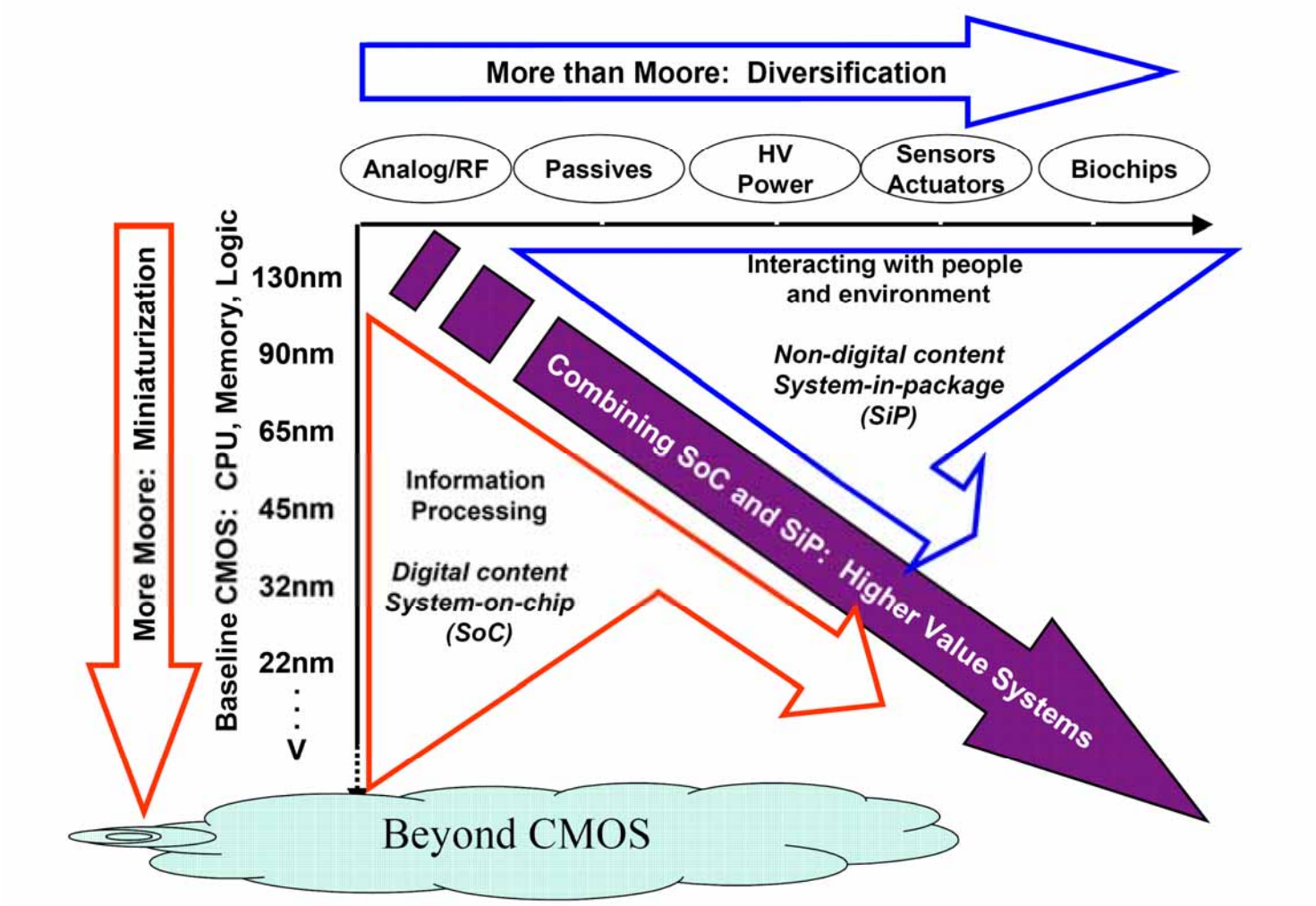
4. Increase in production cost.

After 2020

What will be the world with no gate length reduction?

More Moore and More than Moore

Moore's Law & More

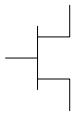
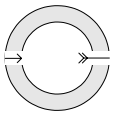
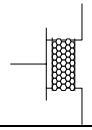
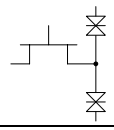
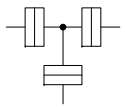
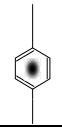
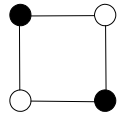
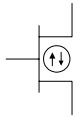


Question what is the other side of the cloud?

ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

Victor V. Zhirnov and Ralph K. Cavin III, ECS 207
Washington DC

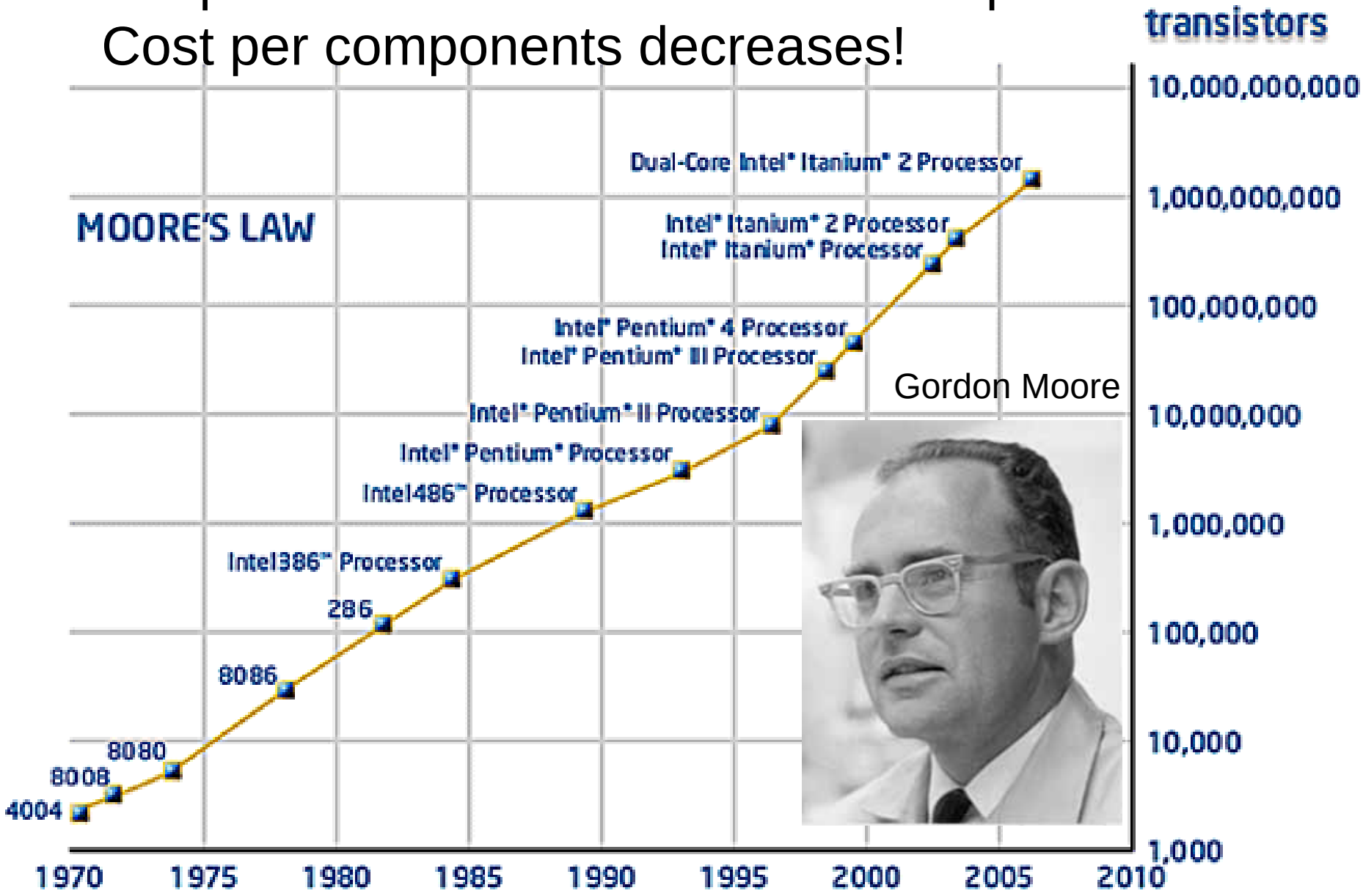
Device								
	FET	*RSFQ*	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*	*Spin transistor*
Cell Size	100 nm	0.3 µm	100 nm	100 nm	40 nm	Not known	60 nm	100 nm
Density (cm^{-2})	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz	1 MHz	30 GHz
Switching Energy, J	2×10^{-18}	$>1.4\times10^{-17}$	2×10^{-18}	$>2\times10^{-18}$	$>1.5\times10^{-17}$	1.3×10^{-16}	$>1\times10^{-18}$	2×10^{-18}
Binary Throughput, $GBit/ns/cm^2$	86	0.4	86	86	10	N/A	0.06	86

We HAVE IDENTIFIED NO VIABLE EMERGING LOGIC TECHNOLOGIES for Information Processing beyond CMOS

We could keep the Moore’s law after 2020
Without downswing the gate length

What is Moore’s law.

Keep increase of the number of components.
Cost per components decreases!



http://www.intel.com/technology/mooreslaw/index.htm

We could keep the Moore's law after 2020
Without downswing the gate length

What is Moore's law.

→ to increase the number (#) of Tr. In a chip

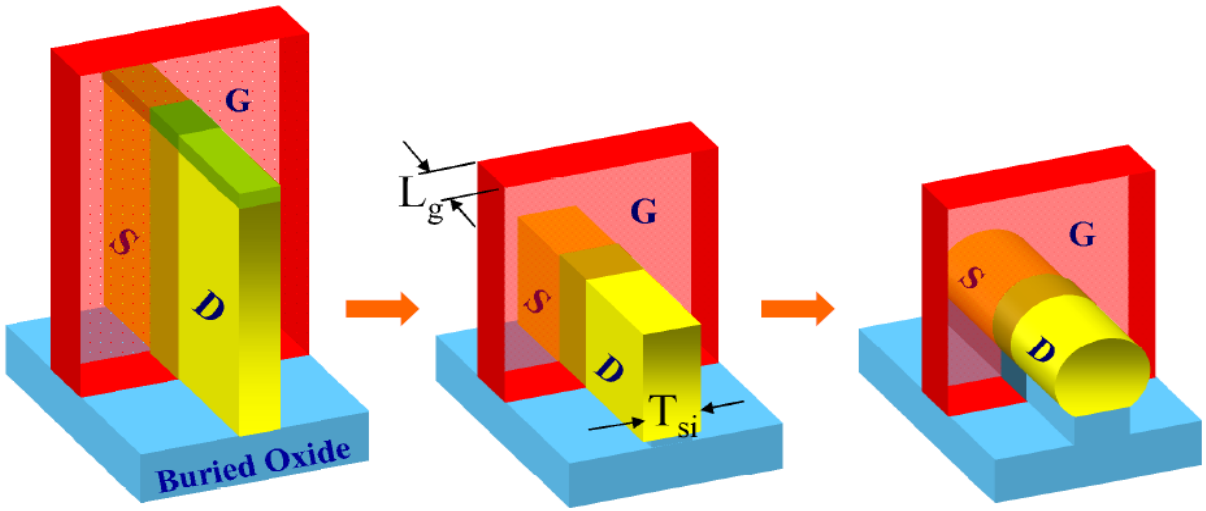
Now, # of Tr. in a chip is limited by power.

→ key issue is to reduce the power.

→ to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.

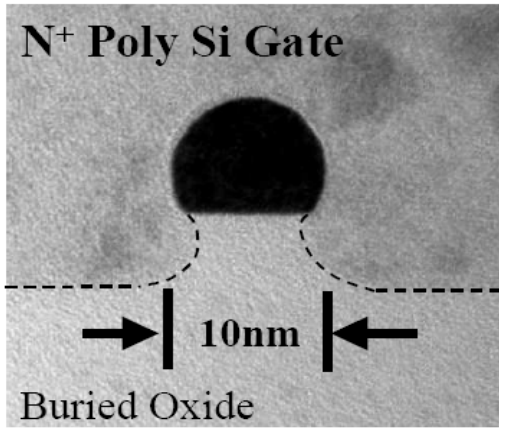
FinFET to Nanowire

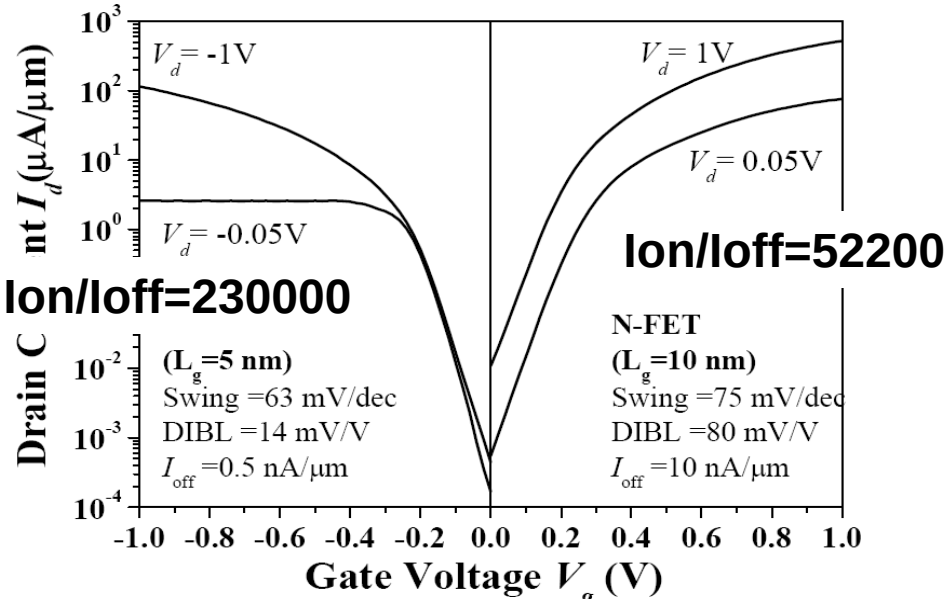


Double-Gate FinFET ($T_{si} = {}^{2}/_{3}\, L_g$)

Omega FinFET ($T_{si} = L_g$)

Nanowire FinFET ($T_{si} = 2L_g$)





Channel conductance is well controlled by Gate even at L=5nm

F.-L.Yang, VLSI2004

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage

M1. Use 1D ballistic conduction

M2. Increase number of quantum channel

M3. Increase the number of wire or tube per area
3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.

1D conduction per one quantum channel:

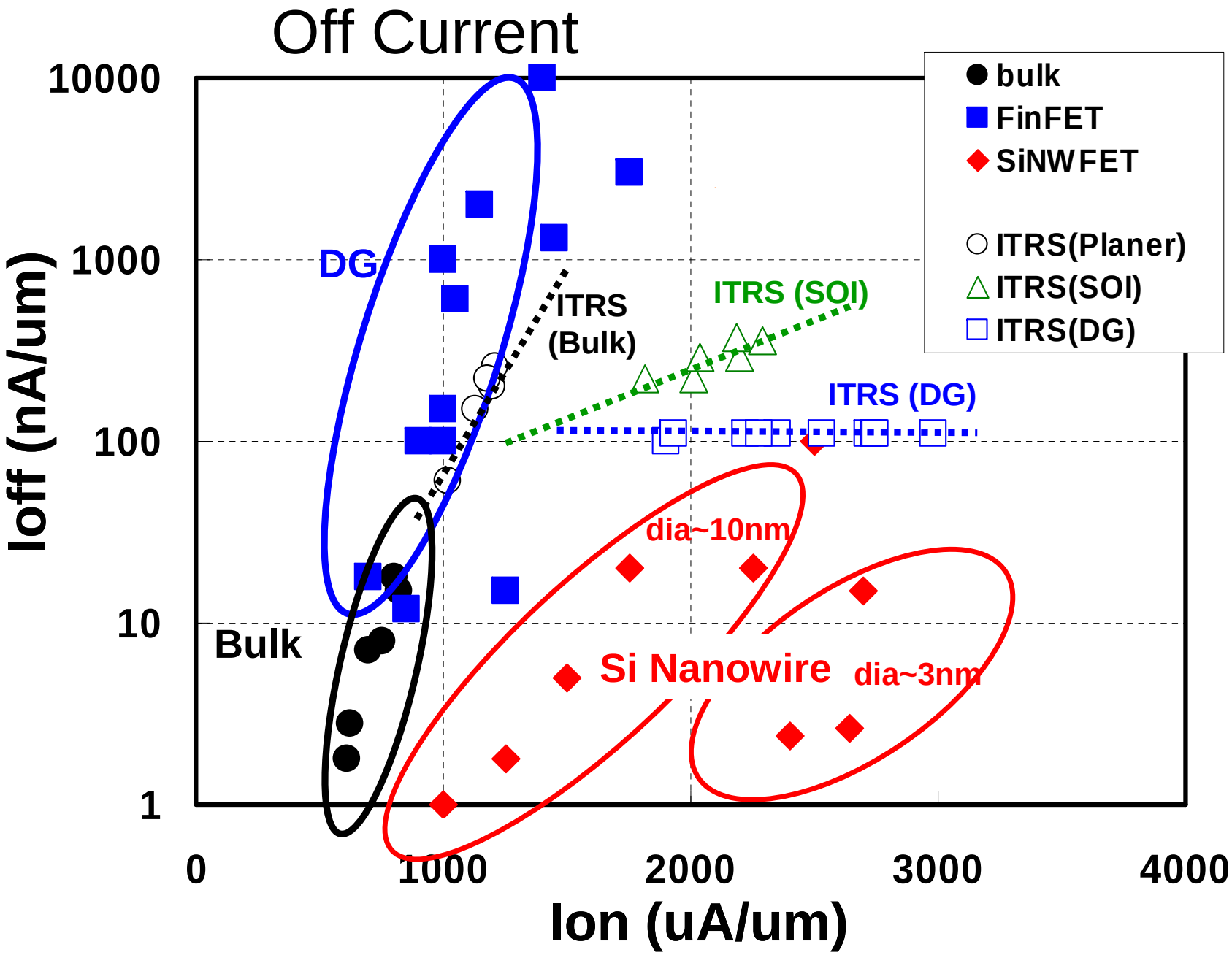
$G = 2e^2/h = 77.5\ \mu S$/wire or tube

regardless of gate length and channel material

That is 77.5 mA/wire at 1V supply

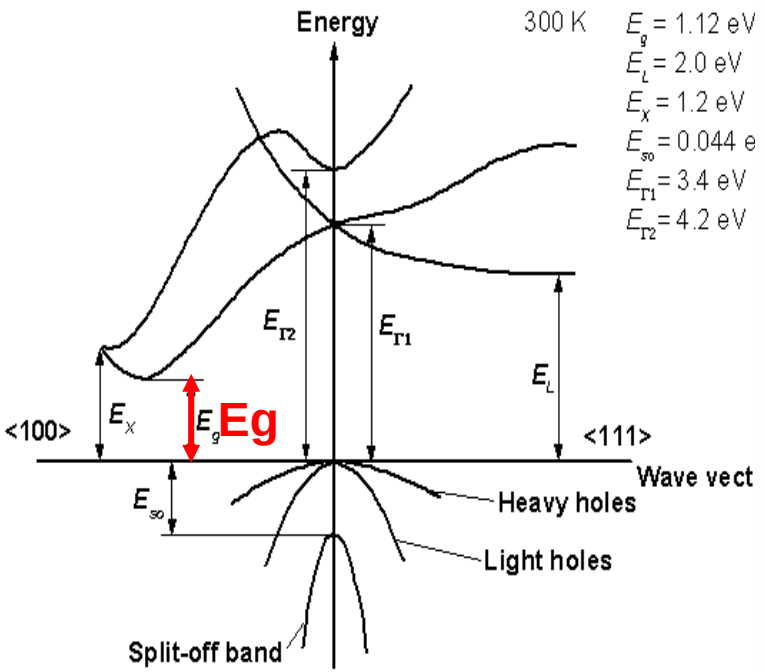
This an extremely high value

However, already 20mA/wire was obtained experimentaly by Samsung

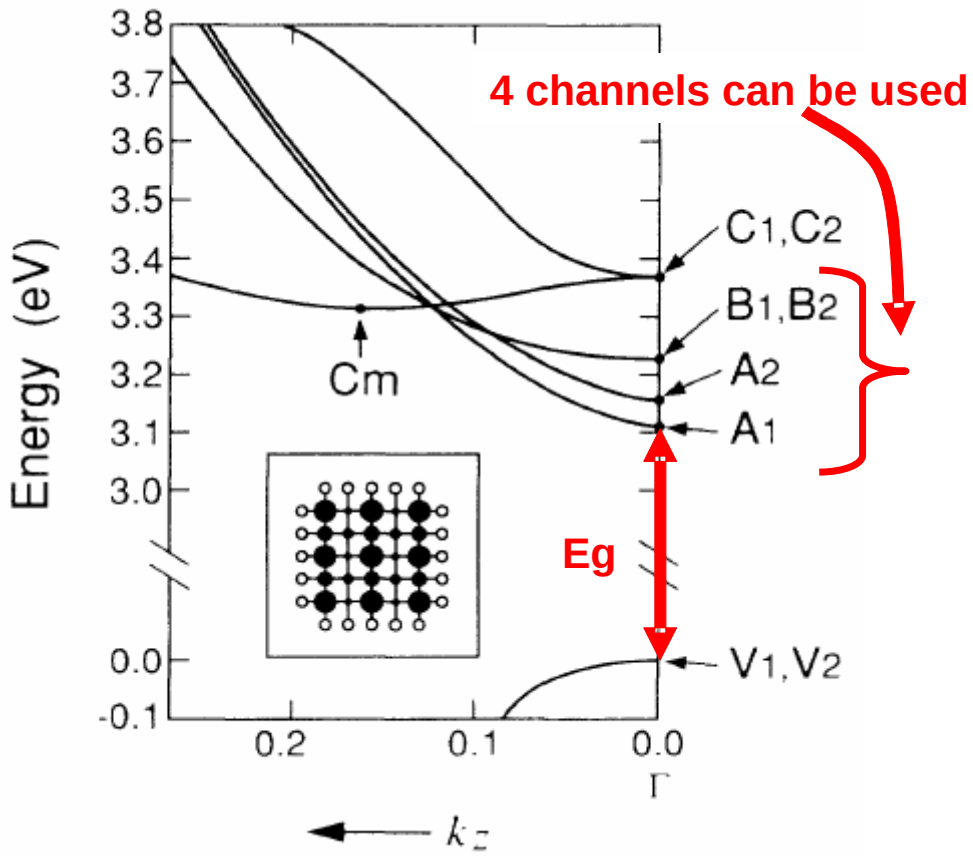

Off Current
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.



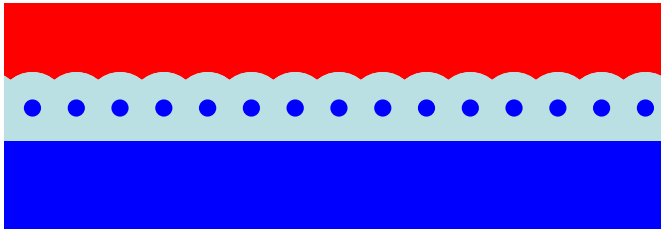
Energy band of Bulk Si



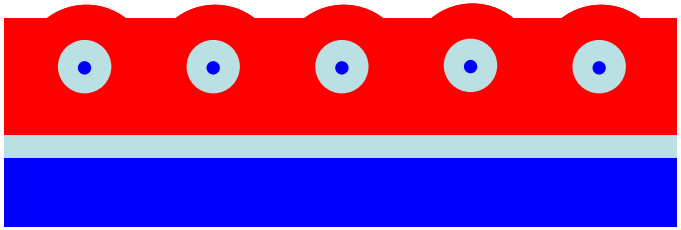
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

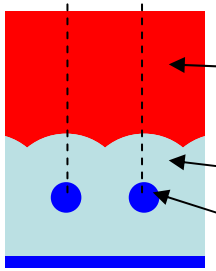
Front gate type MOS 165 wires /μm

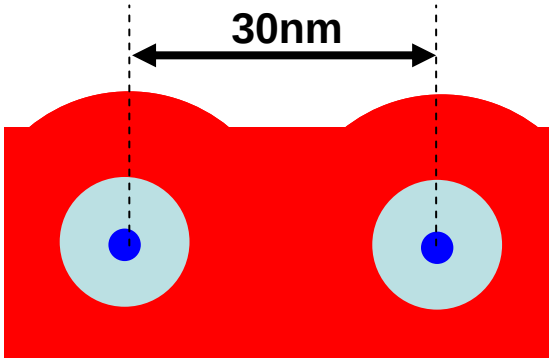


Surrounded gate type MOS 33 wires/μm

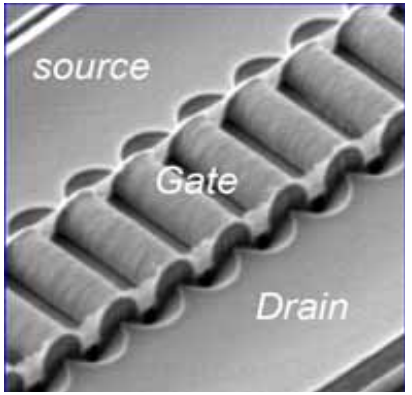


6nm pitch
By nano-imprint method



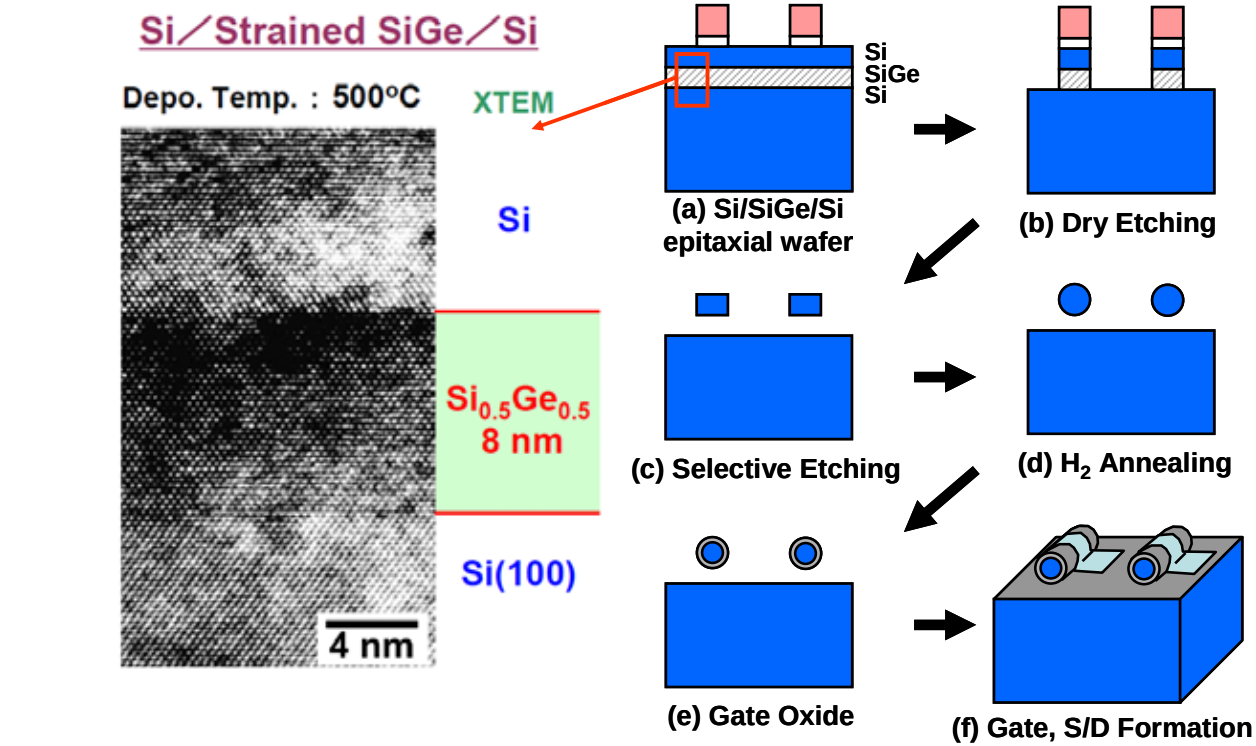


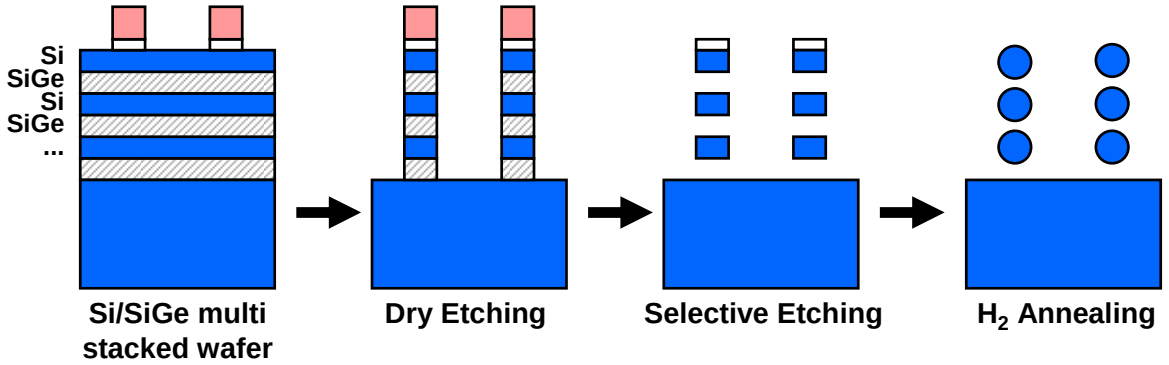
30nm pitch:
EUV lithograpy

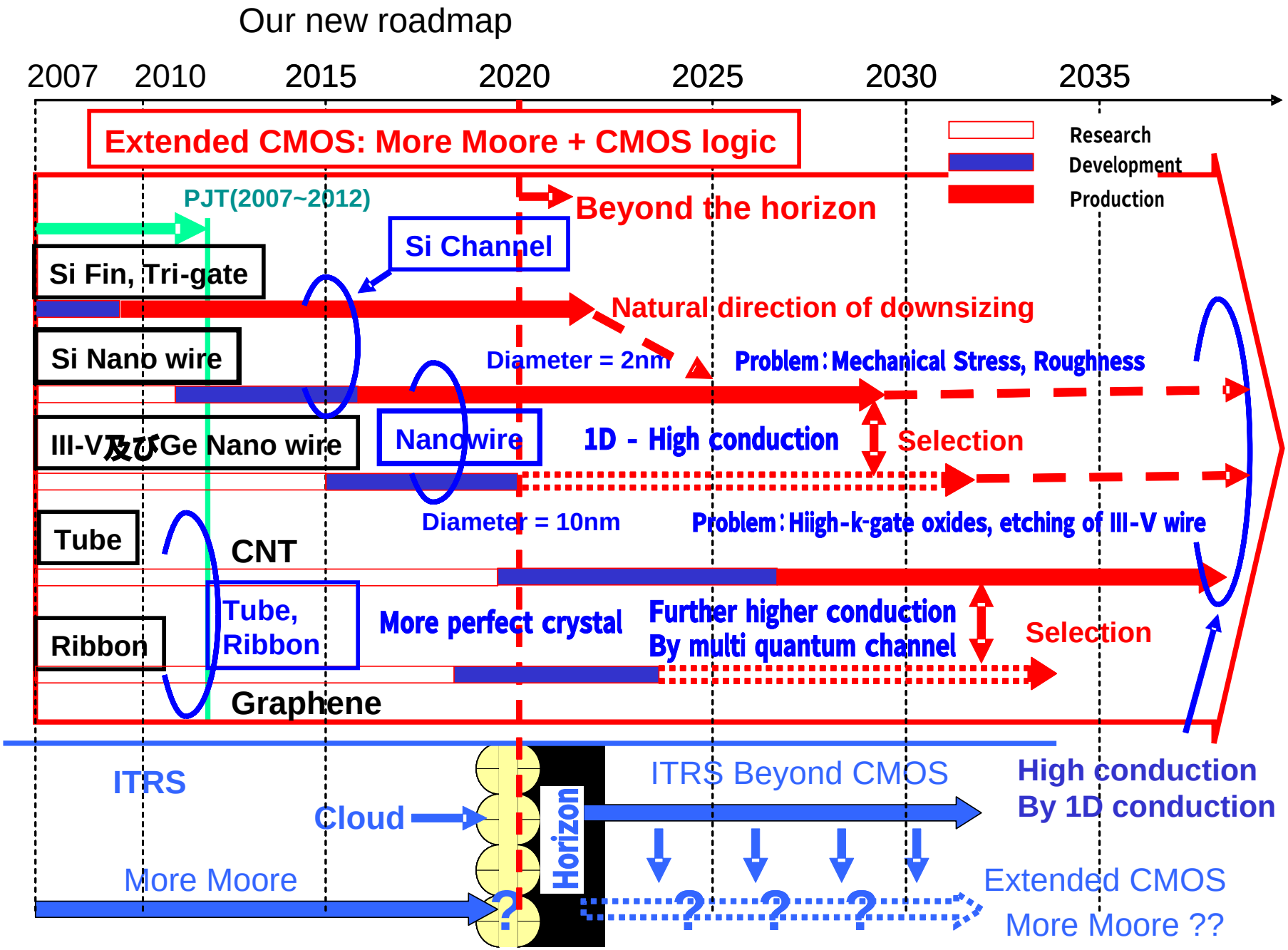


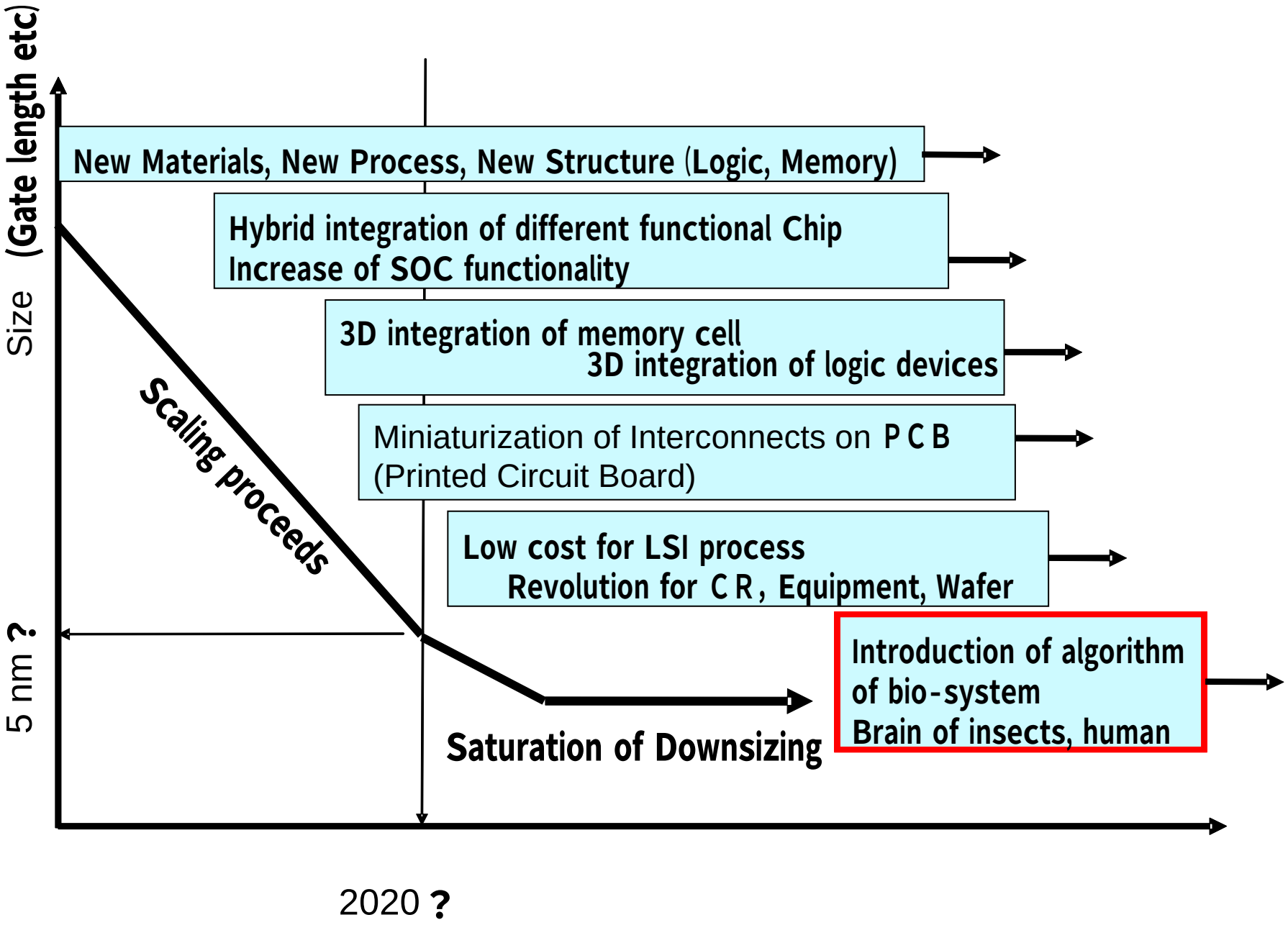
Surrounded gate MOS

Increase the number of wires towards vertical dimension






Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V及びGe Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Graphene
ITRS
Cloud
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
More Moore
?
?
?
?
Extended CMOS
More Moore ??


Size (Gate length etc)
New Materials, New Process, New Structure (Logic, Memory)
Hybrid integration of different functional Chip
Increase of SOC functionality
3D integration of memory cell
3D integration of logic devices
Miniaturization of Interconnects on P C B
(Printed Circuit Board)
Low cost for LSI process
Revolution for C R, Equipment, Wafer
Introduction of algorithm
of bio-system
Brain of insects, human
Scaling proceeds
Saturation of Downsizing
5 nm ?
2020 ?

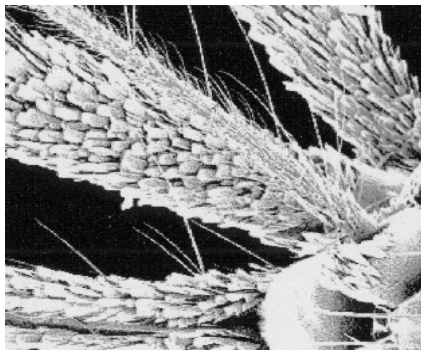
Brain

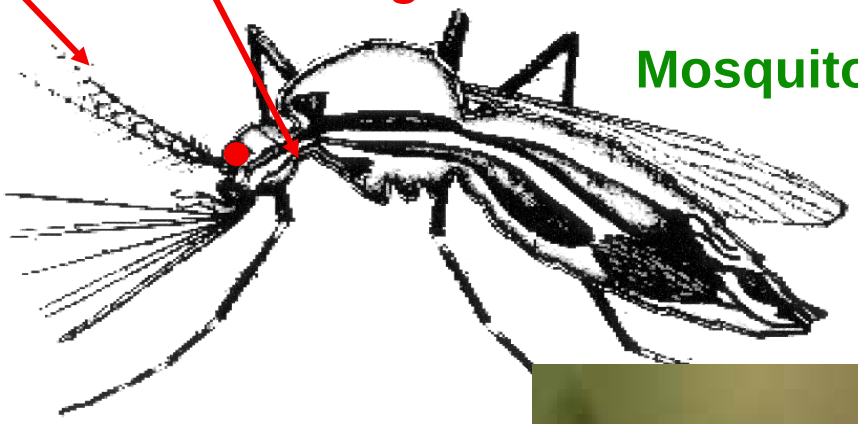
Sensor

Ultra small volume
Small number of neuron cells
Extremely low power

Infrared
Humidity
CO_2

Real time image processing
(Artificial) Intelligence
3D flight control





Mosquito

System and Algorism becomes more important !

But do not know how?

Dragonfly is further high performance

Thank you
for your attention!