CMOS Technology After Reaching The Scale Limit

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Abstract

Progress of CMOS LSI has been accomplished by the downsizing of MOSFETs. However, it has been expected that the downscaling will reach its limits about the gate length of 5 nm around the year of 2020. 2020 is not too far, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit. This paper will discuss the picture of the CMOS technology in the world after the 2020.

1. Introduction

Nowadays, CMOS Large Scale Integrated circuits (LSIs), are really indispensable components for our human society. Needless to say, but almost all the human activities, living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS LSI operation. For example, all the bank activities immediately stop without CMOS computation. Cellular phones do not exist without CMOS technology. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software's required for the integrated circuits.

From now on, the continuous progress of CMOS technologies in terms of high-performance operation and low power consumption is still very important because of the following three reasons. At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required, and the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO_2 gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the 'cooling of the earth' in two ways. One is direct contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by so called 'Green IT' procedure. This can be done by the development of low power and high performance CMOS devices such used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point, and thus, from the global economical point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 8 to 16 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.

It is well known that the progress of CMOS LSI has been accomplished by the downsizing of MOSFETs. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970's. It was fortunate, however, that those limits were proven not to be true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics.

However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. 2020 is not too far, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit. This paper will discuss the picture of the CMOS technology in the world after the 2020.

2. CMOS Downsizing limit and after that

Why it is expected that about 5 nm is the limit of the downsizing? There are four main reasons; A) Difficulty on off-current suppression, B) Difficulty on increase in on-current, C) Difficulty on decrease in gate capacitance, D) Production and development cost increase.

A. Difficulty on off-current suppression

With decrease in gate length, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.

B. Difficulty on increase of on-current

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

C. Difficulty on increase of on-current

One of the scaling merits is to reduce the gate capacitance, C_g, because the switching time of MOSFETs is defined by C_g/I_d, where I_d is the drain on-current. However, C_g will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain depth are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.

E. Possible solution after that

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called 'beyond CMOS' or 'Post Si' new devices, which are believed to really replace CMOS transistors usable for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with 'More Moore' approach with combining that of 'More than Moore.' Then, what is 'More Moore' approach after we reached the downsizing limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the 'More Moore' law for certain period by replacing current CMOS transistors by nanowire or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction, multi-quantum channel per wire/tube and high-density integration of wire/tube in multi-layers. Figure 1 shows our roadmap for wire and tube MOSFETs after 2020. More explanation will be given at the presentation.

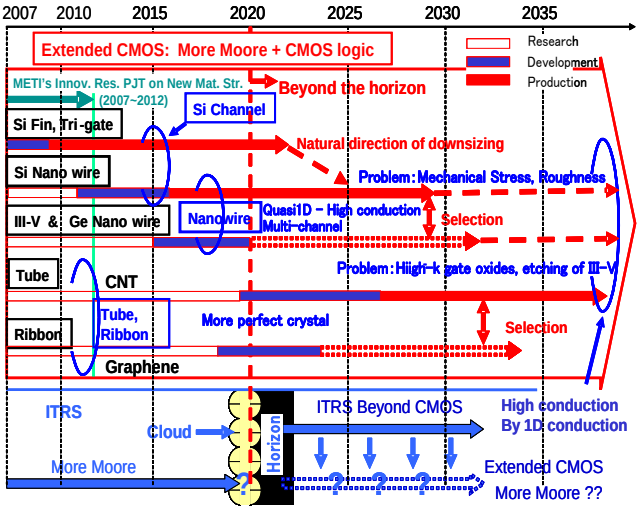

Fig. 1 Our roadmap for wire/tube MOSFETs

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