Advanced Logic Technologies with New Materials and Structures

January 18, 2008

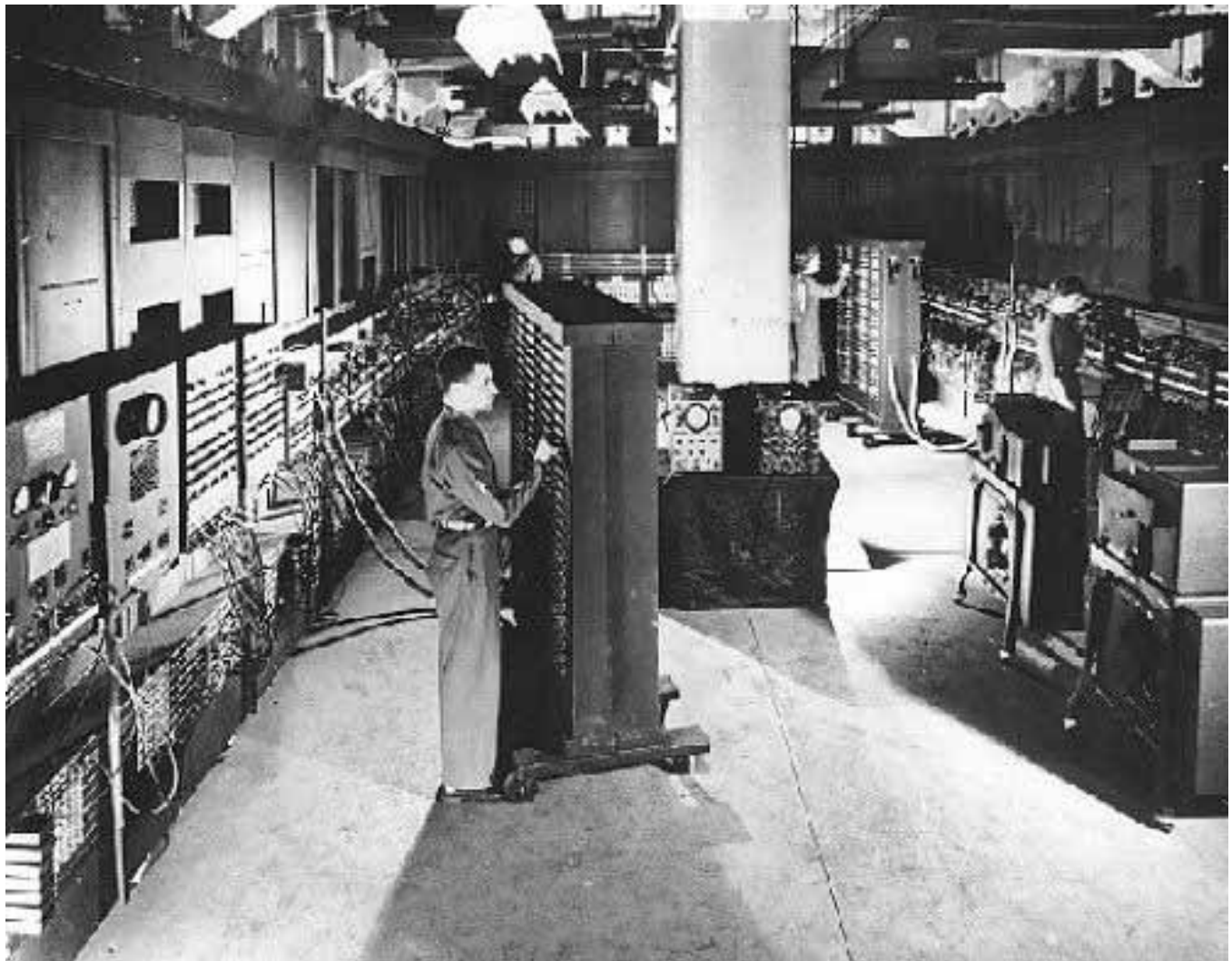
@IEEE ED Bangalore Chapter,
at IIS, Bangalore, India

Hiroshi IWAI
Tokyo Institute of Technology

First Computer Eniac:

made of huge number of vacuum tubes 1946

Problems: Big size, huge power, short life time filament

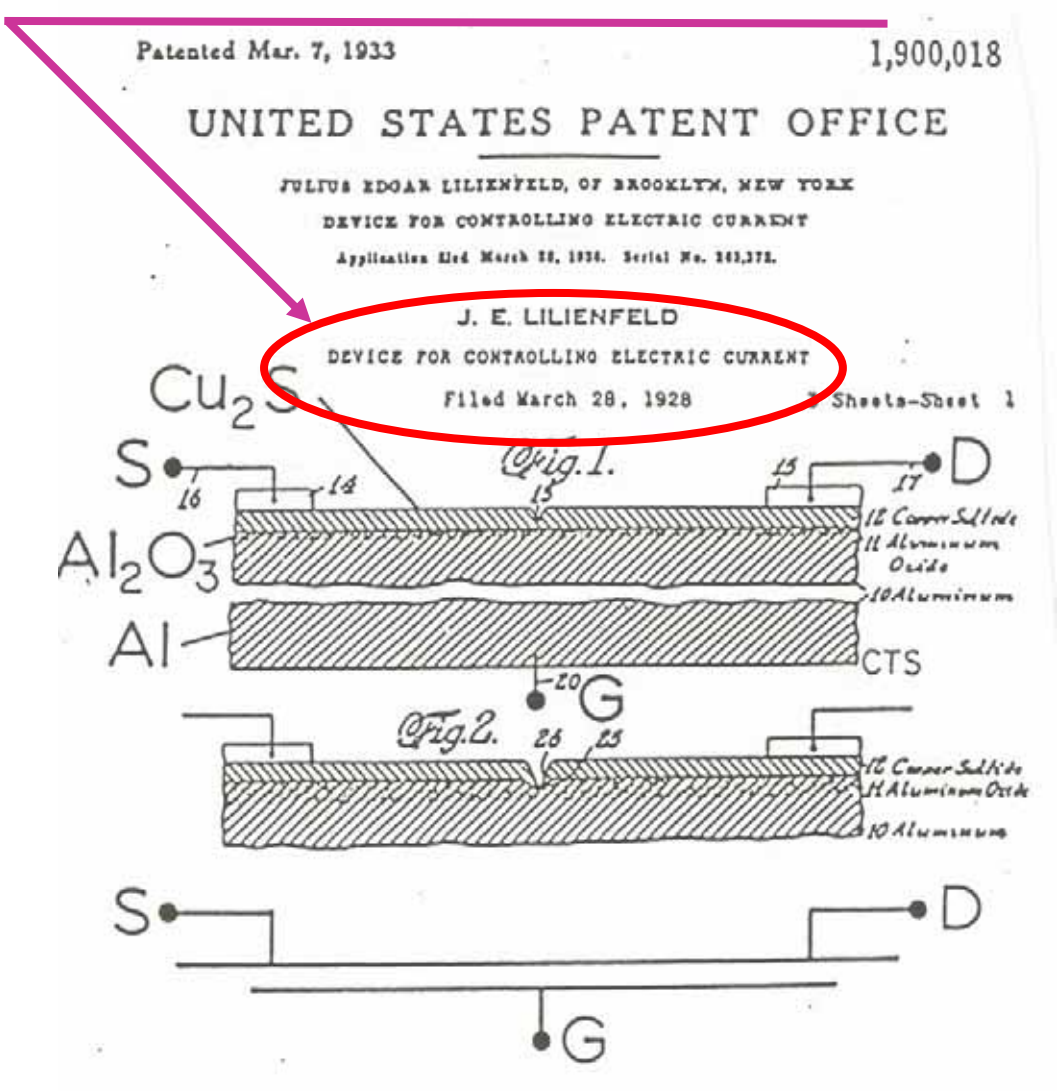


Idea of MOSFETs, 1928

J. E. LILIENFELD

DEVICES FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928



Patented Mar. 7, 1933 1,900,018

UNITED STATES PATENT OFFICE

JULIUS EDGAR LILIENFELD, OF BROOKLYN, NEW YORK

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Application filed March 28, 1928. Serial No. 263,372.

J. E. LILIENFELD

DEVICE FOR CONTROLLING ELECTRIC CURRENT

Filed March 28, 1928 2 Sheets-Sheet 1

Cu_2S

S

D

Al_2O_3

Al

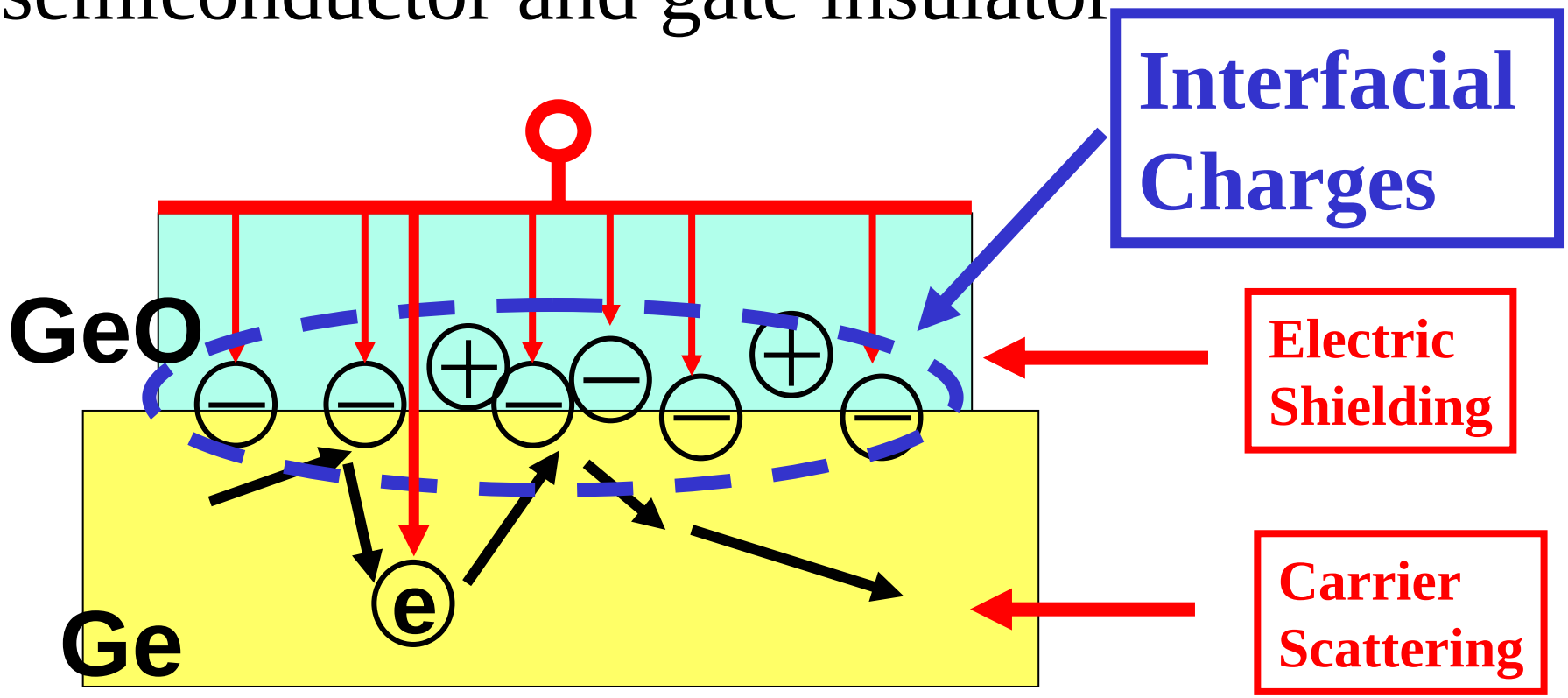
G

Fig. 1.

Fig. 2.

J.E.LILIENFELD

Very bad interface property between the semiconductor and gate insulator



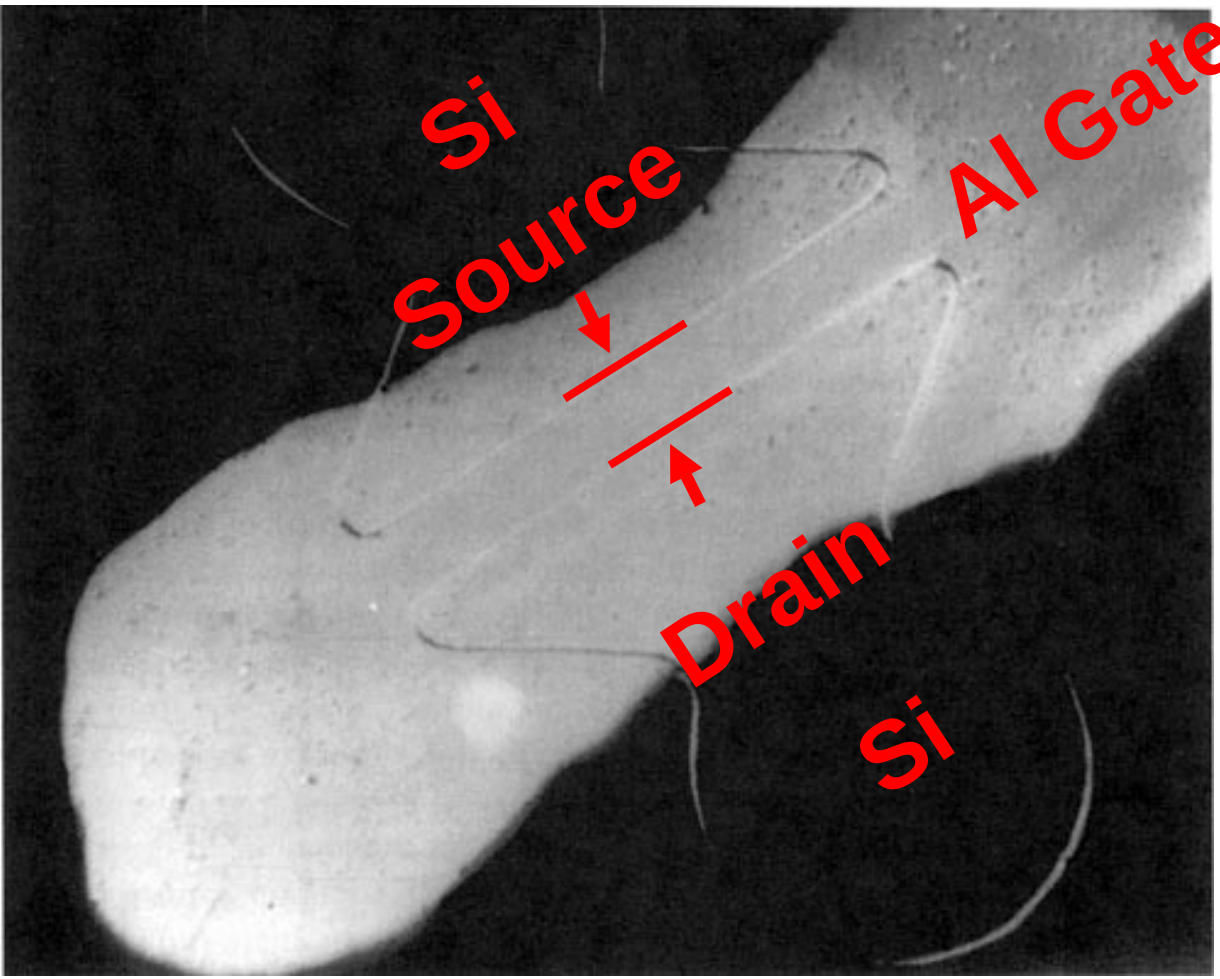
Drain Current was several orders of magnitude smaller than expected

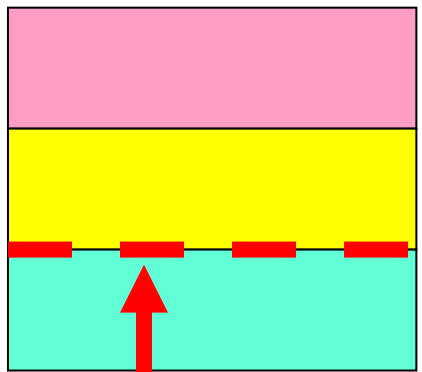
No one could realize MOSFETs. Even Shockley!

1960: First MOSFET
by D. Kahng and M. Atalla

Using Si and SiO2

Top View





Exceptionally good interface

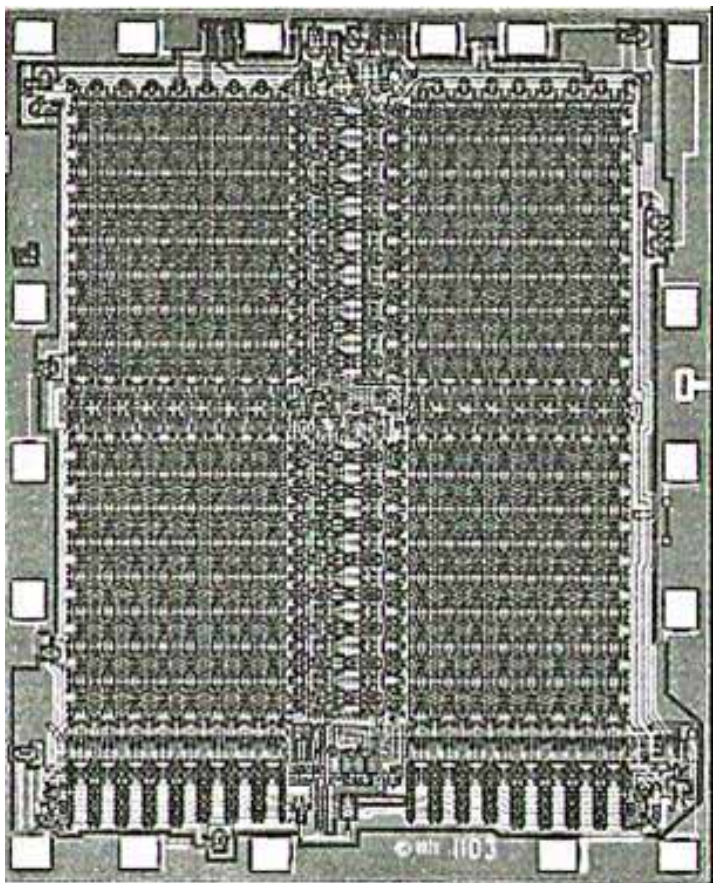
1970:

1st generation of LSIs

2006:

ULSIs

1k bit DRAM Intel → 32 G bit Nand Flash



History of gate stack

Shrinking, Shrinking, and Shrinking!

and then, Shrinking, Shrinking, and Shrinking!

$C, V \propto L$ C: Capacitance V: Voltage

Switching speed CV/I → Decrease

Power consumption $CV^2/2$ → Decrease

Integration density: $1/L^2$ → Increase

	1970	2007
Gate length	10,000 nm	25 nm
Gate Oxd Thickness	100 nm	1 nm

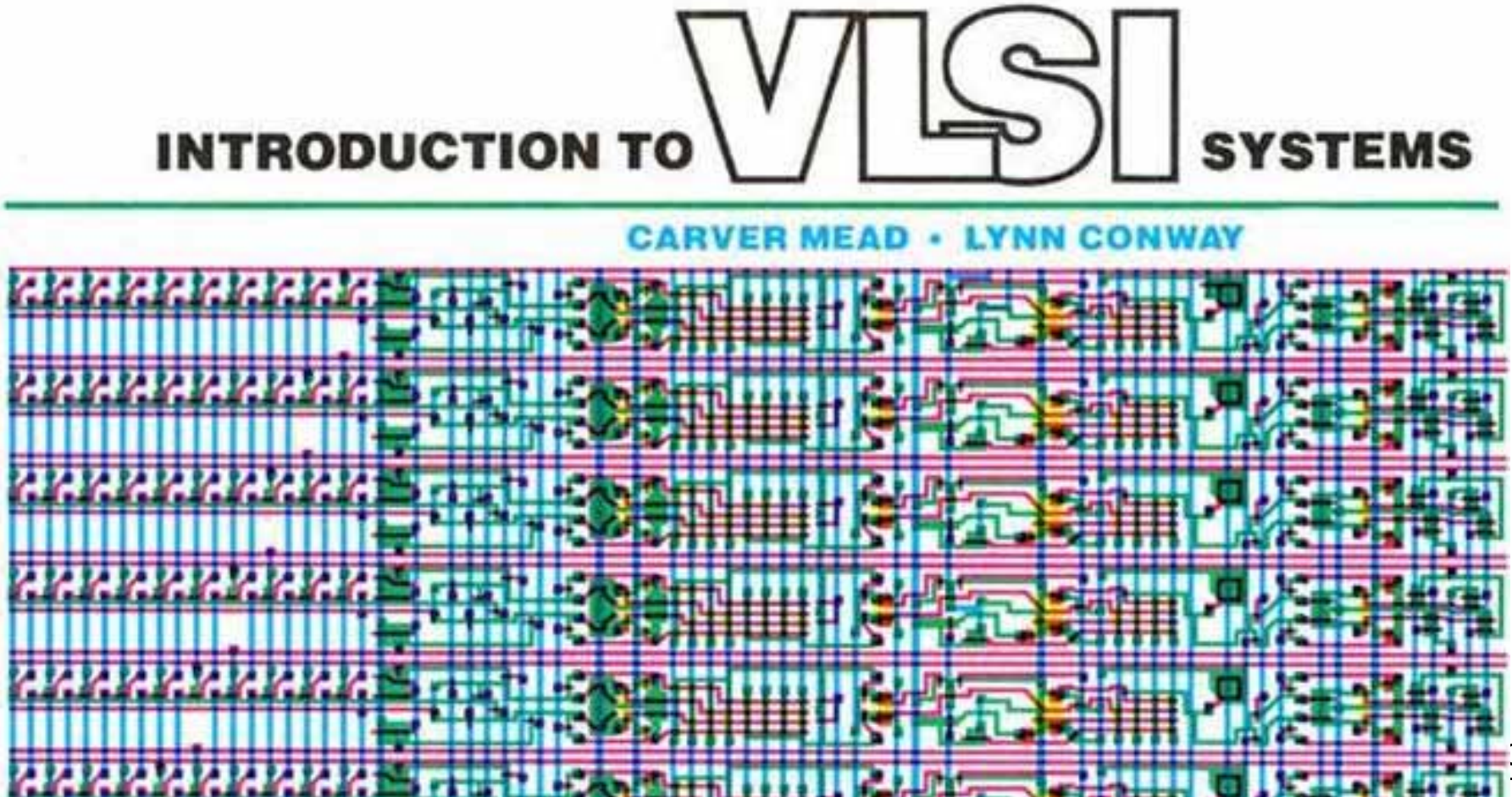
Downsizing of the components has been the driving force for circuit evolution

1900	1950	1960	1970	2000
Vacuum Tube	Transistor	IC	LSI	ULSI
10 cm	cm	mm	10 μm	100 nm
10^{-1}m	10^{-2}m	10^{-3}m	10^{-5}m	10^{-7}m

In 100 years, the feature size reduced by one million times.

We have never experienced such a tremendous reduction in human history.

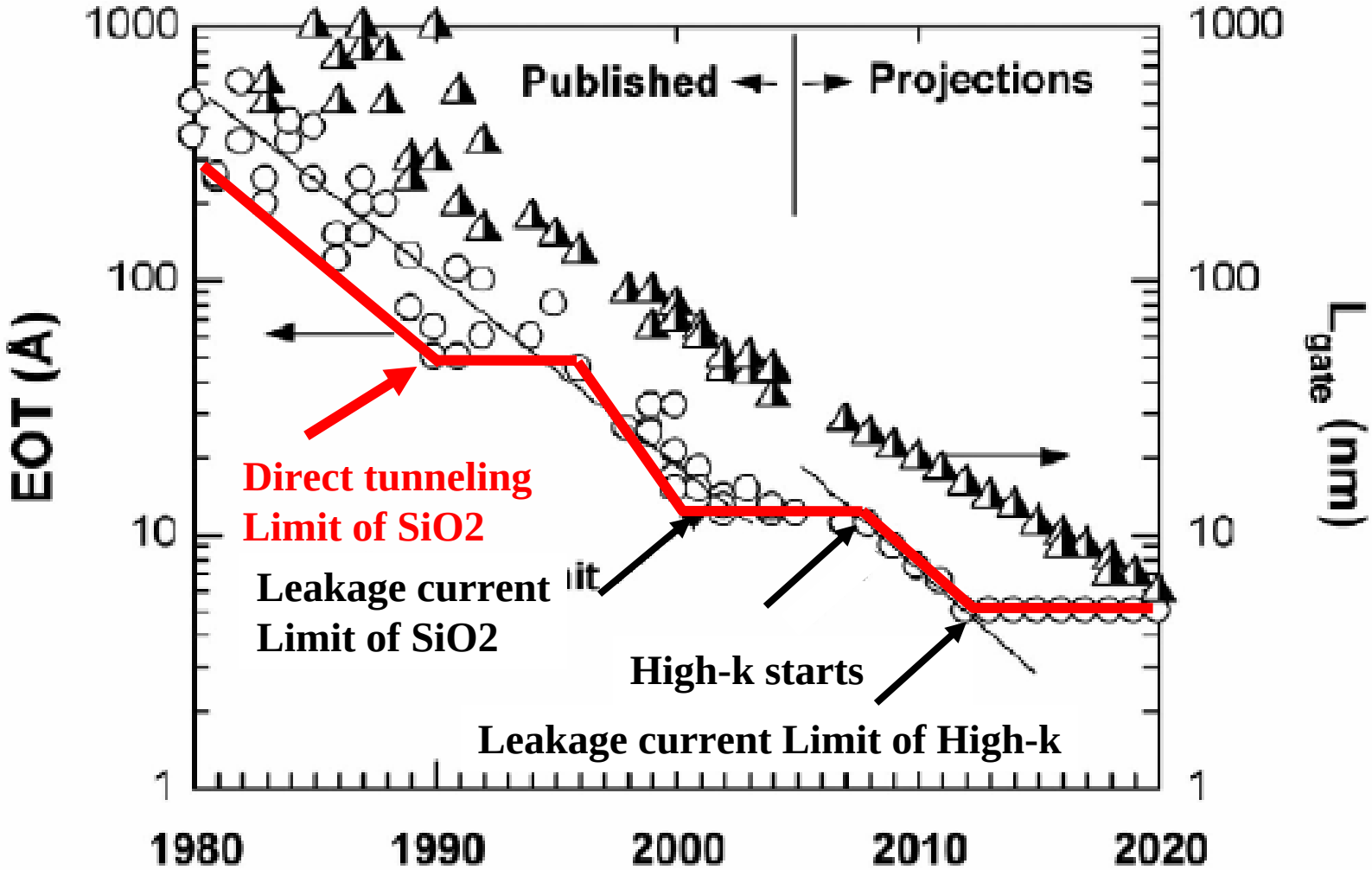
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.



VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

MOSFET gate oxide thickness trend



EOT: Equivalent Oxide Thickness to that of SiO2

B. H. Lee et al., materials today (2006)

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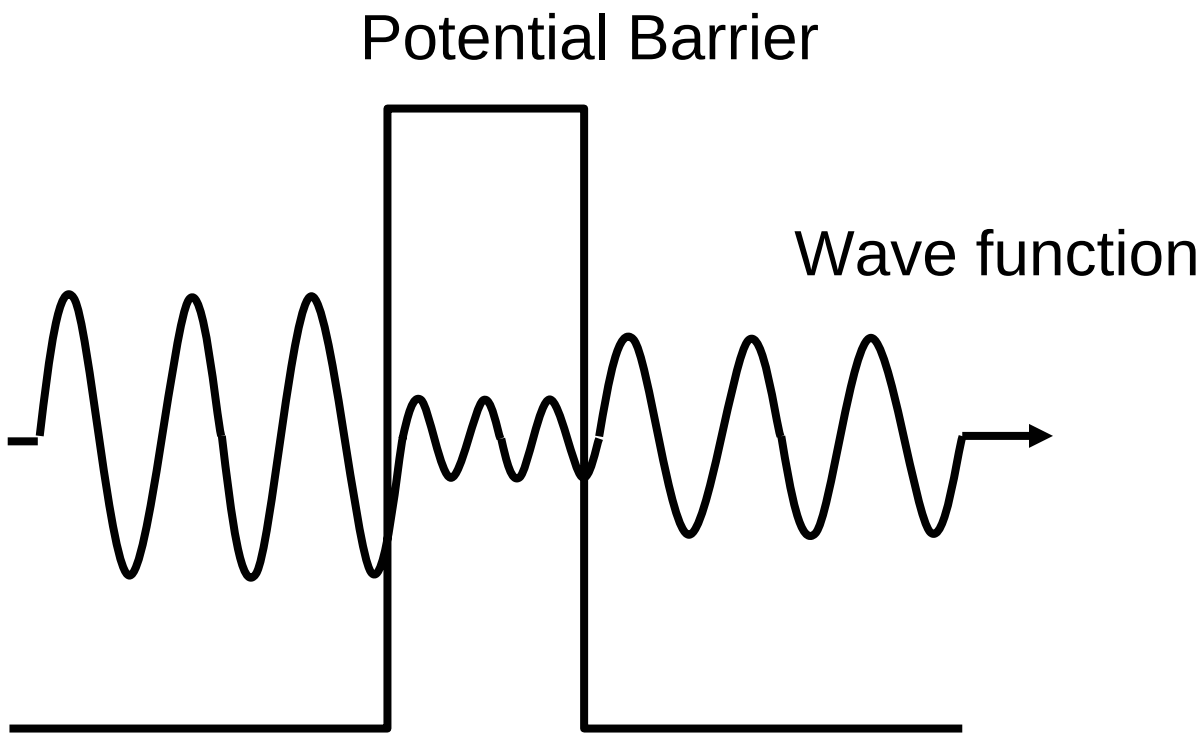
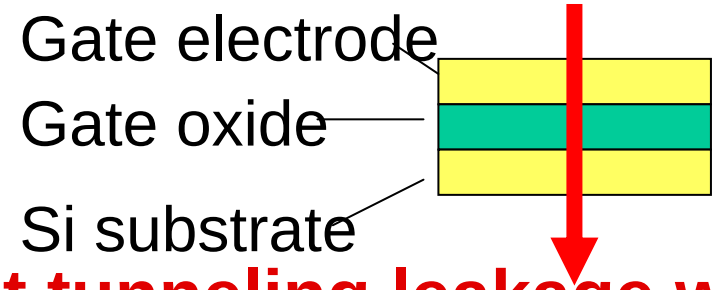
Direct-tunneling effect



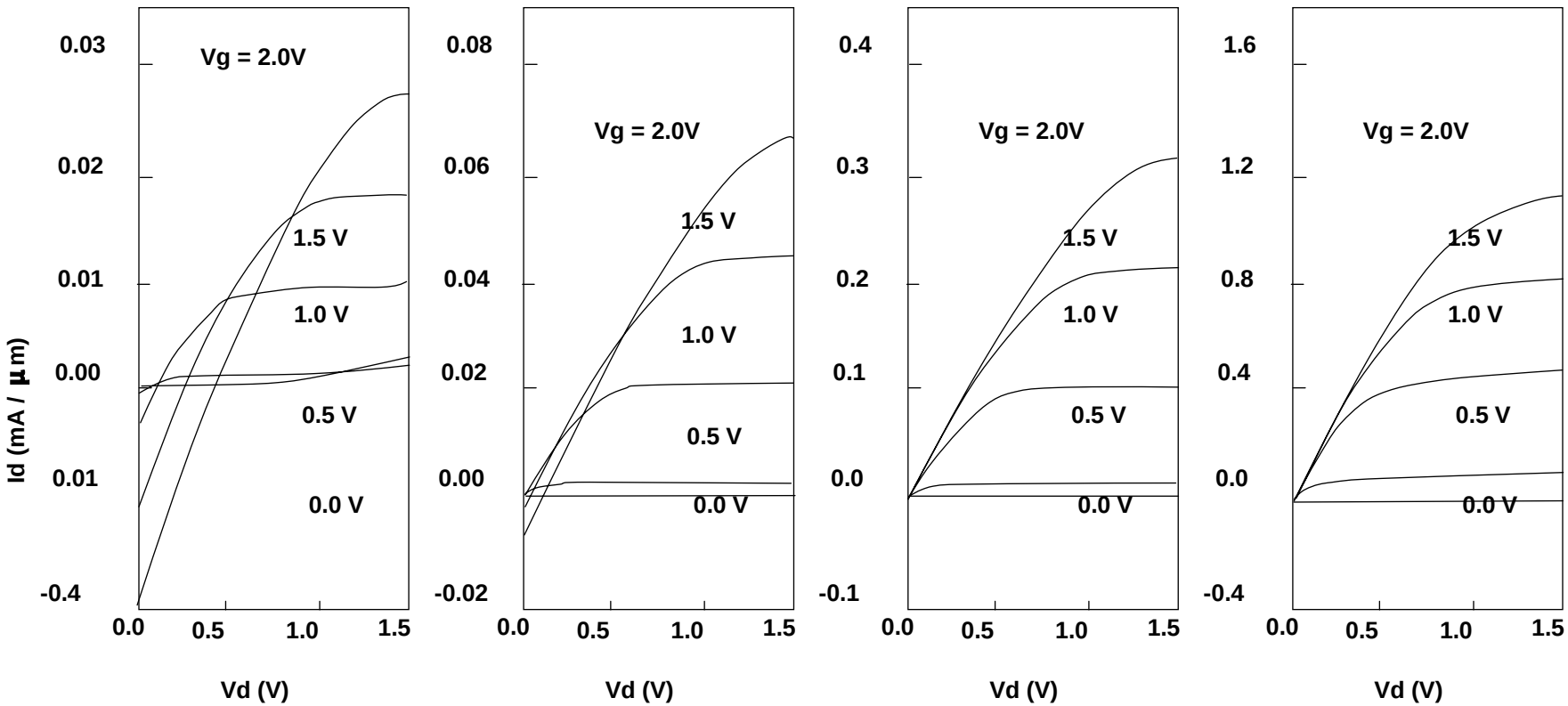


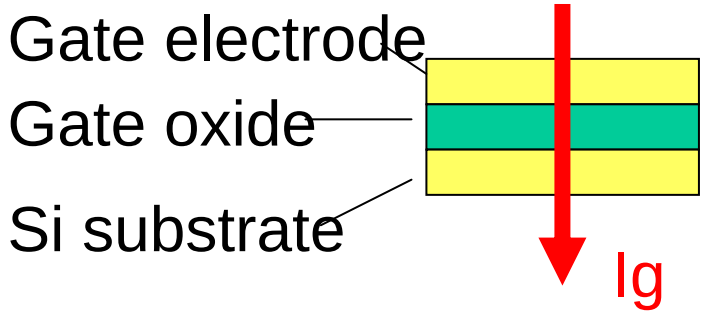
Direct tunneling leakage current start to flow when the thickness is 3 nm.

Direct tunneling leakage was found to be OK! In 1994

MOSFETs with 1.5 nm gate oxide

Lg = 10 μm Lg = 5 μm Lg = 1.0 μm Lg = 0.1μm





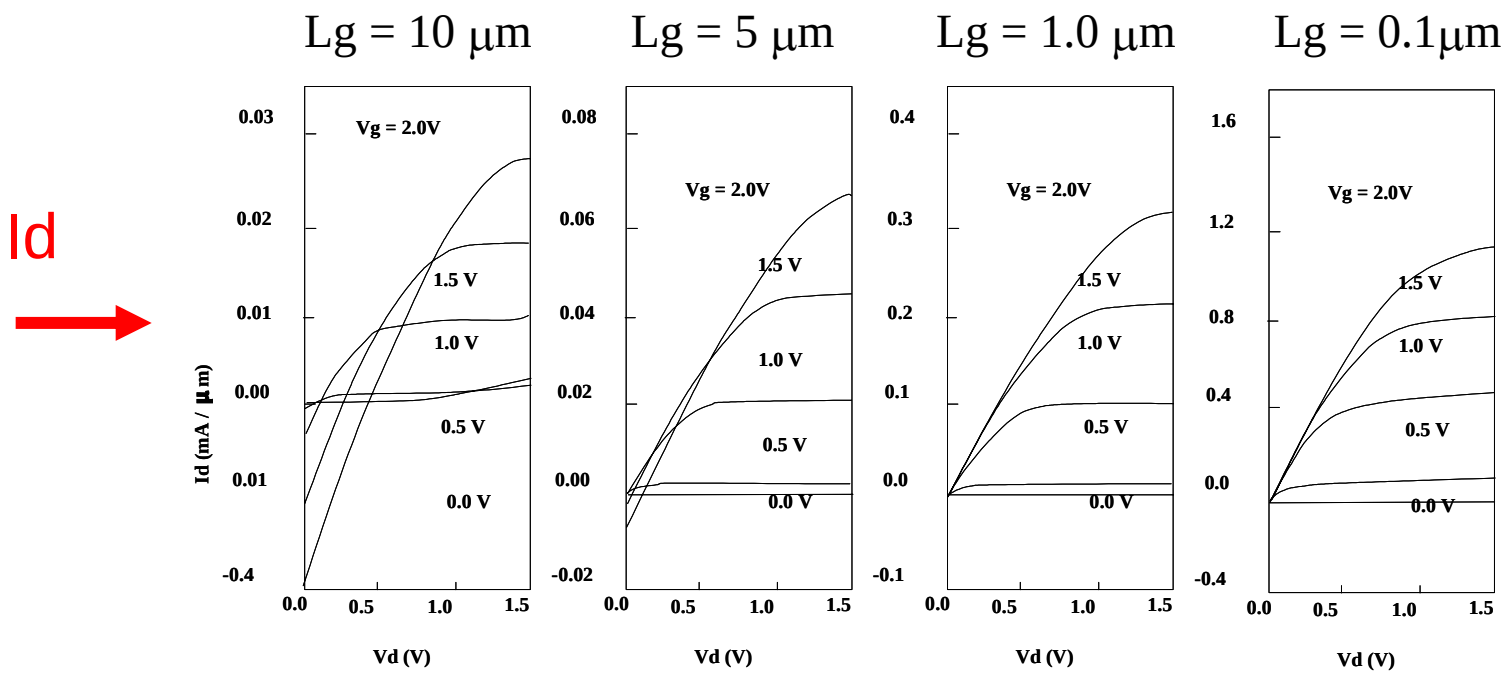
Direct tunneling leakage current start to flow when the thickness is 3 nm.

Gate leakage: Ig ∝ Gate Area ∝ Gate length (Lg)

Drain current: Id ∝ 1/Gate length (Lg)

Lg → small,

Then, Ig → smalll, Id → large, Thus, Ig/Id → small



Transistor Scaling Continues

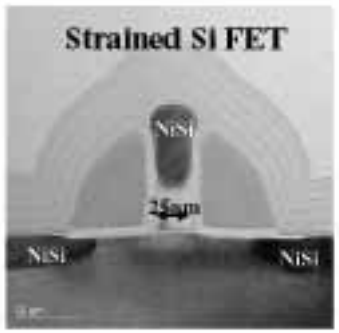
90nm node

Lg=50nm

65nm node

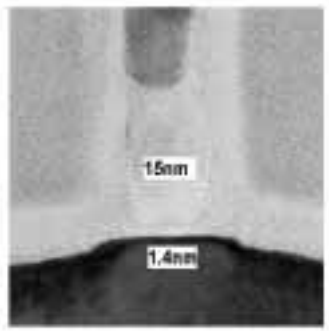
Lg=35nm

45nm node



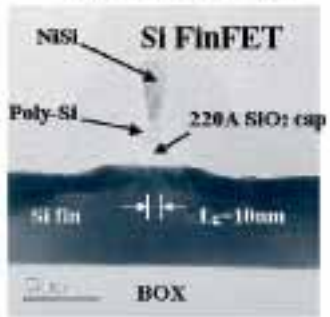
Lg=25nm

32nm node

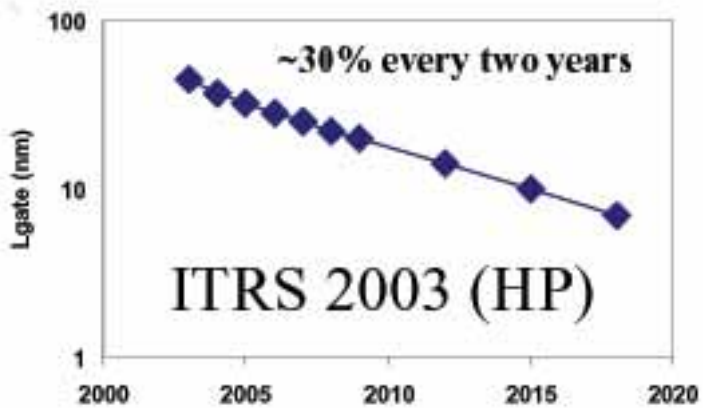


Lg=15nm

22nm node



Lg=10nm

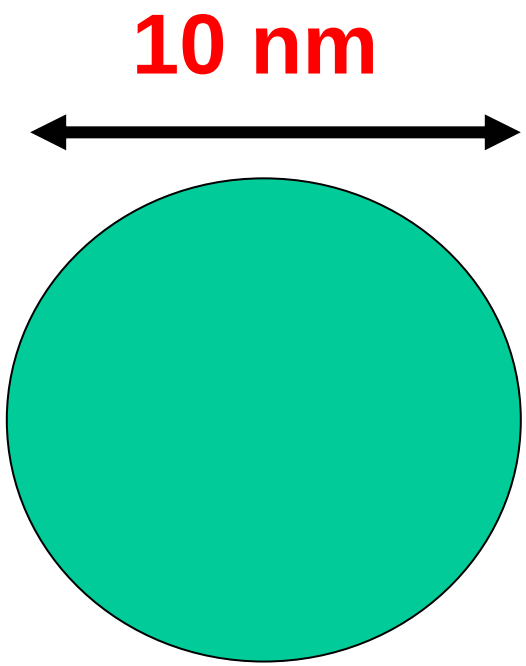


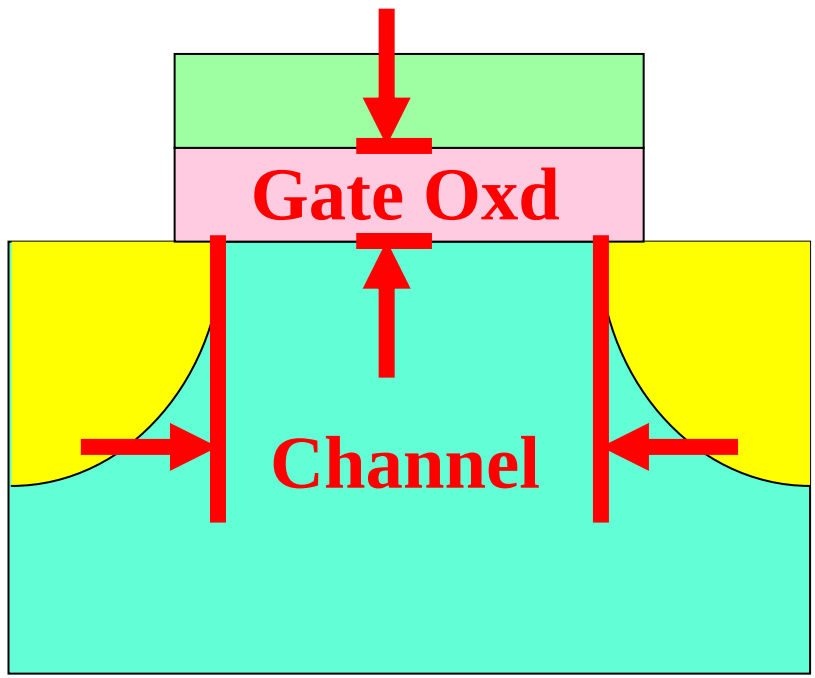
Qi Xinag, ECS 2004, AMI

Downsizing limit?

Channel length?

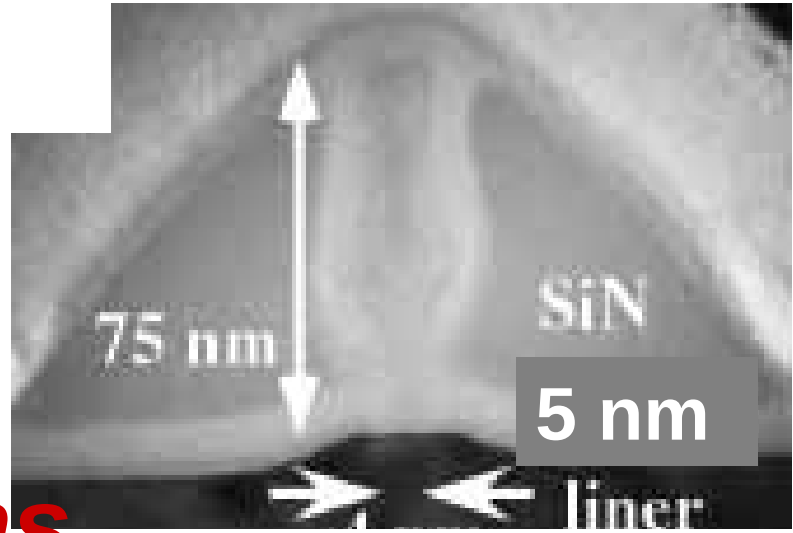
Electron wave length



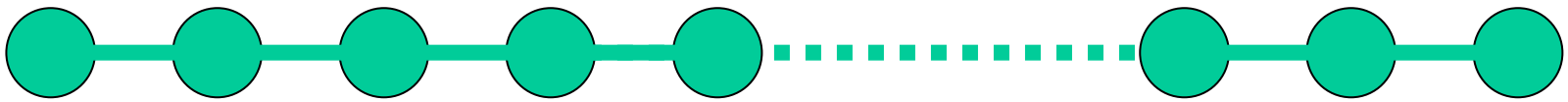


5 nm gate length CMOS

Is a Real Nano Device!!

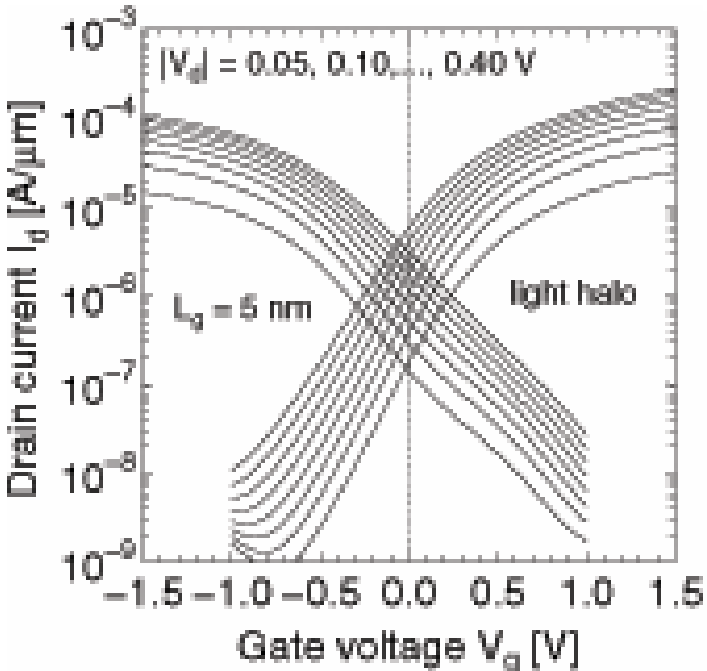


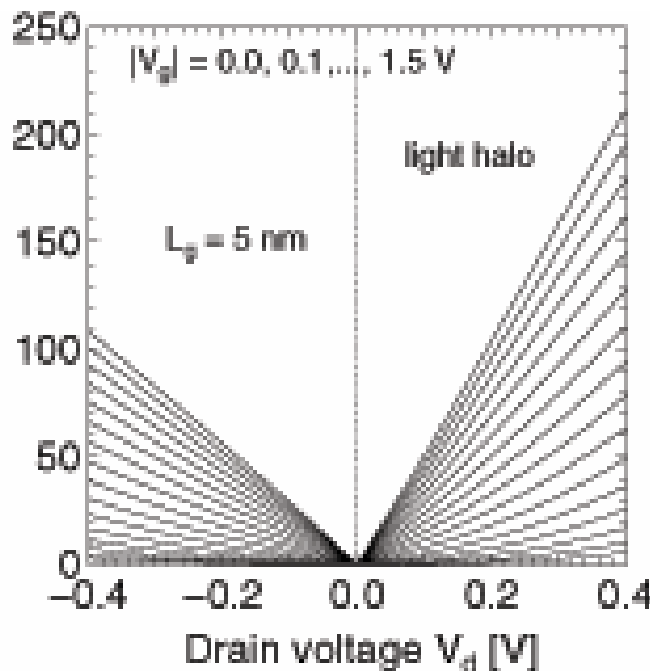
Length of 18 Si atoms



H. Wakabayashi et.al, NEC

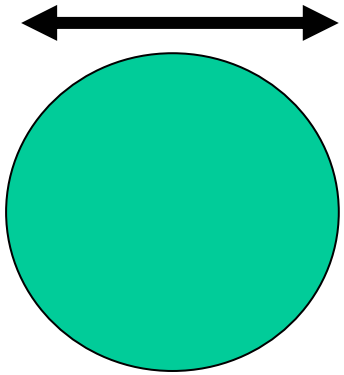
IEDM, 2003





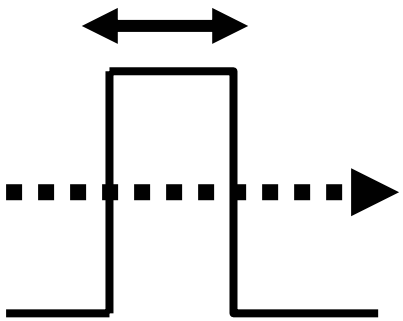
Electron wave length

10 nm



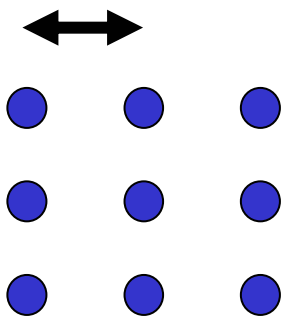
Tunneling distance

3 nm



Atom distance

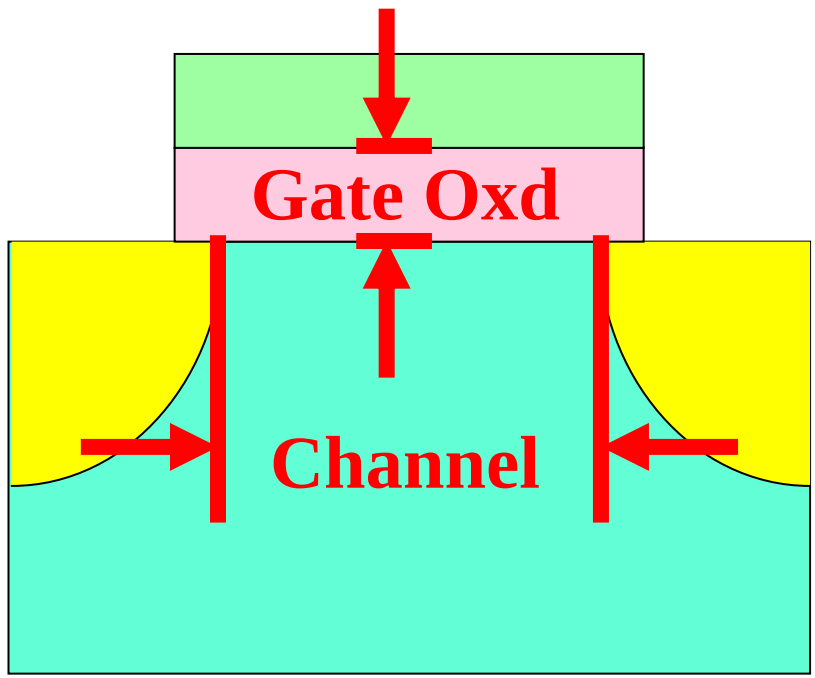
0.3 nm



Downsizing limit!

Channel length

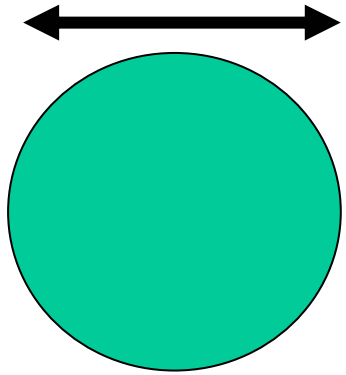
Gate oxide thickness



Prediction now!

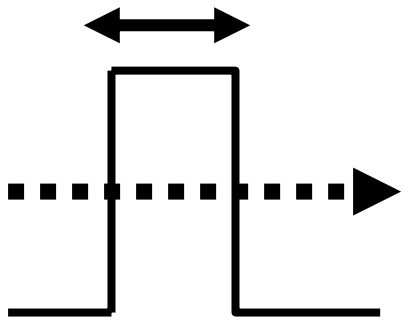
Electron wave length

10 nm



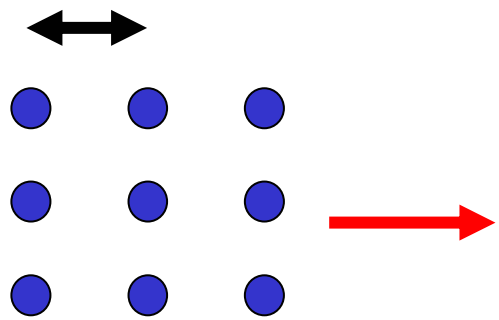
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

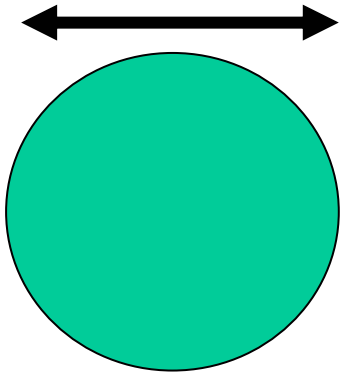
Lg = 2 ~ 1.5 nm?

Below this,
no one knows future!

Prediction now!

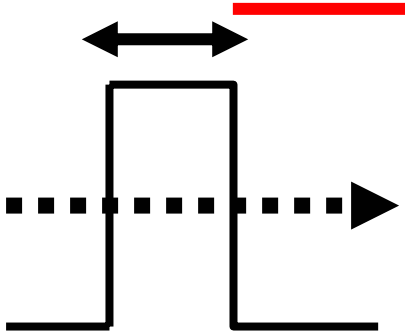
Electron wave length

10 nm



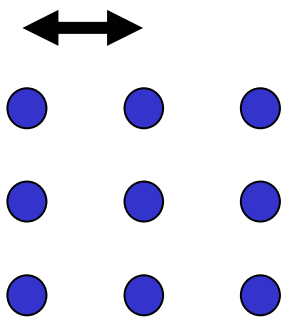
Tunneling distance

3 nm



Atom distance

0.3 nm



Gate length

Prediction at present

Practical limit because of off-leakage between S and D?

Lg = 5 nm?

MOSFET operation

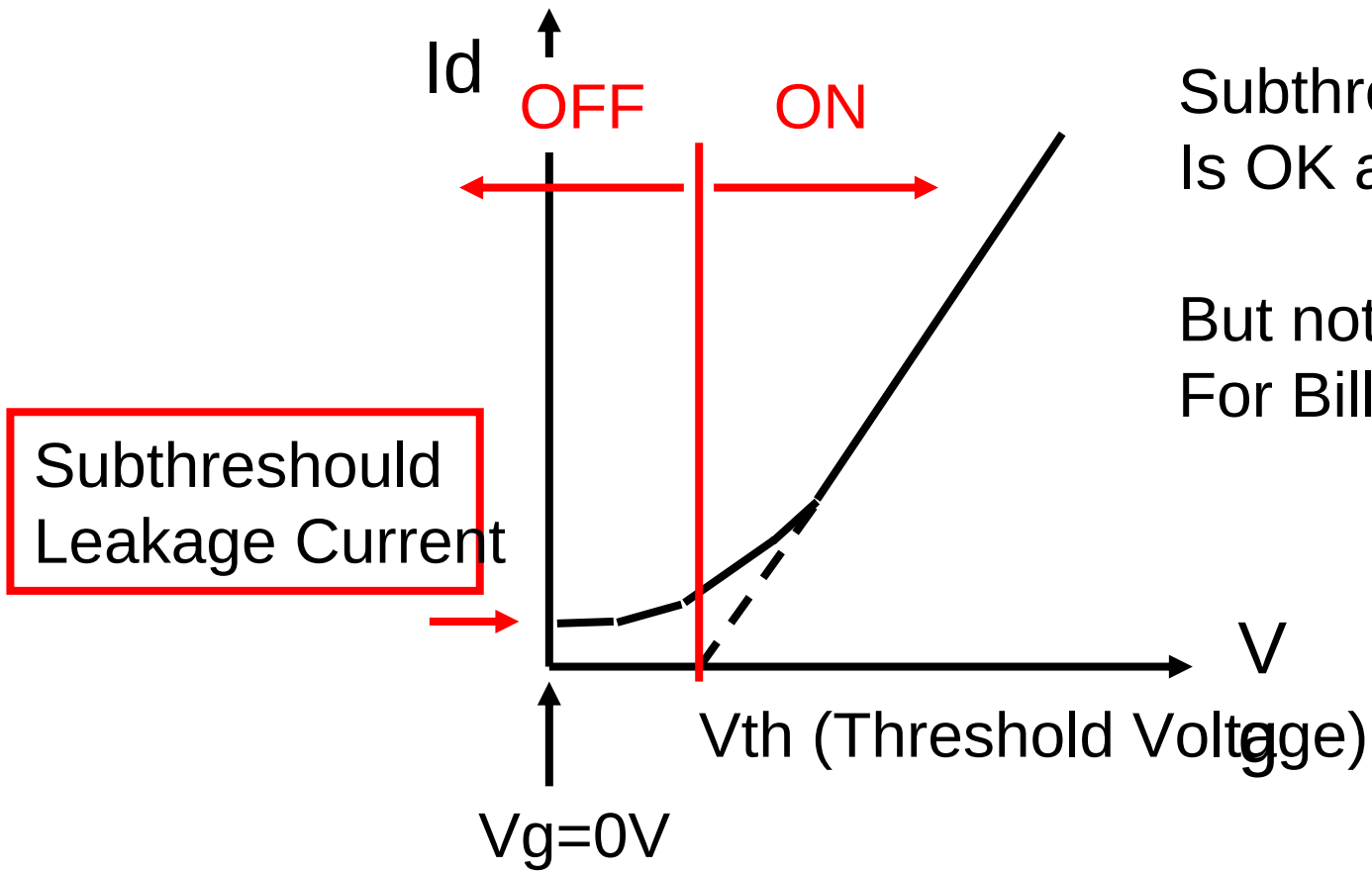
Lg = 2 ~ 1.5 nm?

But, no one knows future!

Maybe, practical limit around 5 nm.

When Gate length Smaller,

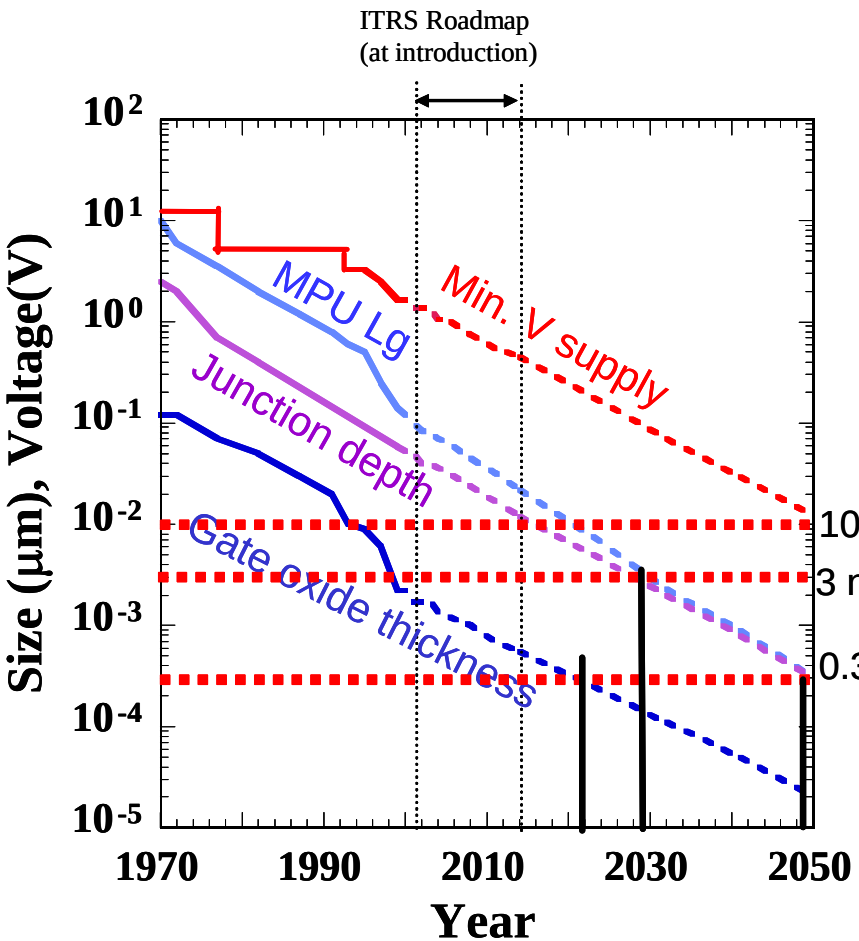
→ Subthrehold Leakage Current Larger

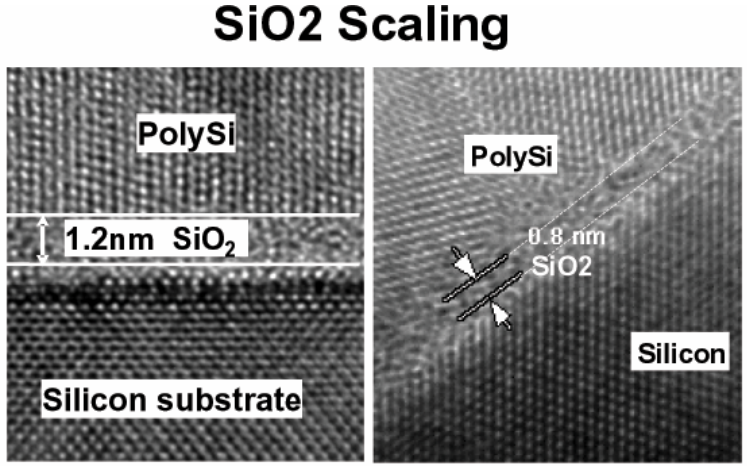


Subthreshold Current
Is OK at Single Tr.

But not OK
For Billions of Trs.

Scaling Limit in MOSFET





- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

10 nm Wave length of electron

3 nm Direct-tunneling limit in SiO_2

0.3 nm Distance between Si atoms

ULTIMATE LIMIT

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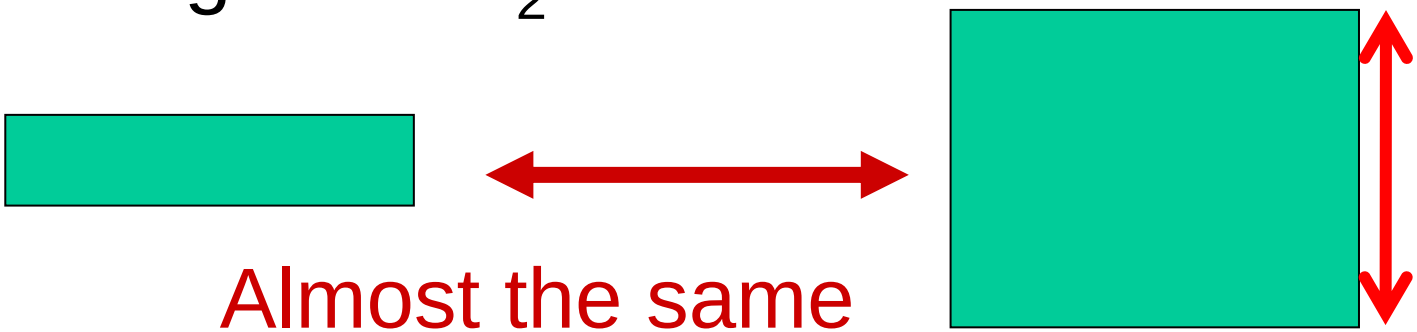
So, we are now in the limitation of downsizing?

Do you believe this or do not?

There is a solution! K: Dielectric Constan
To use high-k dielectrics

Thin gate SiO_2

Thick gate high-k dielectrics



Thick

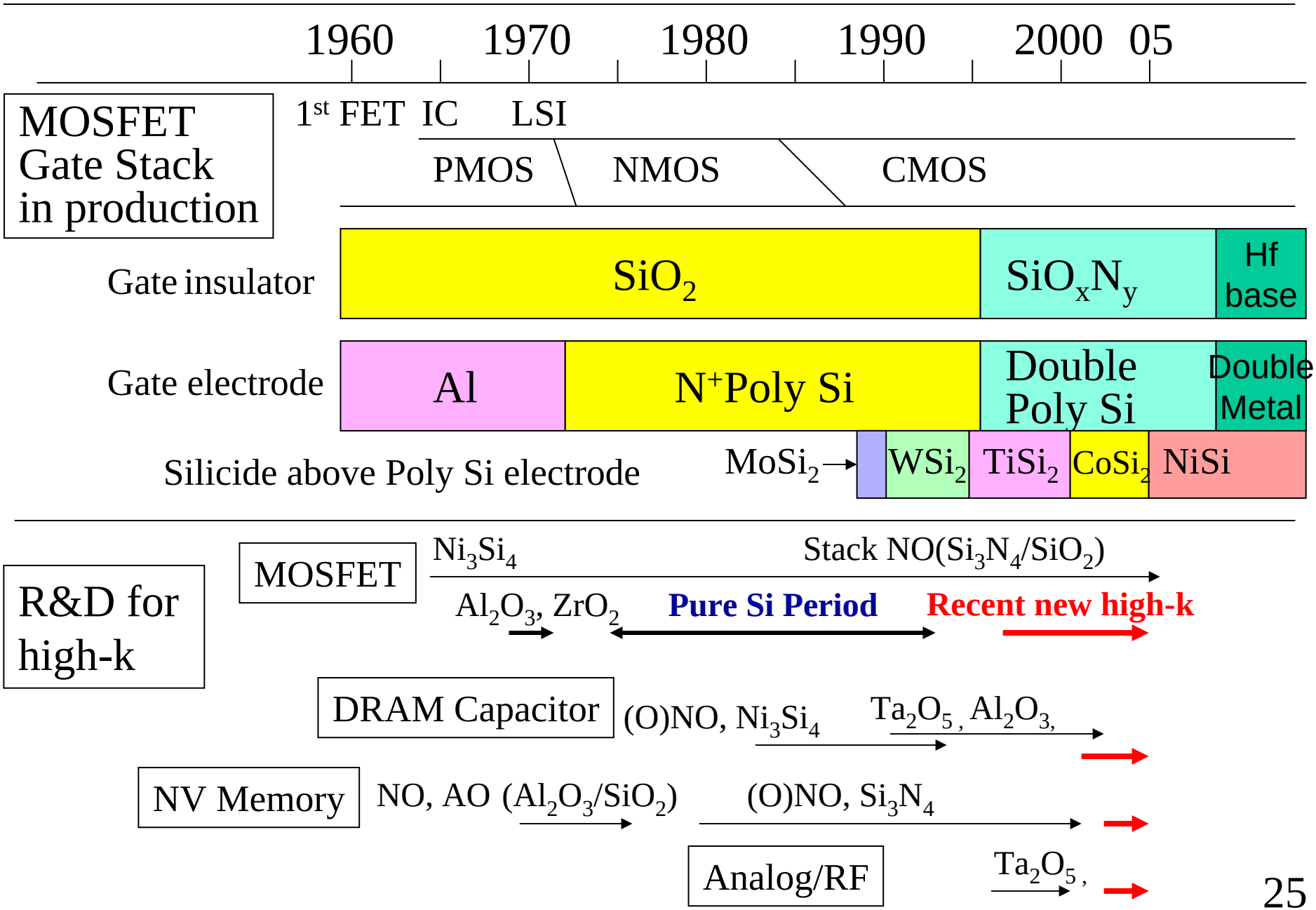
Small leakage Current

Almost the same electric characteristics

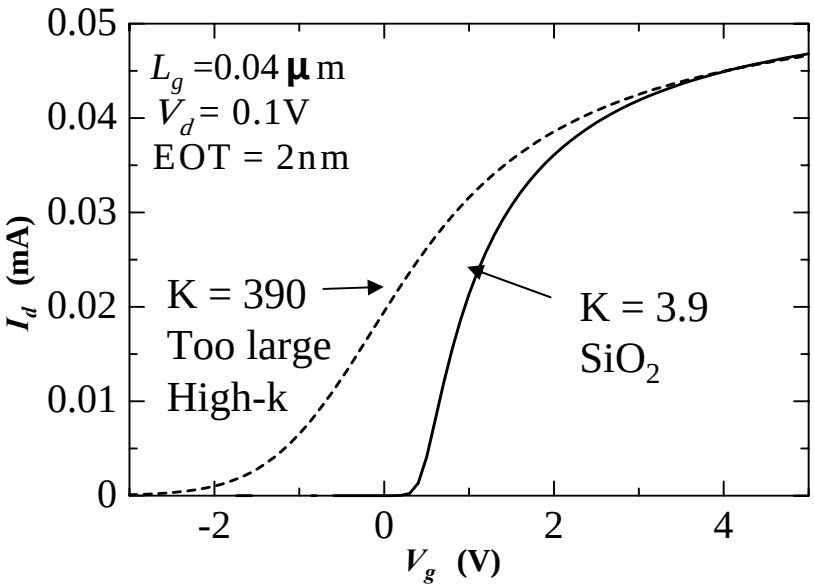
However, very difficult and big challenge!

Remember MOSFET had not been realize without Si/SiO_2!

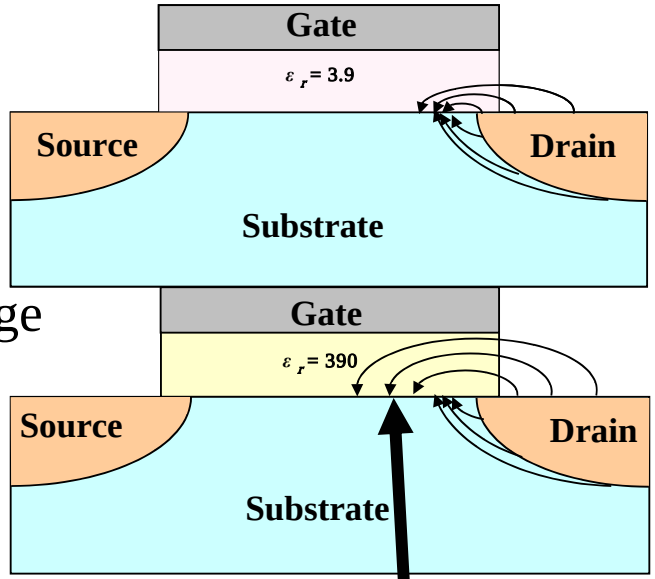
Historical Trend of New Material for Gate Stack



Too large high-k cause significant short channel effect

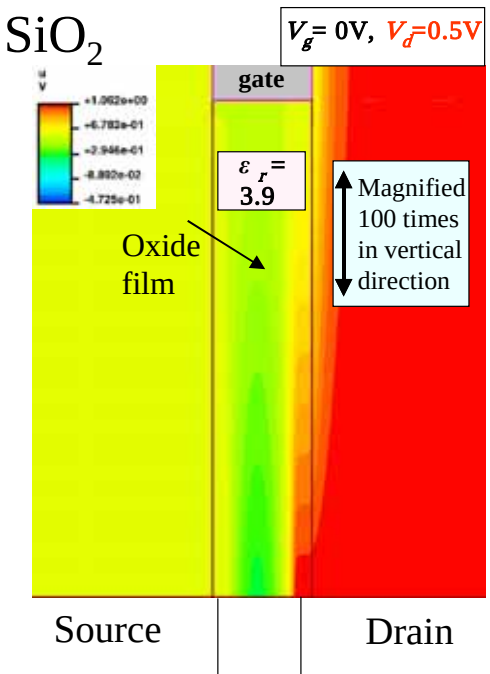


SiO_2

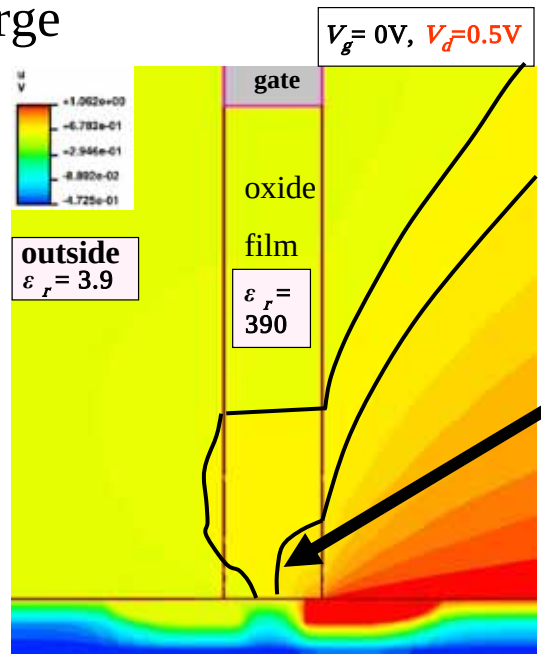


Too large high-k

SiO_2



Too large high-k



Penetration of lateral field from Drain through high-k causes significant short channel effects

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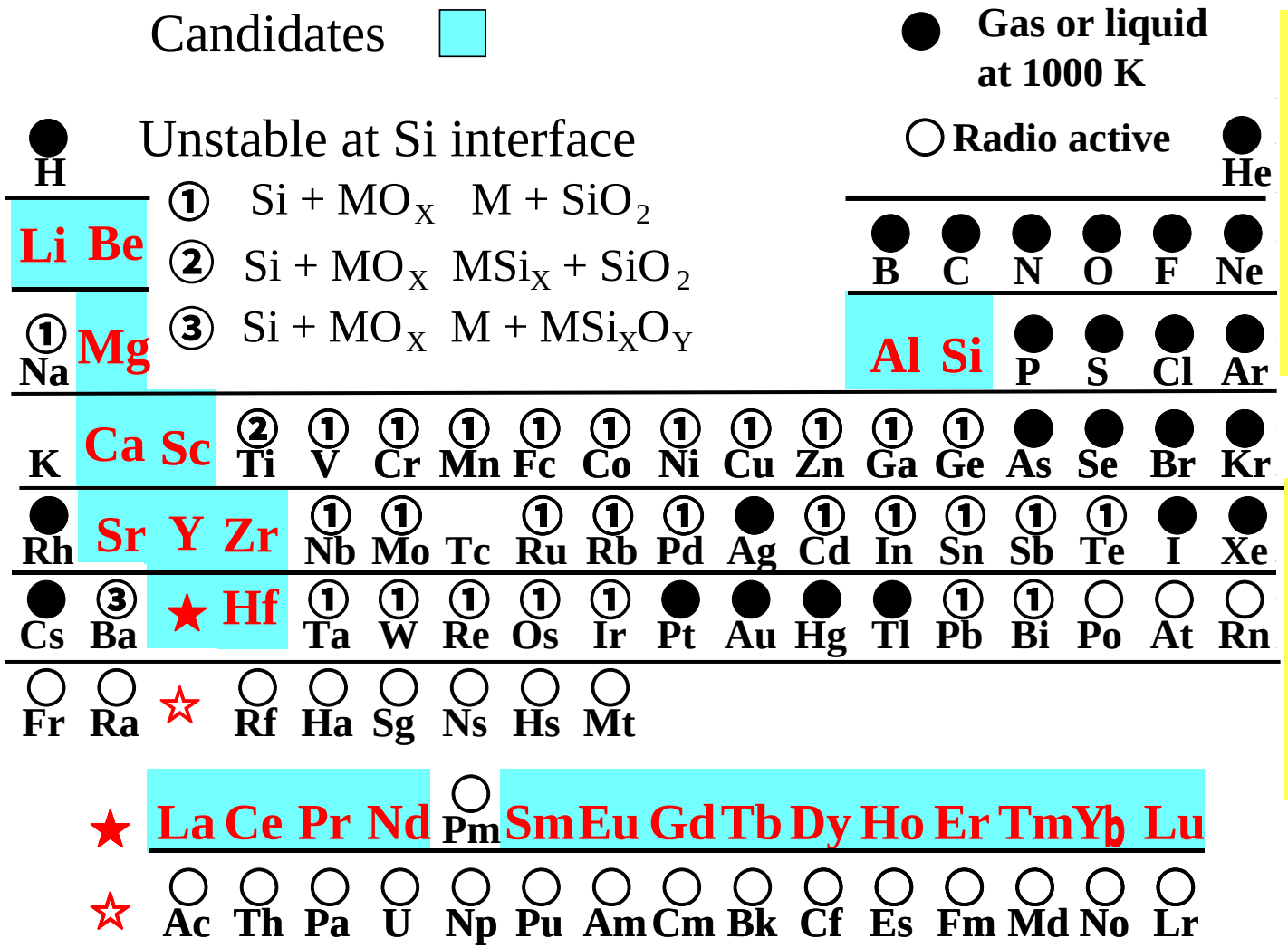
Choice of High-k



HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

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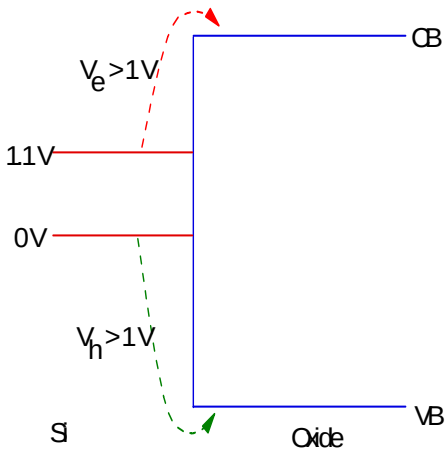
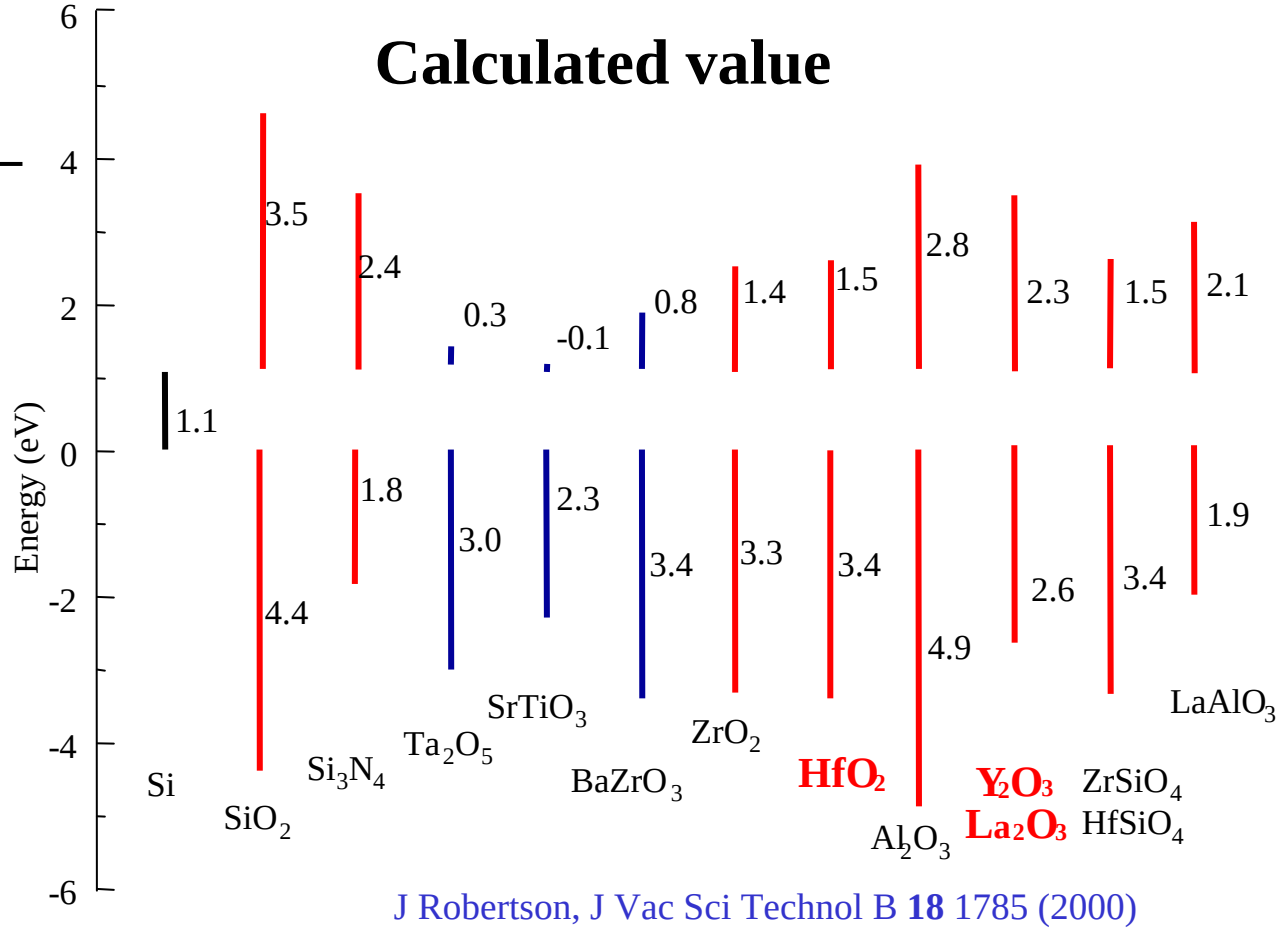
Band Offsets



Dielectric constant



J Robertson, J Vac Sci Technol B **18** 1785 (2000)

SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

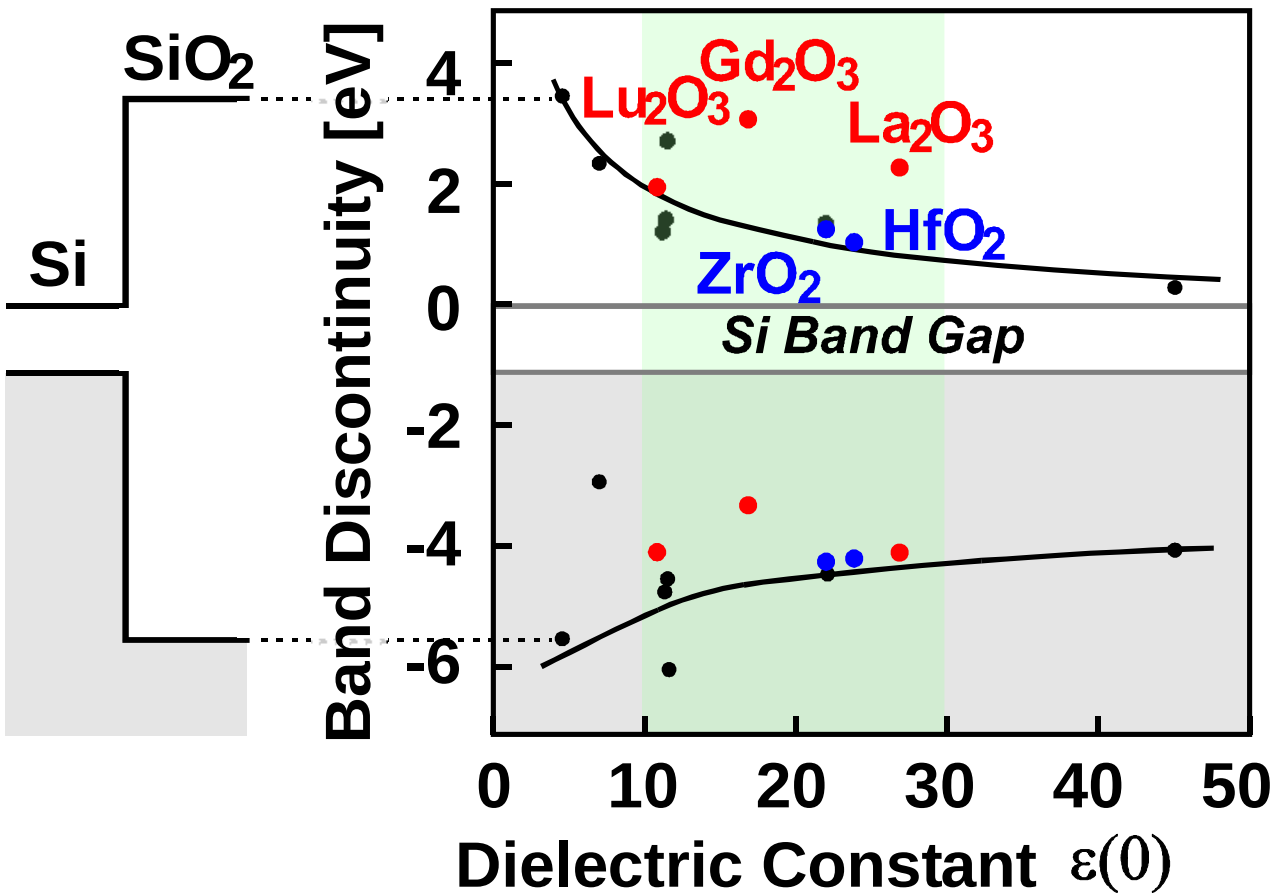
Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

28

Energy Barrier Offset of La2O3



XPS measurement by Prof. T. Hattori, INFOS 2003

29

Intel's announcement, January 26, 2007, and IEDM Dec 2007

Hafnium-based high-k material by ALD: EOT= 1nm
Specific gate metals (Intel's trade secret)
Different Metals for NMOS and PMOS
Use of 193nm dry lithography

From 65 nm to 45 nm Tech.

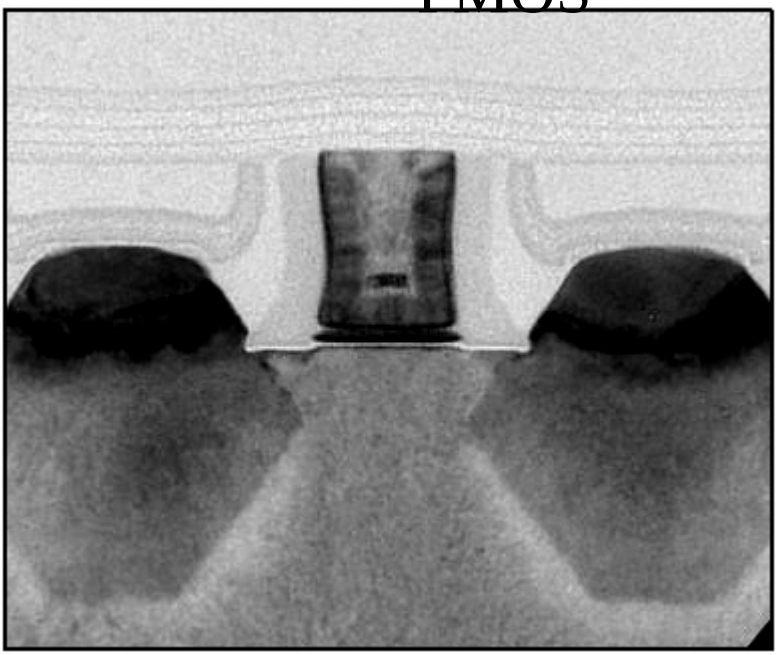
Tr density: 2 times increase
Tr switching power: 30% reduction
Tr switching speed: 20% improvement
S-D leakage power: 5 times reduction
Gate oxide leakage: 10 times reduction

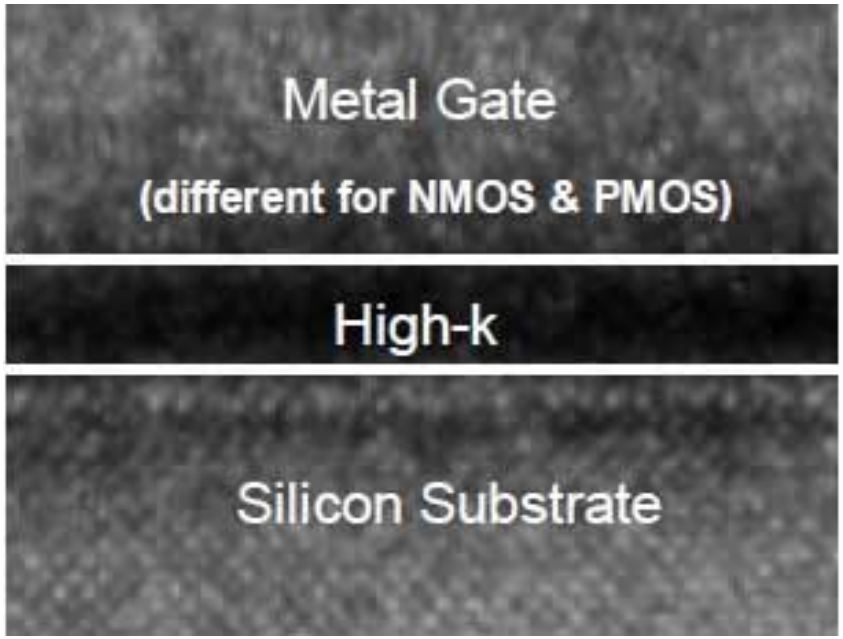
45nm processors (Core™2 family processors "Penryn") running Windows* Vista*, Linux* etc.

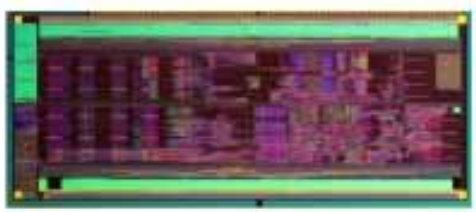
45nm production in the second half of 2007

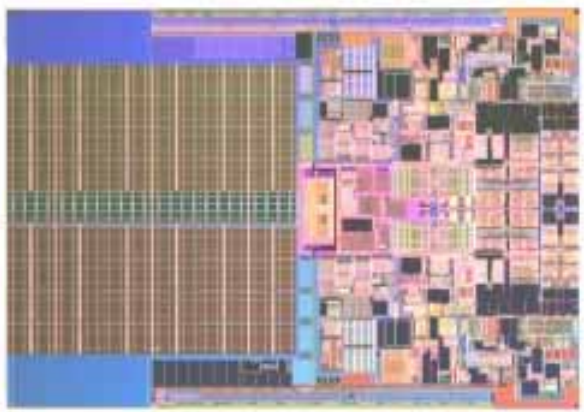
30

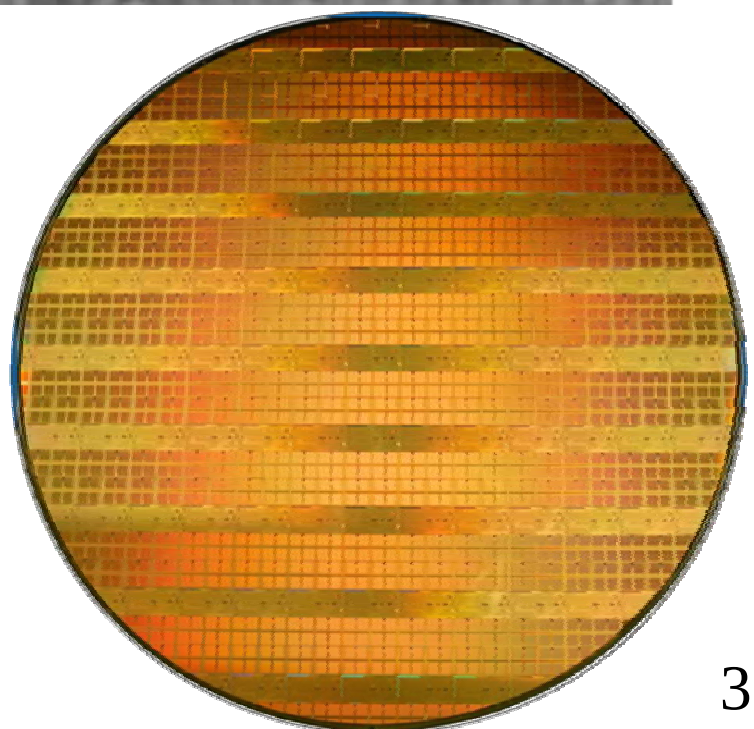
PMOS



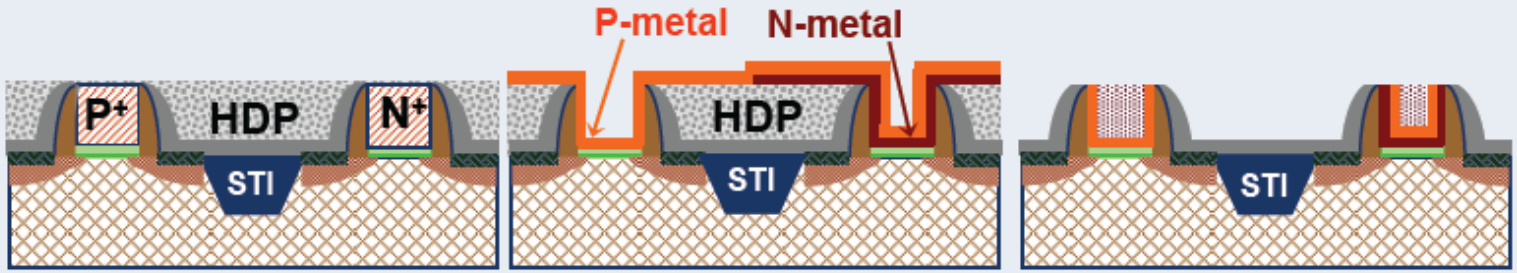

Metal Gate
(different for NMOS & PMOS)
High-k
Silicon Substrate







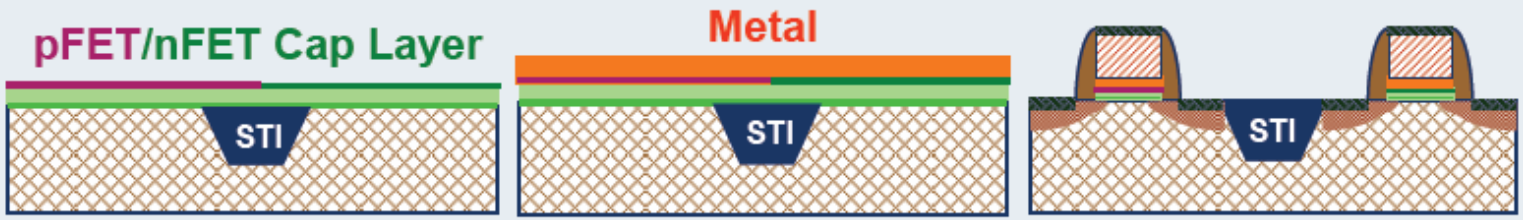
Replacement Metal Gate (Damascene)



Advantages
- Low thermal budget (metal gate deposition after S/D anneals)
- Known metal work function

Challenges
- Cost
- Extendibility to narrower CDs

Gate-First Process

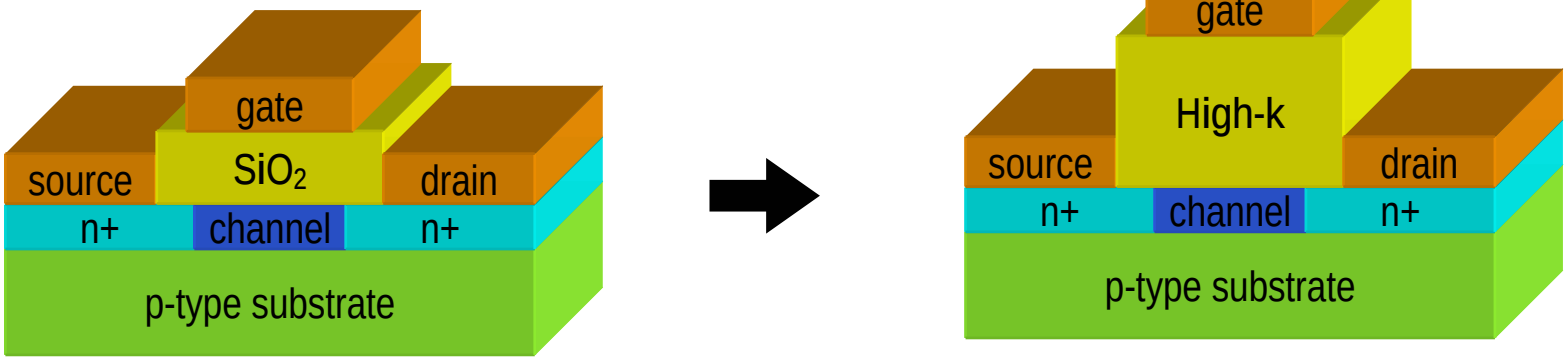


Advantages
- Compatible with high thermal budget process
- Follows standard CMOS flow

Challenges
- NMOS and PMOS cap layer integration is challenging

High-k with EOT = 0.5 nm

MOSFET



	2005	2007	2009	2011
Physical Gate Length (nm)	**32**	**25**	**20**	**16**
Equivalent Oxide Thickness (nm)	**1.2**	**1.1**	**0.9**	**0.5, 0.8(DG)**

ITRS 2006

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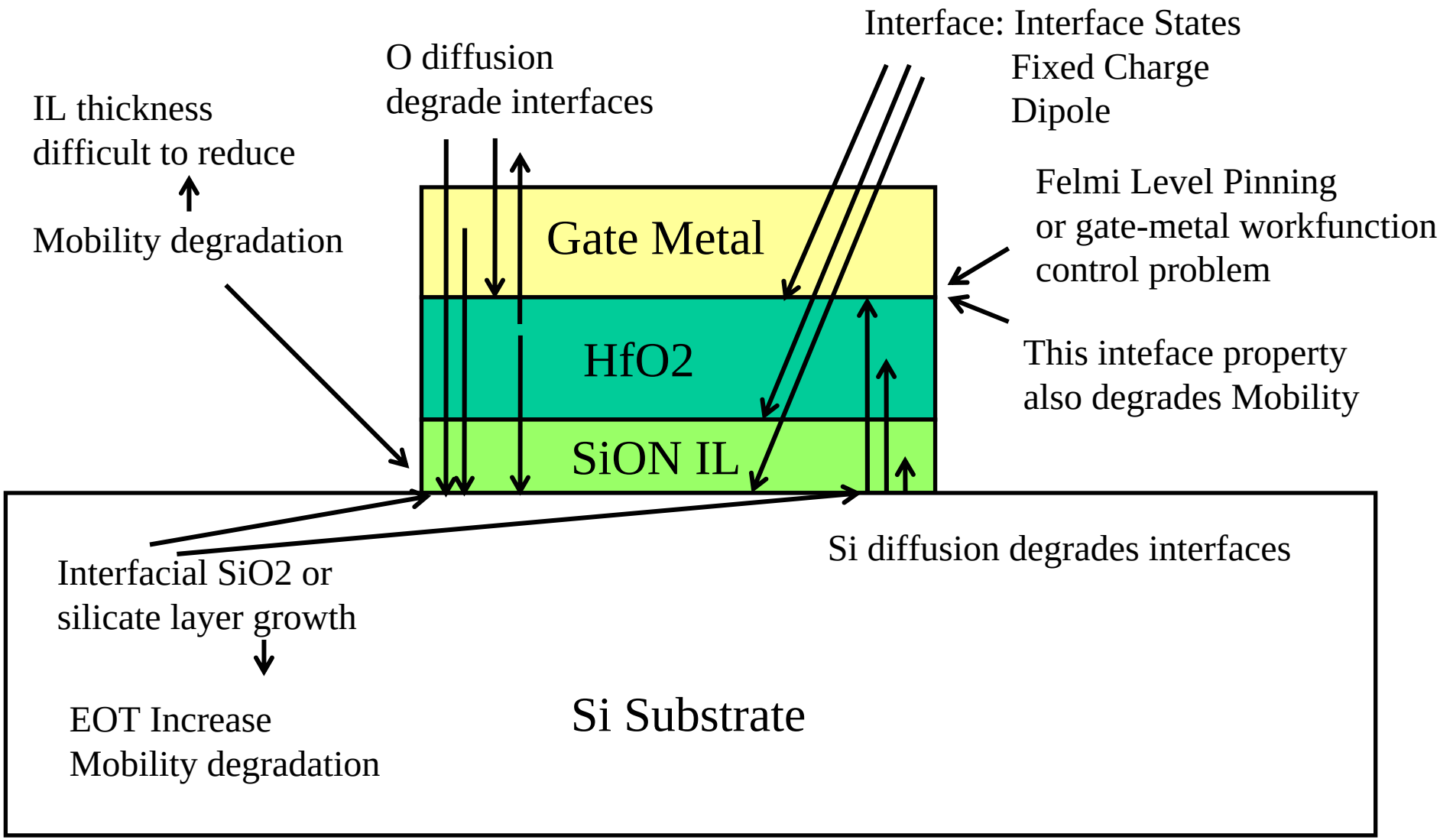
Now, interest is High-k for EOT < 1nm

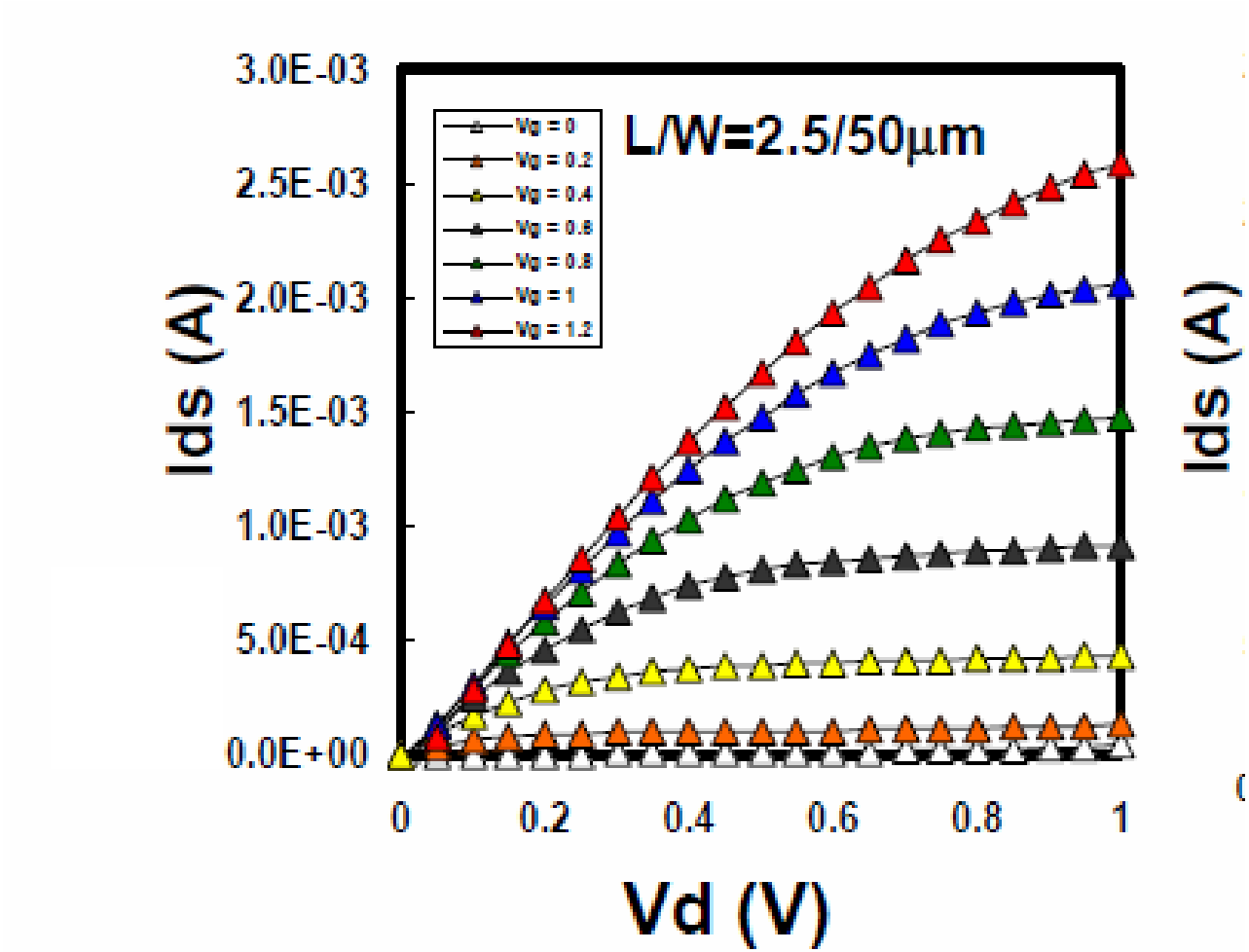
Many Problems for thinning EOT



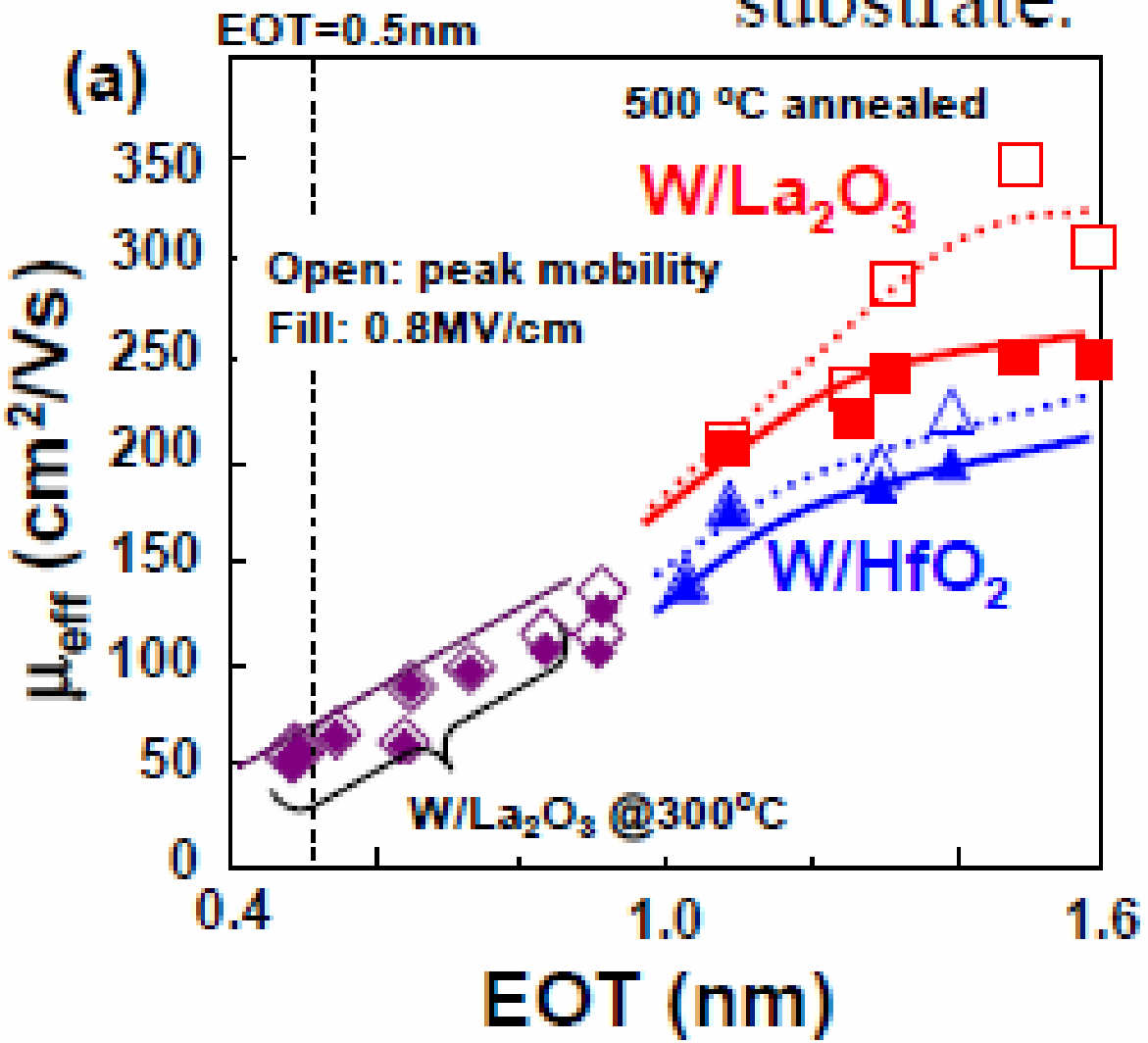
34

EOT = 0.48 nm Our results

Transistor with La2O3 gate insulator



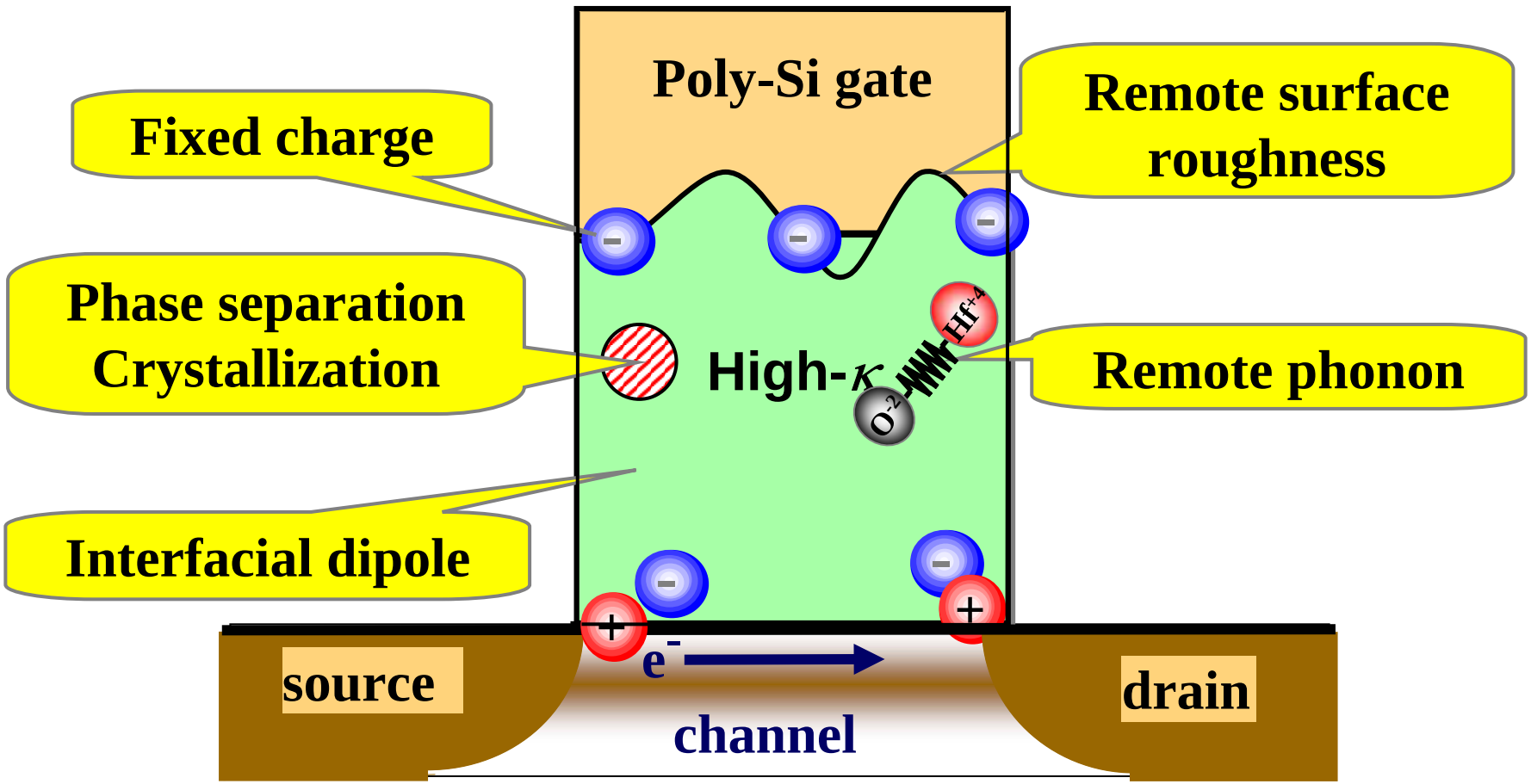
substrate.



36

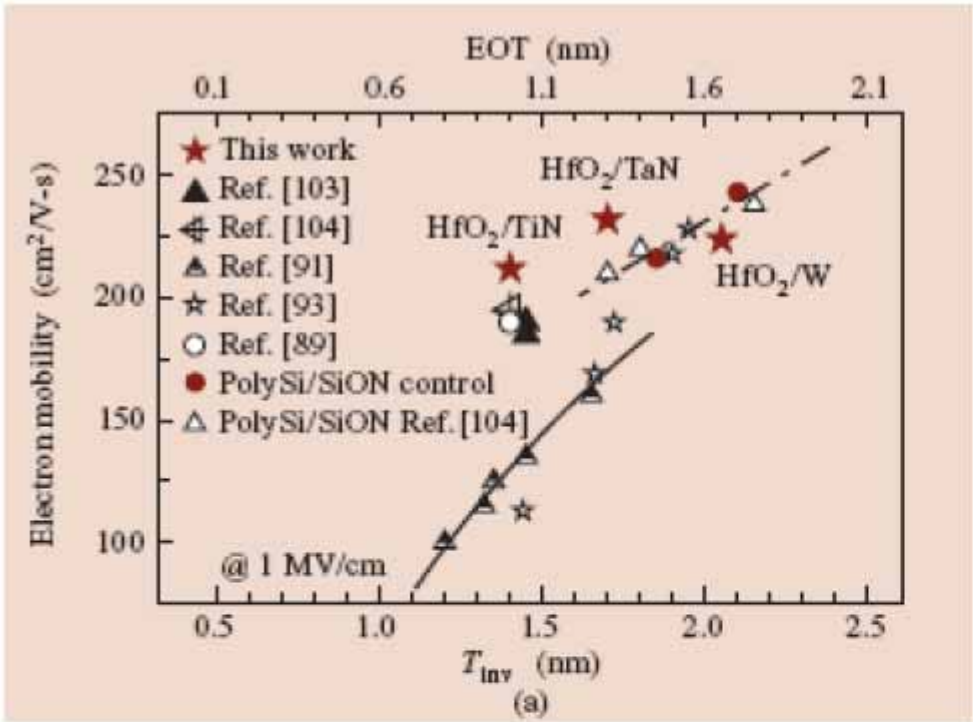
Mobility degradation causes for High-k MOSFETs (HfO_2, Al_2O_3 based oxide)

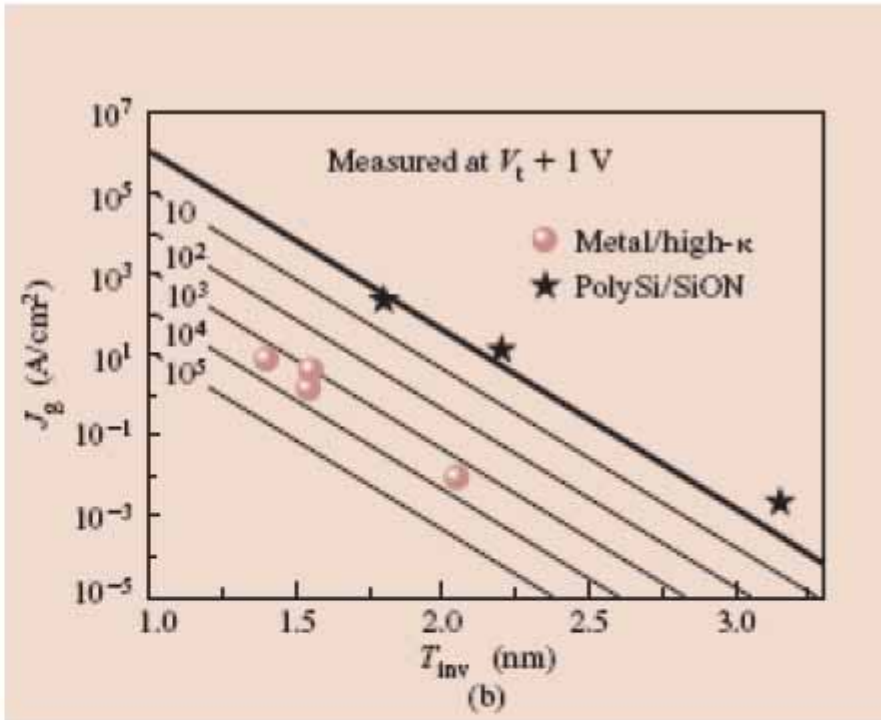
Remote scattering is dominant



S. Saito et al., IEDM 2003,
S. Saito et al., ECS Symp. on ULSI Process Integration

37





PVD TiN, ALD TaN, CVD W on High-k:

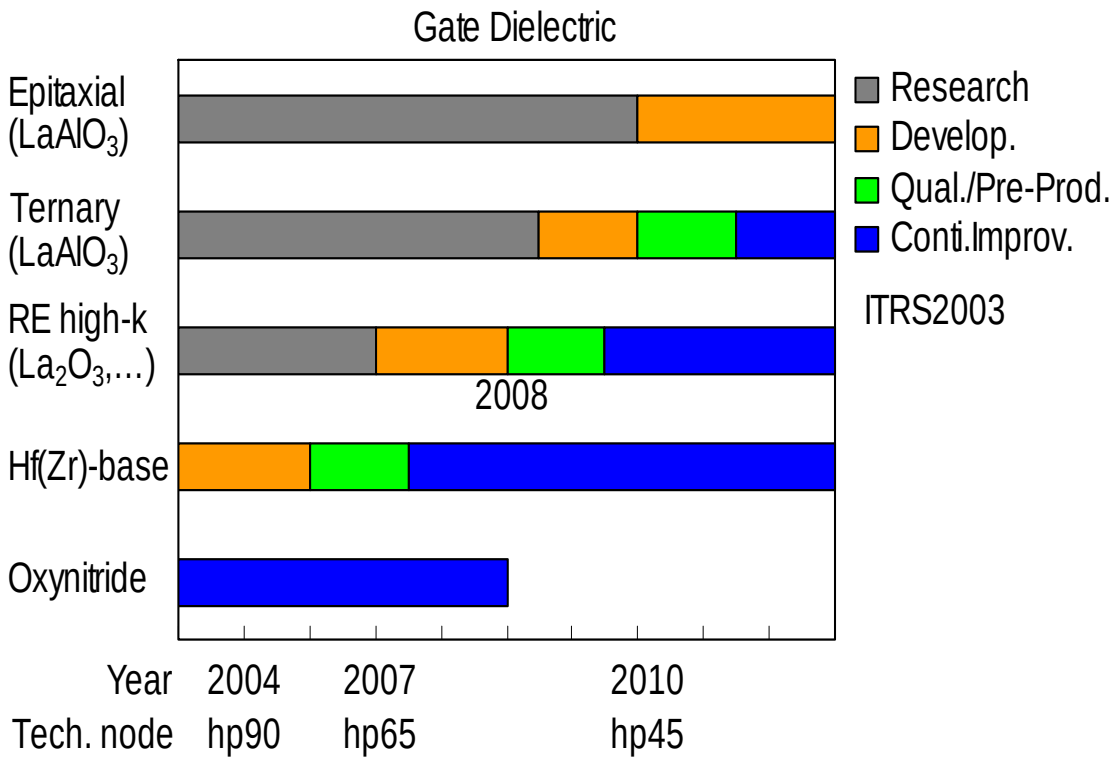
- 4-5 Orders Magnitude Improvement in Gate Leakage
- Equivalent Electron Mobility as that of Oxynitride

Source: E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006

Reza Arghavani, Ph.D.,Applied Materials ,IEDM 2007 Short Course

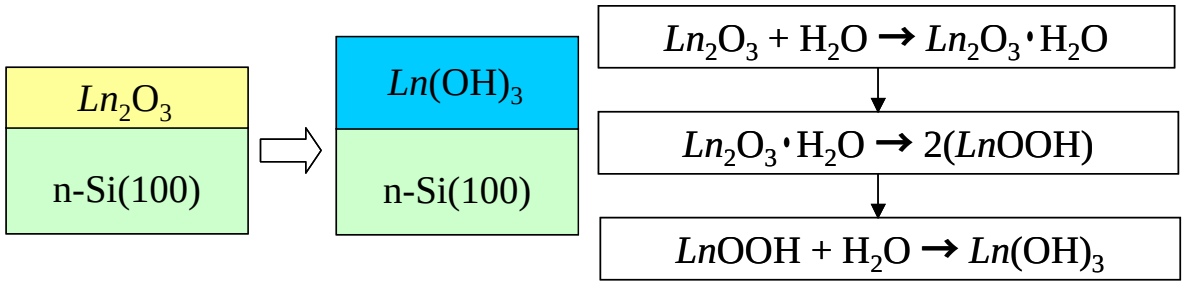
Thinning EOT toward 0.5-0.7 nm
Keeping good mobility with thinning IL

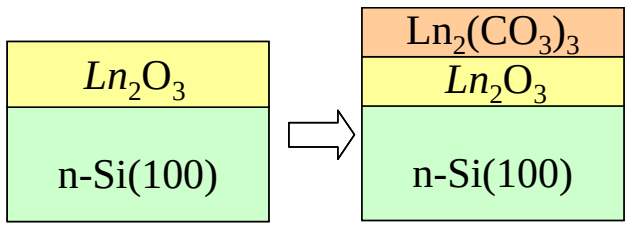
Searching new materials:
→ La2O3 based / Rare earth oxides

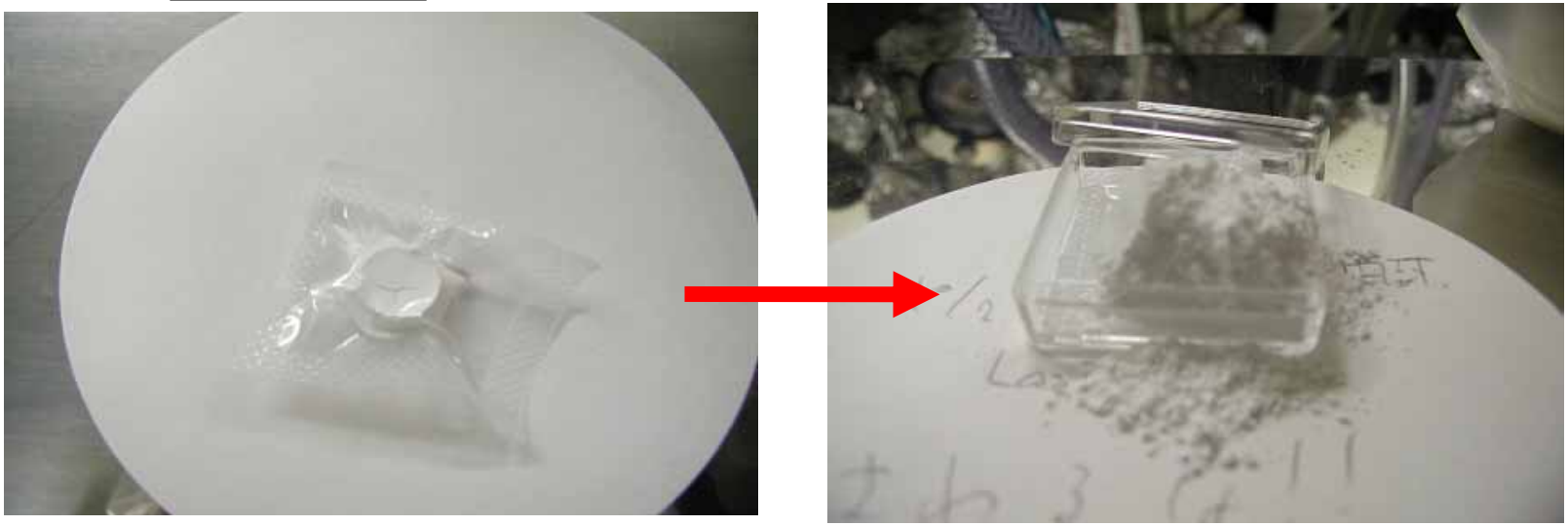


ITRS 2003

Hygroscopic Properties of La2O3

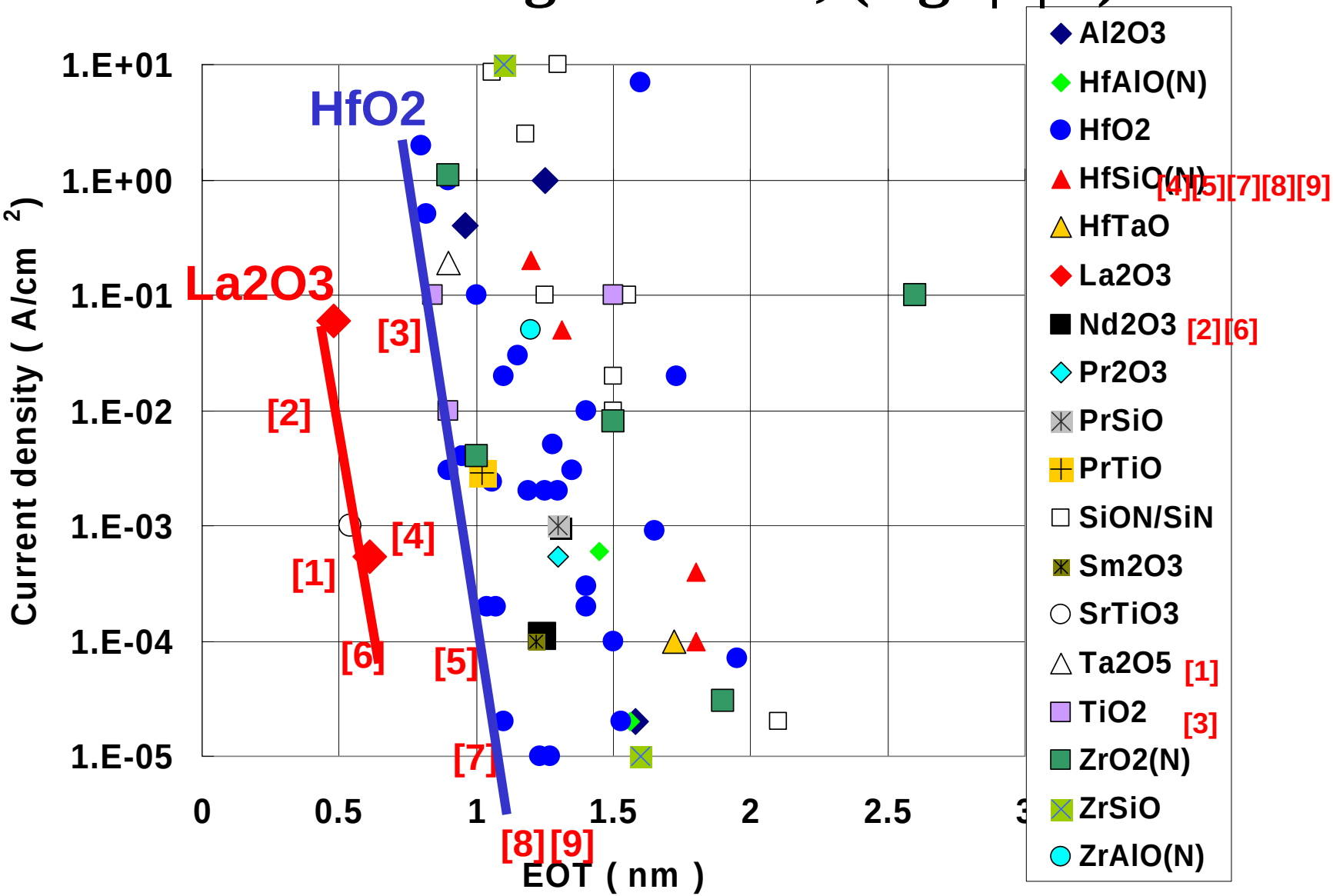






After 30 hours in clean room (temperature & humidity controlled)

Gate Leakage vs EOT, (Vg=|1|V)



Effect of gate workfunction

N-MOSFET: N-Poly Si gate electrode

Typical Vth = 0.25 ~ 0.6 V

P-MOS FET: P-Poly Si gate electrode

Typical Vth = -0.25 ~ -0.6 V

Vfb difference between N-Poly and P-Poly is 1.15 eV (Ideally)

P-MOSFET with N-Poly gate electrode

Vth → -1.4 ~ -1.75 too big

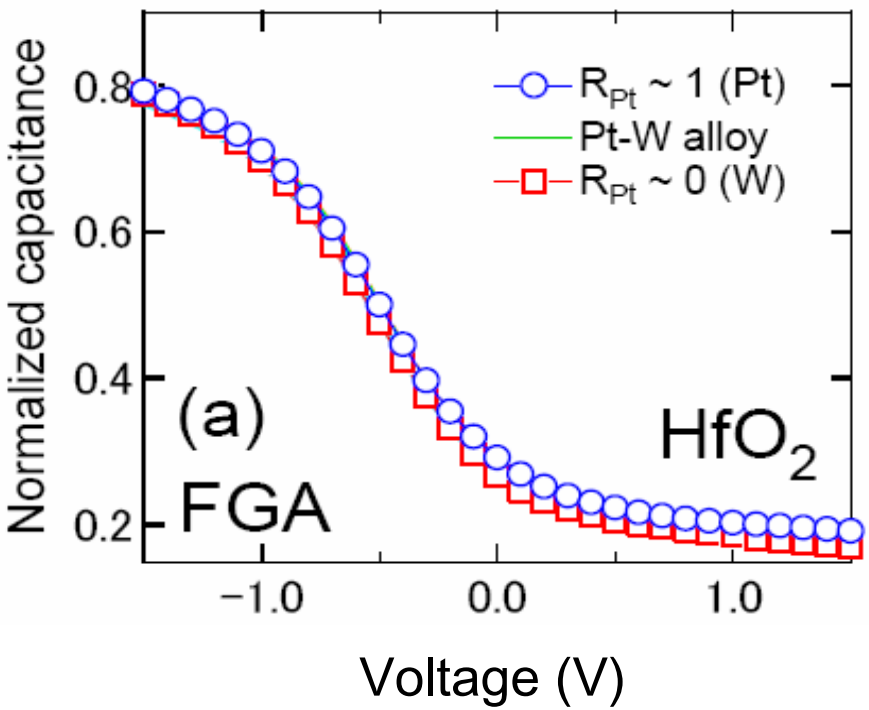
difficult to be adjusted by channel implantation

42

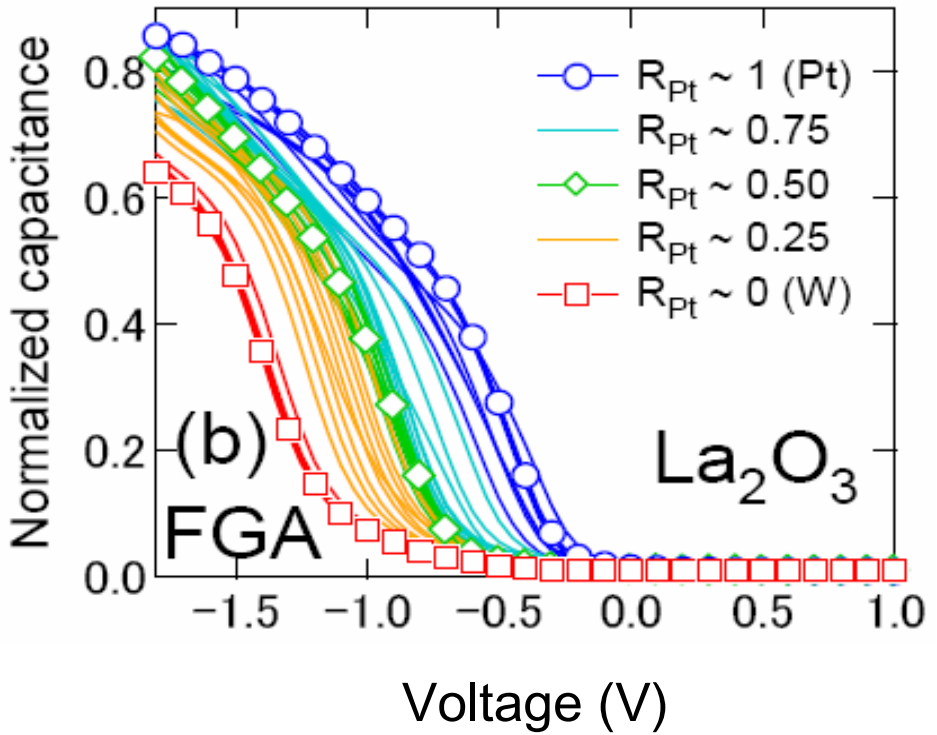
No FLP for La_2O_3

Changing Pt/W ratio of gate electrode

HfO_2

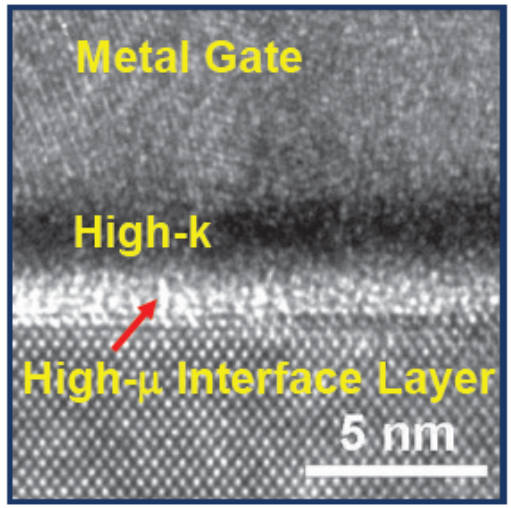


La_2O_3



K.Ohmori, SSDM2006

One Dielectric, Two Φ_m Metals vs. Two Dielectric Stacks, One Φ_m Metal



Using the Same Initial Gate Dielectric Stack

Gate Pre-Clean

RTO/DPN/PNA

ALD HfO_2

Integration Approach A

Two Distinct Metals Required

nFET	pFET
TaN[1]	WN[3]
TaC[2]	

[1] E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006
[2] W.J. Taylor, etal (Freescale), IEDM p. 625, 2006
[3] P-C. Jiang, etal, APL 89, 2006, H. Matsuhashi and S. Nishikawa, JJAP v33, 1994

Integration Approach B

One Metal Only With Nanoscale Cap Layers (Dipole Approach)

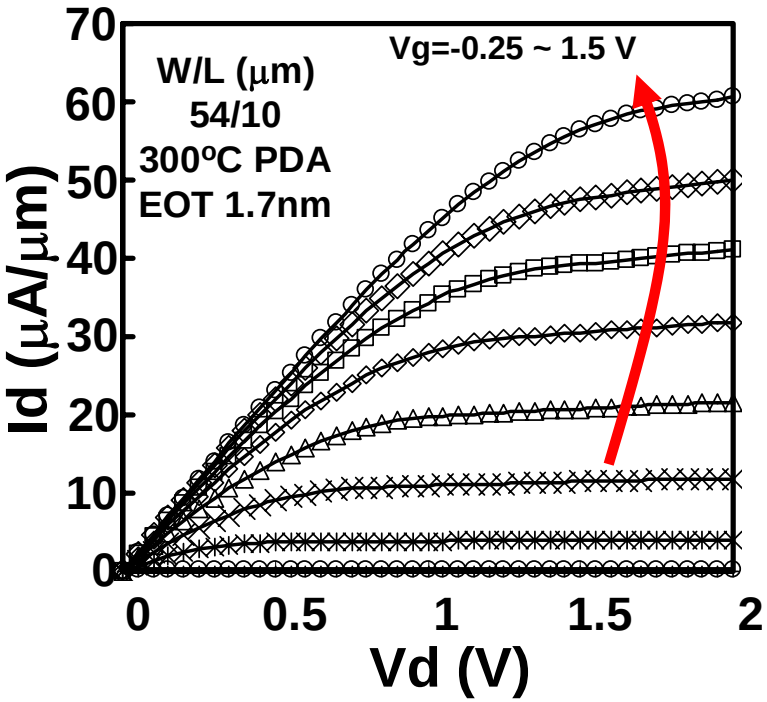
nFET	LaO_x[1]
pFET	Al-based[2]

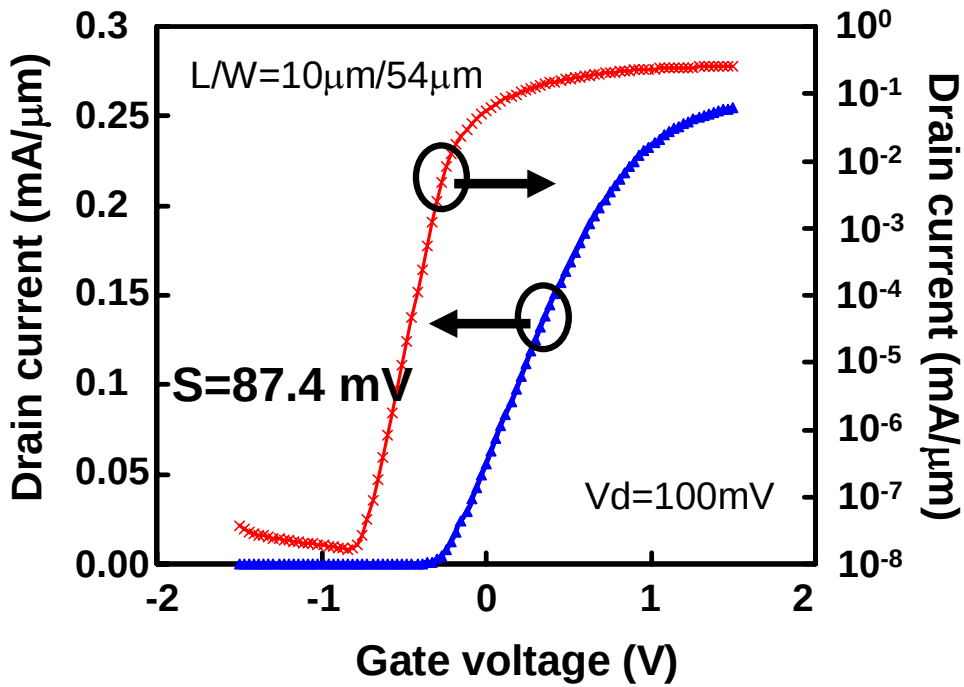
[1] V. Narayanan, et. al. (IBM), 2006 Symp. on VLSI Tech. Dig
[2] H.N. Alshareef, et. al. (SEMATECH), Appl. Phys. Lett. **88**, 112114 (2006)

Electrical Characteristics of La2O3 n-MOSFET

$Al/La_2O_3/p\text{-}Si/Al$

Process
- La_2O_3 300 °C deposition
- PDA N_2 300 °C 10 min

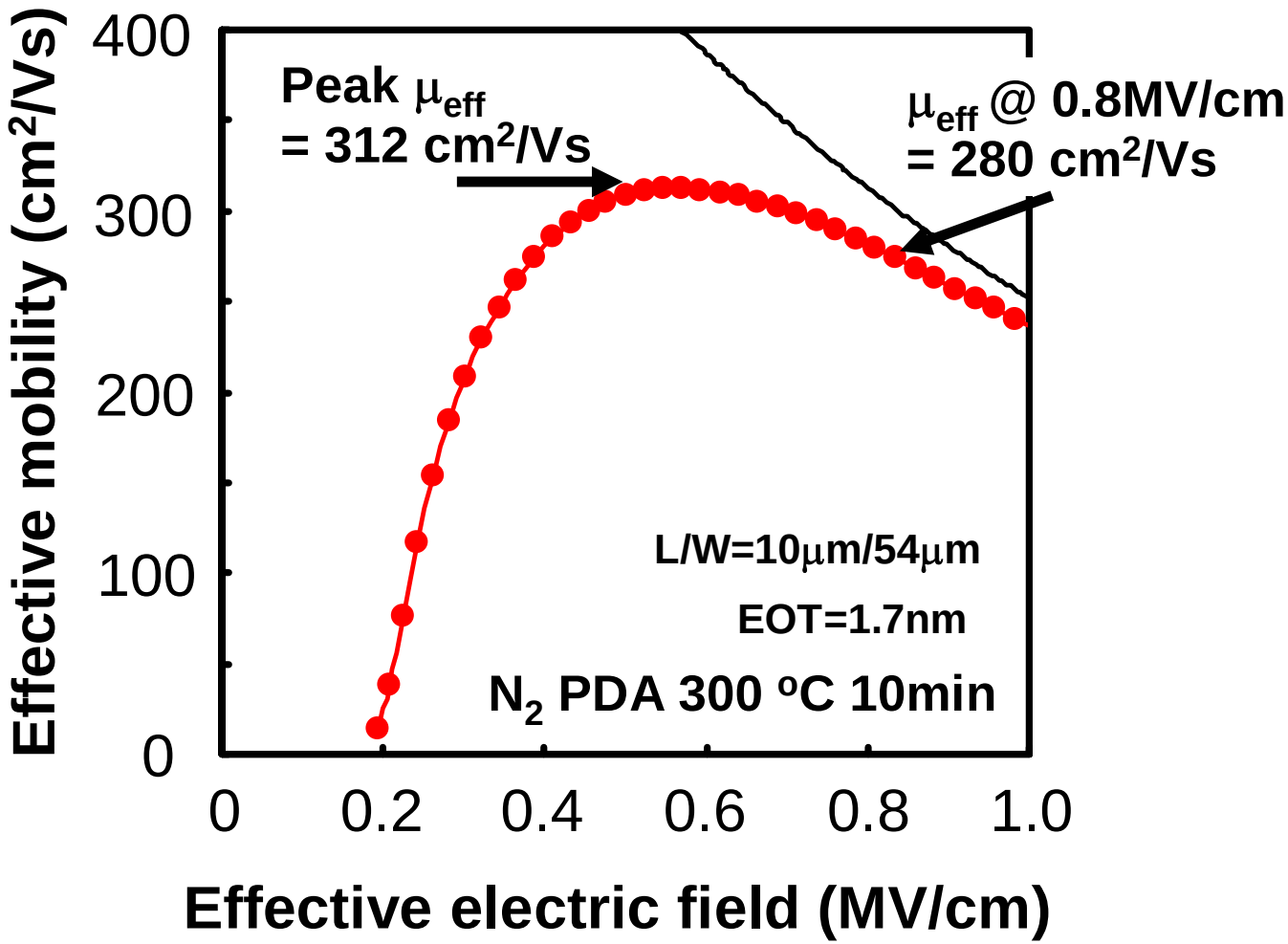




Good electrical characteristics can be obtained.

K. Kakushima et al. Si Nanoelec. Workshop 2006

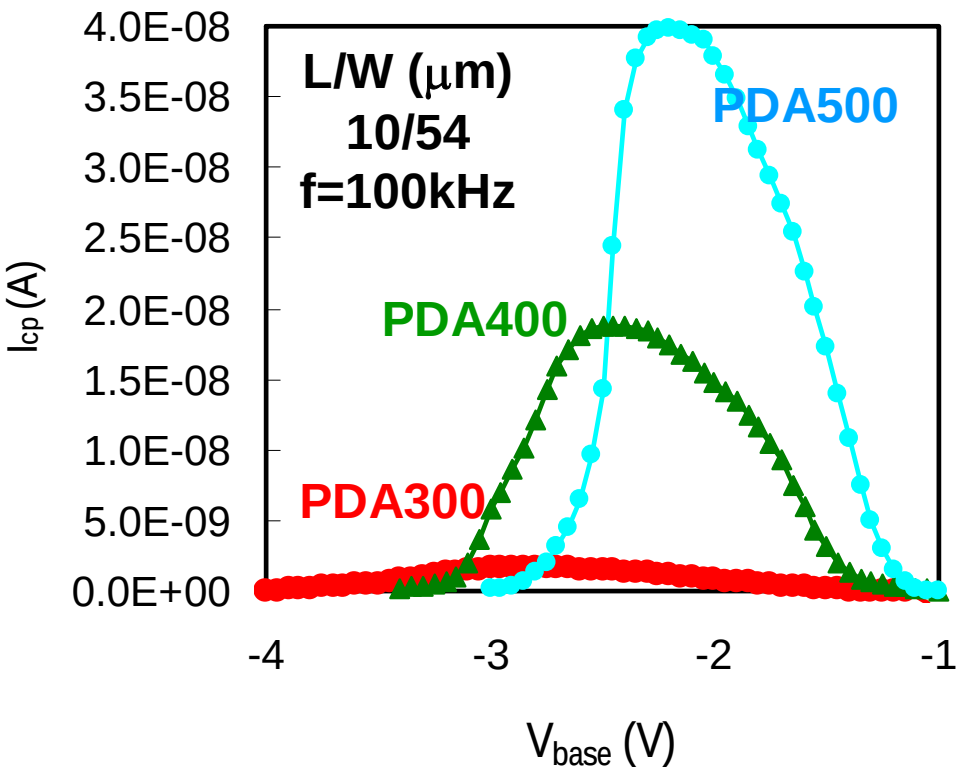
Effective Mobility of La_2O_3 MOSFET

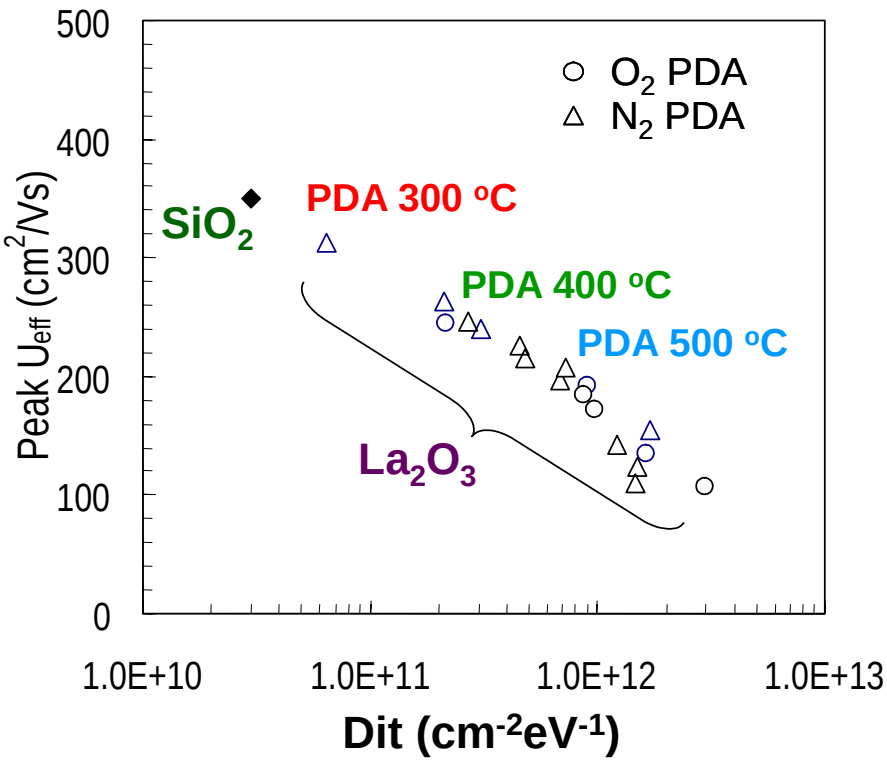


High effective mobility of 312 cm²/Vs can be obtained with La_2O_3

K. Kakushima et al. Si Nanoelec. Workshop 2006

Interfacial State Density

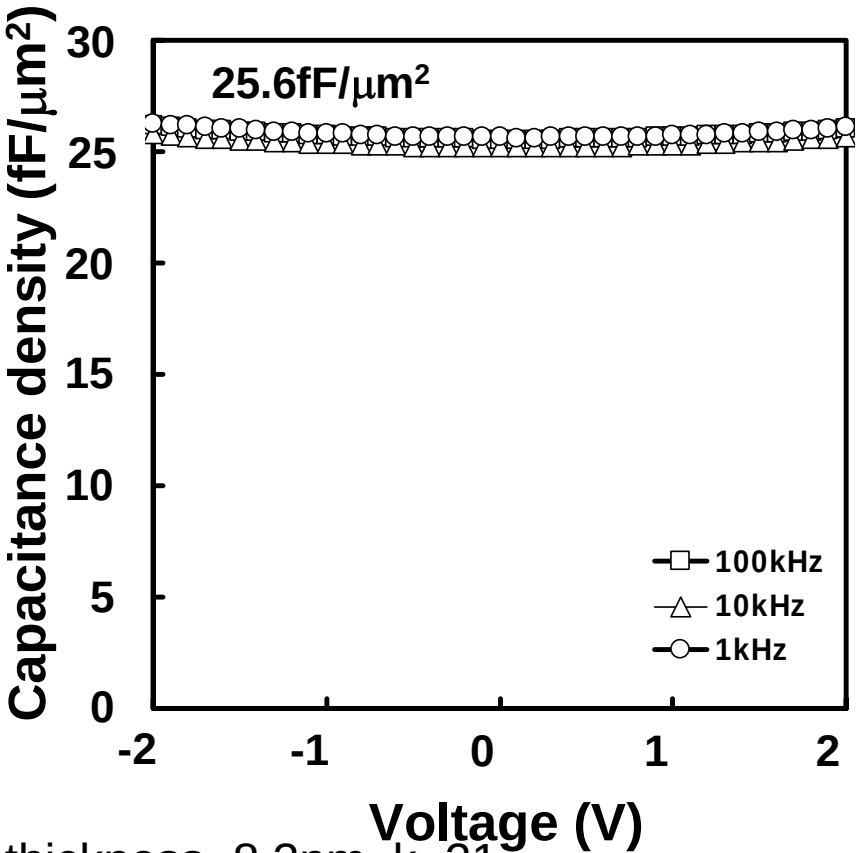




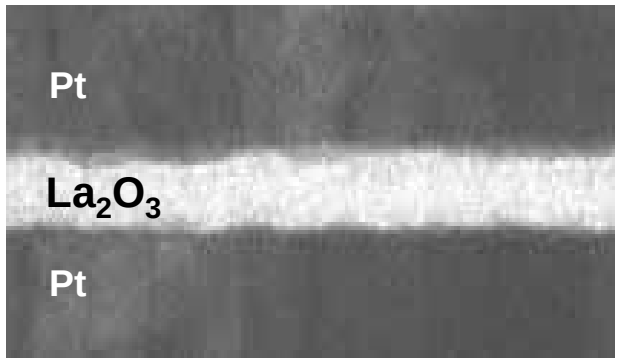
Interface state density increases at higher temperature annealing

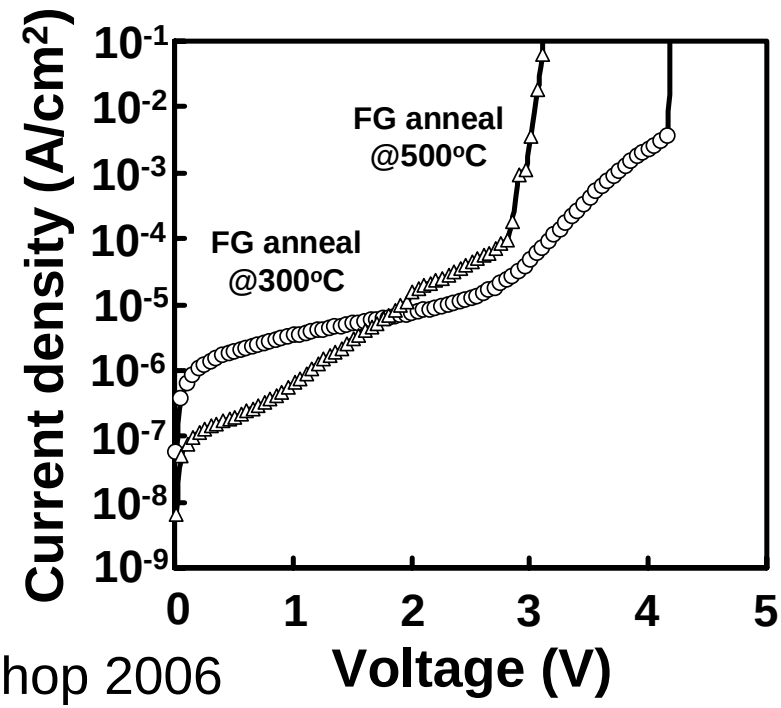
K. Kakushima et al. Si Nanoelec. Workshop 2006

$Pt/La_2O_3/Pt$ MIM Capacitor



thickness=8.3nm, k=21





La_2O_3 : Heat endurance is good

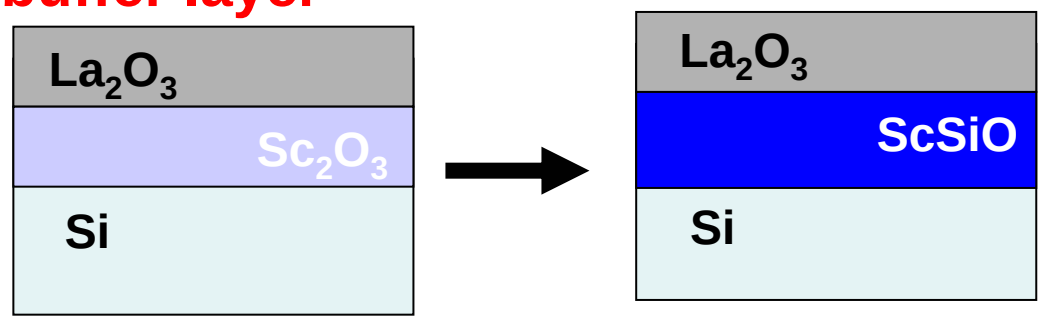
K. Kakushima et al. Si Nanoelec. Workshop 2006

La2O3 Gate Insulator for High Temperature Process

High temperature annealing above 500°C

SiOx based interfacial layer formation
- **Increase in EOT**
- **Higher Dit**

Interfacial Layer Suppression using buffer layer

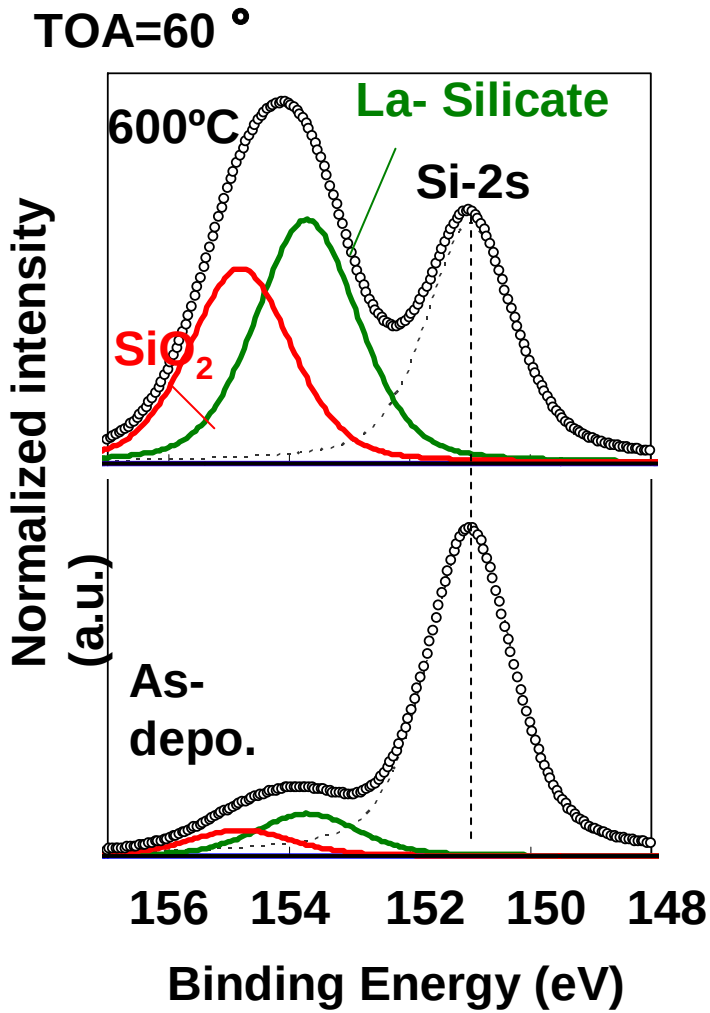


Free Energy (kJ/mol)

Sc_2O_3 **ΔG= -1901 + 0.287 * T**

Y_2O_3 **ΔG= -1895 + 0.281 * T**

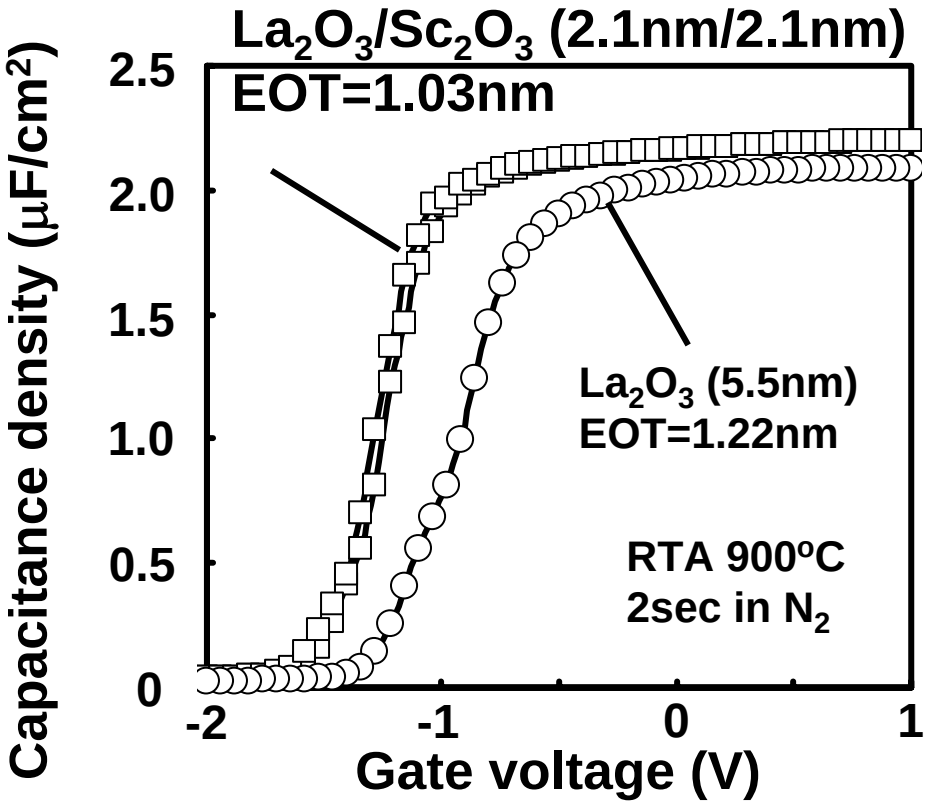
La_2O_3 **ΔG=-1785 + 0.277 * T**

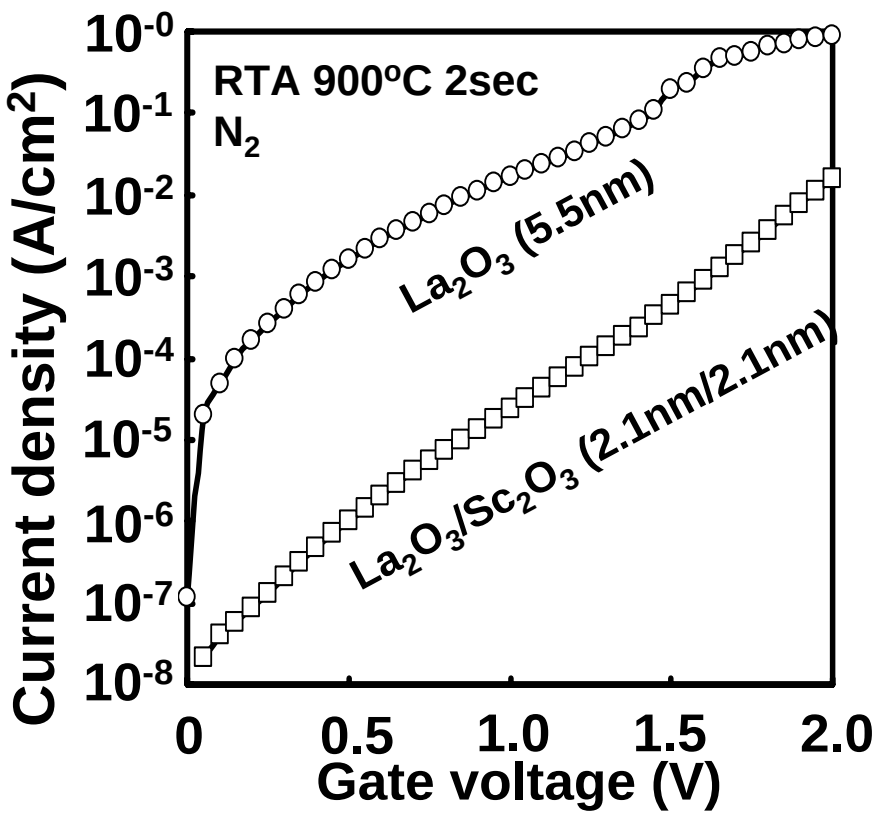


XPS analysis of La_2O_3/Si

K. Kakushima et al. Si Nanoelec. Workshop 2006

Sc_2O_3 Buffer Layer for High Temperature Process





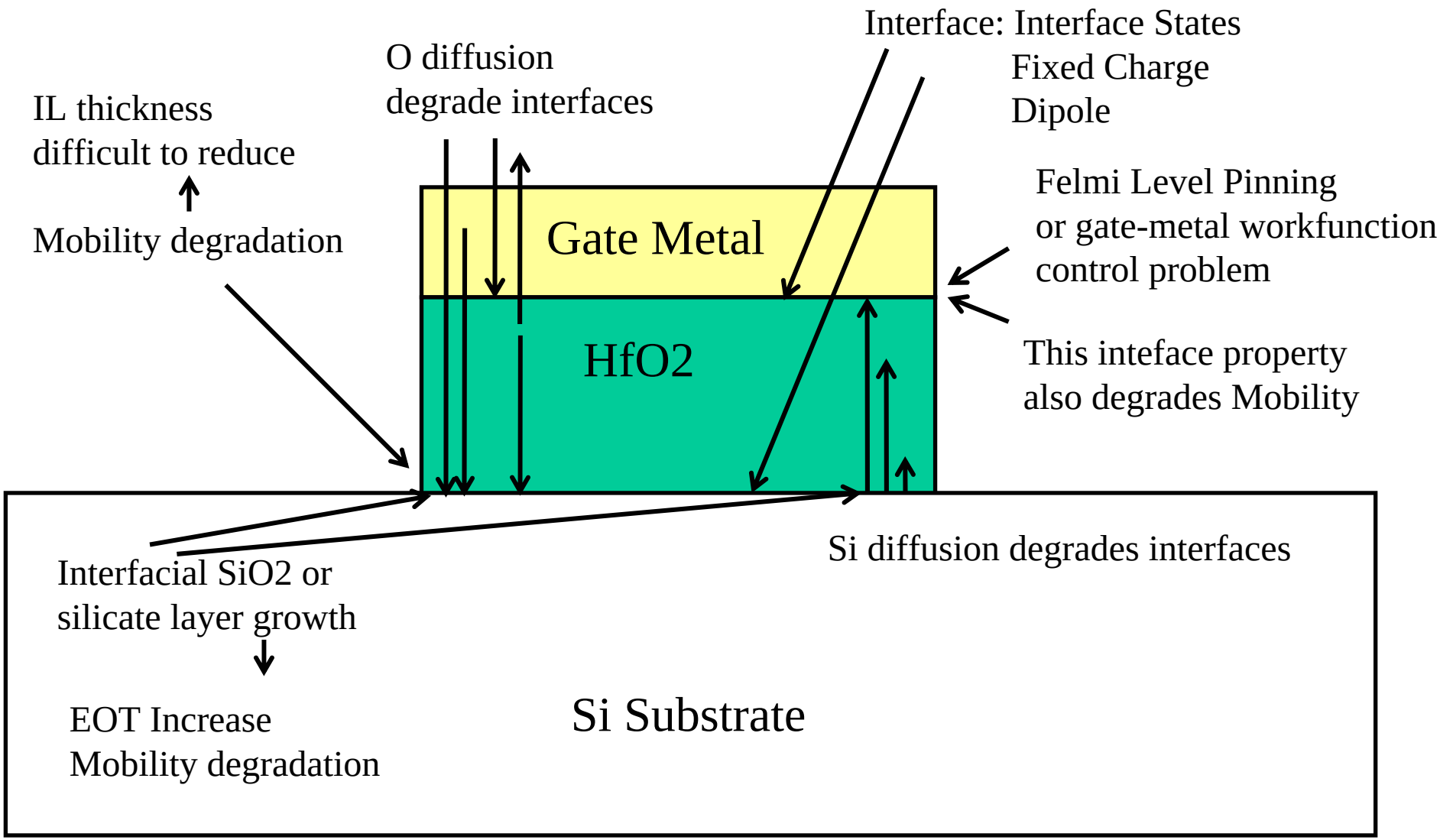
Leakage current suppression without degrading the CV curve

High temperature stability can be obtained with Sc_2O_3 buffer layer

K. Kakushima et al. Si Nanoelec. Workshop 2006

Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT



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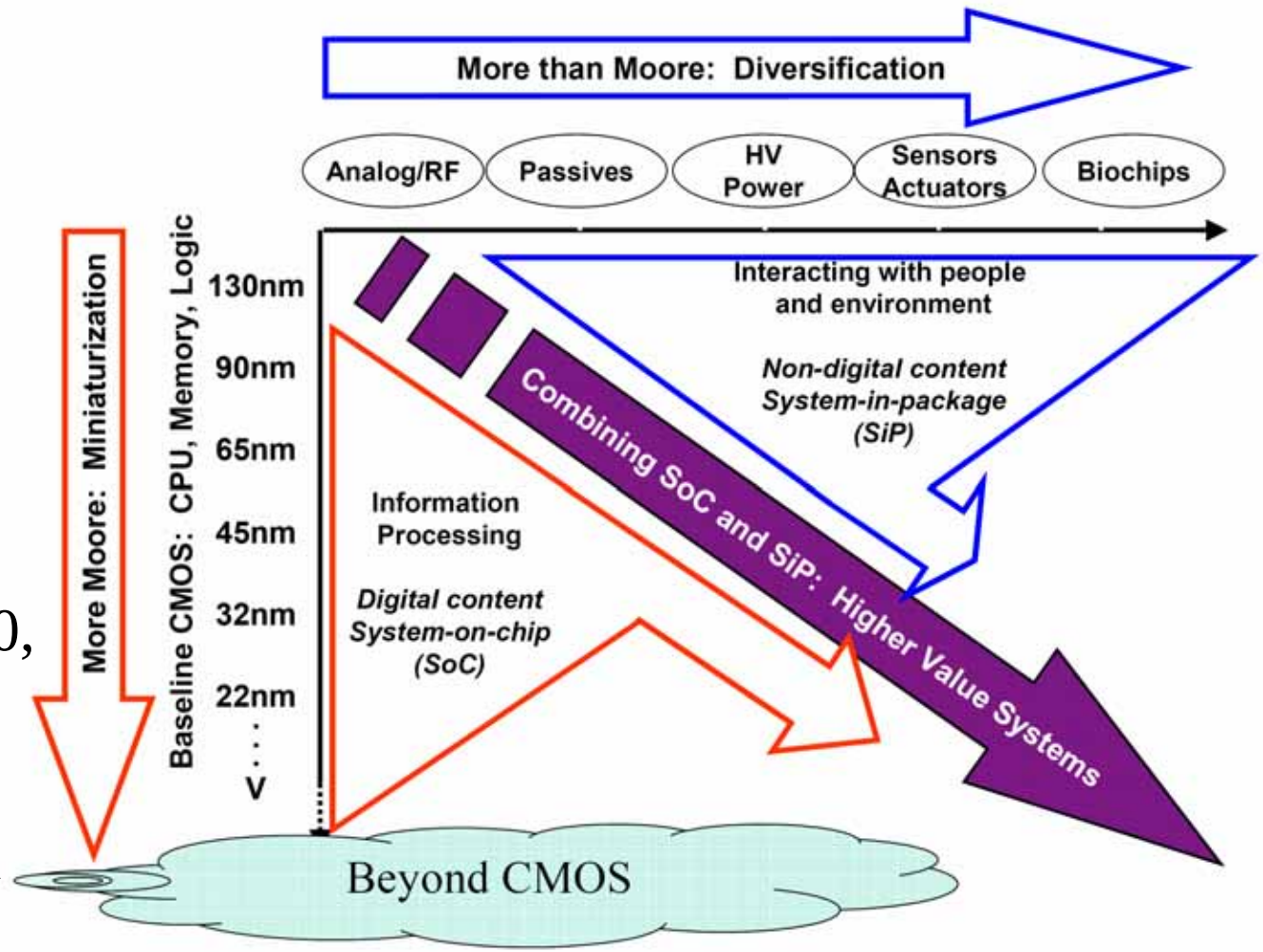
What will be issues for next 25 years?

Down to 2032?

ITRS Roadmap?

→ There is no roadmap after 2020.

More Moore and More than Moore



Beyond the Year of 2020, No roadmap

Question what is the other side of the cloud?

ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

World until 2020:

Scaling down approach will continue.

Two issues

New materials beyond HfSiON for

EOT = 1 ~ 0.5 nm

Multigate/Fin-FET structure

World beyond 2020:

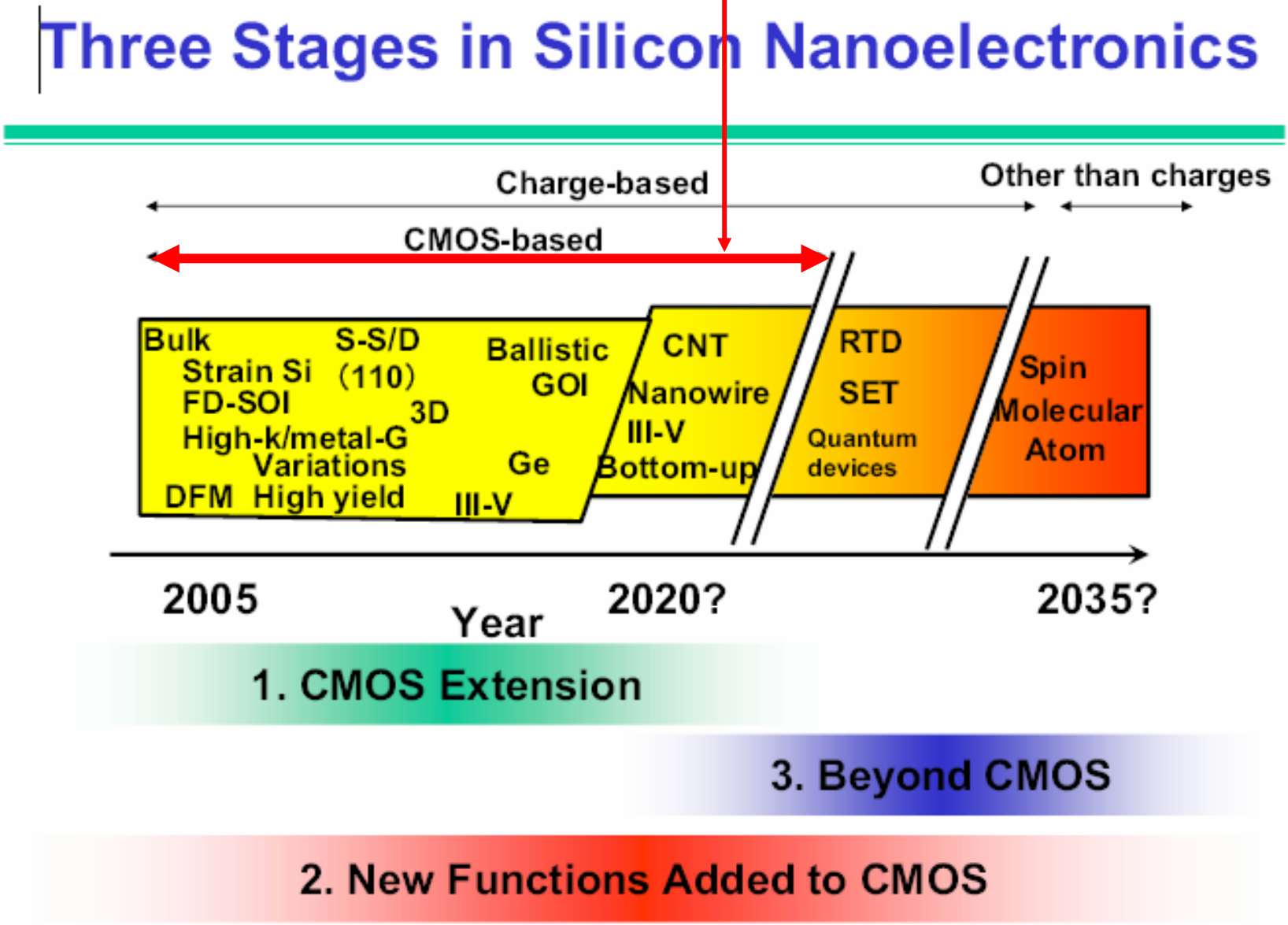
Totally, new paradigm after reaching the downsizing limit.

World beyond 2020:

Totally, new paradigm after reaching the downsizing limit.

What will be?

Question: Will CMOS end in 2020?



http://www.rcns.hiroshima-u.ac.jp/21coe/pdf/5th_WS/2-4-2_Hiramoto.pdf

After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.

After 2020

4 reasons for no downsizing anymore
or No decrease in gate length

---

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.

2. Increase of Off-current (Subthreshold current)

3. No decrease of gate capacitance because of parasitic components such as sidewall

4. Increase in production cost.

After 2020

What will be the world with no gate length reduction?

ITRS said before

---

around 2020,

Ge/III-V Channel FETs, Nanowire FET,
CNT FETs would be a good candidates

---

after 2020,

CMOS based devices would die
and will be replaced by new functional devices
such as RTD, SET, Spin, Molecular, Atom

My view

---

around 2020,

Ge/III-V Channel FETs, CNT FETs would be still too early for 2020. They are good candidates after.

---

after 2020,

CMOS based devices still continue for the main stream

We could keep the Moore's law after 2020
Without downswing the gate length

What is Moore's law.

→ to increase the number (#) of Tr. In a chip

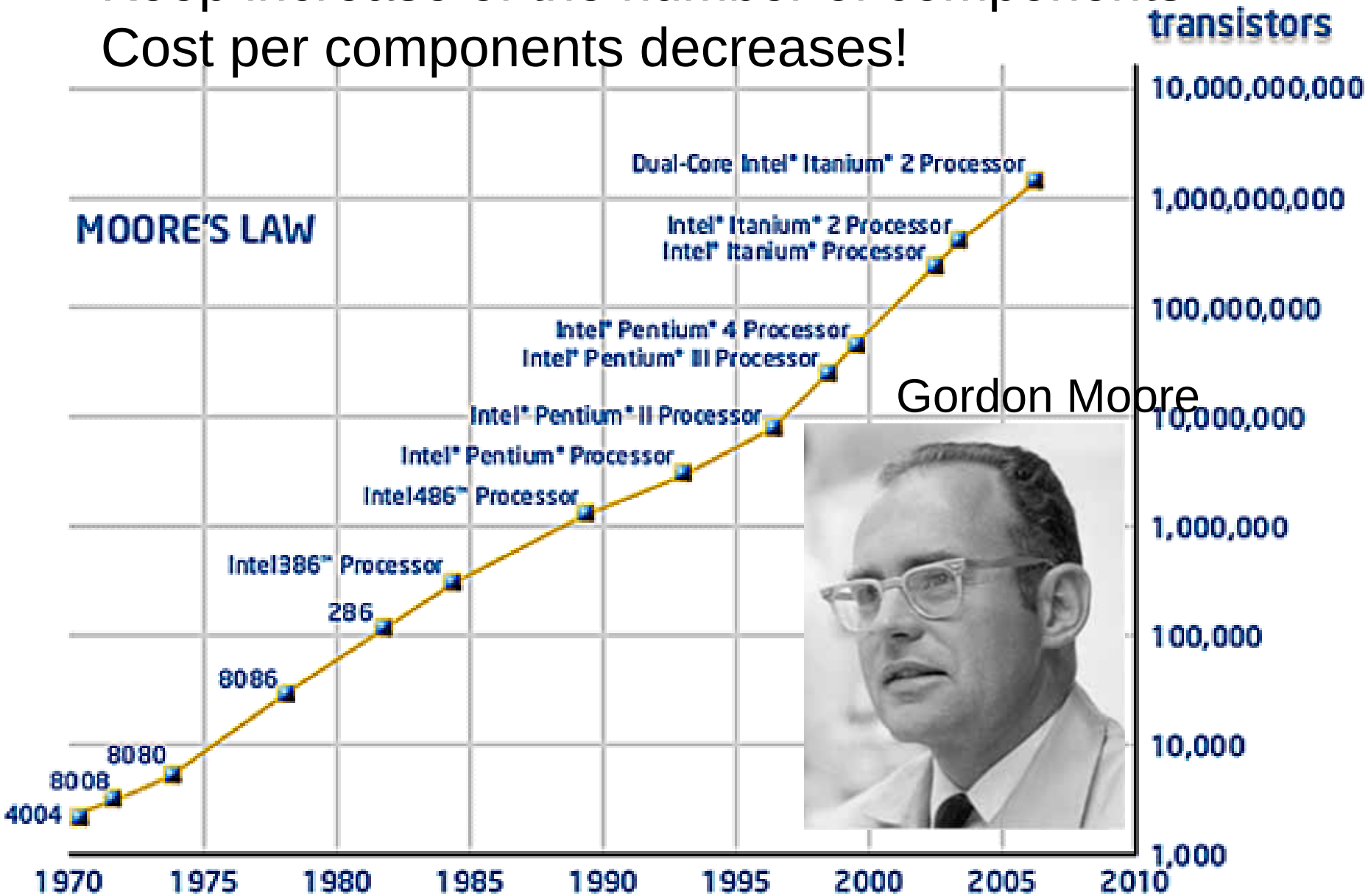
Now, # of Tr. in a chip is limited by power.

→ key issue is to reduce the power.

→ to reduce the supply voltage is still effective

To develop devices with sufficiently high drain current under low supply voltage is important.

Keep increase of the number of components.
Cost per components decreases!



http://www.intel.com/technology/mooreslaw/index.htm

Selection of MOSFET structure for high conduction:
Nano-wire or Nano-tube FETs is promissing

3 methods to realize High-conduction at Low voltage

1. Use 1D ballistic conduction

2. Increase number of quantum channel

3. Increase the number of wire or tube per area
   3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.

1D conduction per one quantum channel:

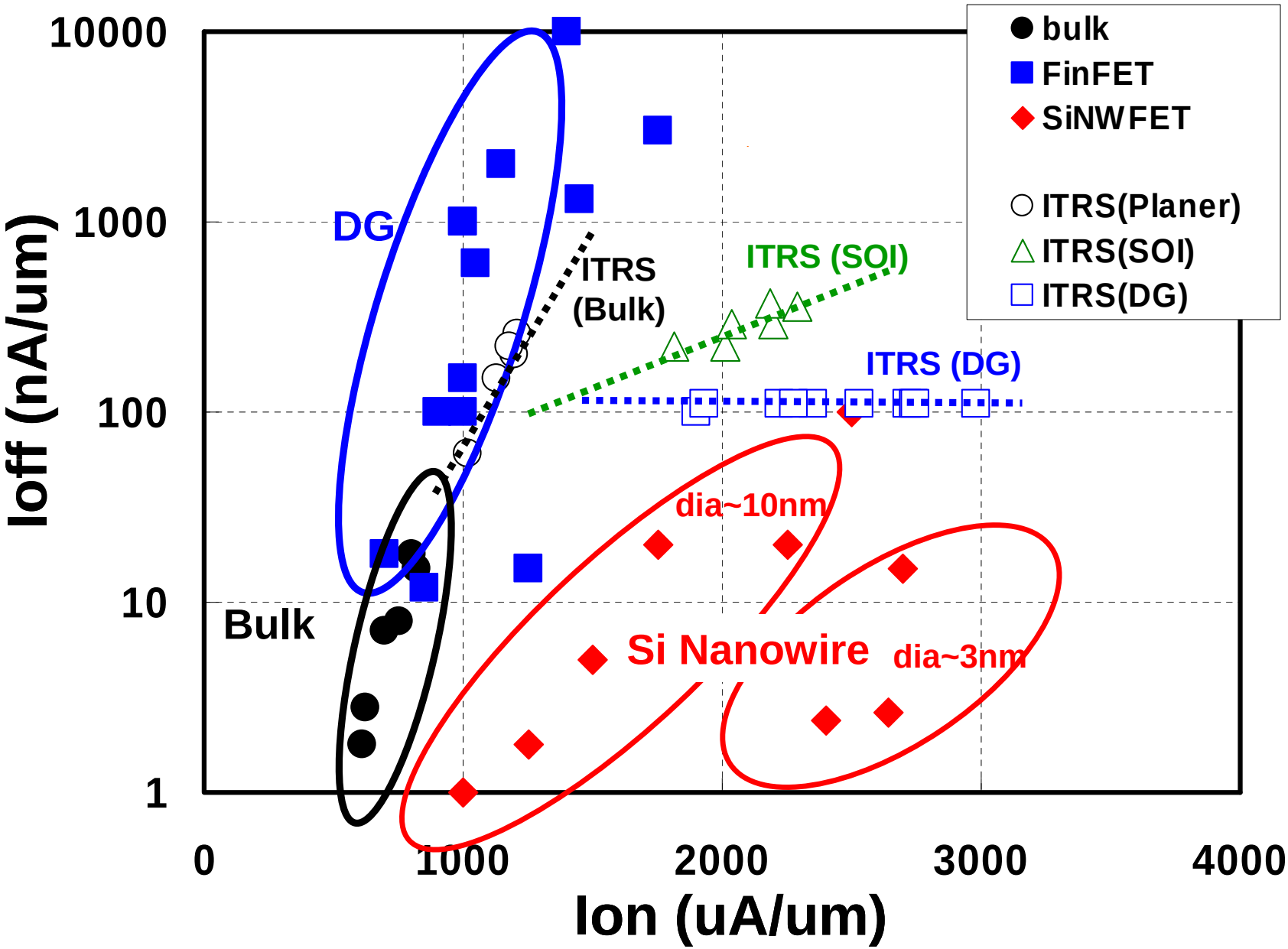
$G = 2e^2/h = 77.5\ \mu S$/wire or tube

regardless of gate length and channel material

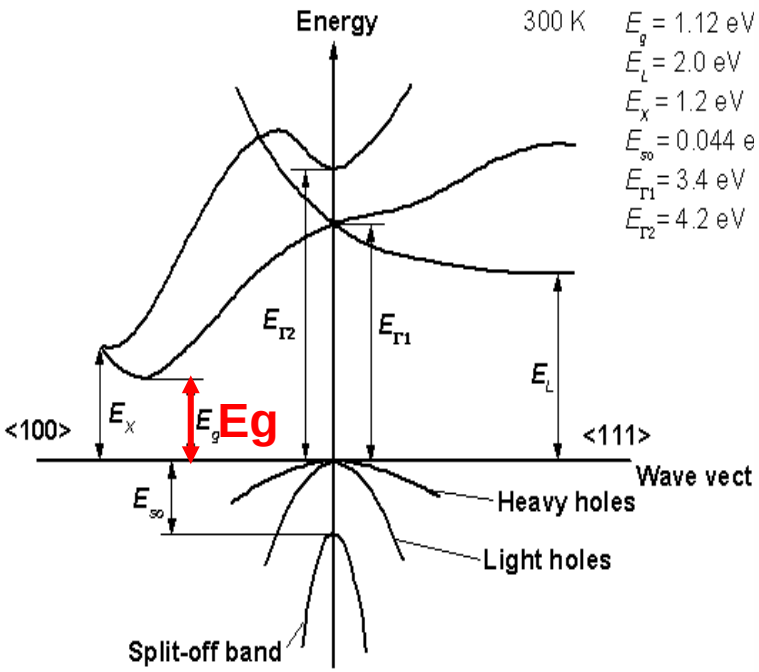
That is 77.5 mA/wire at 1V supply

This an extremely high value

However, already 20 mA was obtained experimentally in Samusung.

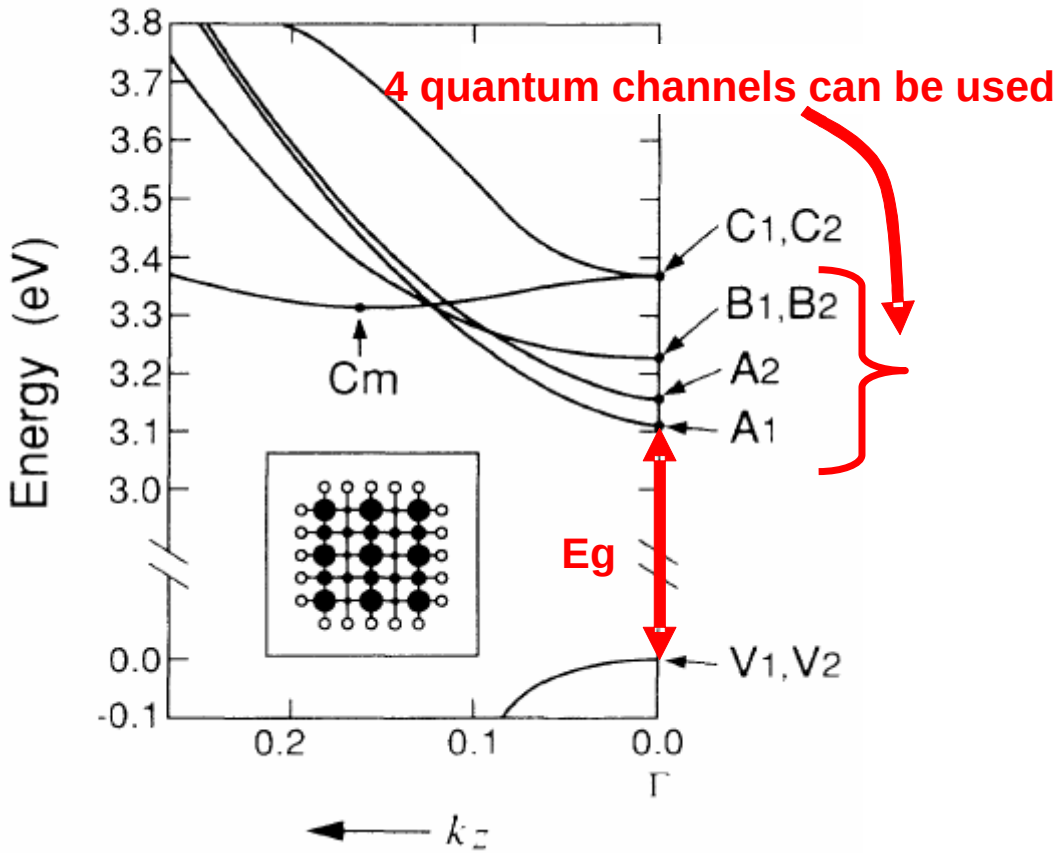

10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
DG
ITRS
(Bulk)
ITRS (SOI)
ITRS (DG)
dia~10nm
Bulk
Si Nanowire
dia~3nm

Increase the Number of quantum channels



Energy band of Bulk Si

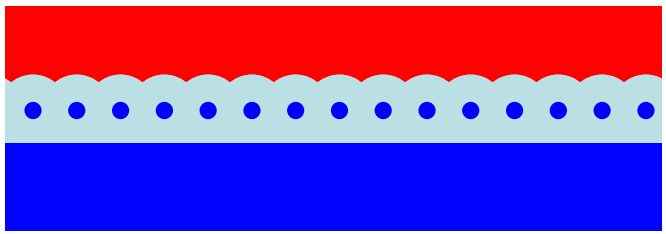
By Prof. Shiraishi of Tsukuba univ.



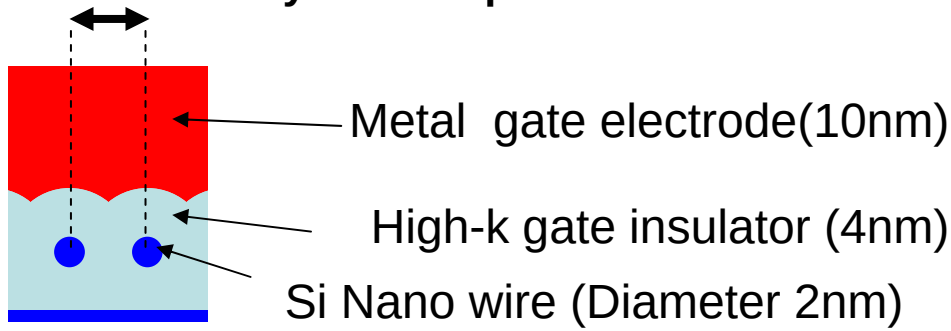
Energy band of 3 x 3 Si wire

Maximum number of wires per 1 μm

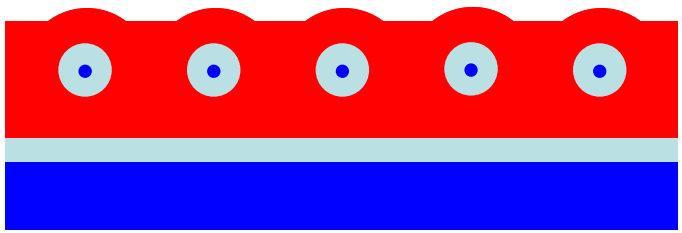
Front gate type MOS 165 wires /μm

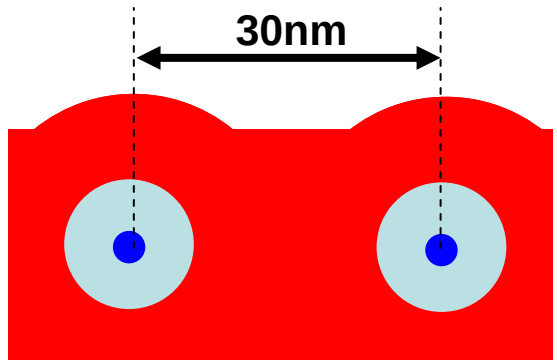


6nm pitch
By nano-imprint method

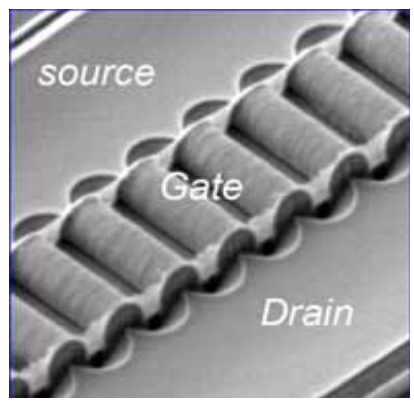


Surrounded gate type MOS 33 wires/μm



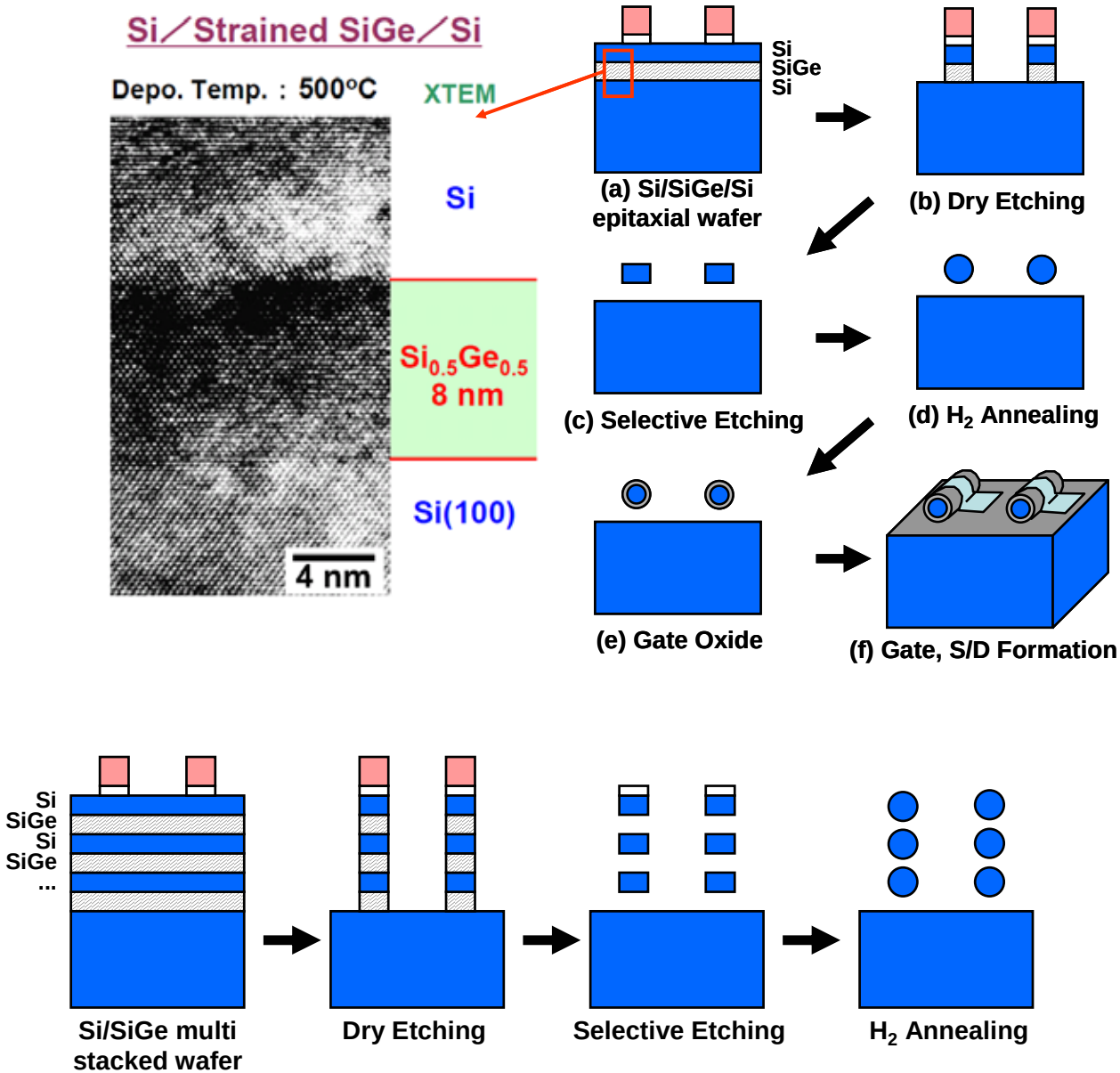


30nm pitch:
EUV lithograpy



Surrounded gate MOS

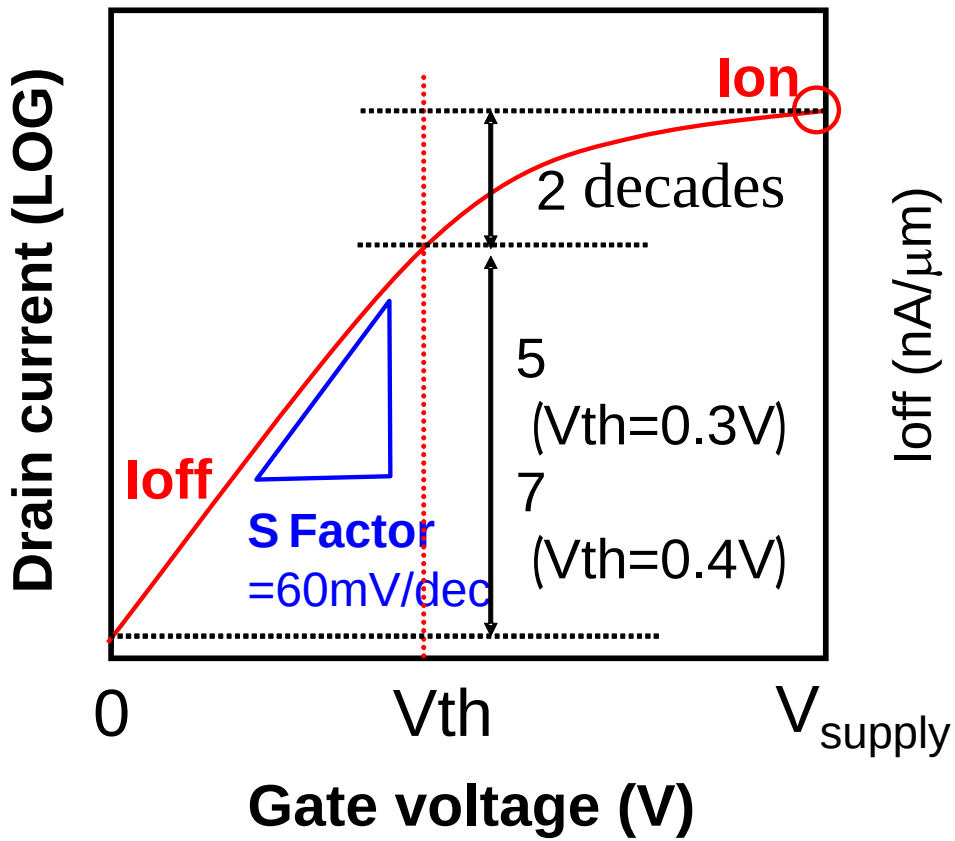
Increase the number of wires towards vertical dimension

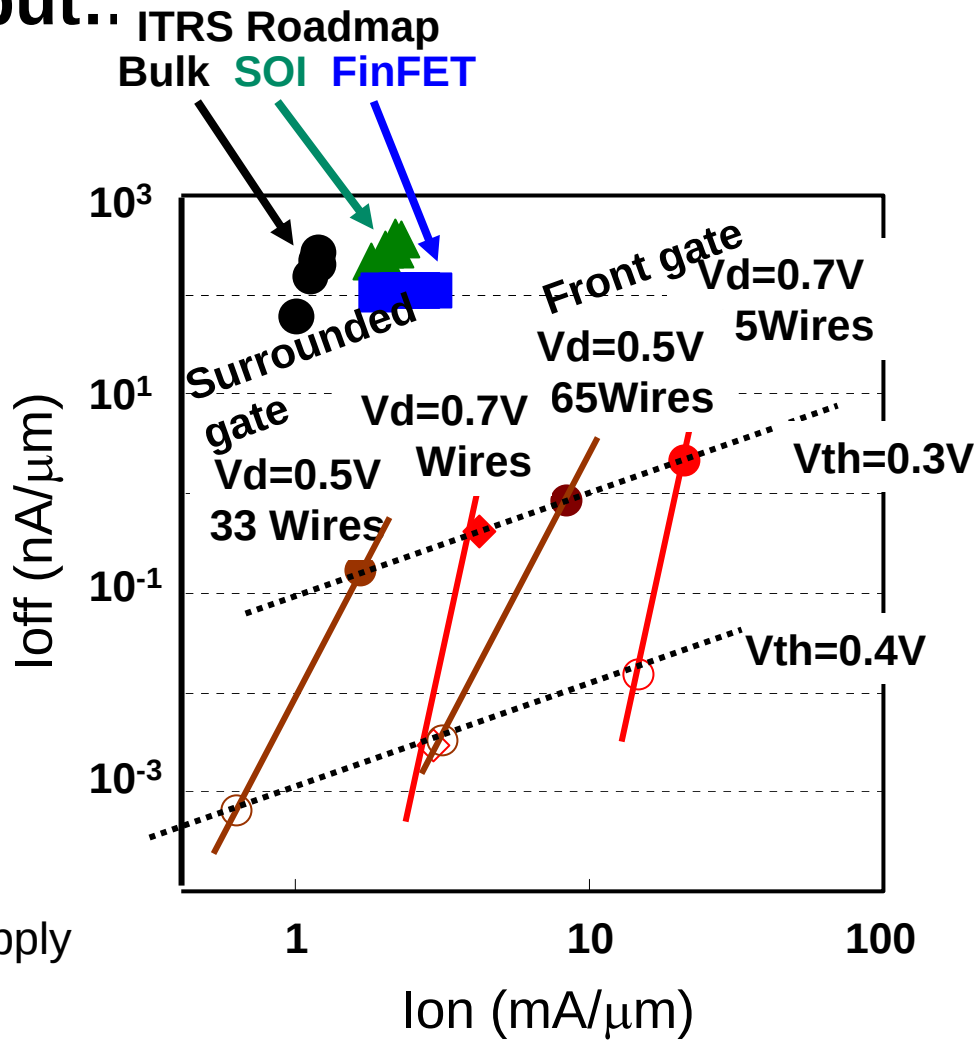


Estimation of Ion and Ioff of 1D conduction MOSFETs

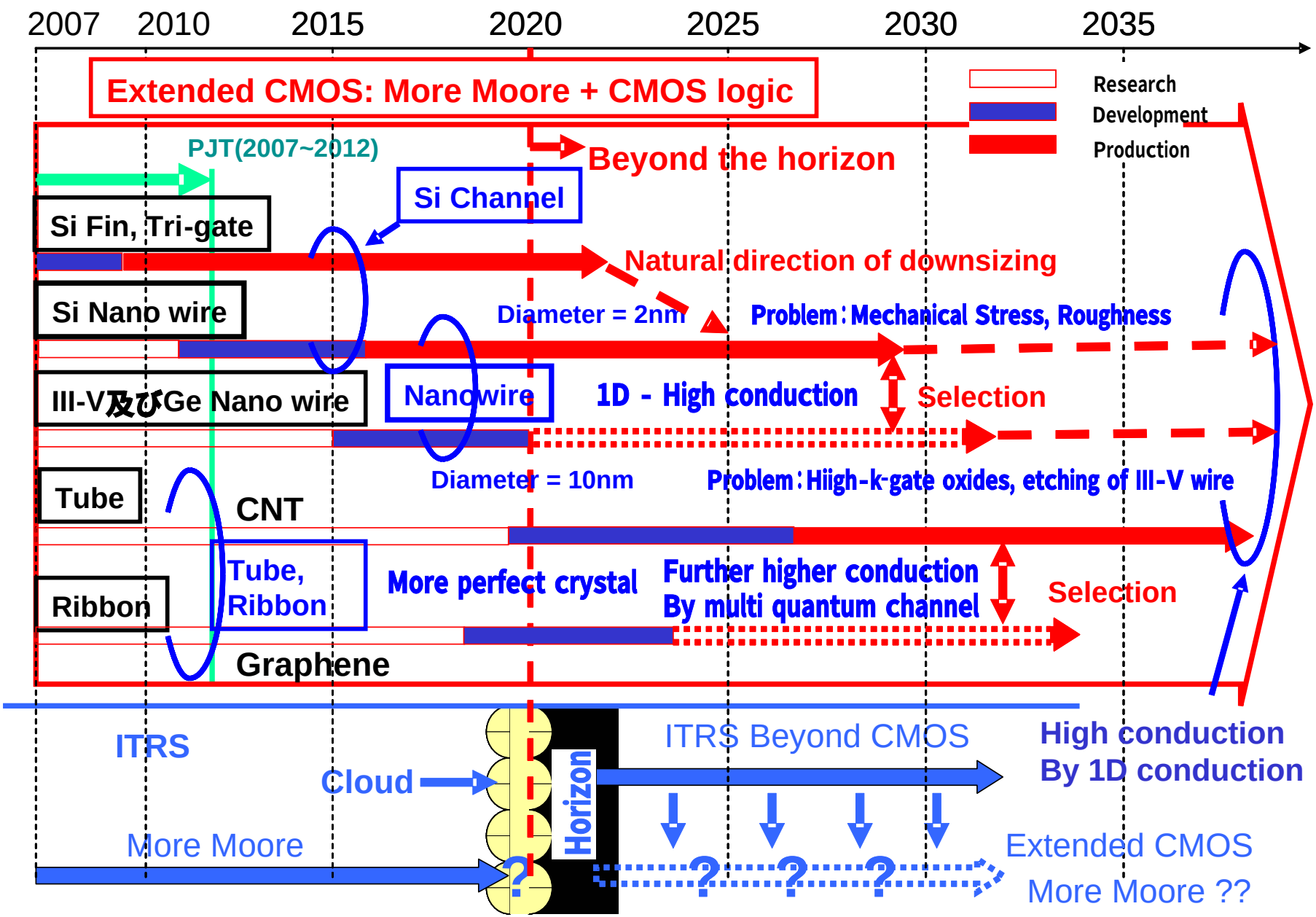
For optimum prediction:

At this moment, too much optimistic and more accurate calculation is necessary, but..





Our new roadmap



Thank you
for your attention!