Advanced Logic Technologies with New Materials and Structures

January 18, 2008

@IEEE ED Bangalore Chapter, at IIS, Bangalore, India

Hiroshi IWAI
Tokyo Institute of Technology
First Computer Eniac:
made of huge number of vacuum tubes 1946
Problems: Big size, huge power, short life time filament
J. E. LILIENFELD

IDEAS FOR CONTROLLED ELECTRIC CURRENT

Filed March 28, 1928

Idea of MOSFETs, 1928

J.E.LILIENFELD
Very bad interface property between the semiconductor and gate insulator

Drain Current was several orders of magnitude smaller than expected

No one could realize MOSFETs. Even Shockley!
1960: First MOSFET by D. Kahng and M. Atalla

Top View

Using Si and SiO2

Exceptionally good interface
1970: 1st generation of LSIs

1k bit DRAM Intel

2006: ULSIs

32 G bit Nand Flash
History of gate stack

Shrinking, Shrinking, and Shrinking!
and then, Shrinking, Shrinking, and Shrinking!

\[ C, V \propto L \quad C: \text{Capacitance} \quad V: \text{Voltage} \]

- Switching speed: \( CV/I \) \quad \rightarrow \text{Decrease}
- Power consumption: \( CV^2/2 \) \quad \rightarrow \text{Decrease}
- Integration density: \( 1/L^2 \) \quad \rightarrow \text{Increase}

<table>
<thead>
<tr>
<th>Year</th>
<th>Gate length</th>
<th>Gate Oxd Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td>10,000 nm</td>
<td>100 nm</td>
</tr>
<tr>
<td>2007</td>
<td>25 nm</td>
<td>1 nm</td>
</tr>
</tbody>
</table>
Downsizing of the components has been the driving force for circuit evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>1900</th>
<th>1950</th>
<th>1960</th>
<th>1970</th>
<th>2000</th>
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<tbody>
<tr>
<td>Vacuum Tube</td>
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<tr>
<td>Feature Size (cm)</td>
<td>10</td>
<td>cm</td>
<td>mm</td>
<td>10 µm</td>
<td>100 nm</td>
</tr>
<tr>
<td>Feature Size (m)</td>
<td>10^{-1}m</td>
<td>10^{-2}m</td>
<td>10^{-3}m</td>
<td>10^{-5}m</td>
<td>10^{-7}m</td>
</tr>
</tbody>
</table>

In 100 years, the feature size reduced by one million times. We have never experienced such a tremendous reduction in human history.
VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.
Finally, there appears to be a fundamental limit of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.
EOT: Equivalent Oxide Thickness to that of SiO₂

B. H. Lee et al., materials today (2006)
Direct-tunneling effect

Potential Barrier

Wave function
Direct tunneling leakage was found to be OK! In 1994 MOSFETs with 1.5 nm gate oxide had a significant leakage current when the thickness of the gate oxide was 3 nm. The diagram below shows the relationship between the drain voltage ($V_d$) and the source current ($I_d$) for different gate lengths ($L_g$) and gate voltages ($V_g$). The plots illustrate how the leakage current changes with varying parameters.
Direct tunneling leakage current start to flow when the thickness is 3 nm.

Gate leakage: \( I_g \propto \text{Gate Area} \propto \text{Gate length (Lg)} \)

Drain current: \( I_d \propto \frac{1}{\text{Gate length (Lg)}} \)

\( L_g \rightarrow \text{small,} \)

Then, \( I_g \rightarrow \text{small}, \) \( I_d \rightarrow \text{large,} \) \( \text{Thus, } \frac{I_g}{I_d} \rightarrow \text{small} \)
Transistor Scaling Continues

90nm node
Lg=50nm

65nm node
Lg=35nm

45nm node
Strained Si FET
Lg=25nm

32nm node
Lg=15nm

22nm node
Lg=10nm

~30% every two years

ITRS 2003 (HP)

Qi Xinag, ECS 2004, AM
5 nm gate length CMOS

Is a Real Nano Device!!

Length of 18 Si atoms

H. Wakabayashi et.al, NEC

IEDM, 2003
Downsizing limit!

Channel length
Gate oxide thickness

Electron wave length
10 nm

Tunneling distance
3 nm

Atom distance
0.3 nm
Prediction now!

Electron wave length 10 nm

Tunneling distance 3 nm

Atom distance 0.3 nm

MOSFET operation

$Lg = 2 \sim 1.5 \text{ nm}$?

Below this, no one knows future!
Prediction now!

Electron wave length
10 nm

Tunneling distance
3 nm

Gate length
Prediction at present

Practical limit because of off-leakage between S and D?
Lg = 5 nm?

MOSFET operation
Lg = 2 ~ 1.5 nm?

But, no one knows future!
Maybe, practical limit around 5 nm.

When Gate length Smaller,  
\[ \rightarrow \text{Subthreshold Leakage Current Larger} \]

Subthreshold Leakage Current

Id

OFF

ON

Subthreshold Current Is OK at Single Tr.

But not OK For Billions of Trs.
Scaling Limit in MOSFET

By Robert Chau, IWGI 2003

- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

ULTIMATE LIMIT

Wave length of electron
Direct-tunneling limit in SiO2
Distance between Si atoms
So, we are now in the limitation of downsizing?

Do you believe this or do not?
There is a solution! K: Dielectric Constant
To use high-k dielectrics

Thin gate SiO₂  Thick gate high-k dielectrics

Almost the same electric characteristics

However, very difficult and big challenge!
Remember MOSFET had not been realized without Si/SiO₂!
### Historical Trend of New Material for Gate Stack

<table>
<thead>
<tr>
<th>Year</th>
<th>MOSFET</th>
<th>Gate Stack in production</th>
<th>1st FET IC LSI</th>
<th>PMOS</th>
<th>NMOS</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1960</td>
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<td>1970</td>
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<td>1980</td>
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<tr>
<td>1990</td>
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<td>2000</td>
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<tr>
<td>2005</td>
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</tbody>
</table>

**Gate insulator:**
- SiO₂
- SiOₓNᵧ
- Hf base

**Gate electrode:**
- Al
- N⁺Poly Si
- Double Poly Si
- Double Metal

**Silicide above Poly Si electrode:**
- MoSi₂ → WSi₂, TiSi₂, CoSi₂, NiSi

**R&D for high-k:**
- MOSFET: Ni₃Si₄, Al₂O₃, ZrO₂
- Pure Si Period
- Recent new high-k

**DRAM Capacitor:**
- (O)NO, Ni₃Si₄, Ta₂O₅, Al₂O₃

**NV Memory:**
- NO, AO (Al₂O₃/SiO₂)

**Analog/RF:**
- Ta₂O₅
Too large high-k cause significant short channel effect

![Graph showing current density vs. gate voltage](image)

- $L_g = 0.04 \, \text{m}$
- $V_{gd} = 0.1 \, \text{V}$
- $EOT = 2 \, \text{nm}$

- $K = 390$ for Too large High-k
- $K = 3.9$ for SiO$_2$

**SiO$_2$**

- $V_g = 0 \, \text{V}$, $V_d = 0.5 \, \text{V}$

- Magnified 100 times in vertical direction

Penetration of lateral field from Drain through high-k causes significant short channel effects
**Choice of High-k**

<table>
<thead>
<tr>
<th>Candidates</th>
<th>□</th>
<th>Gas or liquid at 1000 K</th>
<th>□</th>
<th>Radio active</th>
<th>□</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>□</td>
<td>Si + MOₓ</td>
<td>M + SiO₂</td>
<td>□</td>
<td>He</td>
</tr>
<tr>
<td>Li Be</td>
<td>□</td>
<td>Si + MOₓ</td>
<td>MSiₓ + SiO₂</td>
<td>□</td>
<td>Ne</td>
</tr>
<tr>
<td>Mg Na</td>
<td>□</td>
<td>Si + MOₓ</td>
<td>M + MSiₓOᵧ</td>
<td>□</td>
<td>Ar</td>
</tr>
<tr>
<td>Al Si P S Cl Ar</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

HfO₂ based dielectrics are selected as the first generation materials, because of their merit in:
1) band-offset,
2) dielectric constant
3) thermal stability

La₂O₃ based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer.

Unstable at Si interface:

- Si + MOₓ → M + SiO₂
- Si + MOₓ → MSiₓ + SiO₂
- Si + MOₓ → M + MSiₓOᵧ

R. Hauser, IEDM Short Course, 1999
**Band Offsets**

**Calculated value**

**Dielectric constant**

\[
\begin{array}{l}
\text{SiO}_2; \ 4 \\
\text{Si}_3\text{N}_4; \sim 7 \\
\text{Al}_2\text{O}_3; \sim 9 \\
\text{Y}_2\text{O}_3; \sim 10 \\
\text{Gd}_2\text{O}_3; \sim 10 \\
\text{HfO}_2; \sim 23 \\
\text{La}_2\text{O}_3; \sim 27 \\
\end{array}
\]

HfO\text{2} was chosen for the 1\text{st} generation
La2O\text{3} is more difficult material to treat

Energy Barrier Offset of La2O3

XPS measurement by Prof. T. Hattori, INFOS 2003
Intel’s announcement, January 26, 2007, and IEDM Dec 2007

Hafnium-based high-k material by ALD: EOT= 1nm
Specific gate metals (Intel’s trade secret)
  Different Metals for NMOS and PMOS
Use of 193nm dry lithography

From 65 nm to 45 nm Tech.
  Tr density: 2 times increase
  Tr switching power: 30% reduction
  Tr switching speed: 20% improvement
  S-D leakage power: 5 times reduction
  Gate oxide leakage: 10 times reduction

45nm processors (Core™2 family processors "Penryn") running
  Windows*, Vista*, Linux* etc.

45nm production in the second half of 2007
PMOS

Metal Gate
(different for NMOS & PMOS)

High-k

Silicon Substrate
**Replacement Metal Gate (Damascene)**

**Advantages**
- Low thermal budget (metal gate deposition after S/D anneals)
- Known metal work function

**Challenges**
- Cost
- Extendibility to narrower CDs

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**Gate-First Process**

**pFET/nFET Cap Layer**

**Advantages**
- Compatible with high thermal budget process
- Follows standard CMOS flow

**Challenges**
- NMOS and PMOS cap layer integration is challenging

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Reza Arghavani, Ph.D., Applied Materials, IEDM 2007 Short Course
High-k with EOT = 0.5 nm

<table>
<thead>
<tr>
<th>Physical Gate Length (nm)</th>
<th>2005</th>
<th>2007</th>
<th>2009</th>
<th>2011</th>
</tr>
</thead>
<tbody>
<tr>
<td>Equivalent Oxide Thickness (nm)</td>
<td>1.2</td>
<td>1.1</td>
<td>0.9</td>
<td>0.5, 0.8(DG)</td>
</tr>
</tbody>
</table>

ITRS 2006
Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT

- IL thickness difficult to reduce
- Mobility degradation
- Interfacial SiO2 or silicate layer growth
- EOT Increase
- Mobility degradation
- O diffusion degrade interfaces
- Interface: Interface States
  - Fixed Charge
  - Dipole
  - Felmi Level Pinning or gate-metal workfunction control problem
  - This interface property also degrades Mobility

Si diffusion degrades interfaces
EOT = 0.48 nm

Our results

Transistor with La2O3 gate insulator
Mobility degradation causes for High-k MOSFETs ($\text{HfO}_2$, $\text{Al}_2\text{O}_3$ based oxide)

Remote scattering is dominant

- Fixed charge
- Phase separation
- Crystallization
- Interfacial dipole
- Remote surface roughness
- Remote phonon

S. Saito et al., IEDM 2003,
S. Saito et al., ECS Symp. on ULSI Process Integration
PVD TiN, ALD TaN, CVD W on High-k:

- 4-5 Orders Magnitude Improvement in Gate Leakage
- Equivalent Electron Mobility as that of Oxynitride

Source: E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006
Thinning EOT toward 0.5-0.7 nm
Keeping good mobility with thinning IL

Searching new materials:
La2O3 based / Rare earth oxides

ITRS 2003

Epitaxial (LaAlO3)
Ternary (LaAlO3)
RE high-k (La2O3,...)
Hf(Zr)-base
Oxynitride

Year
Tech. node
2004 hp90
2007 hp65
2010 hp45

ITRS 2003
Hygroscopic Properties of La2O3

After 30 hours in clean room (temperature & humidity controlled)
Gate Leakage vs EOT, (Vg=|1|V)

Current density (A/cm²)

EOT (nm)

Materials:
- Al₂O₃
- HfAlO(N)
- HfO₂
- HfSiO(N)
- HfTaO
- La₂O₃
- Nd₂O₃
- Pr₂O₃
- PrSiO
- PrTiO
- SiON/SiN
- Sm₂O₃
- SrTiO₃
- Ta₂O₅
- TiO₂
- ZrO₂(N)
- ZrSiO
- ZrAlO(N)
Effect of gate workfunction

N-MOSFET: N-Poly Si gate electrode
Typical $V_{th} = 0.25 \sim 0.6 \text{ V}$

P-MOSFET: P-Poly Si gate electrode
Typical $V_{th} = -0.25 \sim -0.6 \text{ V}$

$V_{fb}$ difference between N-Poly and P-Poly is 1.15 eV (Ideally)

P-MOSFET with N-Poly gate electrode

$V_{th} \rightarrow -1.4 \sim -1.75 \text{ too big}$

difficult to be adjusted by channel implantation
No FLP for La$_2$O$_3$

Changing Pt/W ratio of gate electrode

HfO$_2$

La$_2$O$_3$

K.Ohmori, SSDM2006
One Dielectric, Two $\Phi_m$ Metals vs. Two Dielectric Stacks, One $\Phi_m$ Metal

Integration Approach A

Two Distinct Metals Required

- nFET
- pFET
- TaN\textsuperscript{1}
- WN\textsuperscript{3}
- TaC\textsuperscript{2}

Integration Approach B

One Metal Only With Nanoscale Cap Layers (Dipole Approach)

- nFET
- pFET
- LaO\textsubscript{x}\textsuperscript{1}
- Al-based\textsuperscript{2}

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\textsuperscript{1} E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006
\textsuperscript{2} W.J. Taylor, et al. (Freescale), IEDM p. 625, 2006
\textsuperscript{3} P-C. Jiang, et al., APL 89, 2006, H. Matushishi and S. Nishikawa, JJAP v33, 1994

Reza Arghavani, Ph.D., Applied Materials, IEDM 2007 Short Course
Electrical Characteristics of La$_2$O$_3$ n-MOSFET

Al/La$_2$O$_3$/p-Si/Al

Process
- La$_2$O$_3$ 300 °C deposition
- PDA N$_2$ 300 °C 10 min

Good electrical characteristics can be obtained.
K. Kakushima et al. Si Nanoelec. Workshop 2006
Effective Mobility of La$_2$O$_3$ MOSFET

High effective mobility of 312 cm$^2$/Vs can be obtained with La$_2$O$_3$.

K. Kakushima et al. Si Nanoelec. Workshop 2006
Interface state density increases at higher temperature annealing

K. Kakushima et al. Si Nanoelec. Workshop 2006
Pt/La$_2$O$_3$/Pt MIM Capacitor

![Graph showing capacitance density vs. voltage with a peak at 25.6 fF/µm$^2$.](image)

- Capacitance density (fF/µm$^2$) vs. Voltage (V)
- 25.6 fF/µm$^2$
- Thickness = 8.3 nm, $k = 21$

La$_2$O$_3$ : Heat endurance is good

K. Kakushima et al. Si Nanoelec. Workshop 2006
La2O3 Gate Insulator for High Temperature Process

High temperature annealing above 500°C

SiOx based interfacial layer formation
- Increase in EOT
- Higher Dit

Interfacial Layer Suppression using buffer layer

![Diagram showing La2O3/Si structure with Sc2O3 and ScSiO layers]

Free Energy (kJ/mol)
- \( \text{Sc}_2\text{O}_3 \) \( G = -1901 + 0.287 \times T \)
- \( \text{Y}_2\text{O}_3 \) \( G = -1895 + 0.281 \times T \)
- \( \text{La}_2\text{O}_3 \) \( G = -1785 + 0.277 \times T \)

![XPS analysis of La2O3/Si showing binding energy and normalized intensity]

K. Kakushima et al. Si Nanoelec. Workshop 2006
Sc$_2$O$_3$ Buffer Layer for High Temperature Process

Leakage current suppression without degrading the CV curve

High temperature stability can be obtained with Sc$_2$O$_3$ buffer layer

K. Kakushima et al. Si Nanoelec. Workshop 2006
Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT

- IL thickness difficult to reduce
- O diffusion degrades interfaces
- Interfacial SiO2 or silicate layer growth
- EOT Increase
- Mobility degradation

- Fixed Charge
- Felmi Level Pinning or gate-metal workfunction control problem
- This interface property also degrades Mobility

- Interface: Interface States
  - Dipole
  - Interface States
  - Fixed Charge
What will be issues for next 25 years?

Down to 2032?

ITRS Roadmap?

→ There is no roadmap after 2020.
More Moore and More than Moore

Beyond the Year of 2020, No roadmap

Question what is the other side of the cloud?

ITRS 2005 Edition

World until 2020:
   Scaling down approach will continue.

Two issues
   New materials beyond HfSiON for
       EOT = 1 ~ 0.5 nm
   Multigate/Fin-FET structure

World beyond 2020:
   Totally, new paradigm after reaching
   the downsizing limit.
World beyond 2020:

Totally, new paradigm after reaching the downsizing limit.

What will be?
Three Stages in Silicon Nanoelectronics

1. CMOS Extension
2. New Functions Added to CMOS
3. Beyond CMOS

Charge-based
CMOS-based
Other than charges

2005
2020?
2035?

- Bulk
- S-S/D
- Strain Si (110)
- FD-SOI
- 3D
- High-k/metal-G
- Variations
- DFM
- High yield
- III-V

- Ballistic
- GOI
- CNT
- Nanowire
- III-V
- Bottom-up

- RTD
- SET
- Quantum devices
- Spin
- Molecular
- Atom

Question: Will CMOS end in 2020?

http://www.rcns.hiroshima-u.ac.jp/21coe/pdf/5th_WS/2-4-2_Hiramoto.pdf
After 2020

There is no decrease in gate length around at 10 ~ 5 nm.

4 reasons.
After 2020

4 reasons for no downsizing anymore
or No decrease in gate length

1. No increase of On-current (Drain current) because of already semi-ballistic conduction.

2. Increase of Off-current (Subthreshold current)

3. No decrease of gate capacitance because of parasitic components such as sidewall

4. Increase in production cost.
After 2020

What will be the world with no gate length reduction?
ITRS said before around 2020,

Ge/III-V Channel FETs, Nanowire FET, CNT FETs would be a good candidates after 2020,

CMOS based devices would die and will be replaced by new functional devices such as RTD, SET, Spin, Molecular, Atom
My view

around 2020,

Ge/III-V Channel FETs, CNT FETs would be still too early for 2020. They are good candidates after.

after 2020,

CMOS based devices still continue for the mainstream
We could keep the Moore’s law after 2020 without downswinging the gate length.

What is Moore’s law.

→ to increase the number (#) of Tr. in a chip.

Now, # of Tr. in a chip is limited by power.

→ key issue is to reduce the power.

→ to reduce the supply voltage is still effective.

To develop devices with sufficiently high drain current under low supply voltage is important.
Keep increase of the number of components. Cost per components decreases!

Gordon Moore

Selection of MOSFET structure for high conduction: Nano-wire or Nano-tube FETs is promising

3 methods to realize High-conduction at Low voltage
1. Use 1D ballistic conduction
2. Increase number of quantum channel
3. Increase the number of wire or tube per area 3D integration of wire and tubes

For suppression of Ioff, the Nanowire/tube is also good.
1D conduction per one quantum channel:
\[ G = 2e^2/h = 77.5 \ \mu\text{S/wire or tube} \]
regardless of gate length and channel material

That is 77.5 mA/wire at 1V supply

This an extremely high value

However, already 20 mA was obtained experimentally in Samsung.
Increase the Number of quantum channels

By Prof. Shiraishi of Tsukuba univ.

Energy band of Bulk Si

Energy band of 3 x 3 Si wire
Maximum number of wires per 1 µm

Front gate type MOS 165 wires /µm

Surrounded gate type MOS 33 wires/µm

6nm pitch
By nano-imprint method

Metal gate electrode(10nm)
High-k gate insulator (4nm)
Si Nano wire (Diameter 2nm)

30nm pitch: EUV lithography
Increase the number of wires towards vertical dimension

Si/Strained SiGe/Si
Depo. Temp.: 500°C

Si

Si_Ge
8 nm

Si(100)

- (a) Si/SiGe/Si epitaxial wafer
- (b) Dry Etching
- (c) Selective Etching
- (d) H₂ Annealing
- (e) Gate Oxide
- (f) Gate, S/D Formation

Si/SiGe multi stacked wafer

Dry Etching

Selective Etching

H₂ Annealing
Estimation of Ion andloff of 1D conduction MOSFETs
For optimum prediction:
At this moment, too much optimistic and more accurate calculation is necessary, but...

- ITRS Roadmap
  - Bulk
  - SOI
  - FinFET

- S Factor = 60mV/dec

- Ion (mA/µm)
  - 10^4
  - 10^3
  - 10^2
  - 10^1
  - 10^0

- Ioff (nA/µm)
  - 10^3
  - 10^2
  - 10^1
  - 10^0

- Drain current (LOG)

- S Factor = 60mV/dec

- 2 decades

- 5 (Vth=0.3V)
- 7 (Vth=0.4V)

- Front gate
- Surrounded

- Vd=0.5V
- 65Wires
- Vth=0.3V

- Vd=0.7V
- 5Wires
- Vth=0.4V
Our new roadmap

Extended CMOS: More Moore + CMOS logic

Beyond the horizon

Natural direction of downsizing

Diameter = 2nm

Si Channel

Si Fin, Tri-gate

Si Nano wire

Extended CMOS: More Moore + CMOS logic

Selection

Diameter = 10nm

Nanowire

Tube, Ribbon

Graphene

ITRS

More Moore

ITRS Beyond CMOS

Extended CMOS

More Moore ??

ITRS Beyond CMOS

High conduction

By 1D conduction
Thank you for your attention!