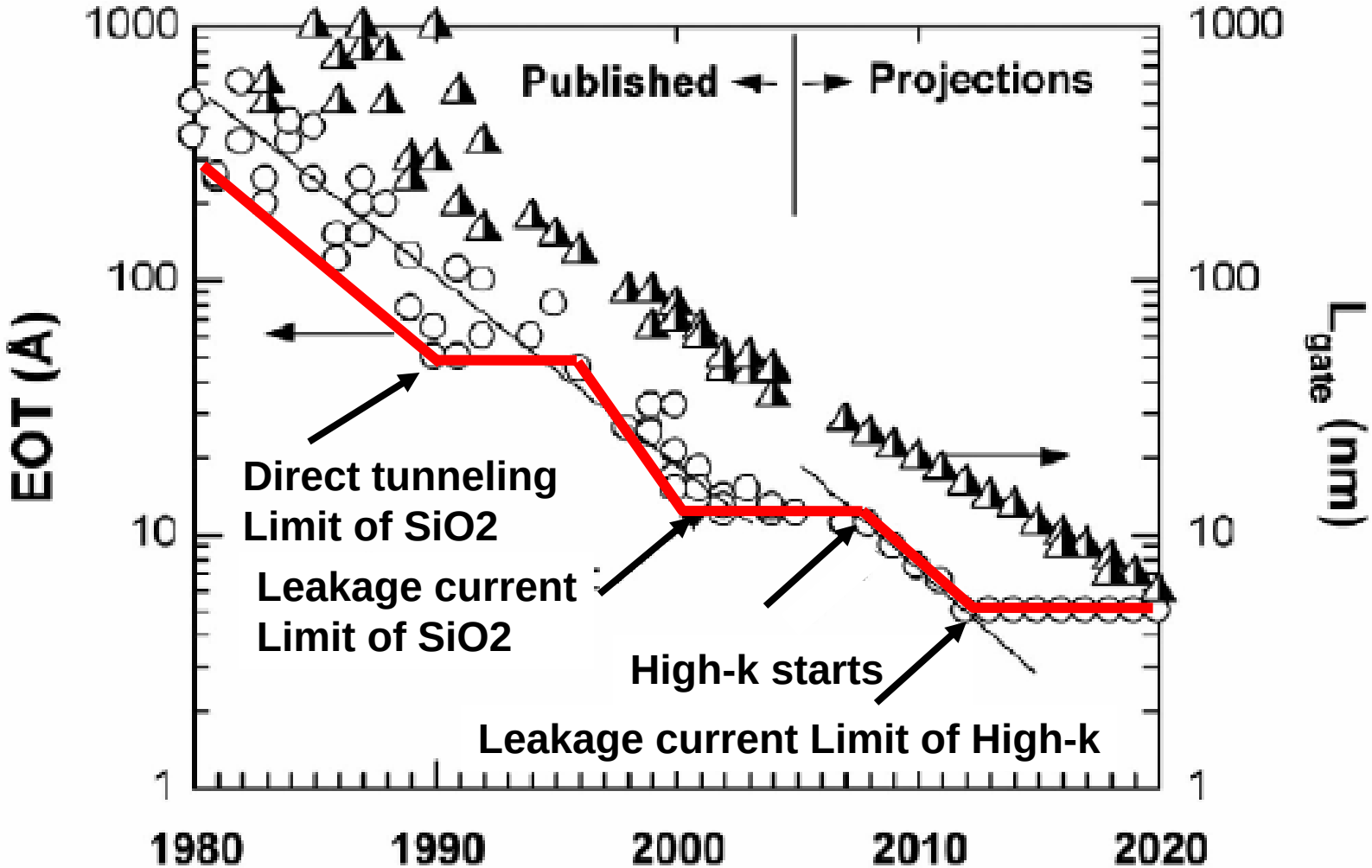
High-k/Metal Gate Technology

January 9, 2008 @IIT-Bombay

Hiroshi Iwai

Frontier Reseach Center,
Tokyo Institute of Technology

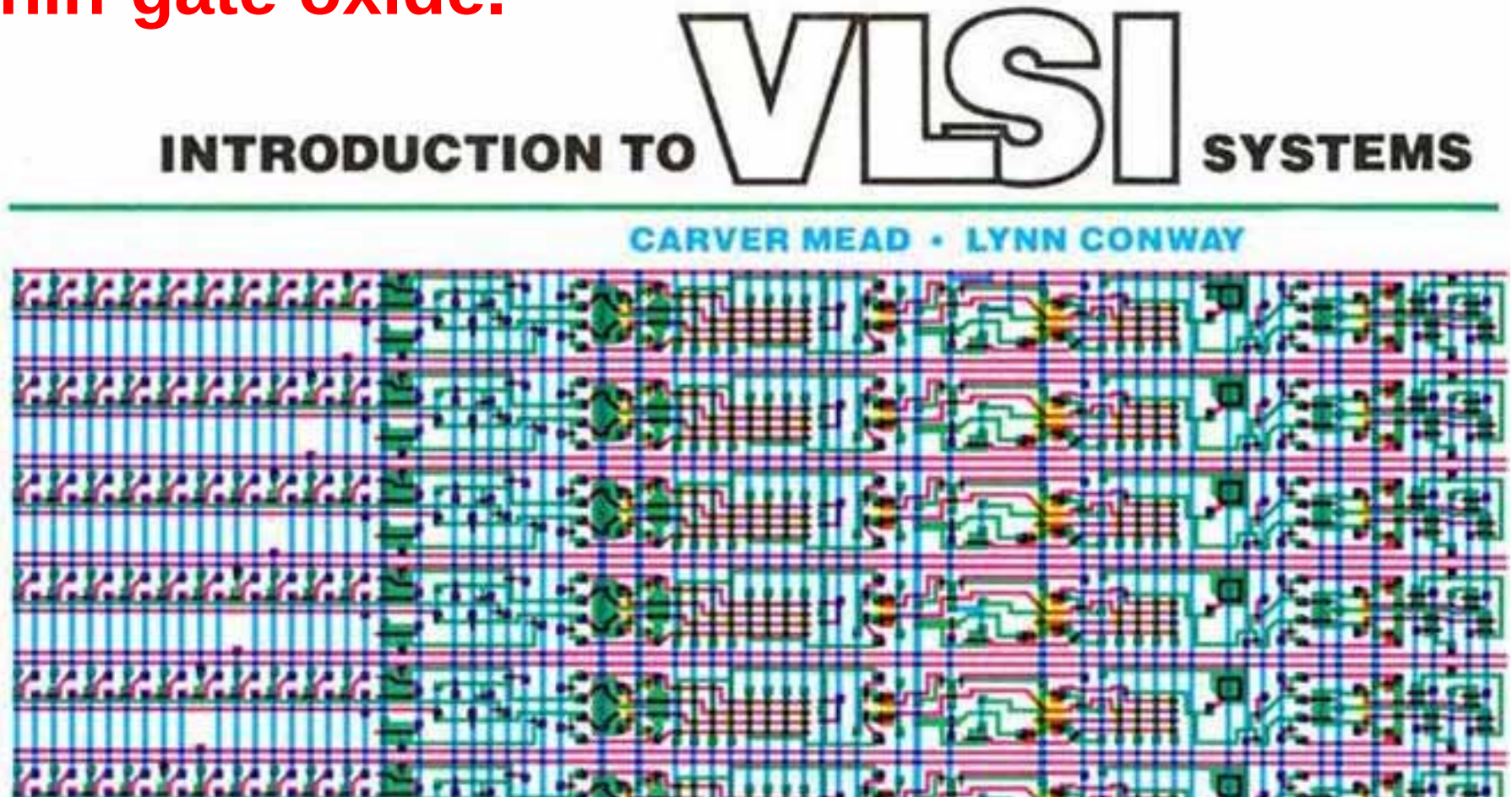
MOSFET gate oxide thickness trend



EOT: Equivalent Oxide Thickness to that of SiO2

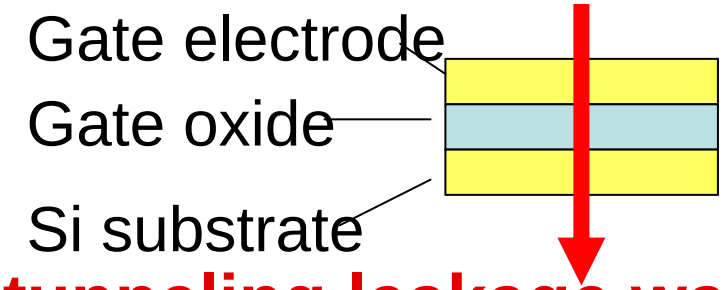
B. H. Lee et al., materials today (2006)

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.



VLSI textbook

Finally, there appears to be a fundamental limit [10] of approximately quarter micron channel length, where certain physical effects such as the tunneling through the gate oxide and fluctuations in the positions of impurities in the depletion layers begin to make the devices of smaller dimension unworkable.

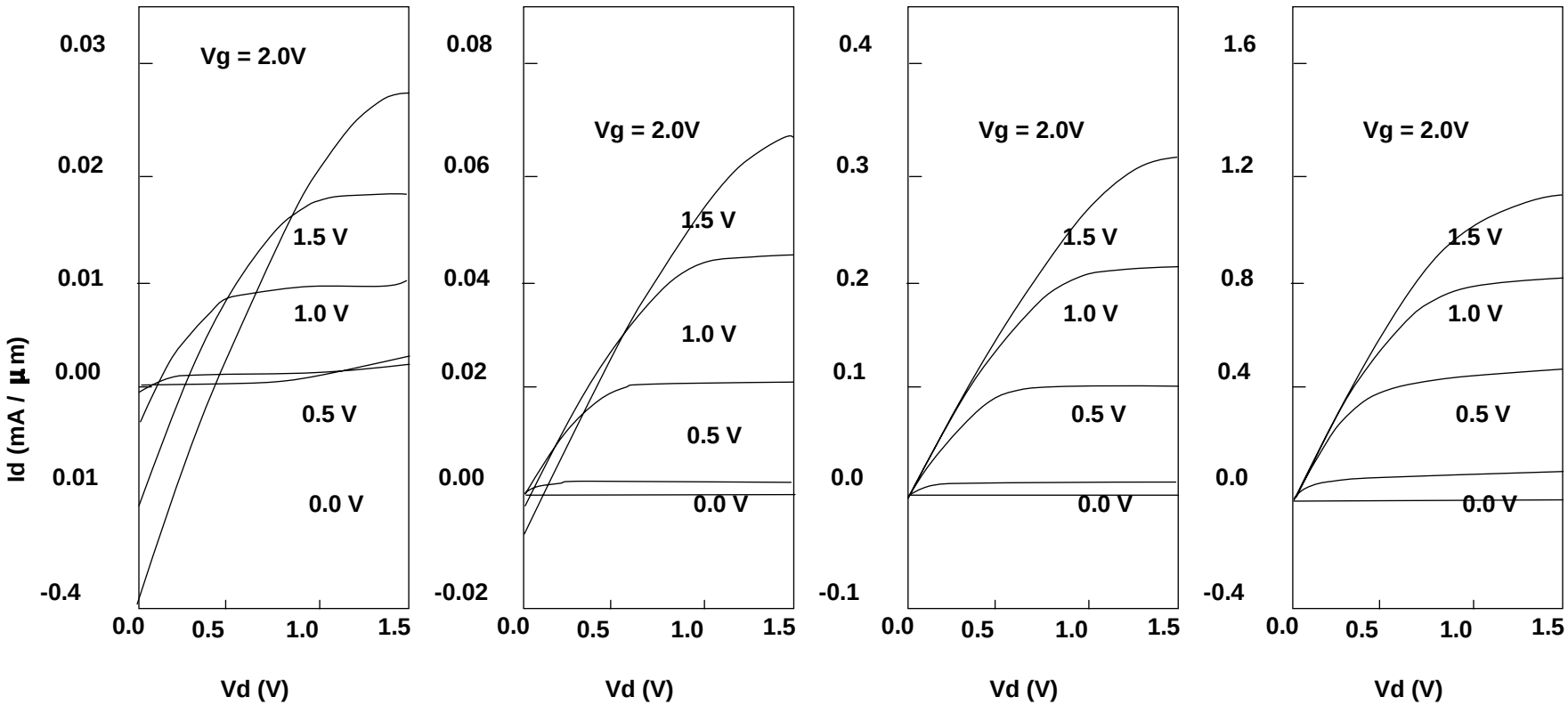


Direct tunneling leakage current start to flow when the thickness is 3 nm.

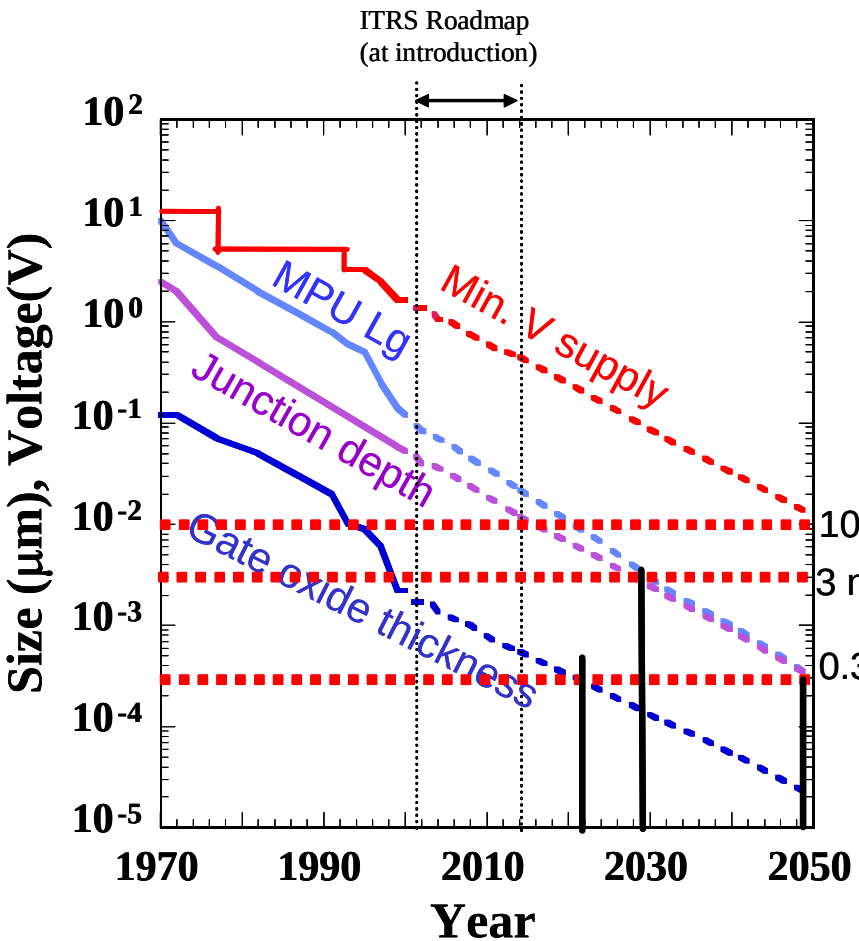
Direct tunneling leakage was found to be OK! In 1994!

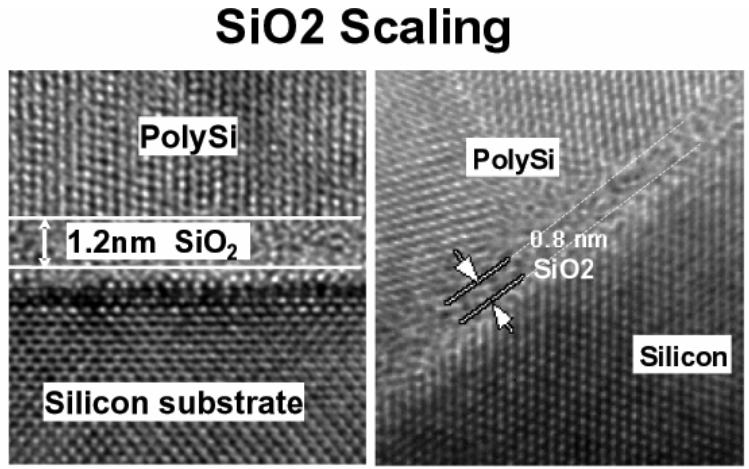
MOSFETs with 1.5 nm gate oxide

Lg = 10 μm Lg = 5 μm Lg = 1.0 μm Lg = 0.1μm



Scaling Limit in MOSFET



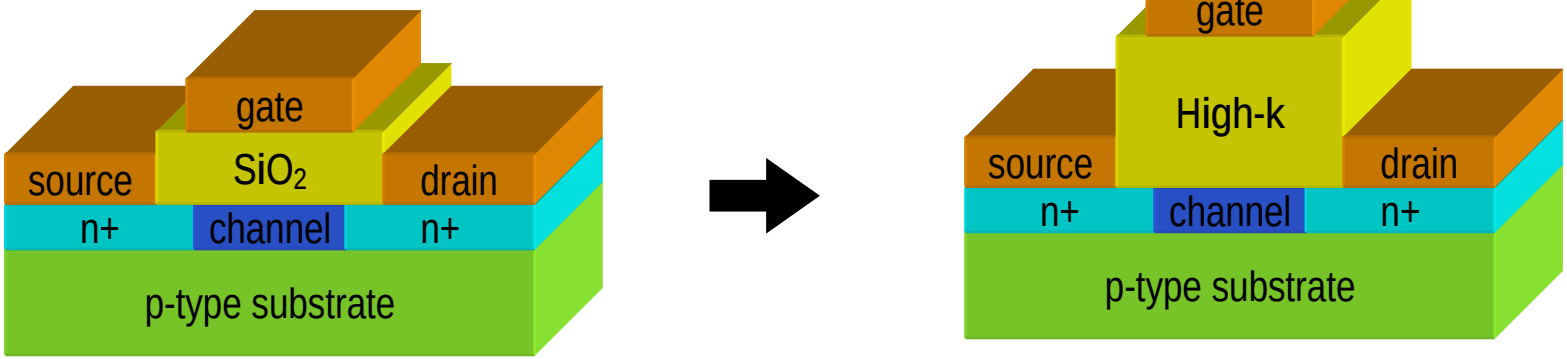


- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

High-k Thin Film for Gate Insulator

MOSFET



	2005	2007	2009	2011
Physical Gate Length (nm)	**32**	**25**	**20**	**16**
Equivalent Oxide Thickness (nm)	**1.2**	**1.1**	**0.9**	**0.5, 0.8(DG)**

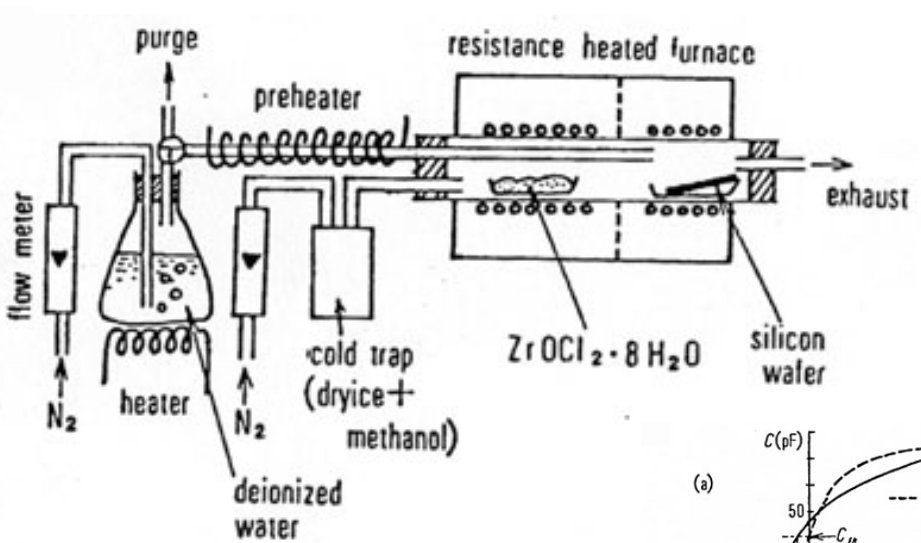
ITRS 2006

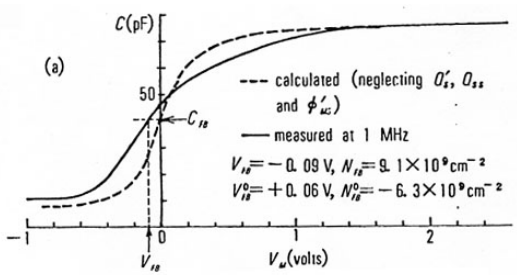
Example of old days: ZrO_2 MOSFETs (1969-70)

PROCEEDINGS OF THE 1ST CONFERENCE ON SOLID STATE DEVICES, TOKYO, 1969
SUPPLEMENT TO THE JOURNAL OF THE JAPAN SOCIETY OF APPLIED PHYSICS VOL. 39, 1970

6-1 ***Low Temperature Vapor Deposition of ZrO_2 Films on Si Surfaces***

Koitiro HOH and Takuo SUGANO
Department of Electronics Engineering,
Faculty of Engineering,
University of Tokyo,





東京大学工学部附属総合試験所
年報 第29巻 (1970)
原稿受付 45年7月1日

ZrO_2/Si 構造の界面キャリヤ移動度と
これを用いた N チャネル・エンハンスメント型 FET*

菅野卓雄** 鳳 紘一郎***

ZrO_2/Si STRUCTURE-- INTERFACE CARRIER MOBILITY AND APPLICATION TO THE N-CHANNEL ENHANCEMENT MODE FET

TAKUO SUGANO** AND KOITIRO HOH***

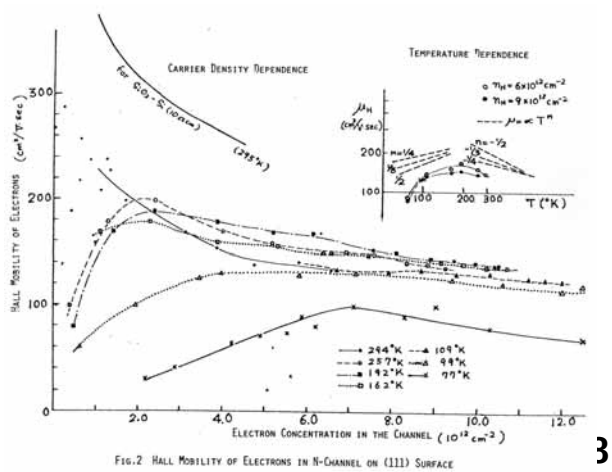
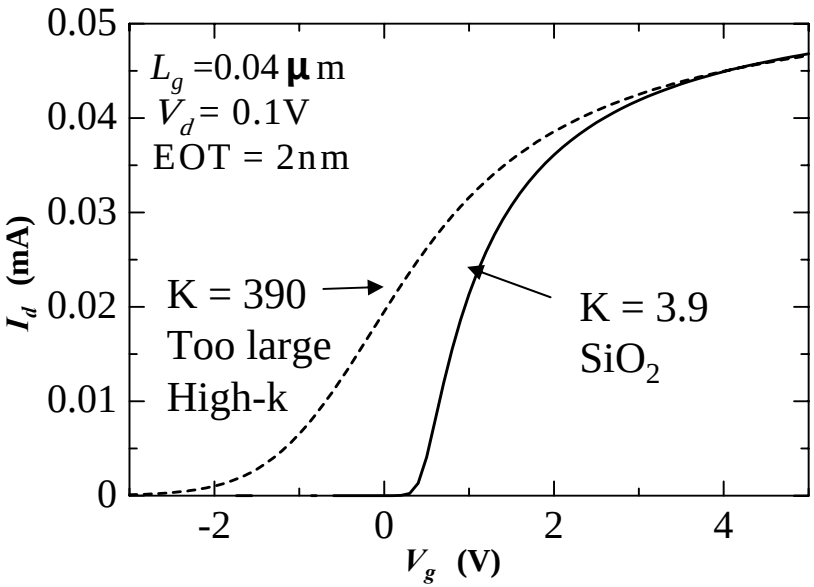
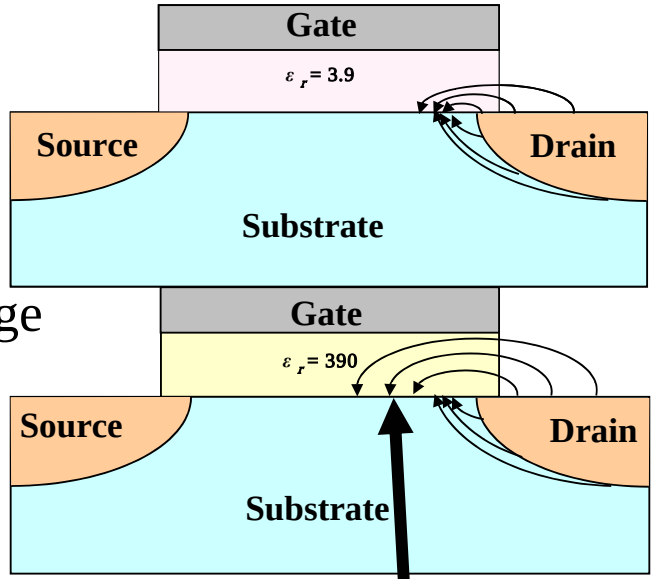


FIG. 2 HALL MOBILITY OF ELECTRONS IN N-CHANNEL ON (111) SURFACE

Too large high-k cause significant short channel effect

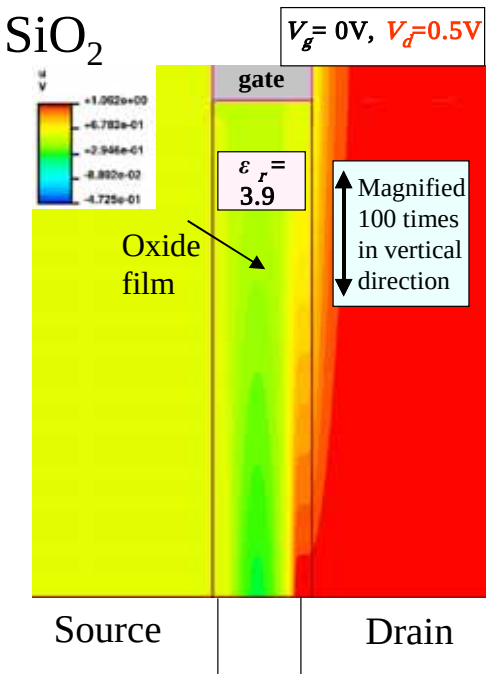


SiO_2

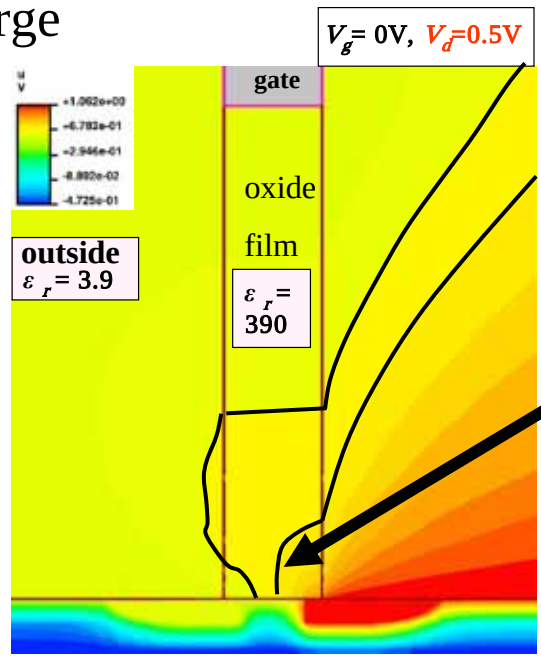


Too large high-k

SiO_2

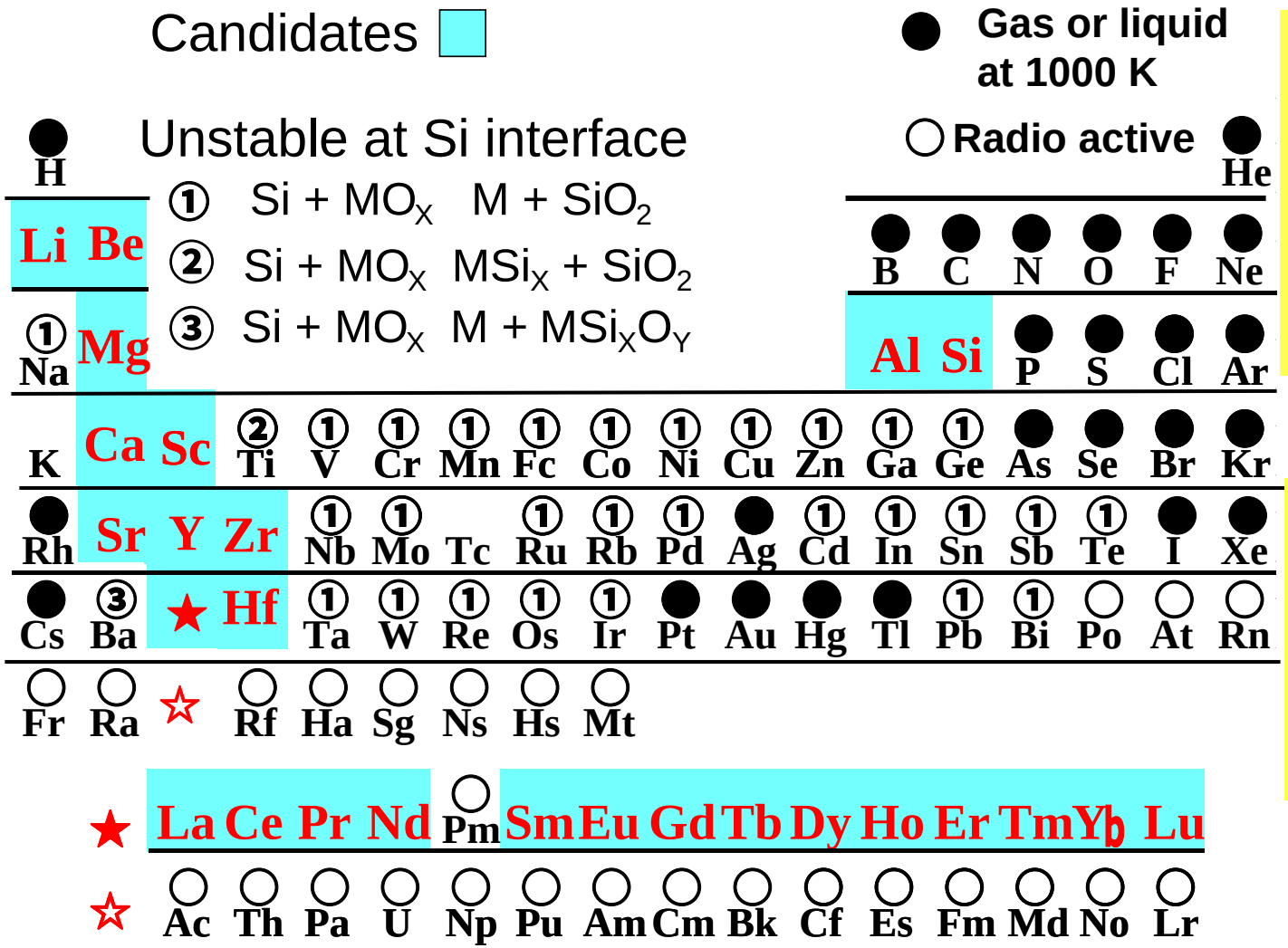


Too large high-k



Penetration of lateral field from Drain through high-k causes significant short channel effects

Choice of High-k

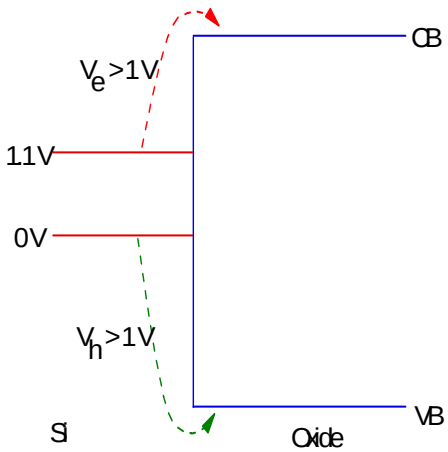


HfO_2 based dielectrics are selected as the first generation materials, because of their merit in
1) band-offset,
2) dielectric constant
3) thermal stability

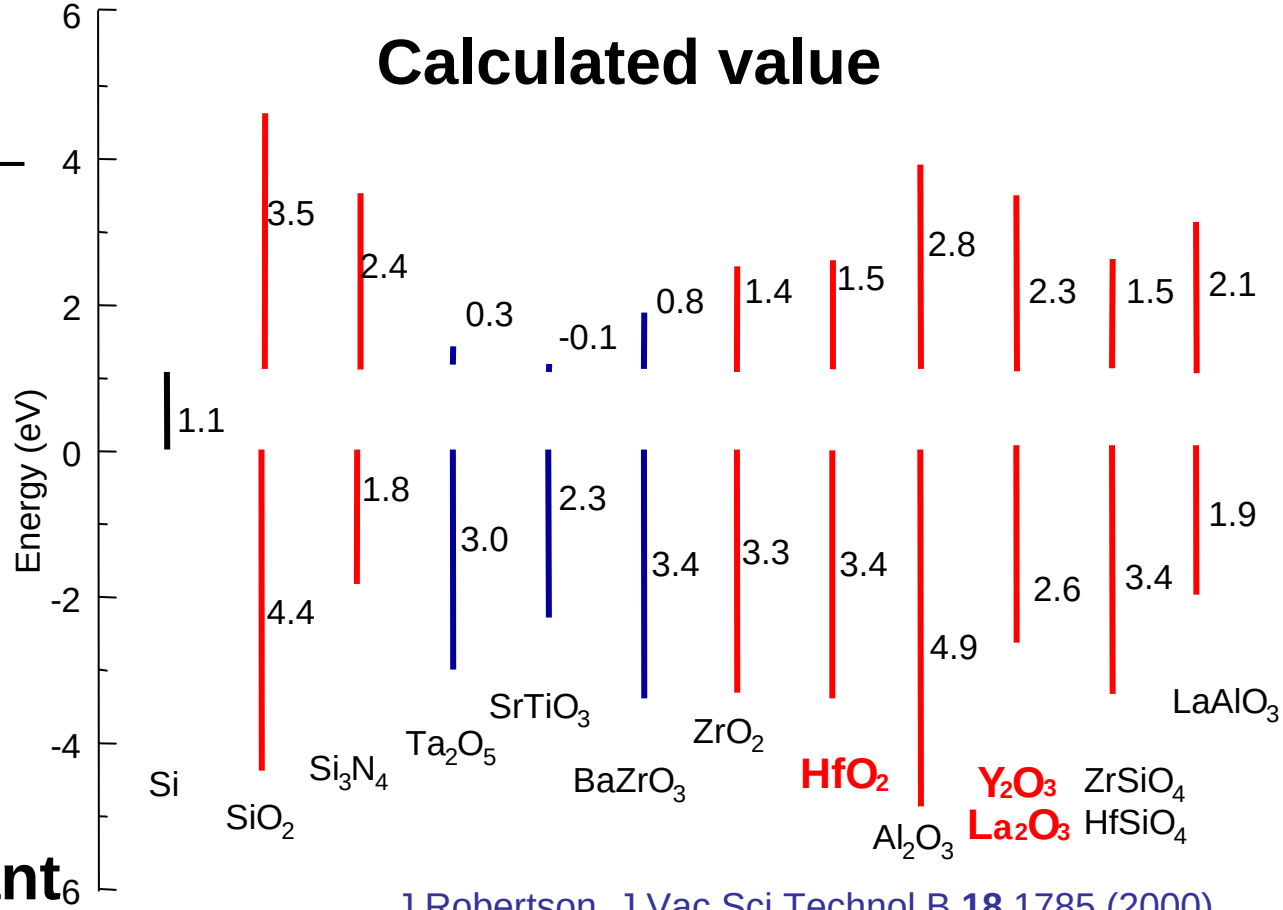
La_2O_3 based dielectrics are thought to be the next generation materials, which may not need a thicker interfacial layer

R. Hauser, IEDM Short Course, 1999
Hubbard and Schlom, J Mater Res 11 2757 (1996)

Band Offsets



Dielectric constant



J Robertson, J Vac Sci Technol B **18** 1785 (2000)

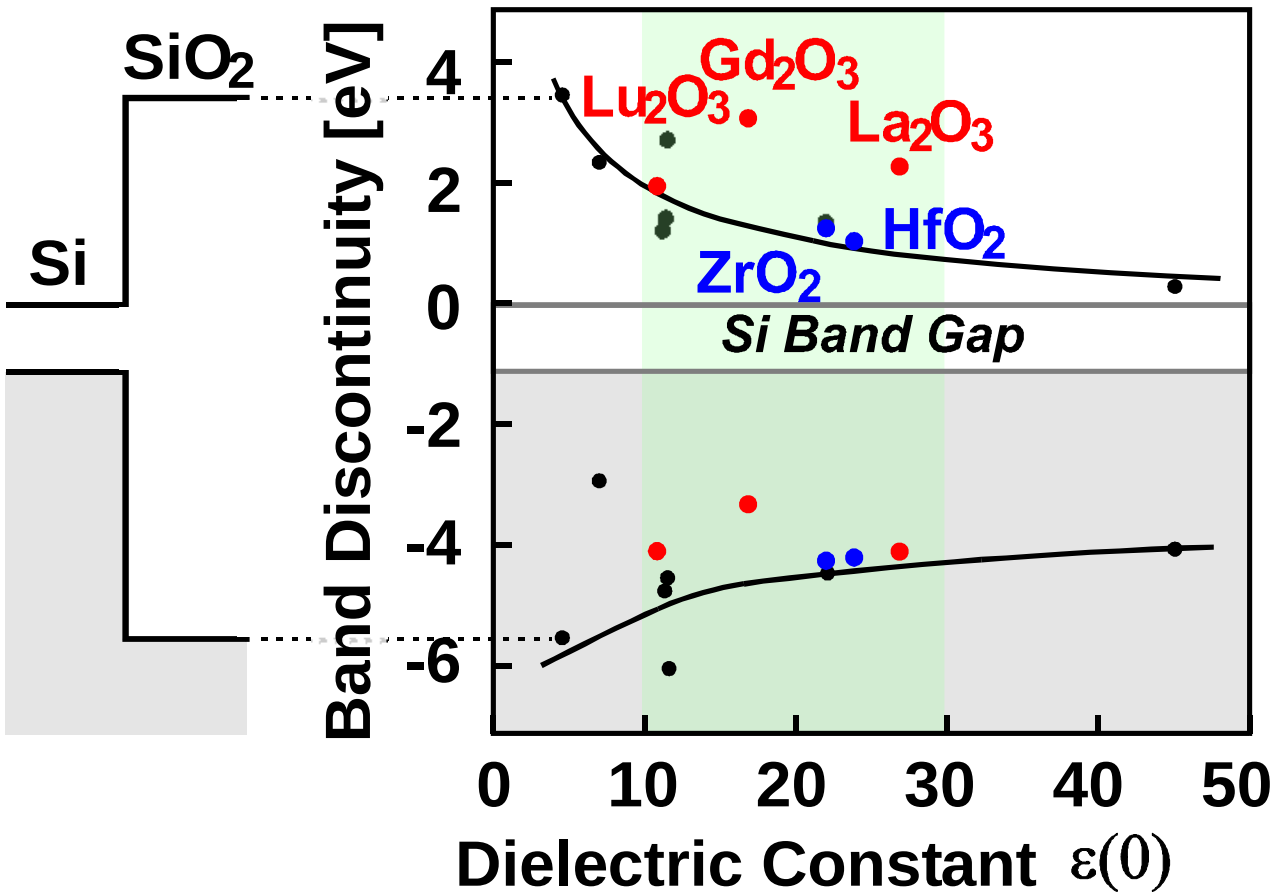
SiO2; 4
Si3N4: ~ 7
Al2O3: ~ 9

Y2O3; ~10
Gd2O3: ~10

HfO2; ~23
La2O3: ~27

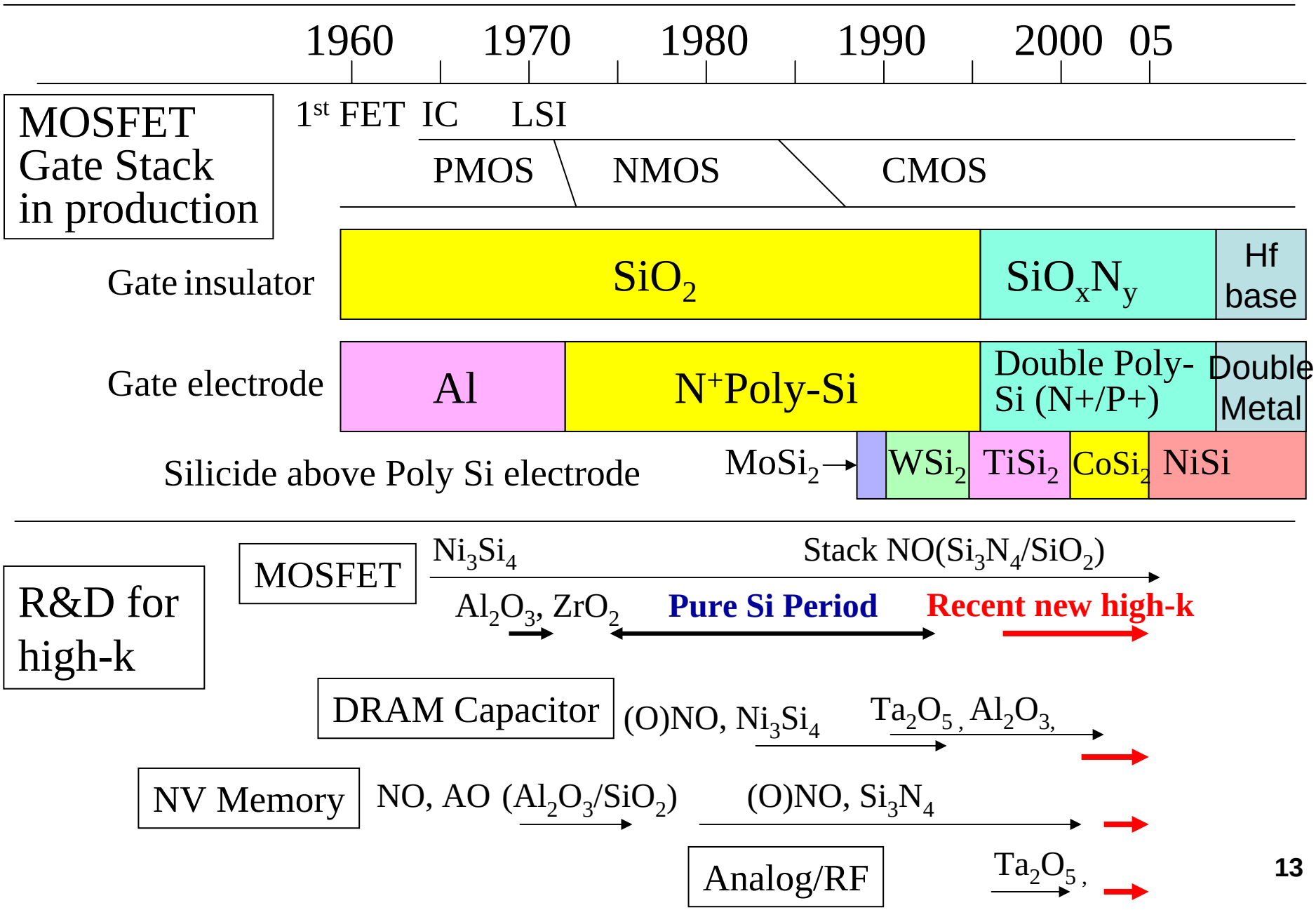
HfO2 was chosen for the 1st generation
La2O3 is more difficult material to treat

Energy Barrier Offset of La2O3



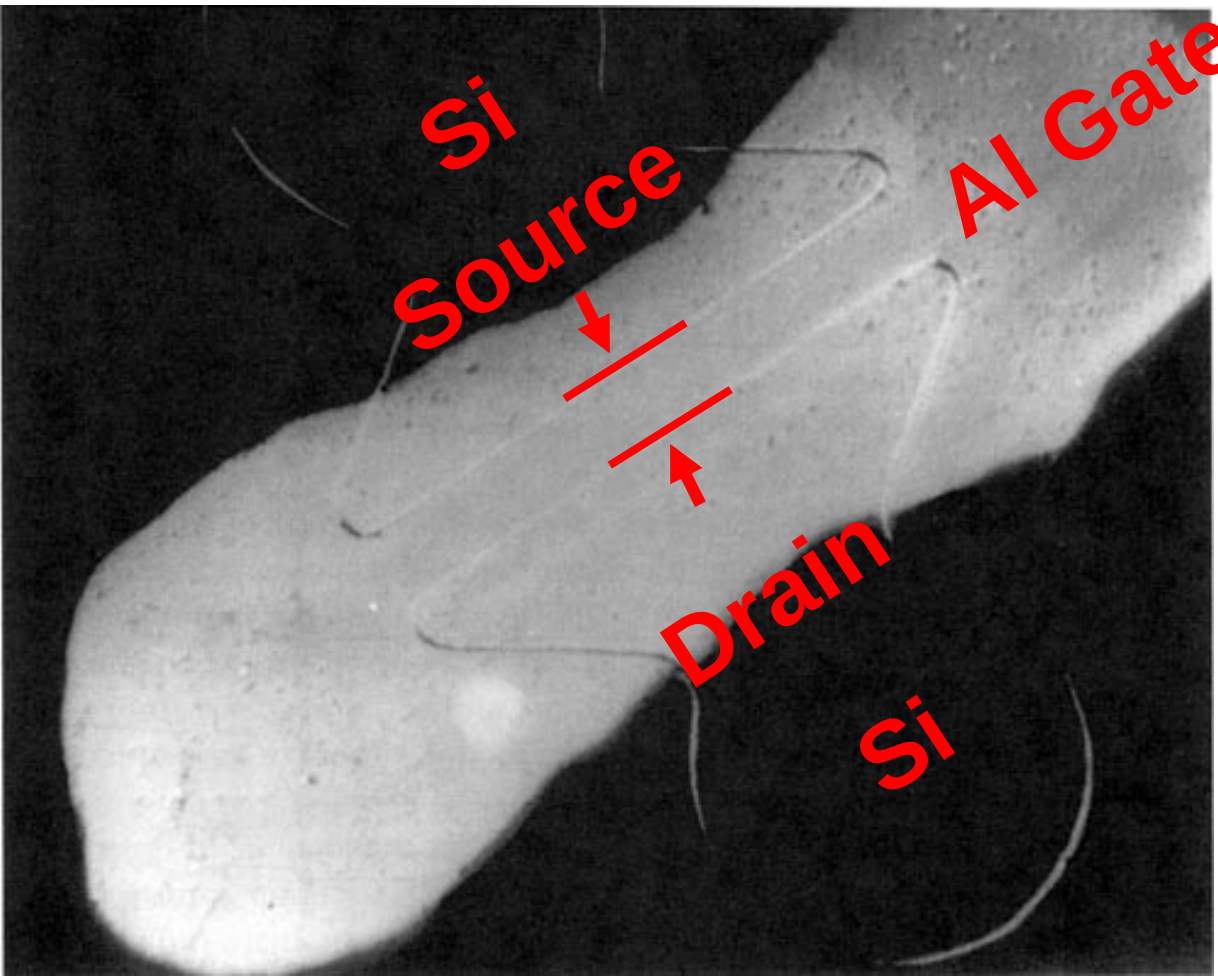
XPS measurement by Prof. T. Hattori, INFOS 2003

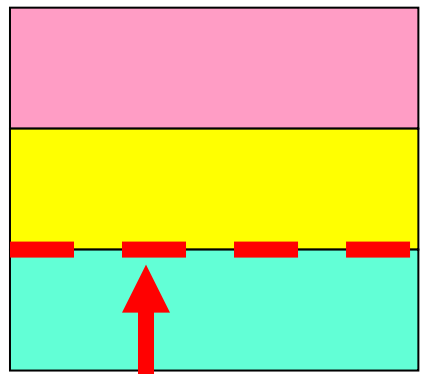
Historical trend of high-k R& D



1960: First MOSFET
by D. Kahng and M. Atalla

Top View





Exceptionally good interface

Overview of Recent High-k gate stack development

98 99 00 01 02 03 04 05

mainstream

ZrO_2 / HfO_2

HfO_2 / $HfSi_xO_y$ / $HfAl_x(Si_y)O_z$

$HfSi_xO_xN_y$ /$HfAl_x$ (Si_y) O_z with IL (Interfacial Layer)

Many problems were found
1)interfacial layer growth
2)phase separation
3)mobility degradation
4)non-uniformity of the film
5)boron penetration, others

Fermi-Level Pinning was recognized

IL and Metal gate are desirable for
1)mobility
2)FLP
3)poly depletion

FUSI / (DM) gate electrode

Problems for LSTP (Low Standby Power) will be somehow manageable with $HfN_xSi_xO_y$ and FUSI, for example

2D Device simulation for short channel MOSFETs

k value should not be too high for suppressing the SHE;
k is possibly less than 50

DM (Dual –metal) gate

HP (High performance) application is not near

Ta_2O_5 / TiO_2

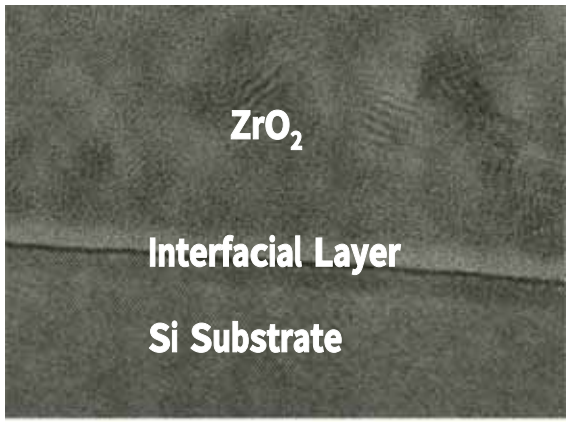
Low band offset for CB is a problem

Lanthanides (La_2O_3 etc. for next generation)

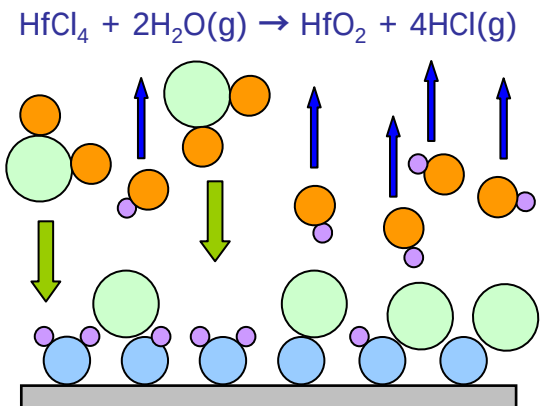
Importance of next regeneration materials is re-recognized because of the possible limitation of thinning HfO_2 type oxides for further 2-3 generations

Problems for high-k in early 2000s

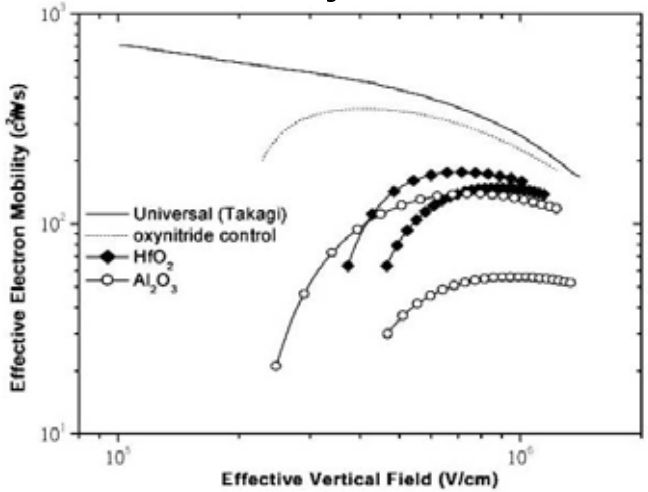
1) Interfacial layer formation
2) Micro crystal growth
3) Lateral oxidation at gate edge
4) Boron penetration



5) Contamination from precursor
6) Non-uniformity and defect

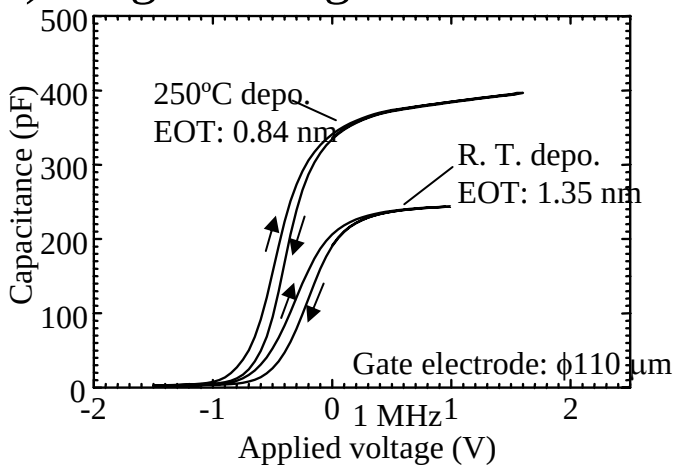


7) Lower mobility



E.P Gusev et al., IEDM Tech. Dig., pp.451-454, 2001

8) Flatband voltage shift
9) Large fixed charge, interface states density
10) Larger leakage current than expected



Intel’s announcement, January 26, 2007, and IEDM Dec 2007

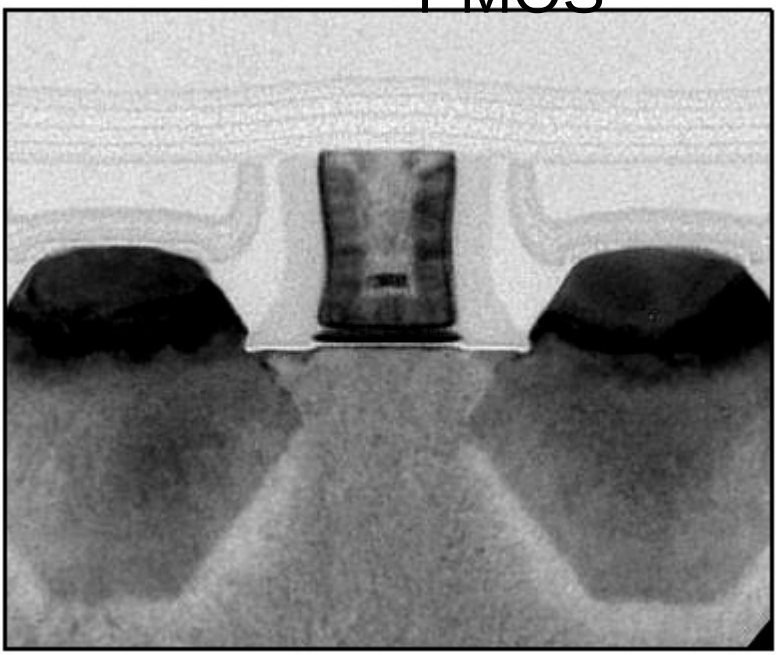
Hafnium-based high-k material by ALD: EOT= 1nm
Specific gate metals (Intel’s trade secret)
    Different Metals for NMOS and PMOS
Use of 193nm dry lithography

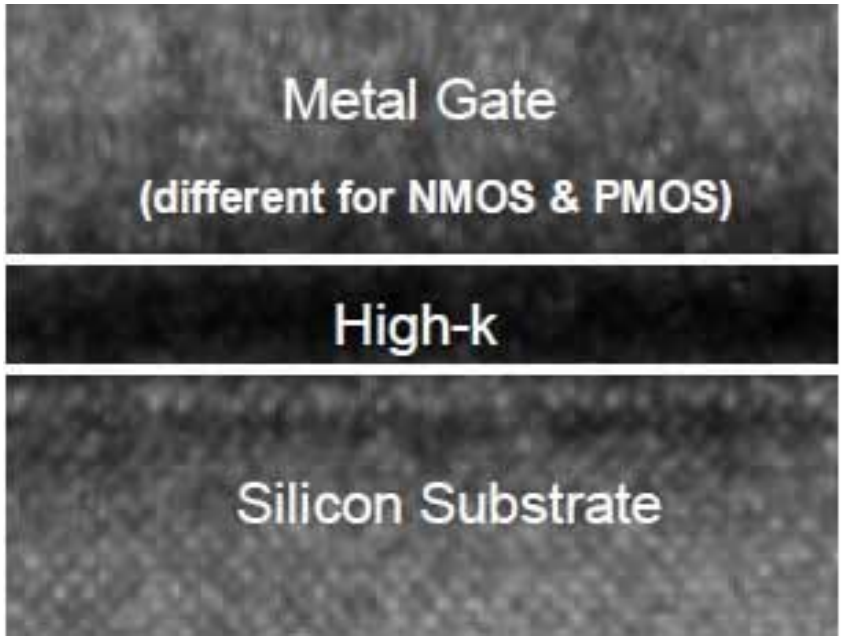
From 65 nm to 45 nm Tech.
    Tr density: 2 times increase
    Tr switching power: 30% reduction
    Tr switching speed: 20% improvement
    S-D leakage power: 5 times reduction
    Gate oxide leakage: 10 times reduction

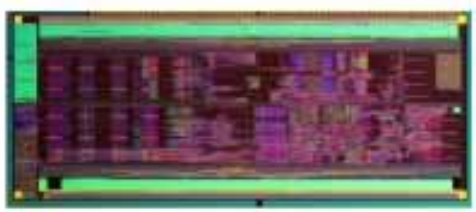
45nm processors (Core™2 family processors "Penryn") running Windows* Vista*, Linux* etc.

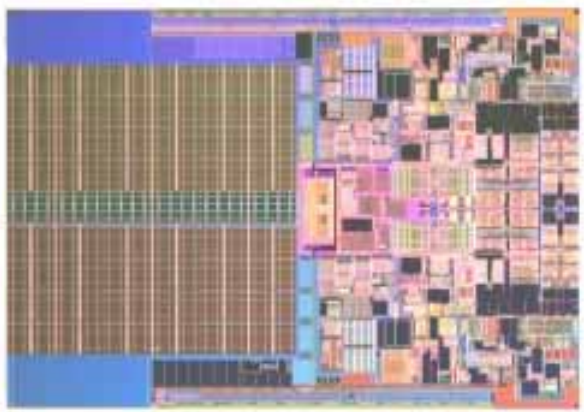
45nm production in the second half of 2007

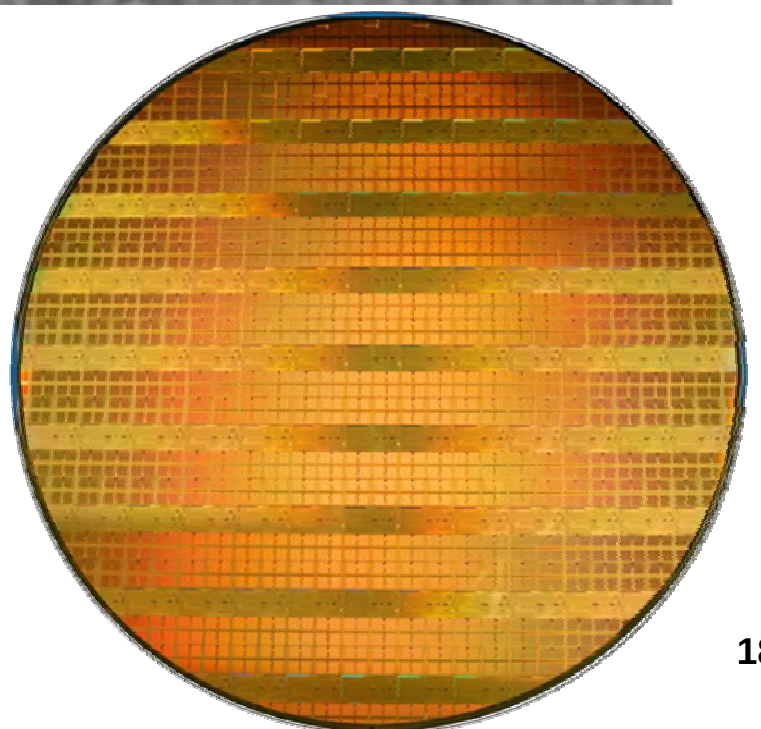
PMOS




Metal Gate
(different for NMOS & PMOS)
High-k
Silicon Substrate







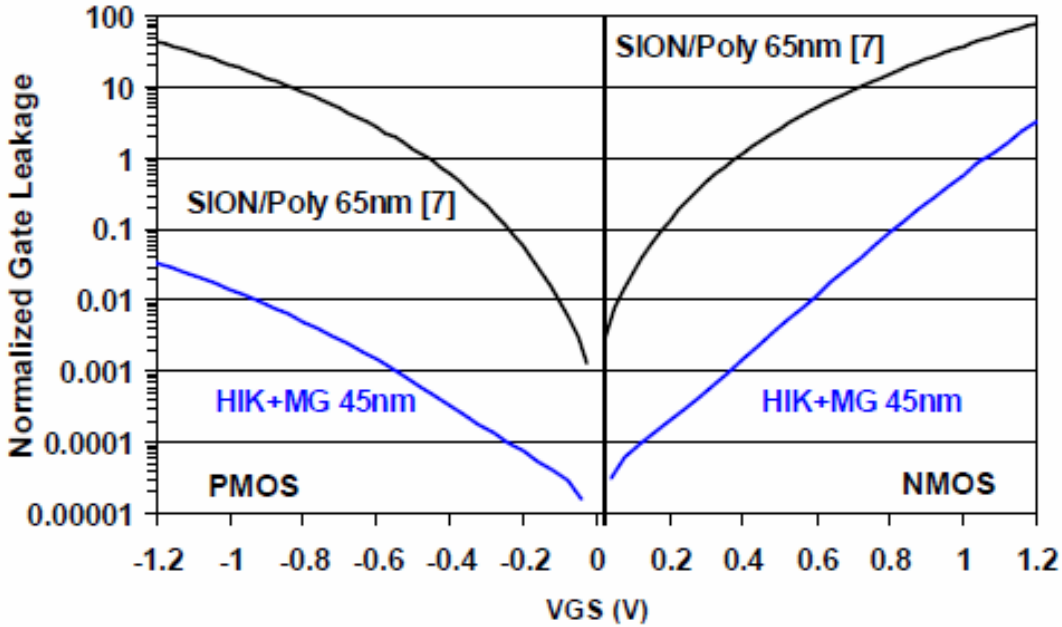
Intel's 45nm Manufacturing

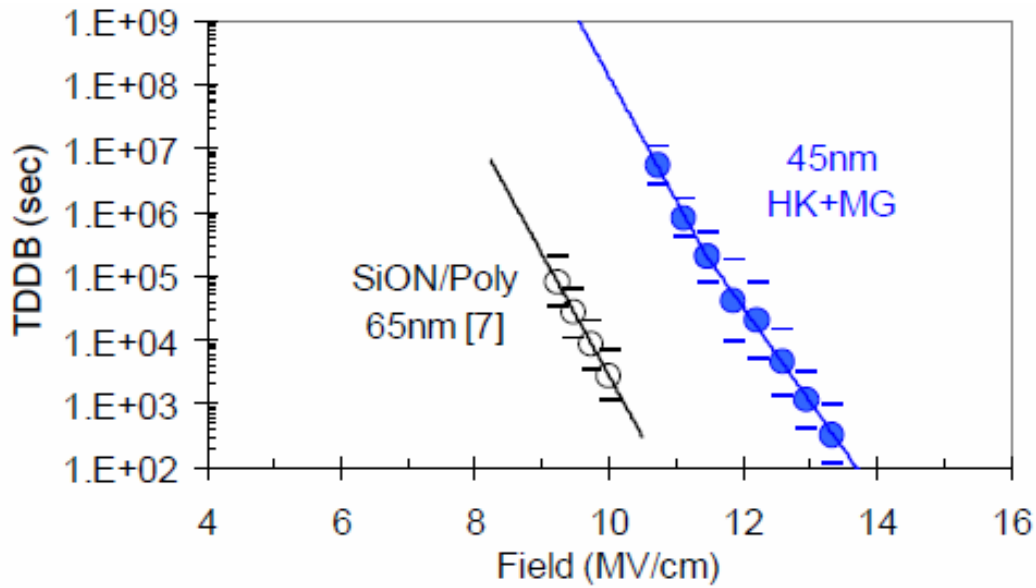
Intel's is currently developing its 45nm process on 300mm wafers in Hillsboro, Oregon, in D1D, a fab with clean-room space equivalent to 3.5 football fields.

Two new 300mm fabs are being built for the coming 45nm ramp: Fab 32 in Ocotillo, Arizona (production due to start in the second half of 2007) and Fab 28 in Israel (production to start in the first half of 2008).

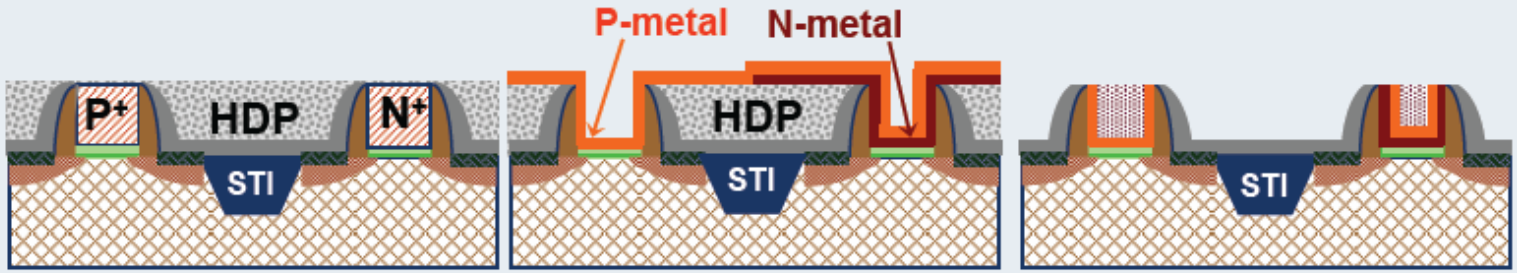
Construction is underway on Intel's 300mm Fab 32 in Chandler, Ariz., one of three Intel fabs that will produce leading-edge microprocessors on 45nm process technology

Fab 32 under construction in Ocotillo, AZ.


Normalized Gate Leakage
100
10
1
0.1
0.01
0.001
0.0001
0.00001
SION/Poly 65nm [7]
SION/Poly 65nm [7]
HIK+MG 45nm
HIK+MG 45nm
PMOS
NMOS
-1.2
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
1.2
VGS (V)


TDDB (sec)
1.E+09
1.E+08
1.E+07
1.E+06
1.E+05
1.E+04
1.E+03
1.E+02
45nm
HK+MG
SiON/Poly
65nm [7]
4
6
8
10
12
14
16
Field (MV/cm)

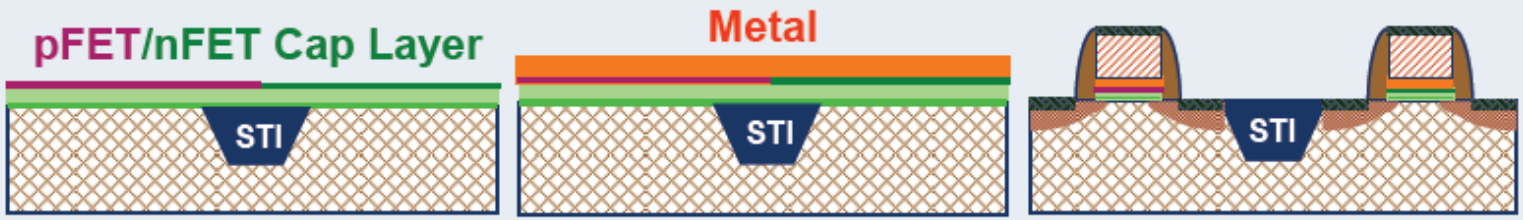
Replacement Metal Gate (Damascene)



Advantages
- Low thermal budget (metal gate deposition after S/D anneals)
- Known metal work function

Challenges
- Cost
- Extendibility to narrower CDs

Gate-First Process



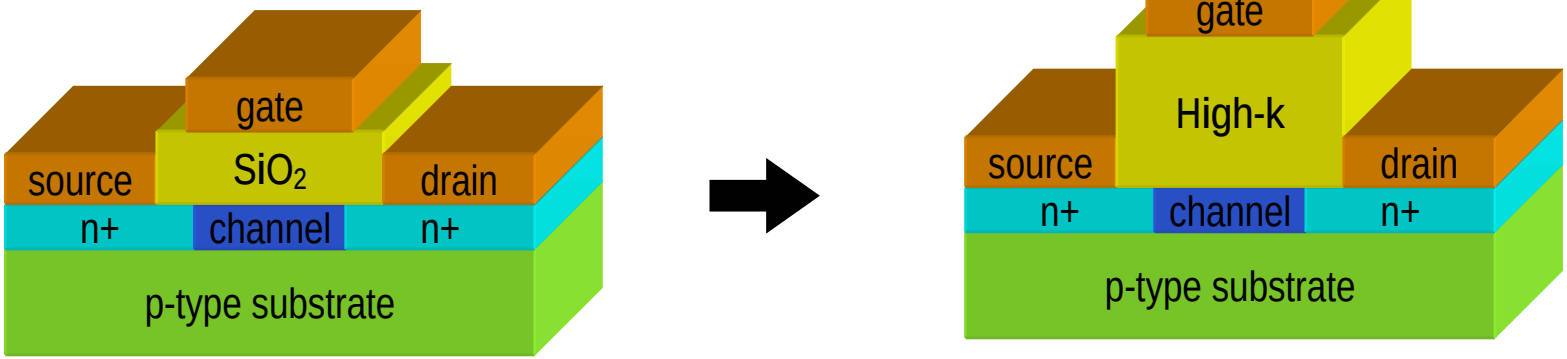
Advantages
- Compatible with high thermal budget process
- Follows standard CMOS flow

Challenges
- NMOS and PMOS cap layer integration is challenging

Reza Arghavani, Ph.D.,Applied Materials ,IEDM 2007 Short Course

High-k Thin Film for Gate Insulator

MOSFET



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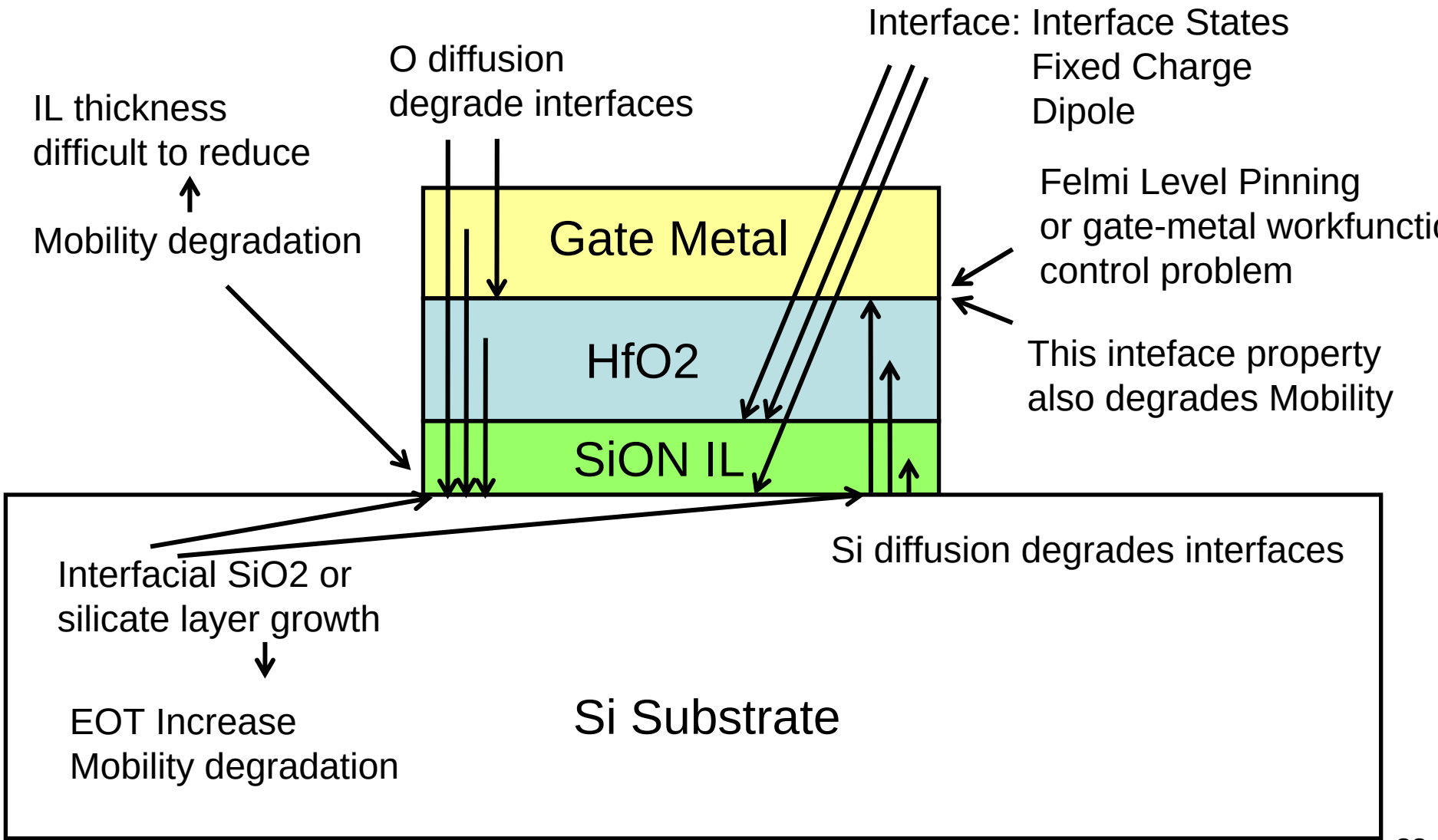
Equivalent Oxide Thickness (nm)	**1.2**	**1.1**	**0.9**	**0.5, 0.8(DG)**

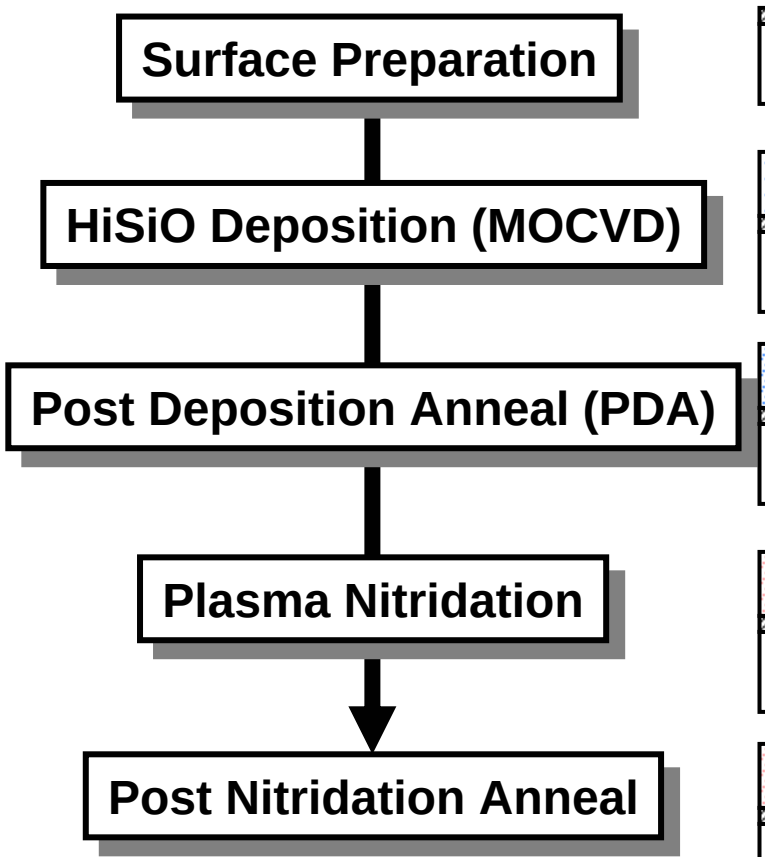
ITRS 2006

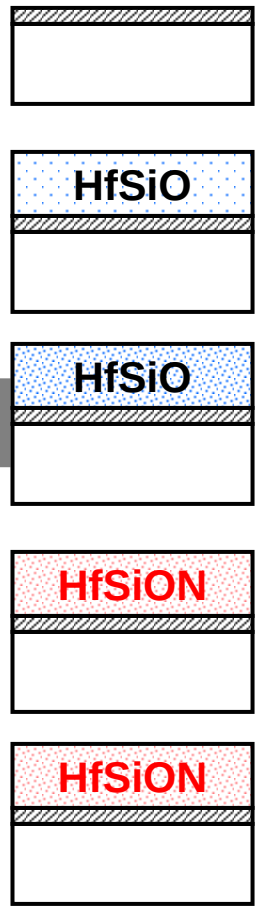
Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT



Typical HfSiON Process Flow

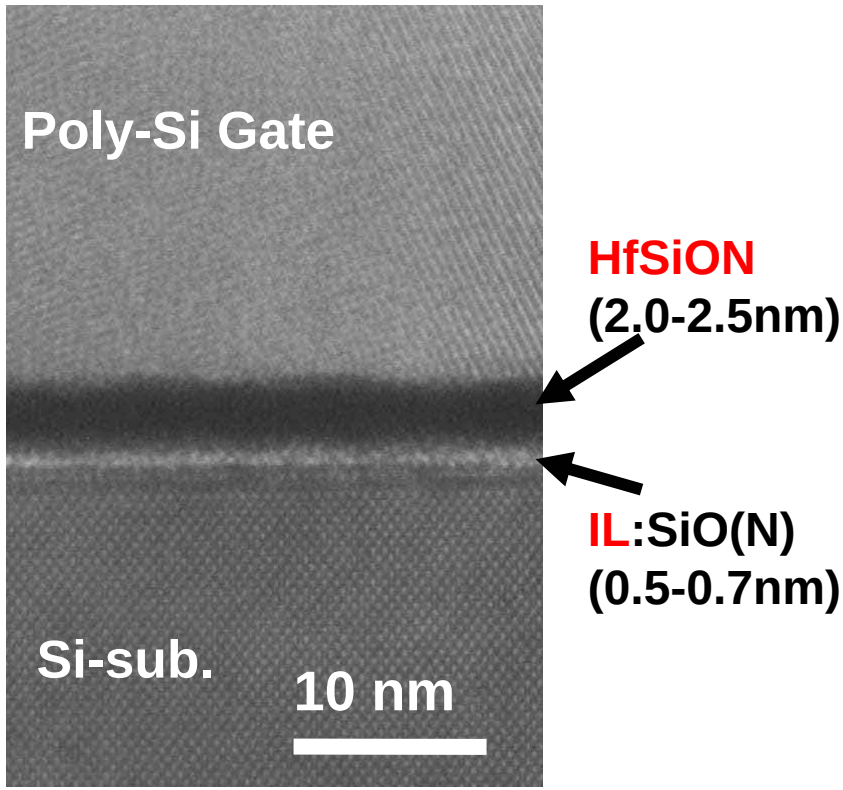




- 0.5~0.7nm of SiO_2 layer
- MOCVD, HfSiO deposition
- Hf concentration (Hf/(Hf+Si)) = 60 %
- Contamination removal & Densification with suppressing phase separation, crystallization, and IL growth
- N incorporation to avoid phase separation, crystallization, and B penetration
- Ar/N2 plasma nitridation
- Plasma damage recovery
- Stabilization of doped N
- High temperature is applicable

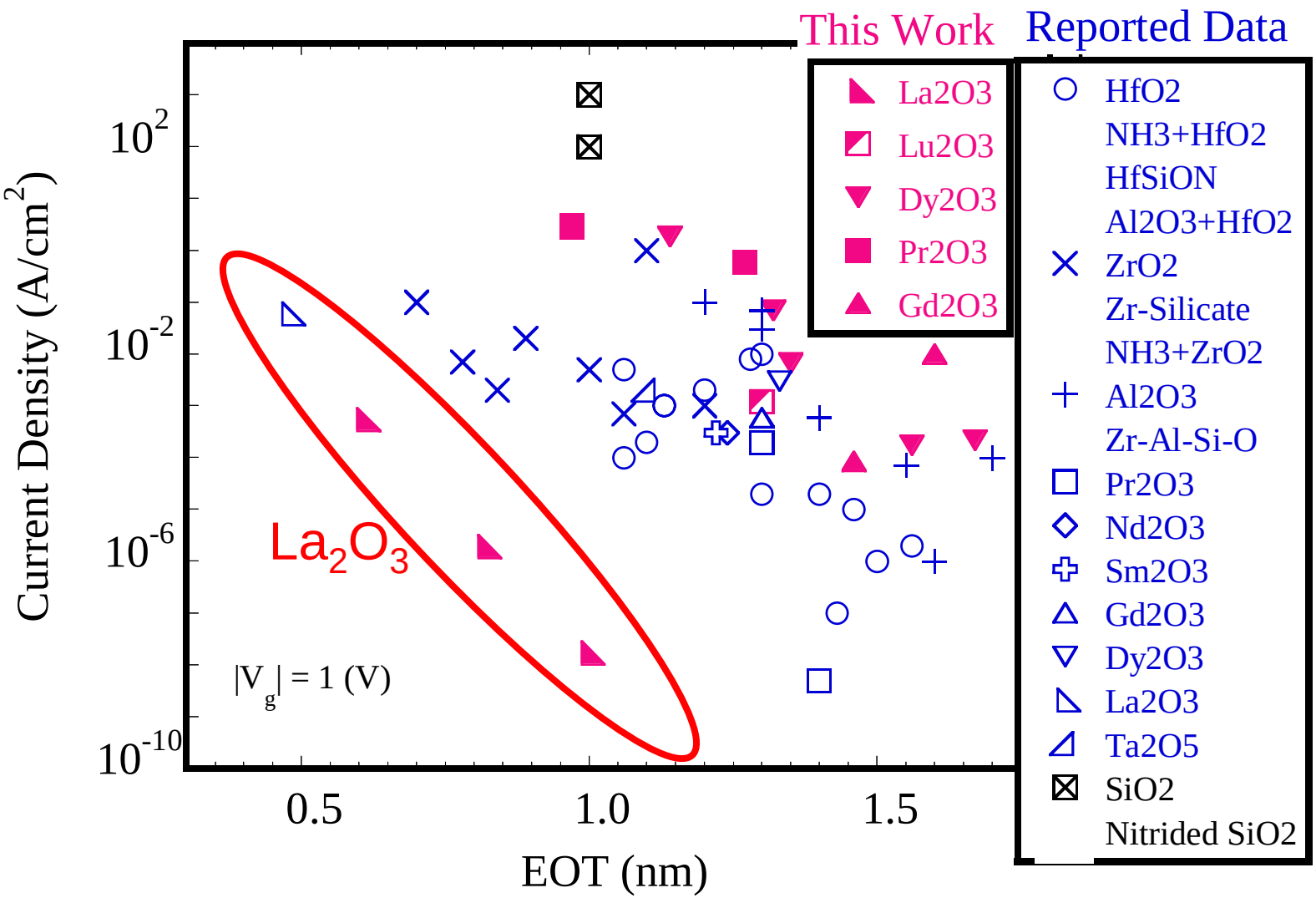
Y. Nara, Selete

Typical IL (Interfacial Layer)



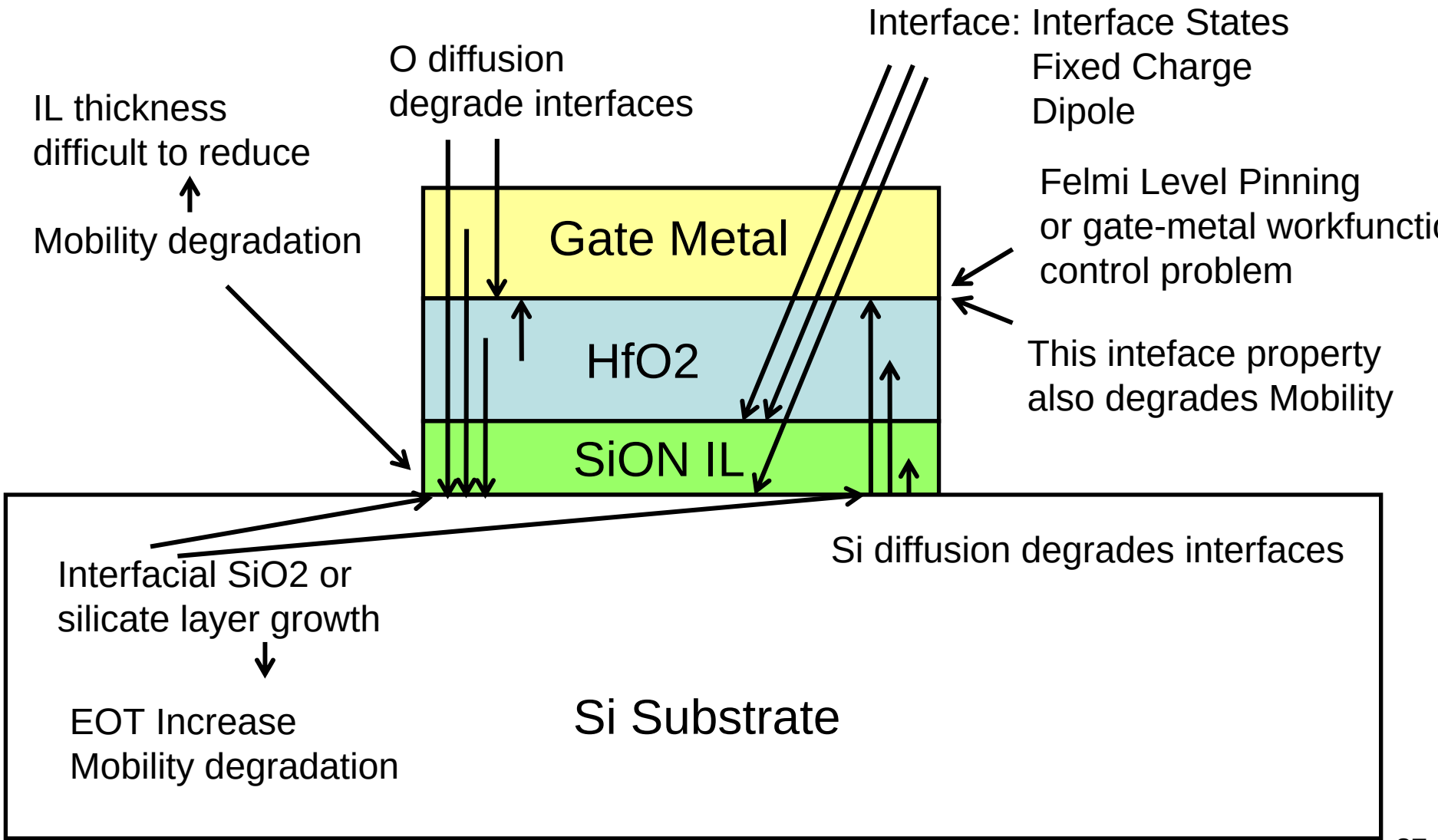
Y. Nara, Selete

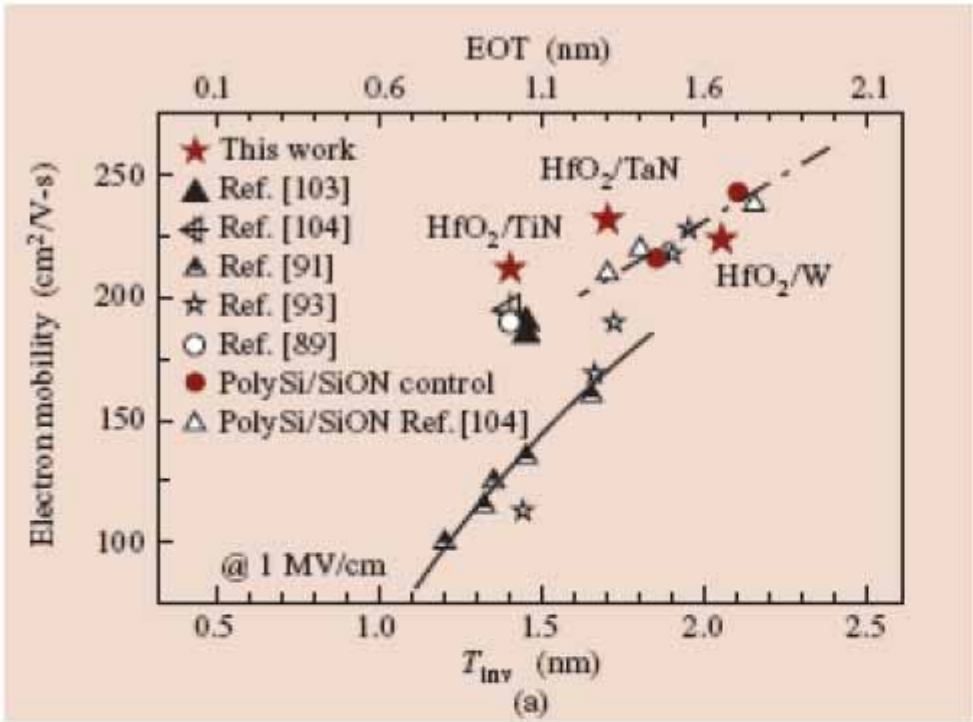
Low Gate Leakage Current with La_2O_3

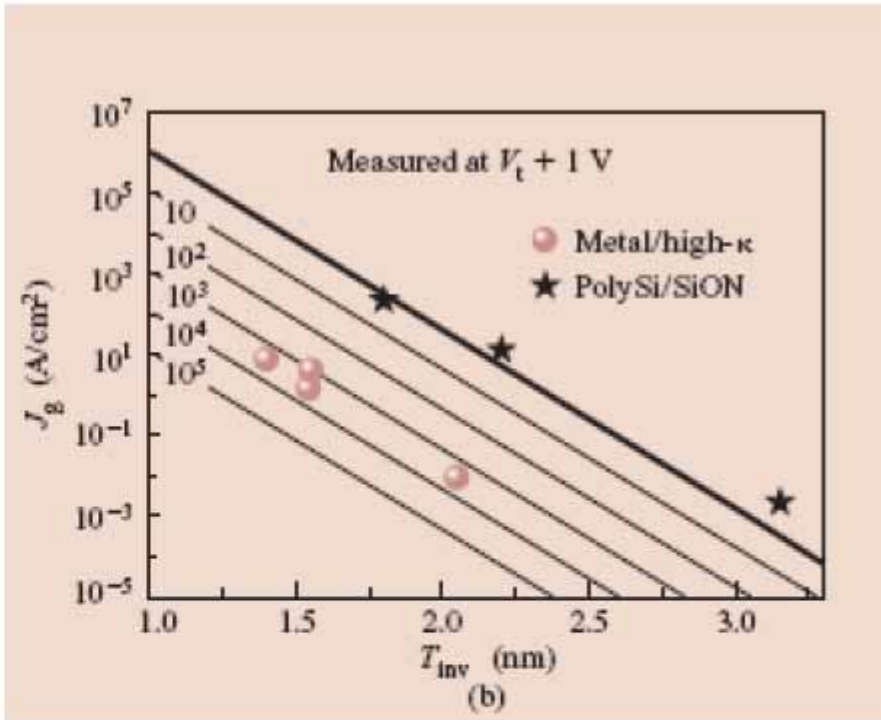


Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT







PVD TiN, ALD TaN, CVD W on High-k:

- 4-5 Orders Magnitude Improvement in Gate Leakage
- Equivalent Electron Mobility as that of Oxynitride

Source: E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006

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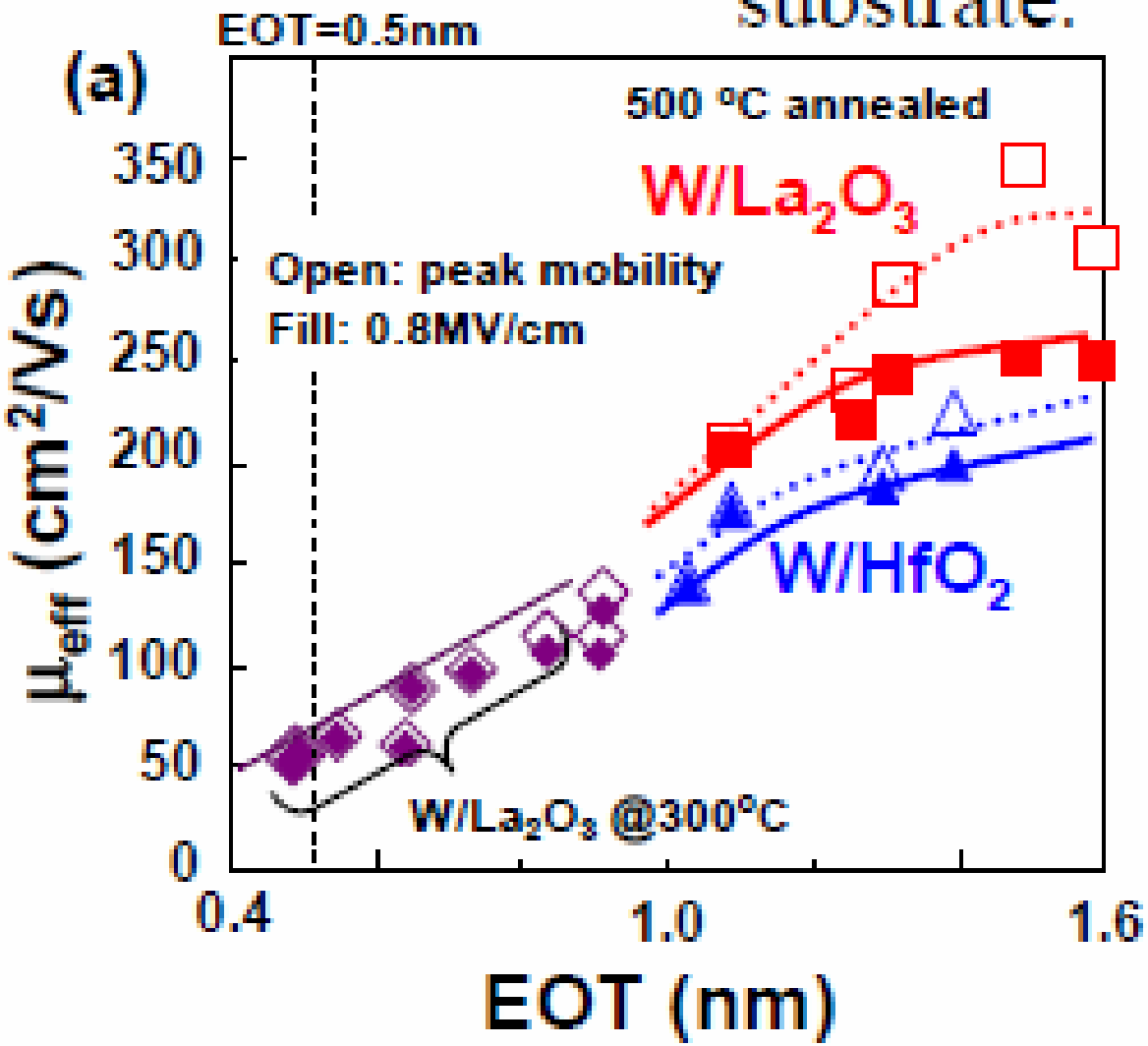
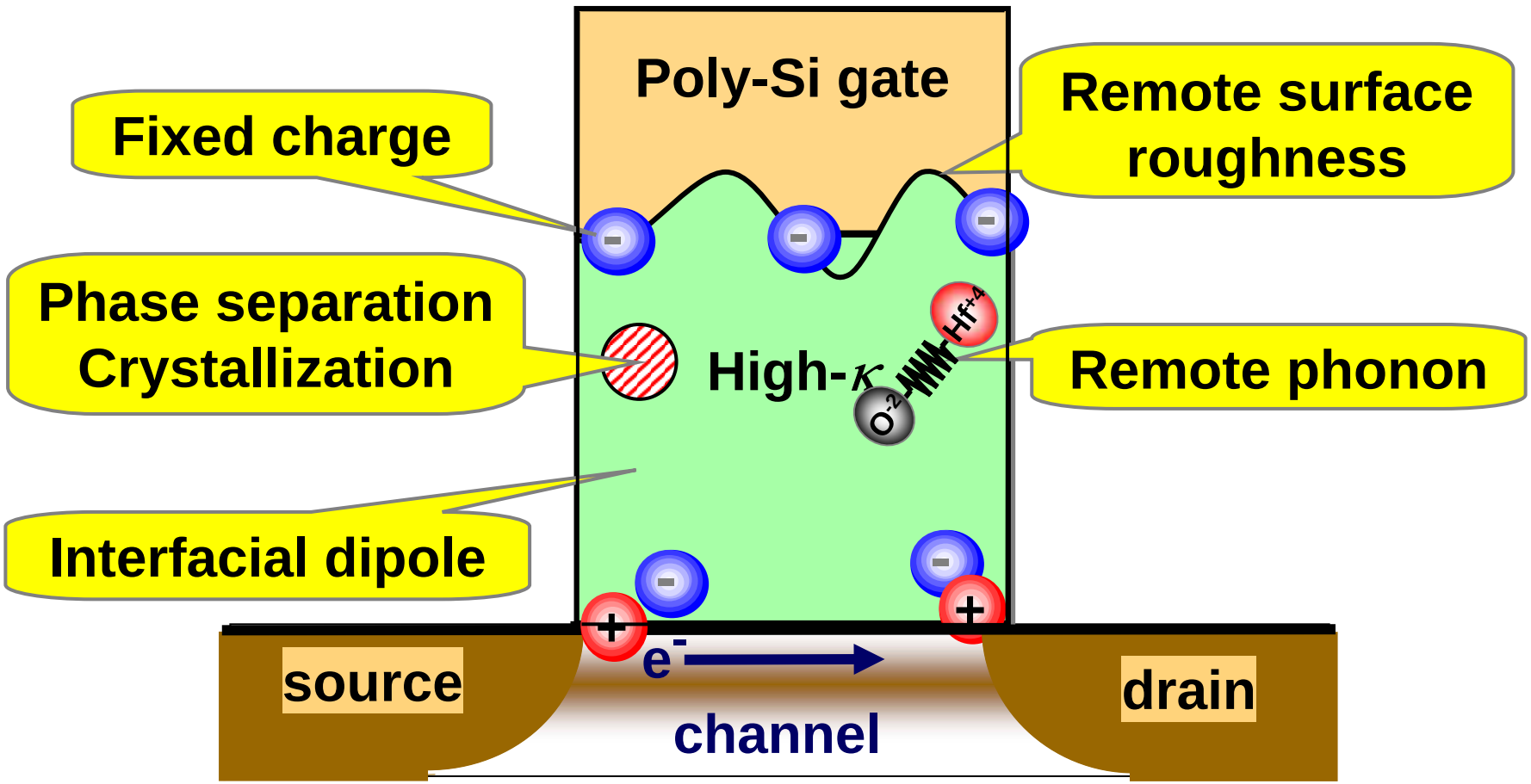
substrate.


EOT=0.5nm
(a)
500 °C annealed
W/La2O3
Open: peak mobility
Fill: 0.8MV/cm
W/HfO2
W/La2O3 @300°C
μeff (cm2/Vs)
350
300
250
200
150
100
50
0
0.4
1.0
1.6
EOT (nm)

Mobility degradation causes for High-k MOSFETs (HfO_2, Al_2O_3 based oxide)

Remote scattering is dominant



S. Saito et al., IEDM 2003,
S. Saito et al., ECS Symp. on ULSI Process Integration

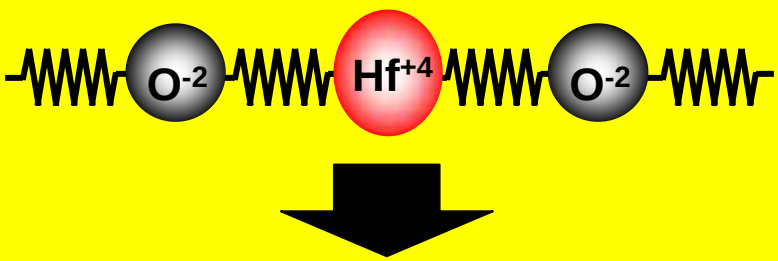
Which is dominant?

RCS (Remote Charge Scattering)?
RPS (Remote Phonon scattering)?

RPS (Remote Phonon scattering)

M. V. Fischetti, *et al.*, JAP (2001).

Origin of high-κ :
large ionic polarizabitily



Strong electron-phonon interaction

From the comparison
Of simulation and
experiments, RCS is much
dominant

Saito, ECS Sypm. On ULSI
Process Integration 2004,

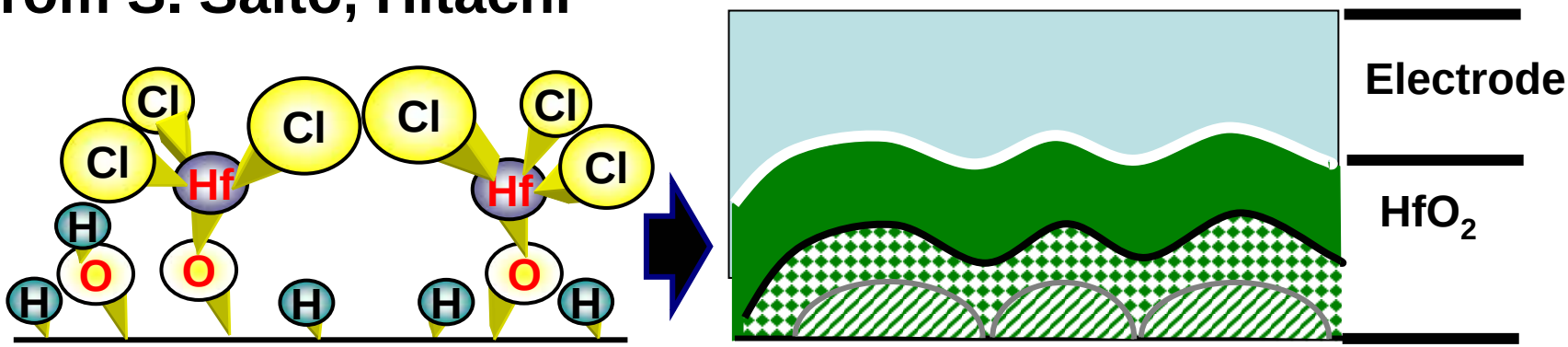
L.A. Rangnarsson, IEDM 2003

O. Weber, IEDM 2004

S. Saito, Hitachi

Remote surface roughness effect

From S. Saito, Hitachi



M. L. Green, *et al.*, JAP (2002).

(1) Induced charge

(2) Induced dipole moment

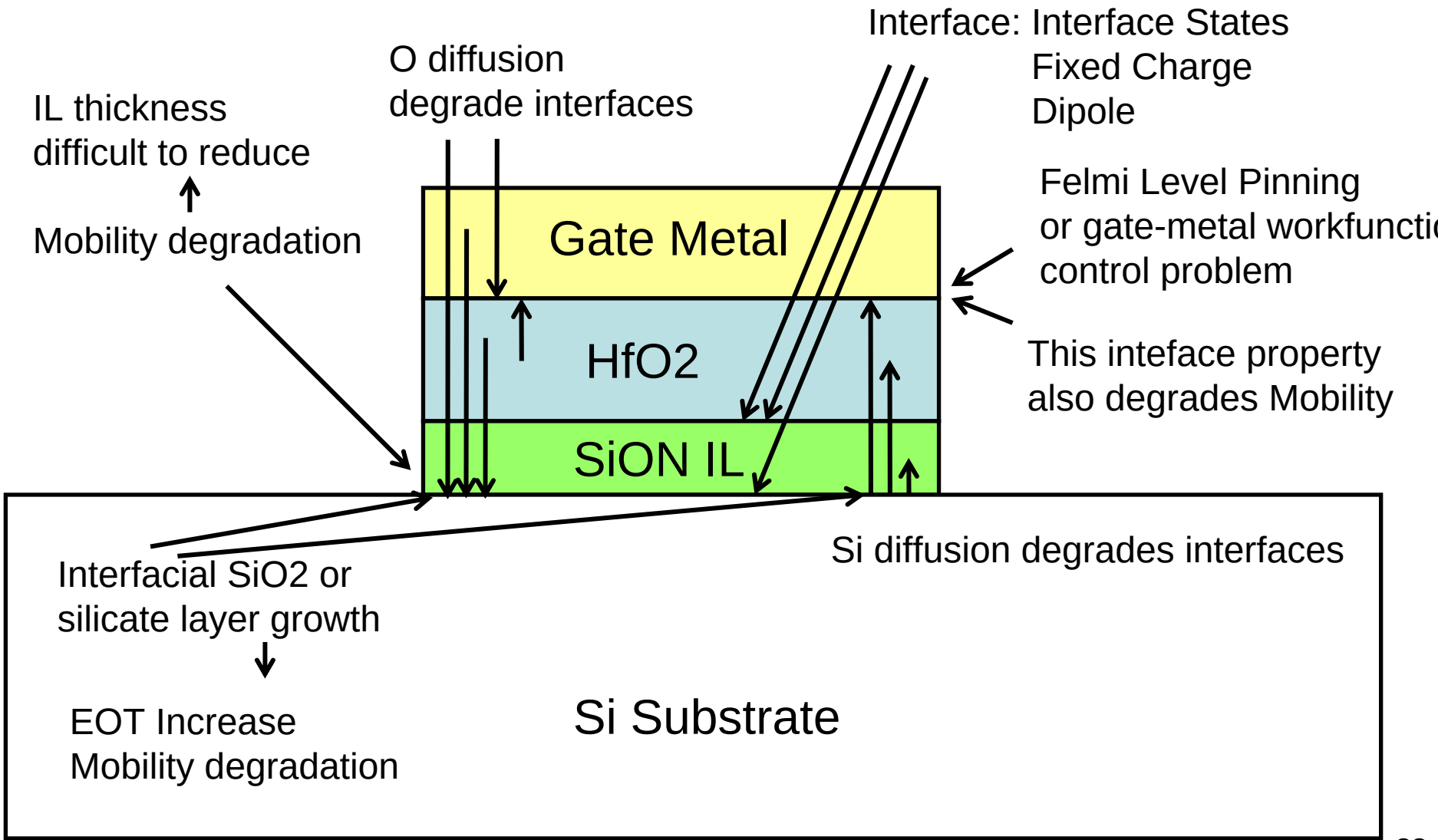
(3) Disturbances of surface potential

(4) Modulation of charge centroid

J. Li and T. P. Ma, JAP (1987); S. Saito, *et al.*, APL (2004)

Now, interest is High-k for EOT < 1nm

Many Problems for thinning EOT



Effect of gate workfunction

N-MOSFET: N-Poly Si gate electrode

Typical Vth = 0.25 ~ 0.6 V

P-MOS FET: P-Poly Si gate electrode

Typical Vth = -0.25 ~ -0.6 V

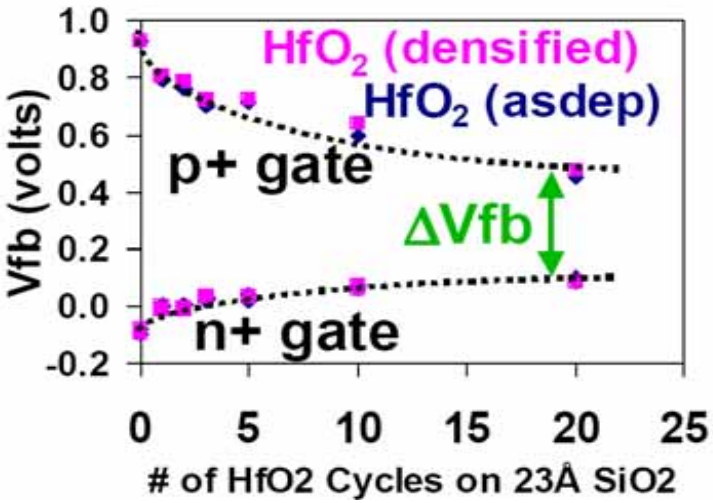
Vfb difference between N-Poly and P-Poly is 1.15 eV (Ideally)

P-MOSFET with N-Poly gate electrode

Vth → -1.4 ~ -1.75 too big

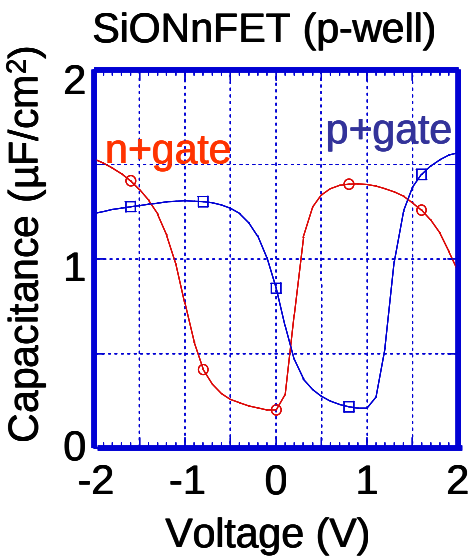
difficult to be adjusted by channel implantation

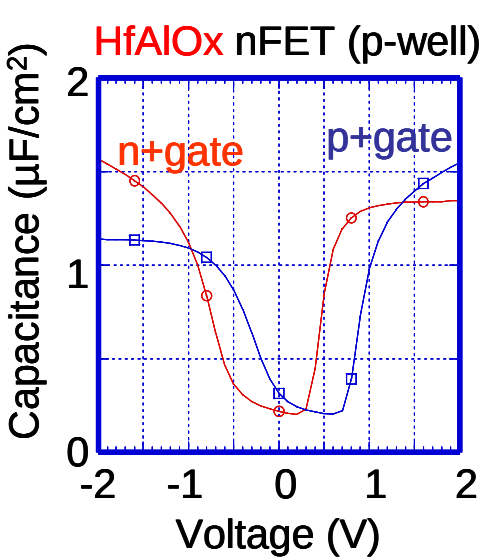
Fermi Level Pinning on HfO_2

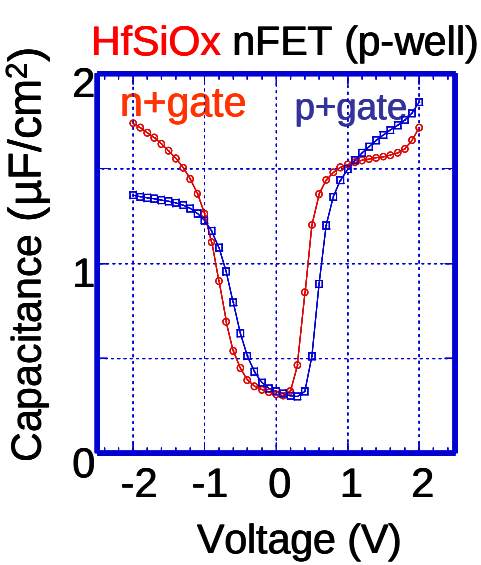


Difficulty in controlling Vth

C.Hobbs, VLSI2003

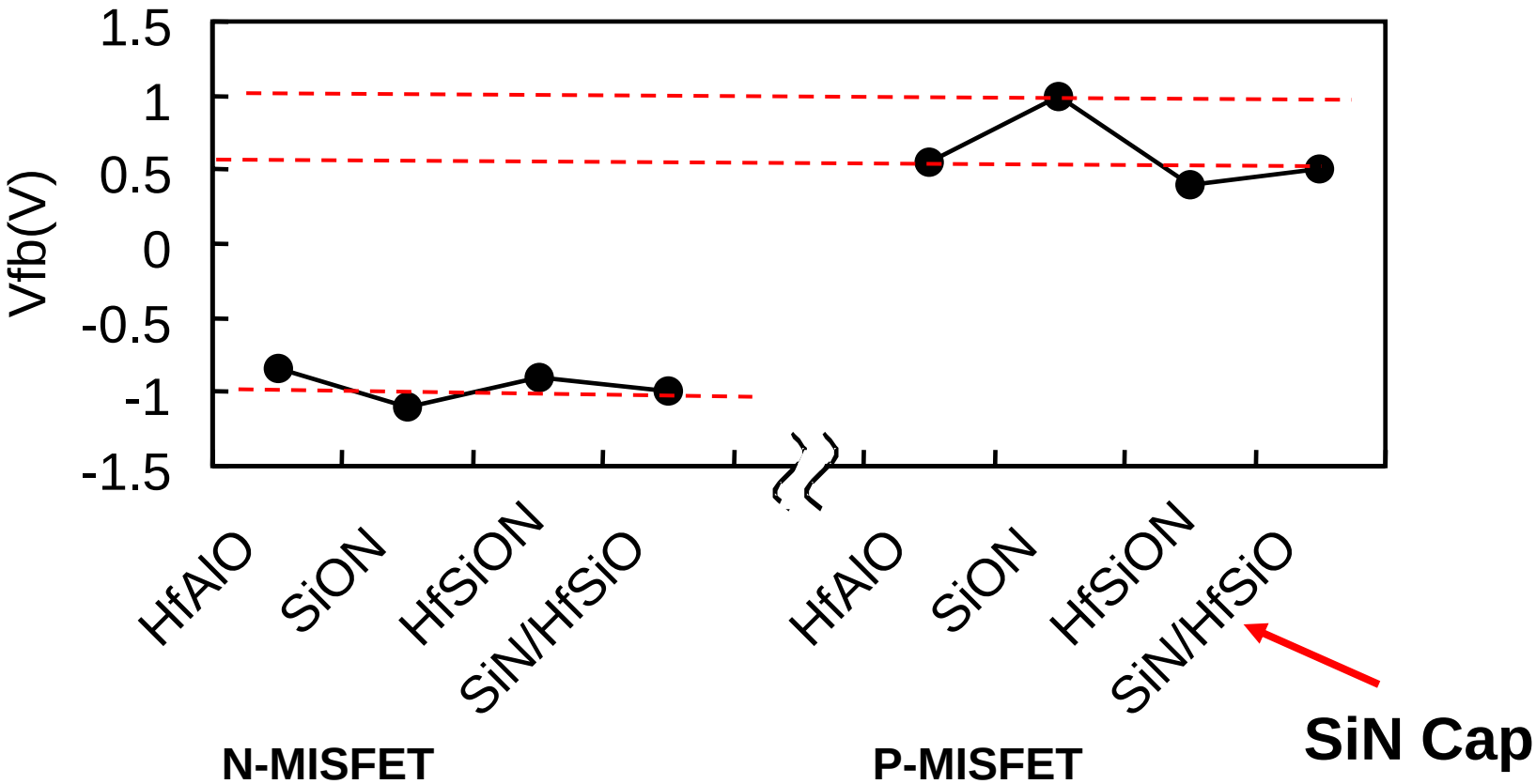






K.Shiraishi, VLSI2004

Flat-band shift due to Fermi Level Pinning



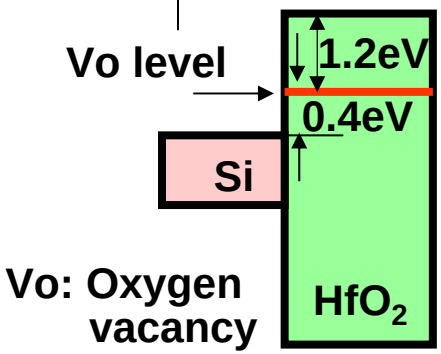
Negative shift of V_{FB} on P-MISEFT(HfSiON) (-0.6 V)
SiN cap cannot recover this shift

K. Nakamura, May 30, 2005 Selete Symposium 2005

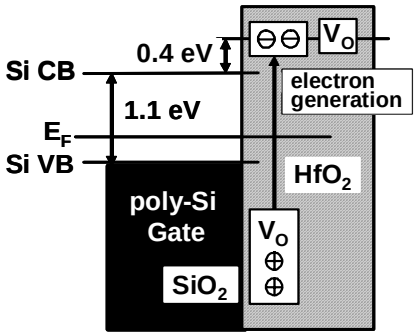
Mechanism of Fermi level pinning

H. Takeuchi, et al. : J. Vac. Sci. Technol A, 22 (2004) 1337.

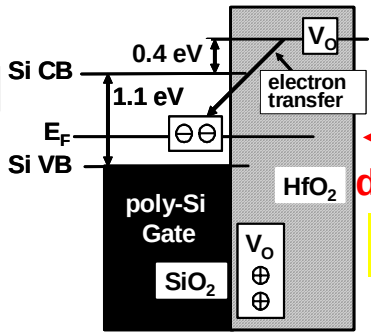
K.Shiraishi, VLSI2004



Vo formation



Electron generation at the oxygen vacancy inside HfO_2 region

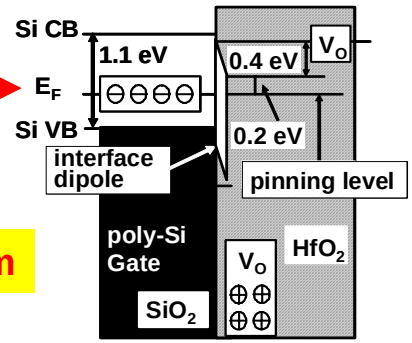


Electron transfer into the poly

Ef pinned

desired

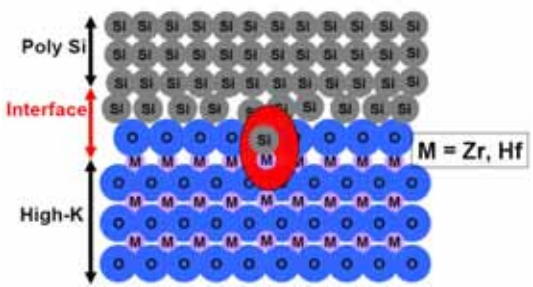
Problem



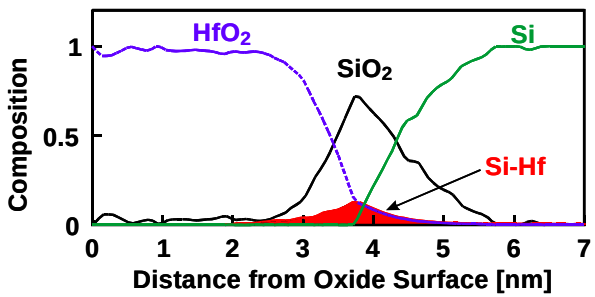
Dipole formation

Fermi level elevation toward the thinning level

Si-Hf bond formation at the interface and O vacancy formation in HfO_2



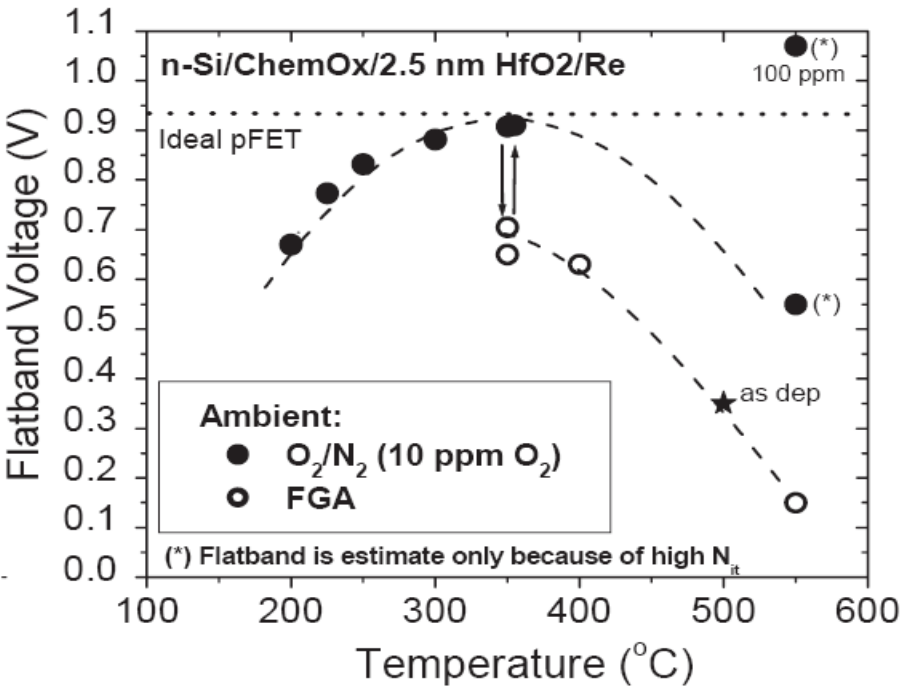
R Chau, IWGI 2003



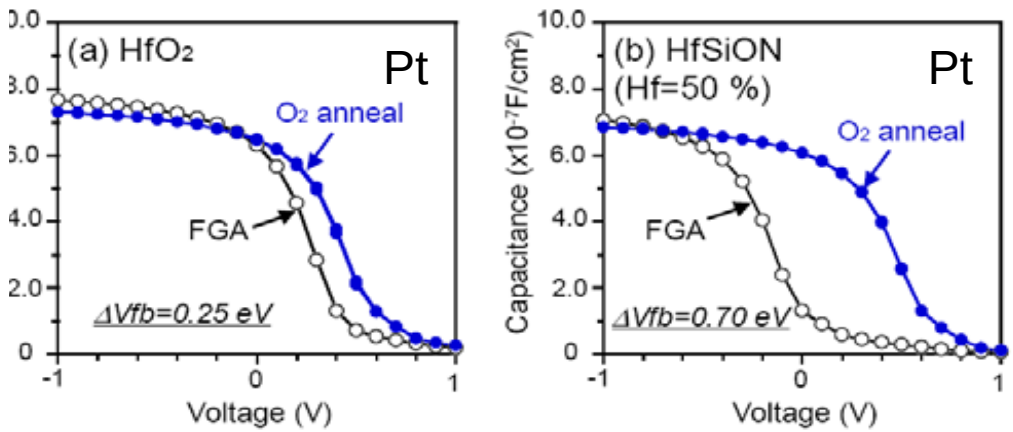
T. Hattori et al., WOFE 2004,
Y. Morisakiet al., IWGI 2001

Because of FLP, Vth of MOSFET becomes too high

Instability of Metal Work Function



E.Cartier, VLSI2005

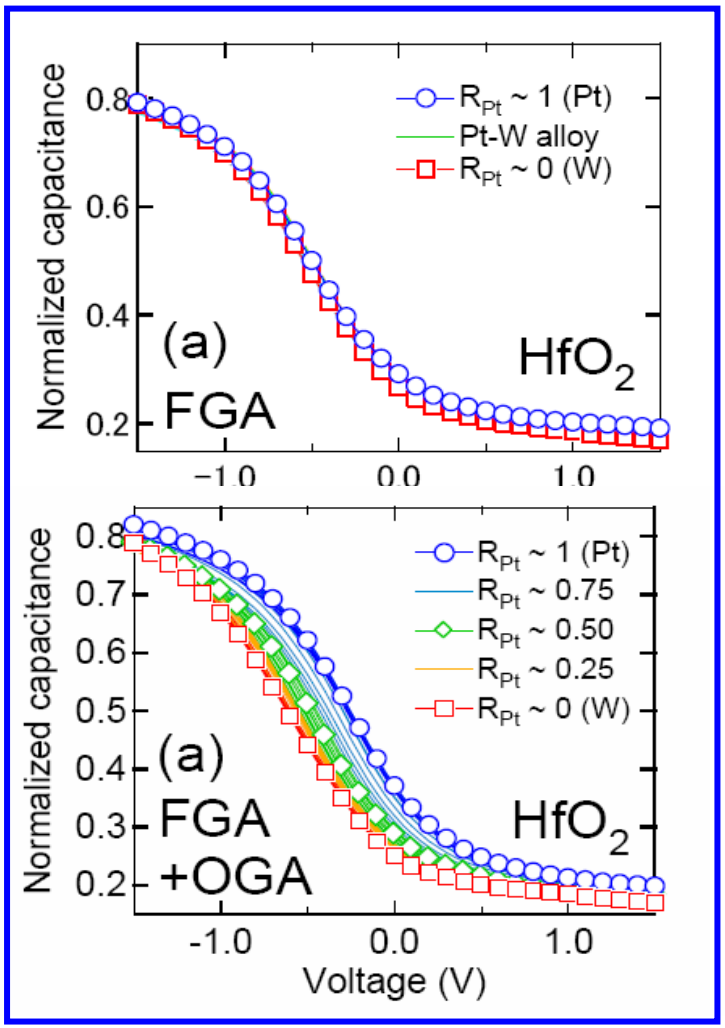


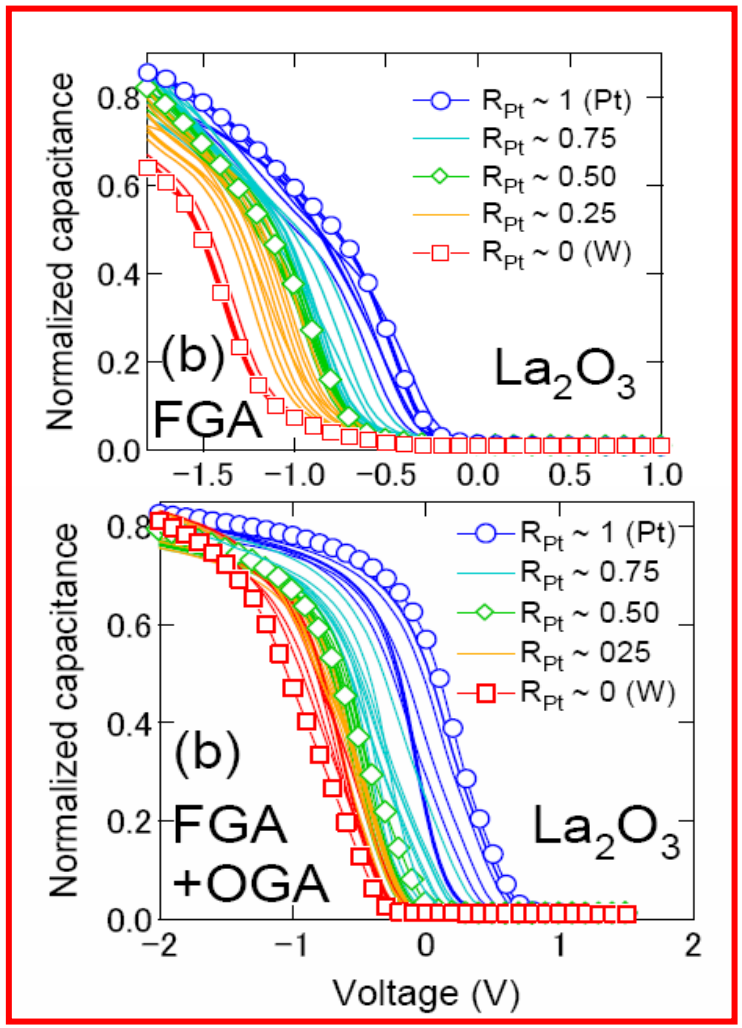
Y.Tsuchiya, SSDM2006

Pt, Re, Pd and Ru on HfO_2 are instable with O_2 and H_2

L.Pantisano, APL(88),243514(2006)

Instability of Metal Work Function

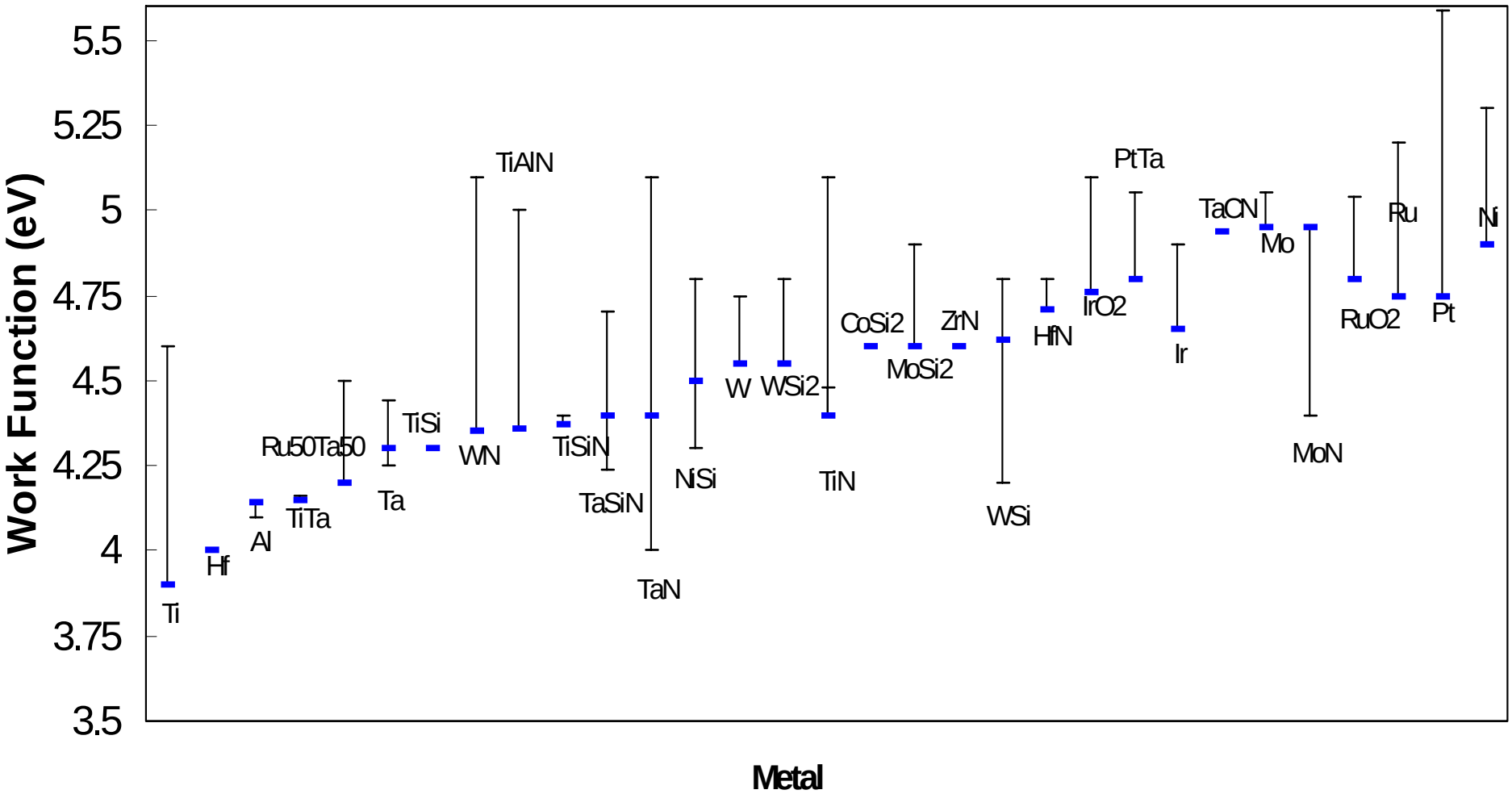




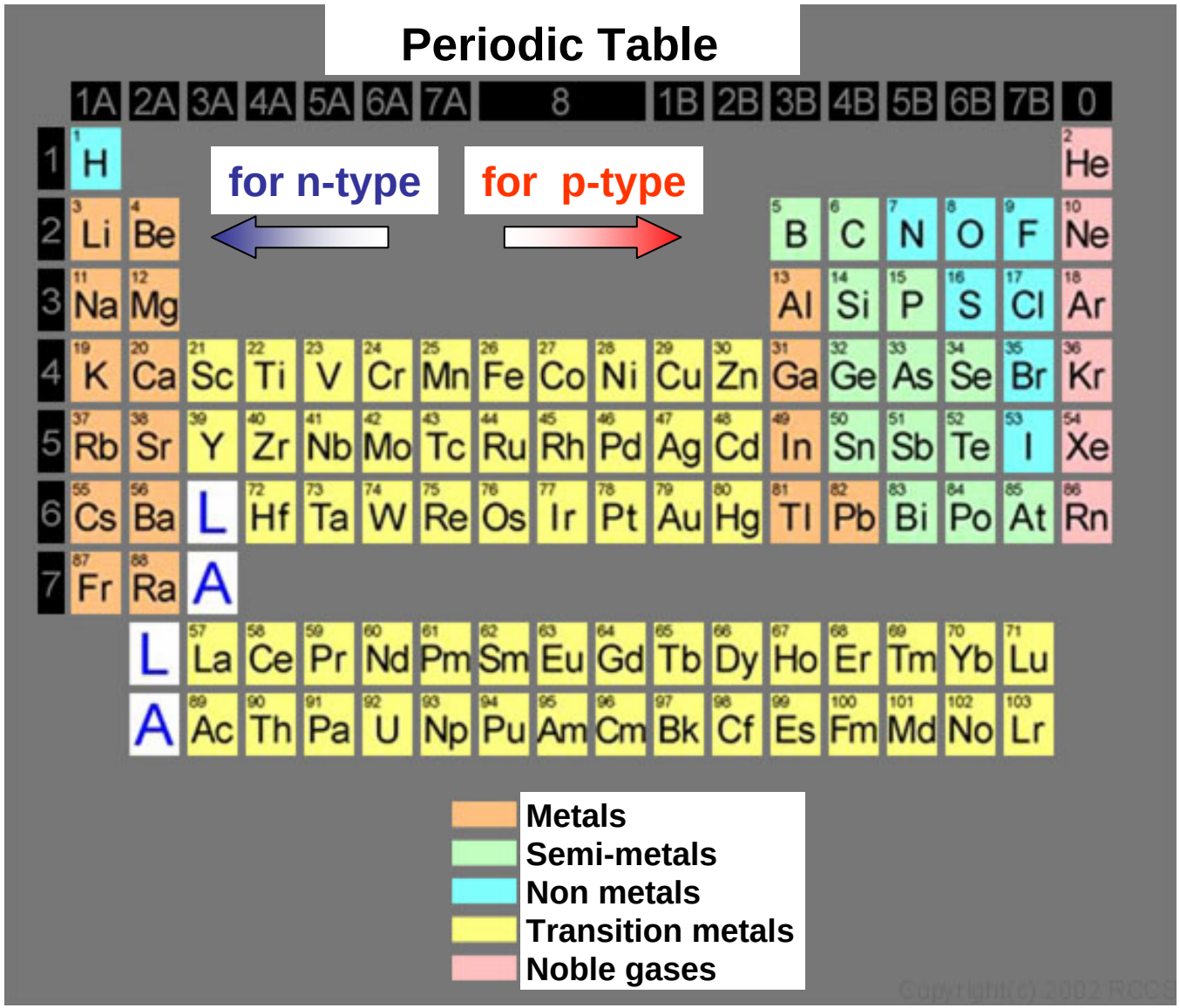
Pt~PtW~W **Wide controllability with La_2O_3**

K.Ohmori, SSDM2006

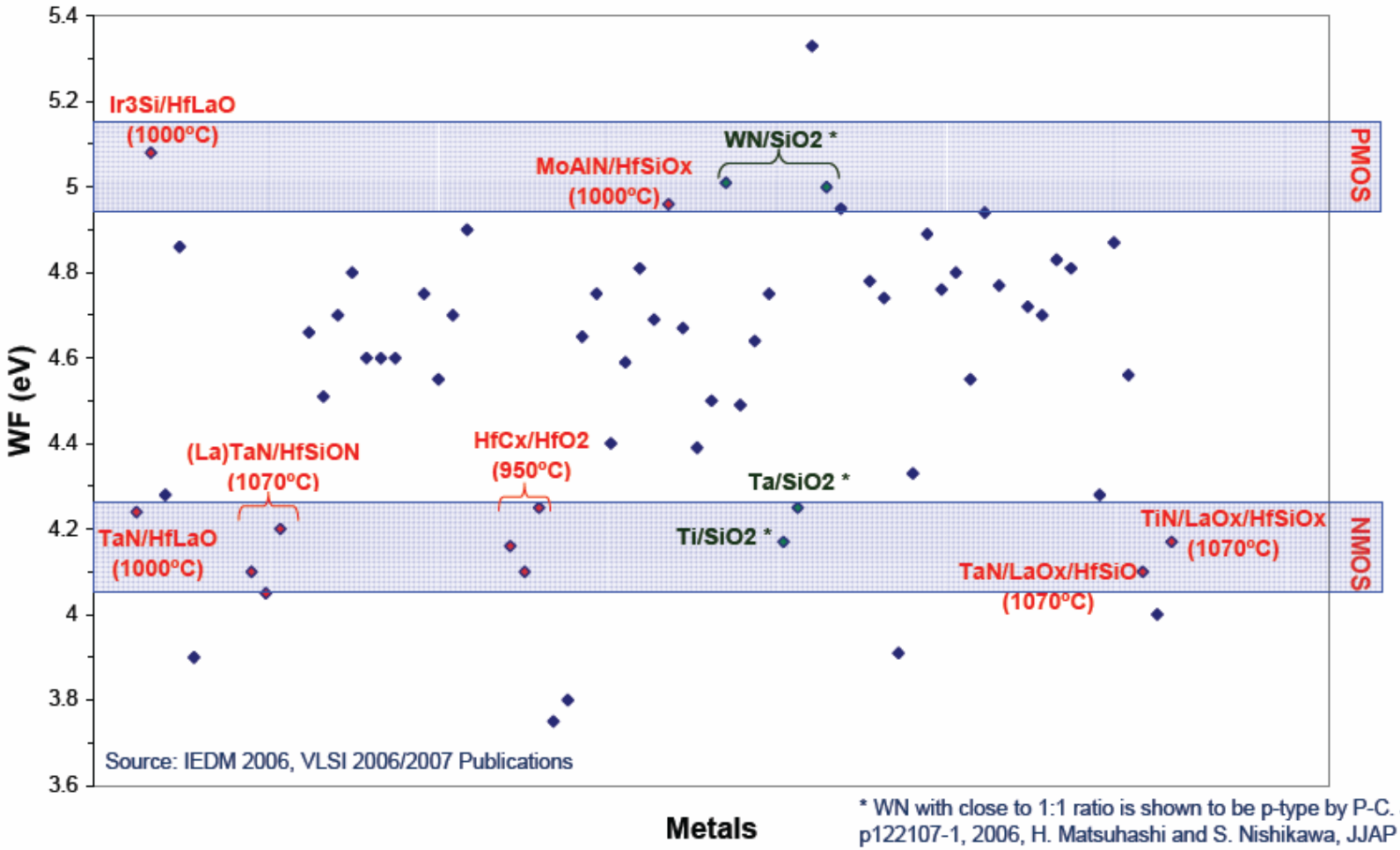
Large Discrepancy in Reported Values for Work Function of Similar Metals by Different groups



Metals for gate electrode



Y. Akasaka, Selete



* WN with close to 1:1 ratio is shown to be p-type by P-C. Jiang, etal, APL 89 p122107-1, 2006, H. Matsuhashi and S. Nishikawa, JJAP v33 p 1293, 1994

- High temperature process integration requires additional modification
  - LaO_x cap layer
  - Incorporation into either high-k or metal gate of additional elements (La, Al)
- Metal gates WN for PMOS and Ti, Ta for NMOS are stable at low temperature

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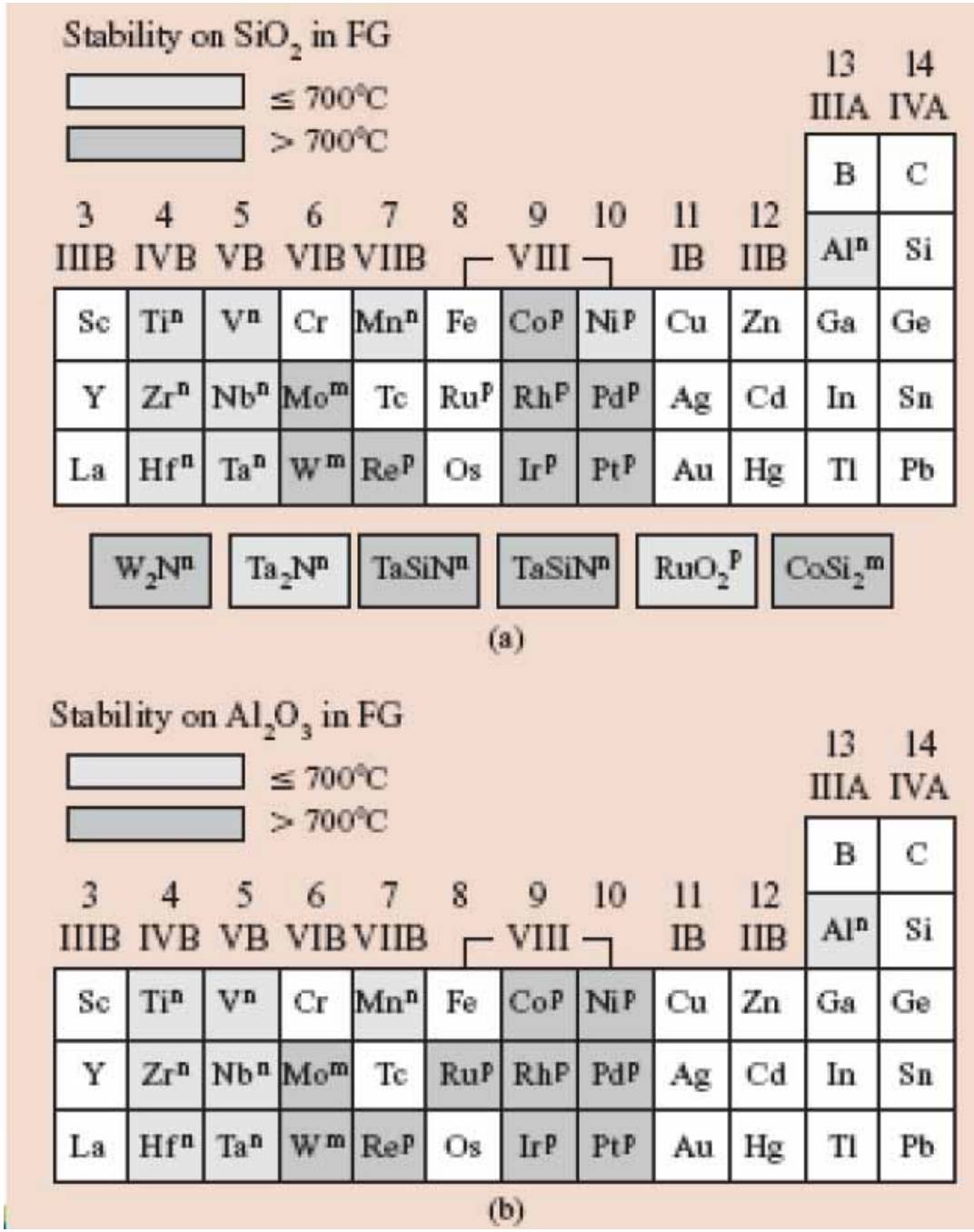
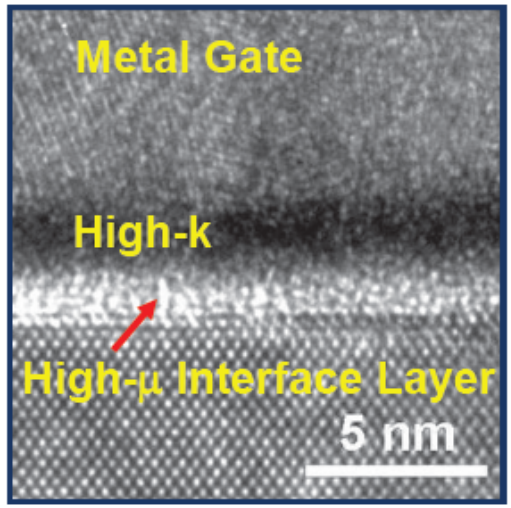
Thermal Stability

- Low Φ_M Metals (4-4.3eV nMOS) are reactive with oxide at >700°C, with the exception of TaN.
- High Φ_M Metals (4.9-5.2eV) are stable at >700 °C.
- Two Φ_M Metals option thus requires a low temperature integration flow.
- Similar results holds for metals on high-k.

Source: E. P. Gusev et al., IBM
J. RES. & DEV. V50, No 4/5 2006



One Dielectric, Two Φ_m Metals vs. Two Dielectric Stacks, One Φ_m Metal



Using the Same Initial Gate Dielectric Stack

Gate Pre-Clean

RTO/DPN/PNA

ALD HfO_2

Integration Approach A

Two Distinct Metals Required

nFET	pFET
TaN[1]	WN[3]
TaC[2]	

[1] E. P. Gusev et al., IBM J. RES. & DEV. V50, No 4/5 2006
[2] W.J. Taylor, etal (Freescale), IEDM p. 625, 2006
[3] P-C. Jiang, etal, APL 89, 2006, H. Matsuhashi and S. Nishikawa, JJAP v33, 1994

Integration Approach B

One Metal Only With Nanoscale Cap Layers (Dipole Approach)

nFET	LaO_x[1]
pFET	Al-based[2]

[1] V. Narayanan, et. al. (IBM), 2006 Symp. on VLSI Tech. Dig
[2] H.N. Alshareef, et. al. (SEMATECH), Appl. Phys. Lett. **88**, 112114 (2006)

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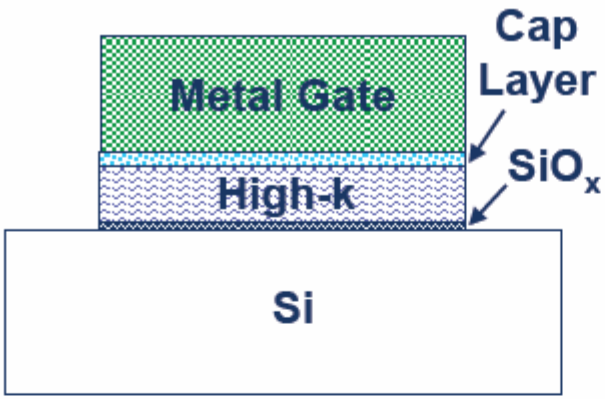
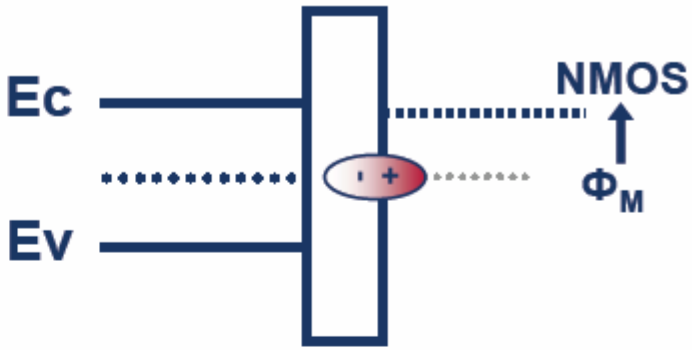
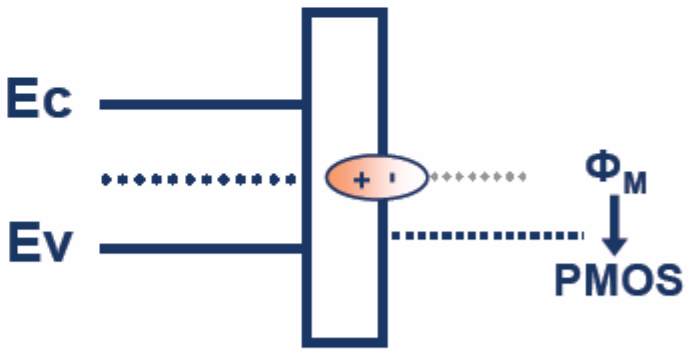
Work Function Tuning Using Dipole Approach



More Electronegative



NMOS Cap: LaO_x
(More Electropositive than Hf)



PMOS Cap: Al-based
(More Electronegative than Hf)

Dielectric cap layers can tune the threshold voltage by intermixing with the high-k and creating a dipole at the high-k/metal gate interface.

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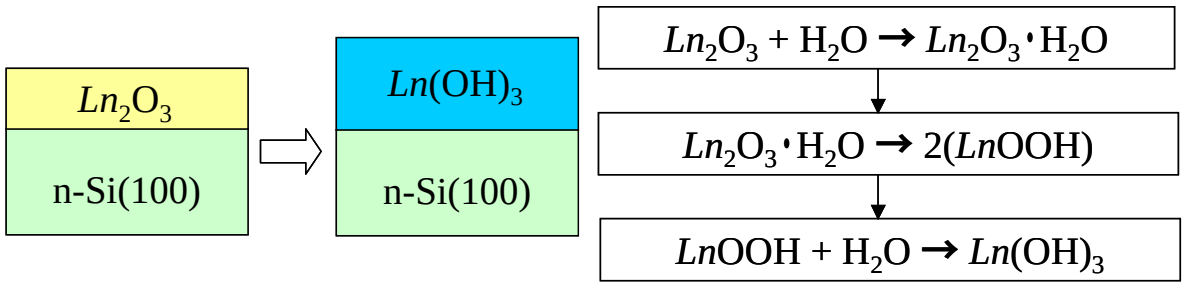
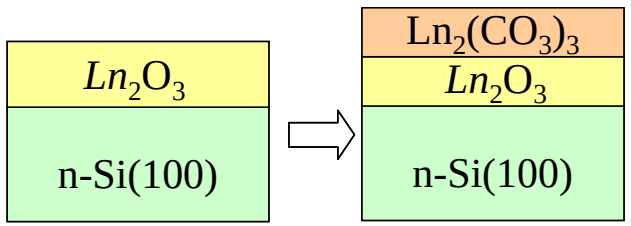
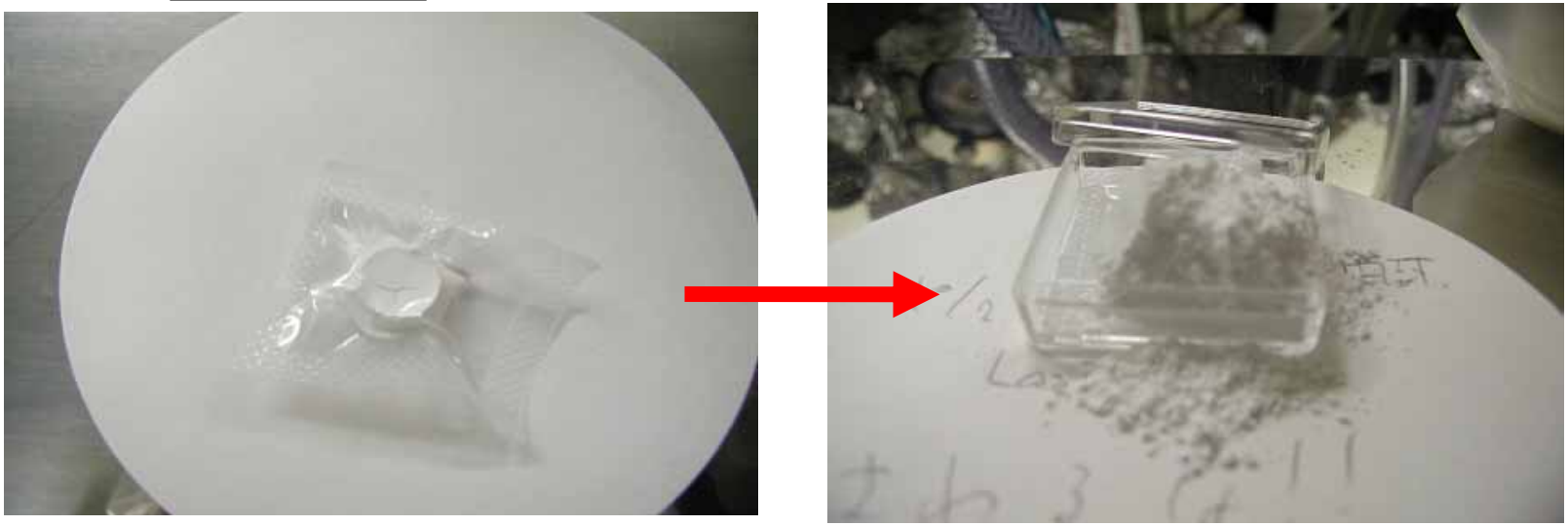
Iwai Lab’s results for La_2O_3 and HfO_2/La_2O_3

Hygroscopic Properties of La_2O_3





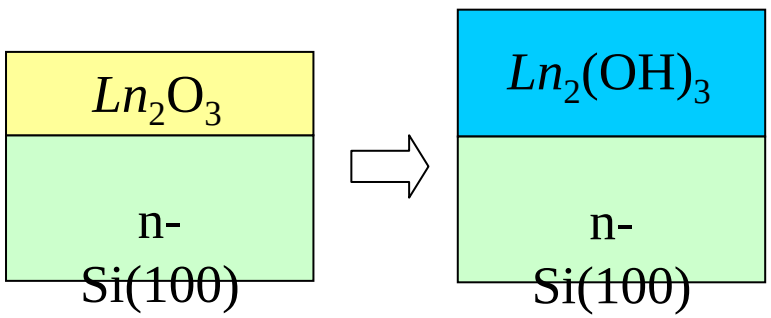


After 30 hours in clean room (temperature & humidity controlled)

Absorption of moisture and CO_2

The oxides become hydroxide and carbonate in H_2O and CO_2 ambient.

hydroxide

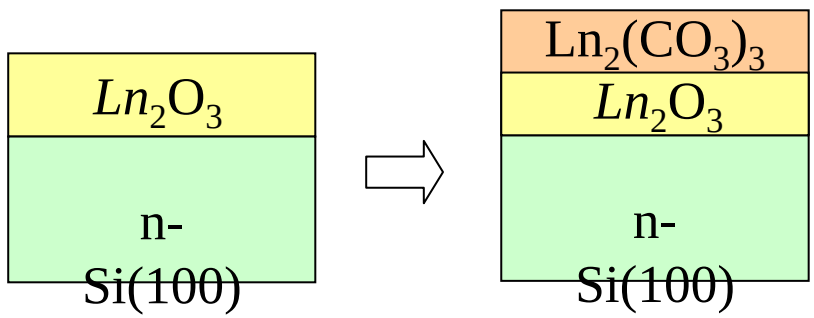


$Ln_2O_3 + H_2O \rightarrow Ln_2O_3 \cdot H_2O$

$Ln_2O_3 + H_2O \rightarrow 2(LnOOH)$

$2Ln(OH) + H_2O \rightarrow 3Ln_2(OH)_3$

carbonate

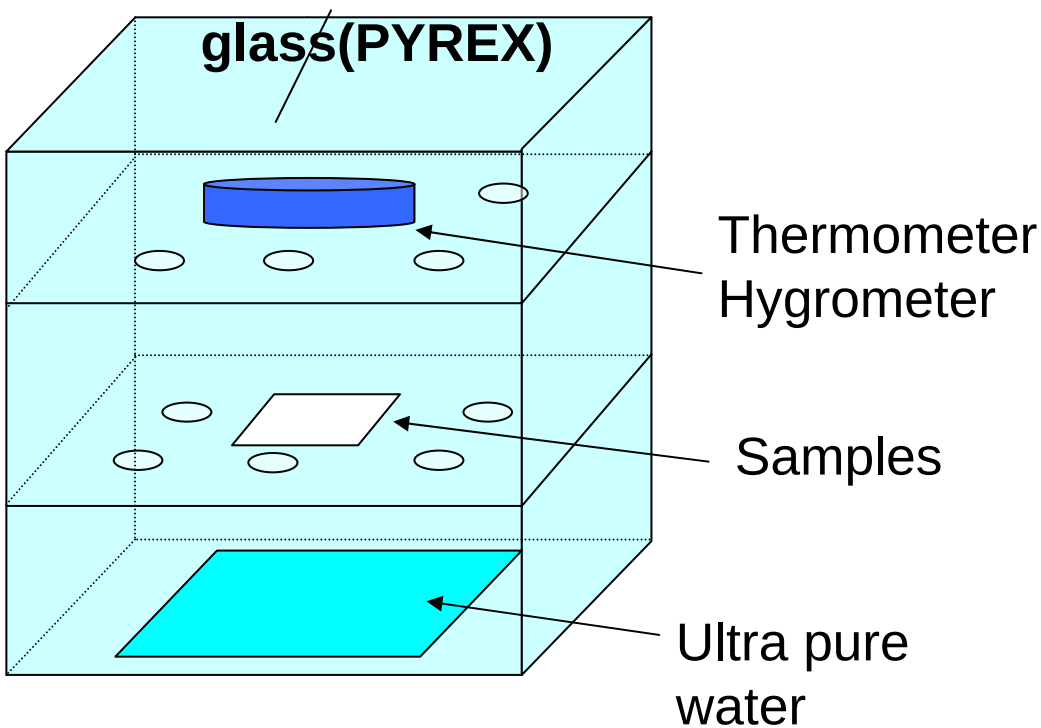


$Ln_2O_3 + CO_2 \rightarrow Ln_{2O2}(CO_3)$

※*Ln*：Lanthanide

Experimental apparatus

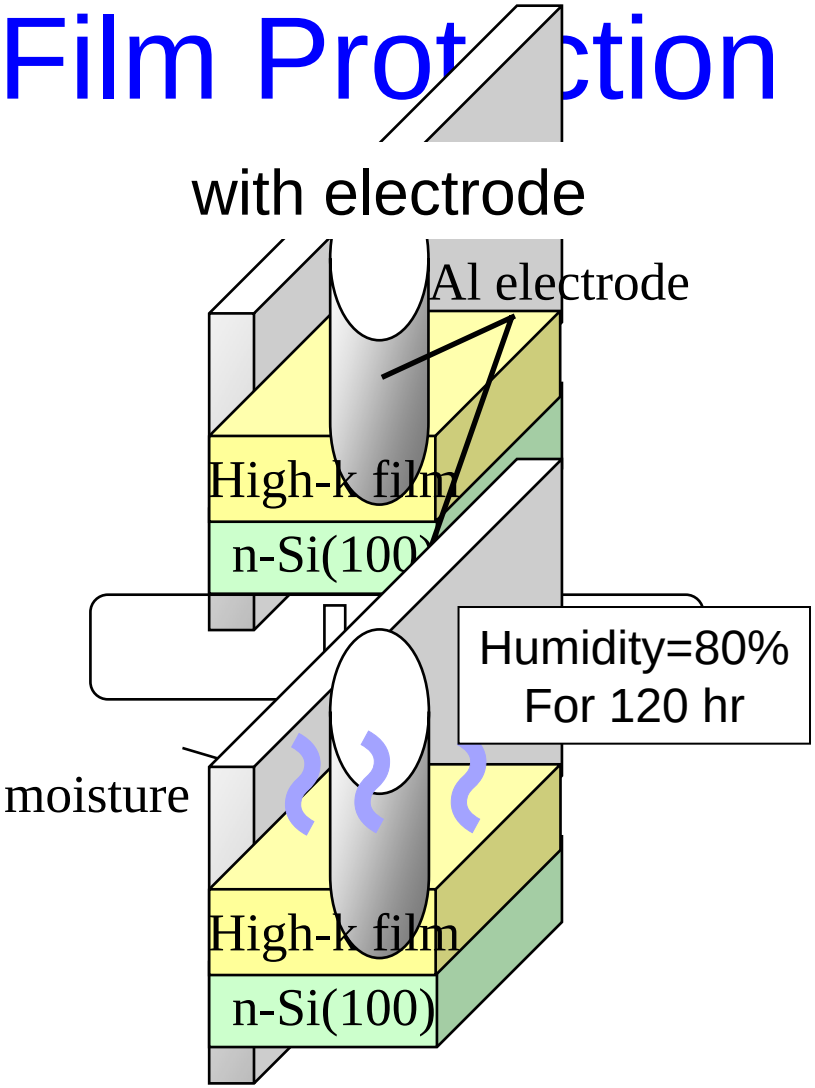
Temperature: ~20°C
Humidity: 80%
Humidification time:
0 ~120 hrs

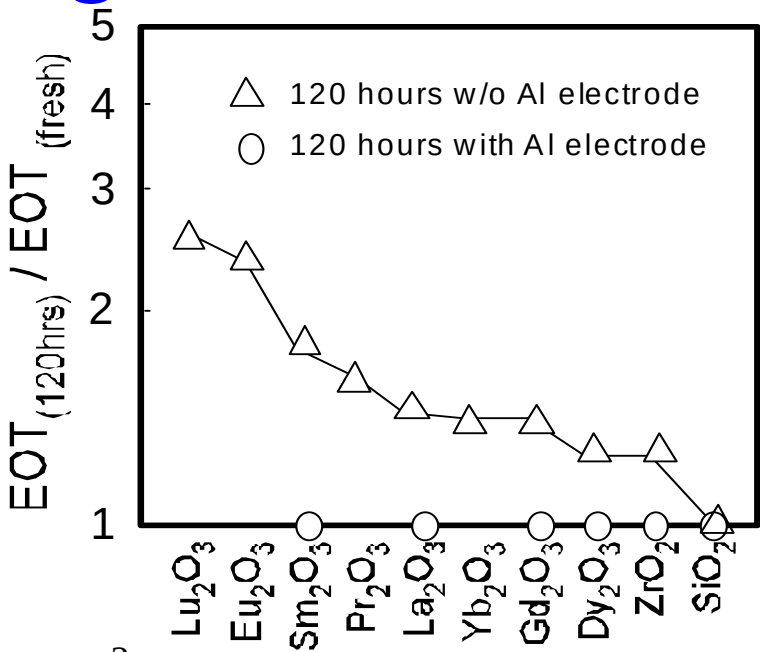


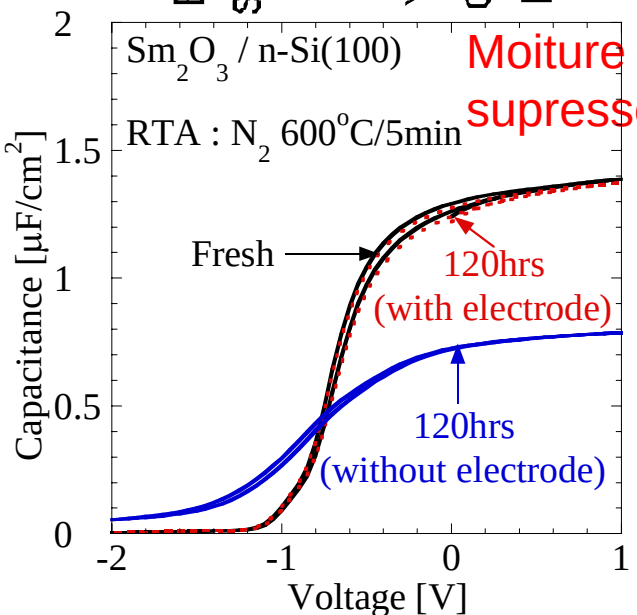
glass (PYREX) acryl (PMMA)

*PMMA : $CH_2C(CH)_3COOCH_3$

Film Protection against Moisture



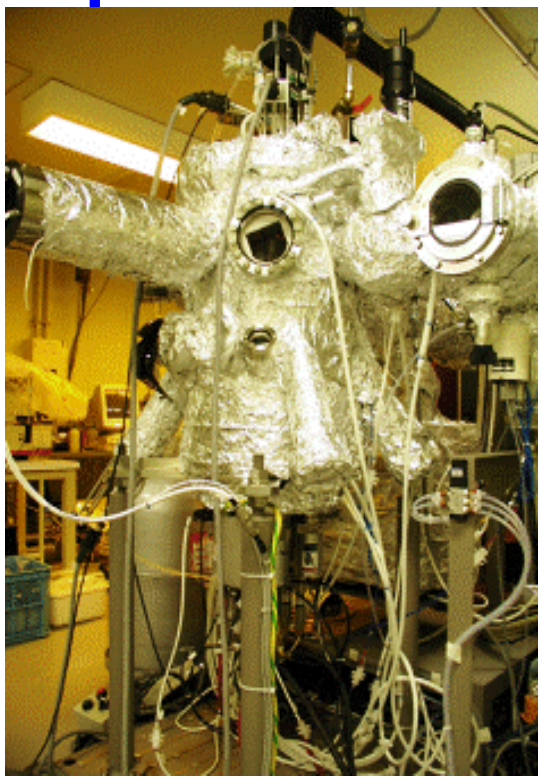


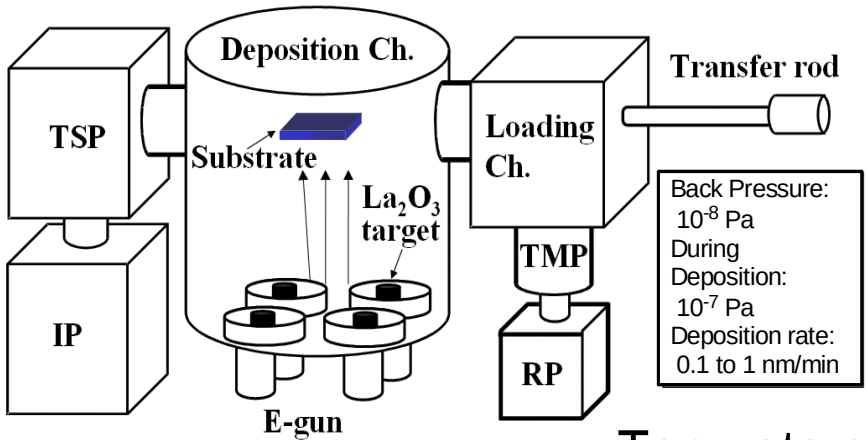


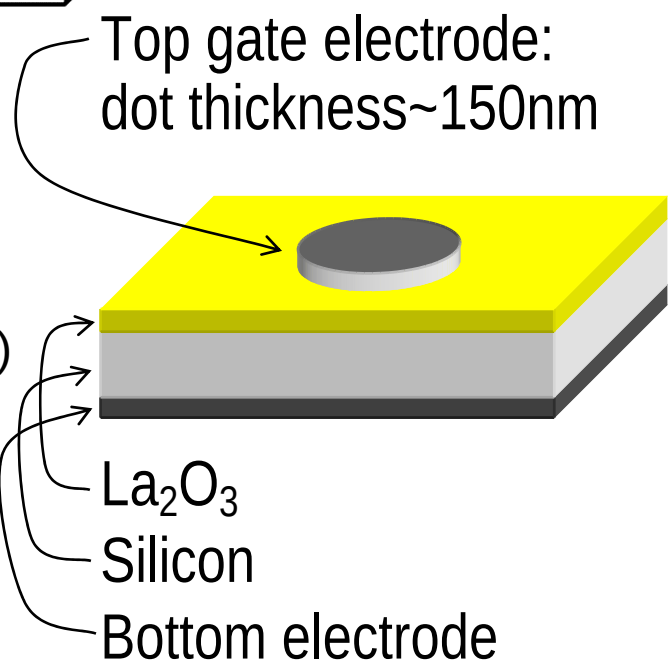
Moiture absorption can be supressed by Al electrode

Need to minimize the time to from gate metal after PDA

Experimental Procedure





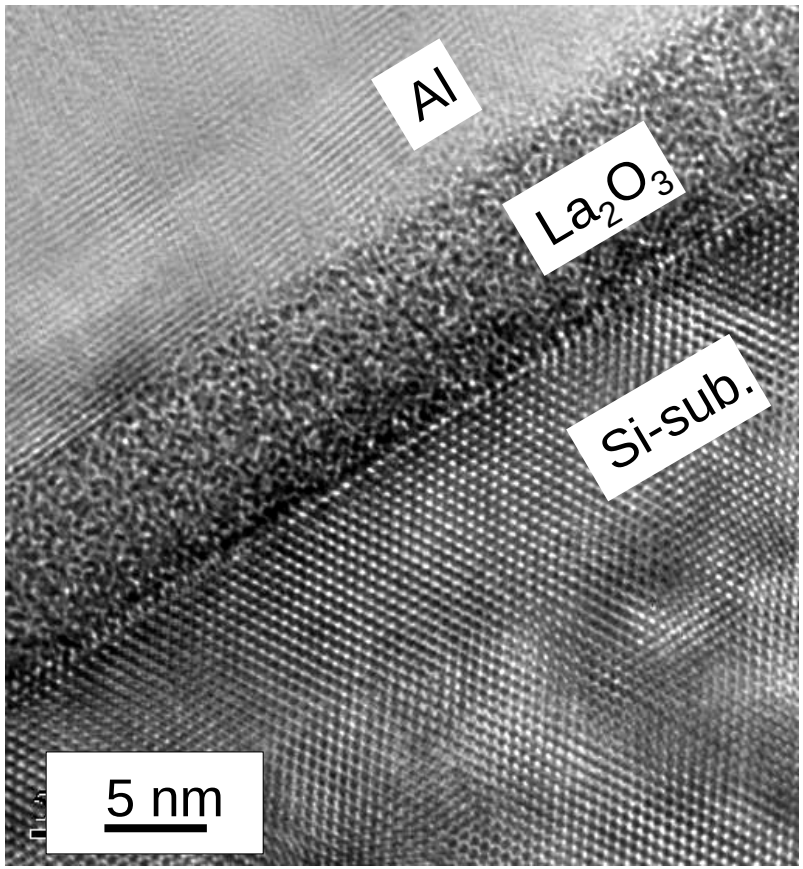


E-beam evaporation in ultra-high vacuum (10^{-7} Pa) at with substrate heater

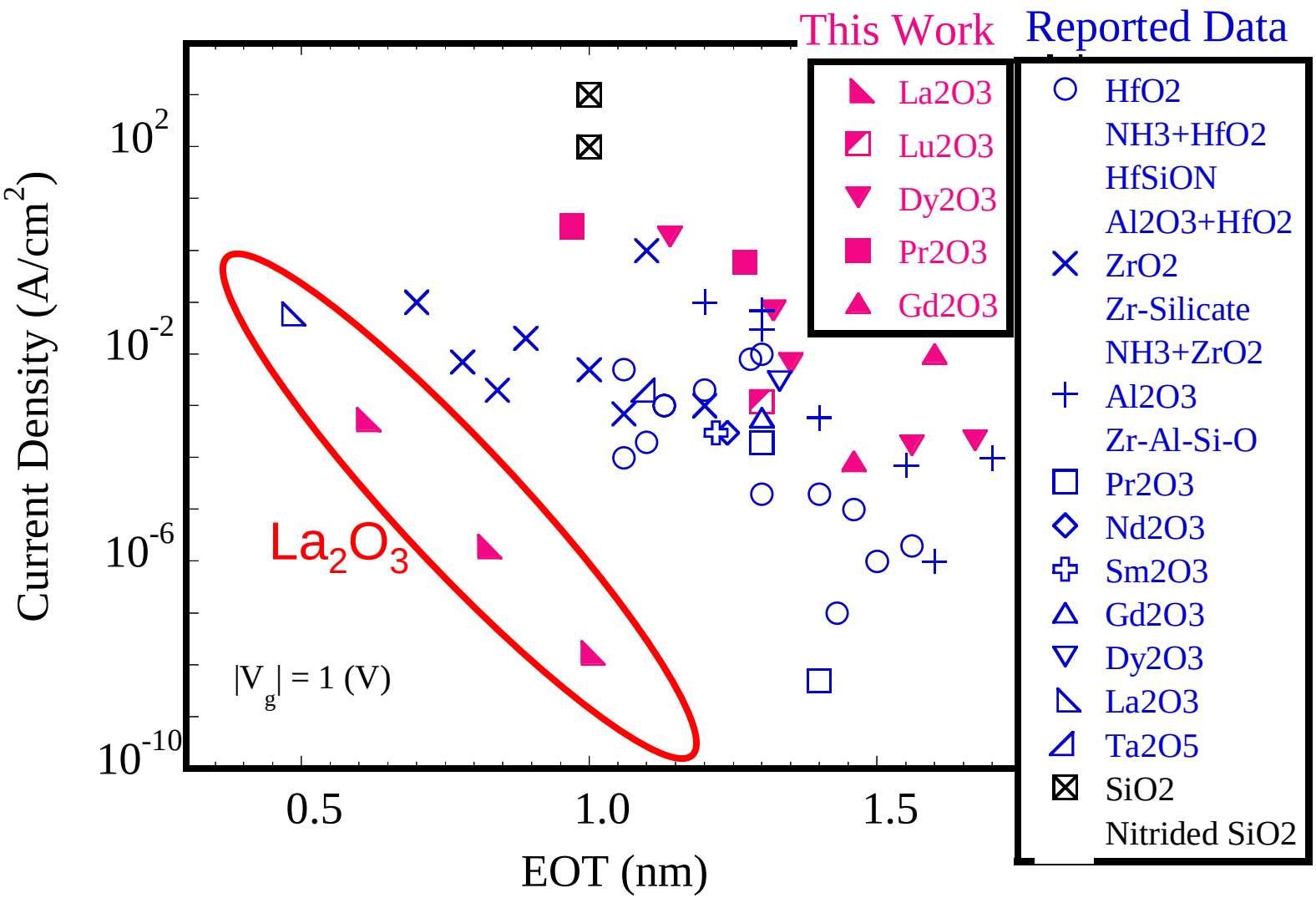
Annealing in IR lamp heater in N2 or O2 ambient

Simple & Pure material examination

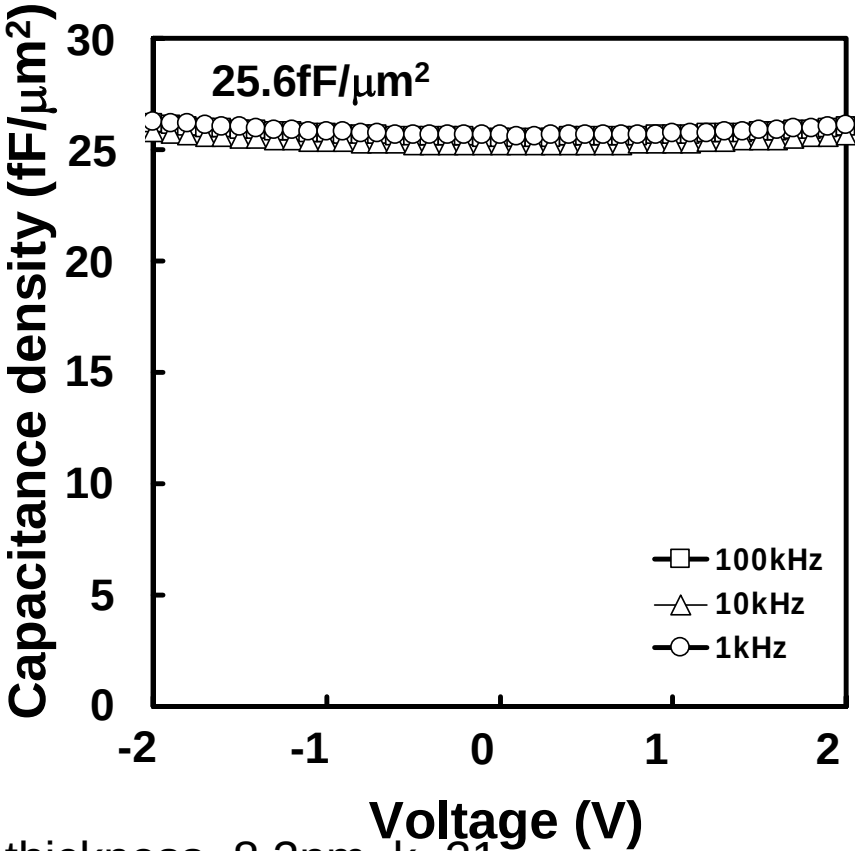
Deposition Temp. = 250^{o}C, Tphy = 10 nm, Annealed in O_2 400^{o}C 5min



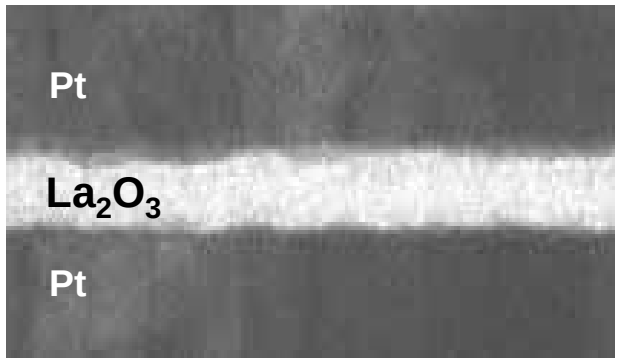
Low Gate Leakage Current with La_2O_3

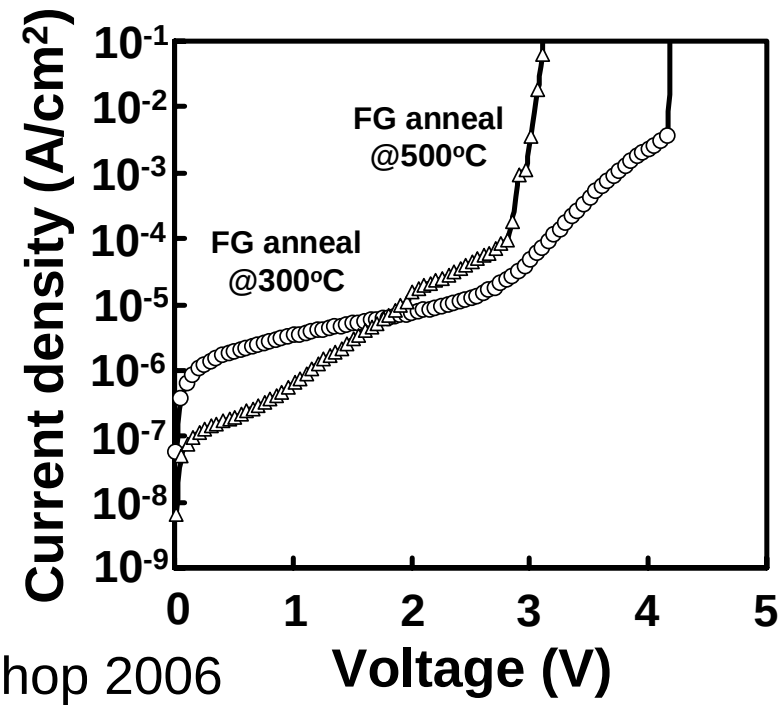


$Pt/La_2O_3/Pt$ MIM Capacitor



thickness=8.3nm, k=21





La_2O_3 : Hear endurance is good

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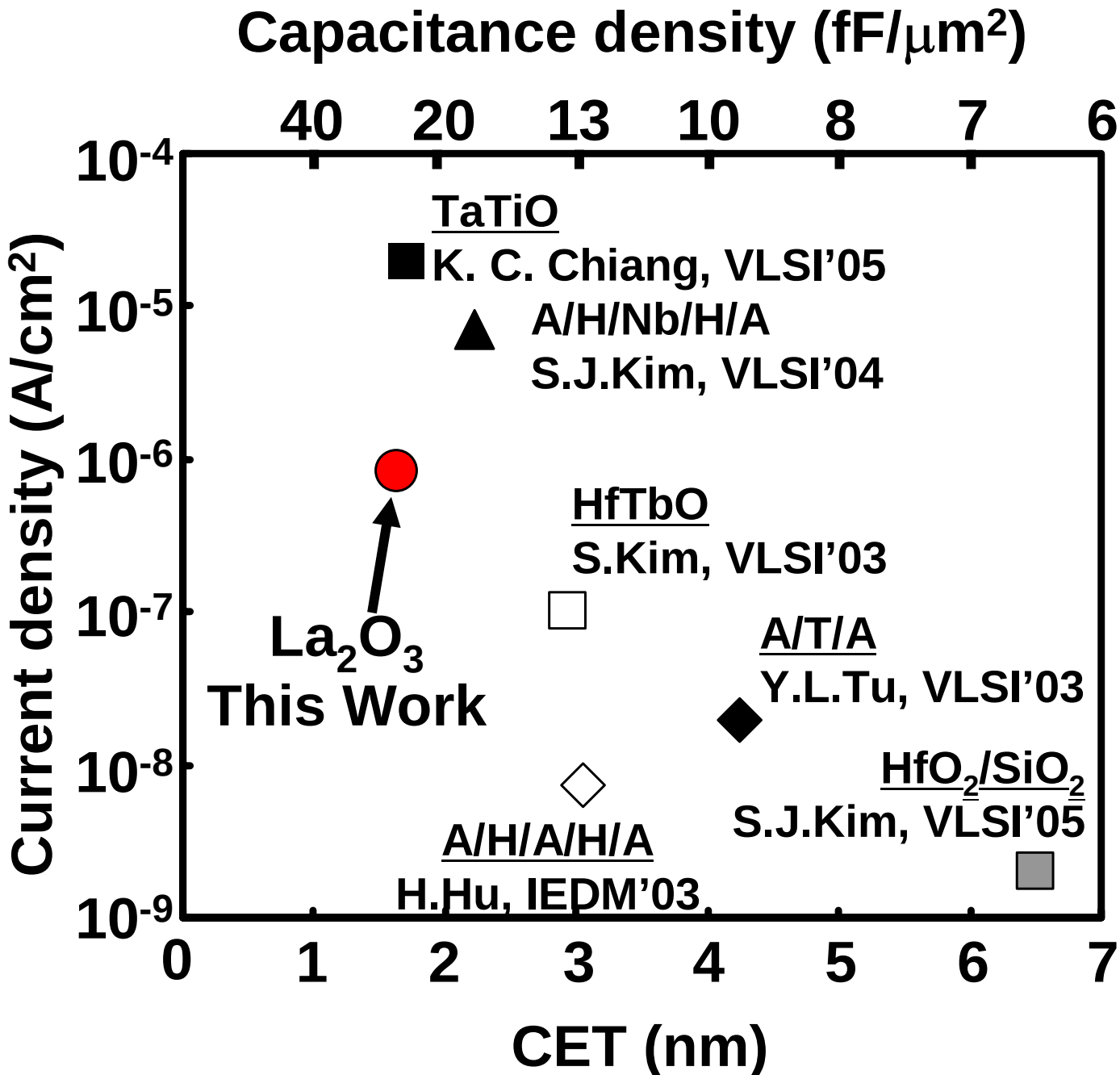

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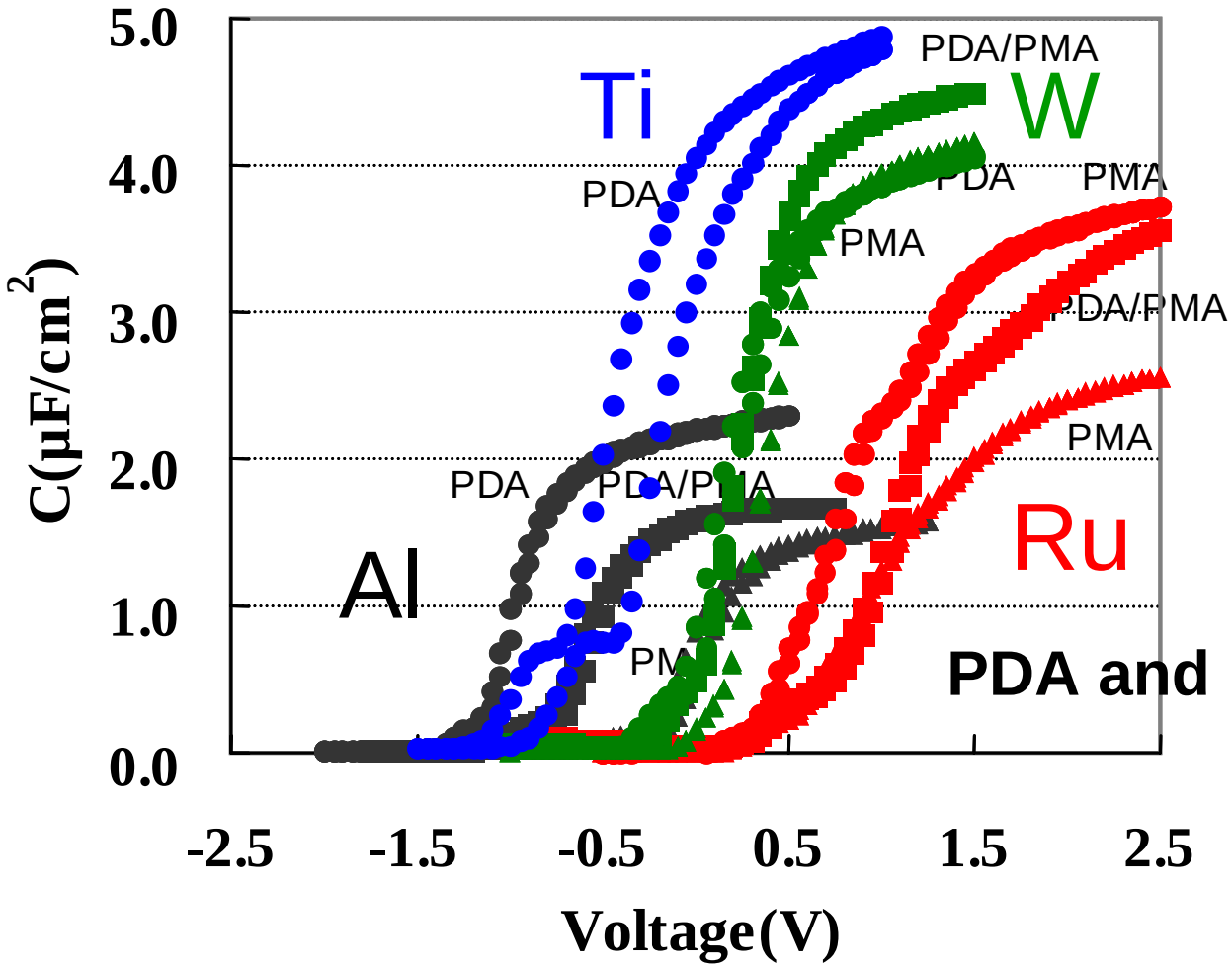
No Fermi Level Pinning with La_2O_3



Threshold voltage (Vth) can be adjusted using Metal Wokfunction

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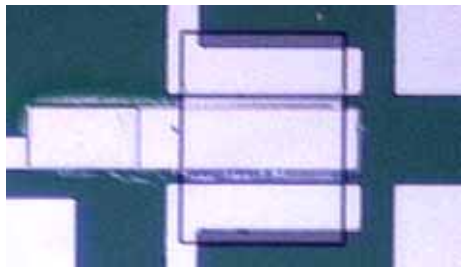
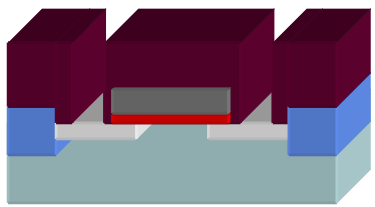
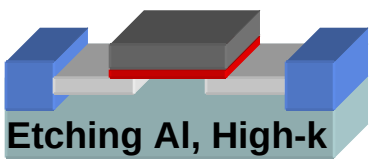
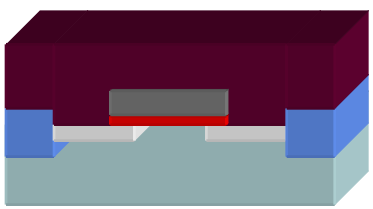
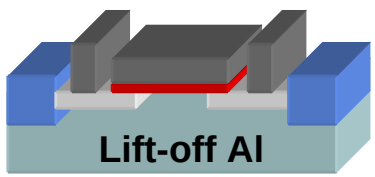
La_2O_3 Gated MOSFET Fabrication











Source/Drain pre-formed Substrate

↓

SPM, DHF cleanning

↓

La2O3 deposition

↓

(PDA)

↓

Al gate deposition and patterning

↓

(PMA)

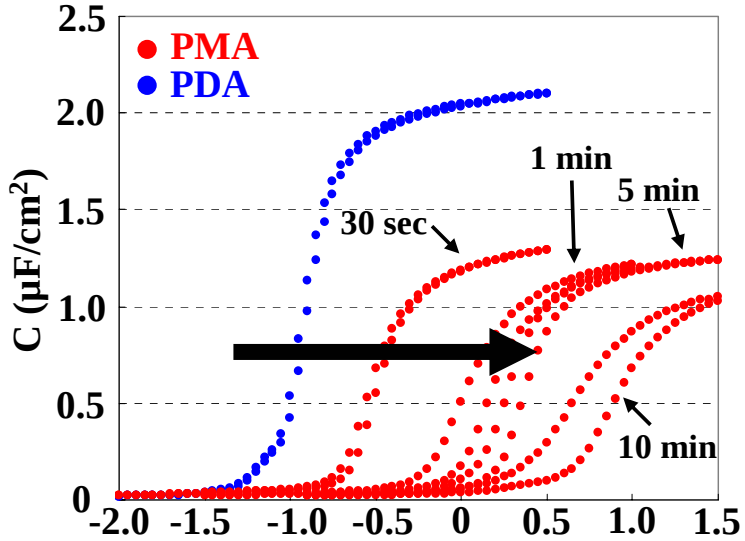
↓

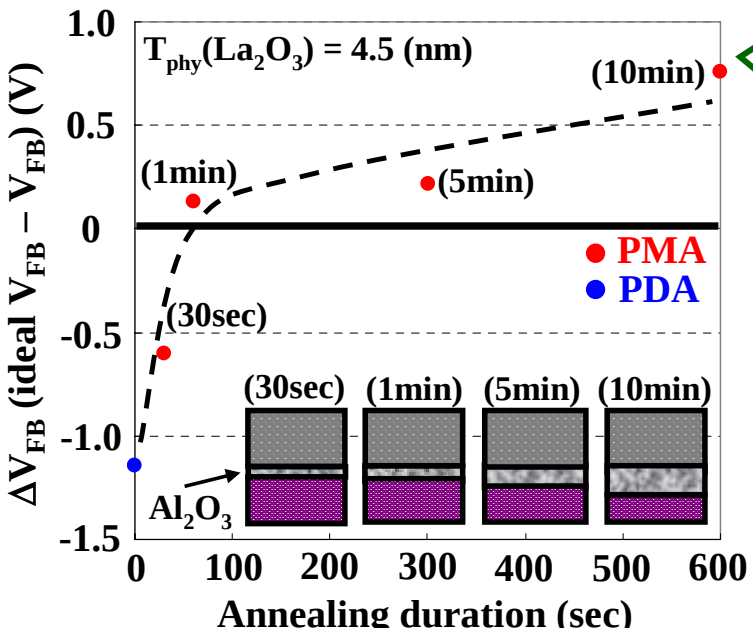
La2O3 etching for S/D contacts

↓

Al lift-off for S/D pads

Post Metallization Annealing (PMA) of Al gated La_2O_3 MOS Capacitor



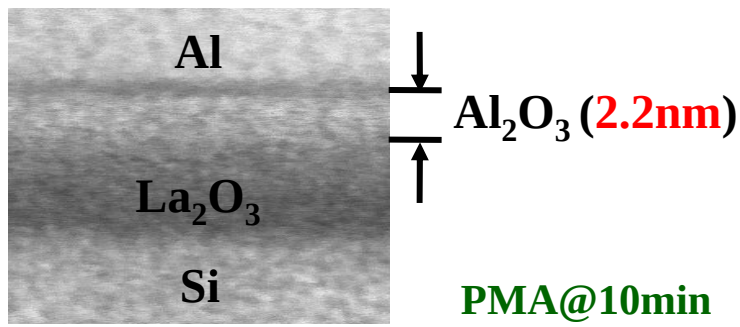


Y. Kuroki, et al., ECS 208th

V_{FB} shift to positive direction (negative charge)

Large EOT increment due to Al2O3 formation

From the TEM observation, the Al_2O_3 thickness of the 10 minutes PMA sample was measured to be 2.2 nm

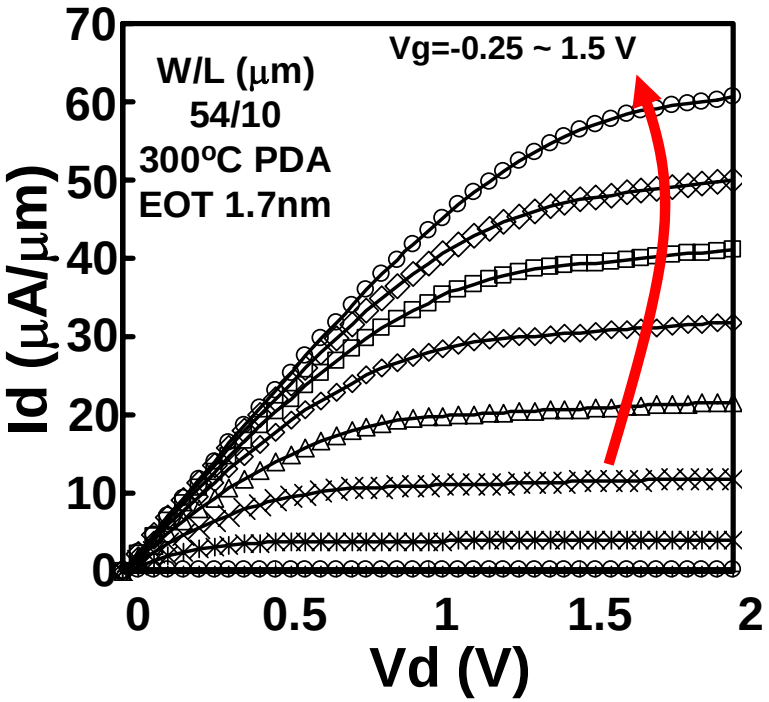


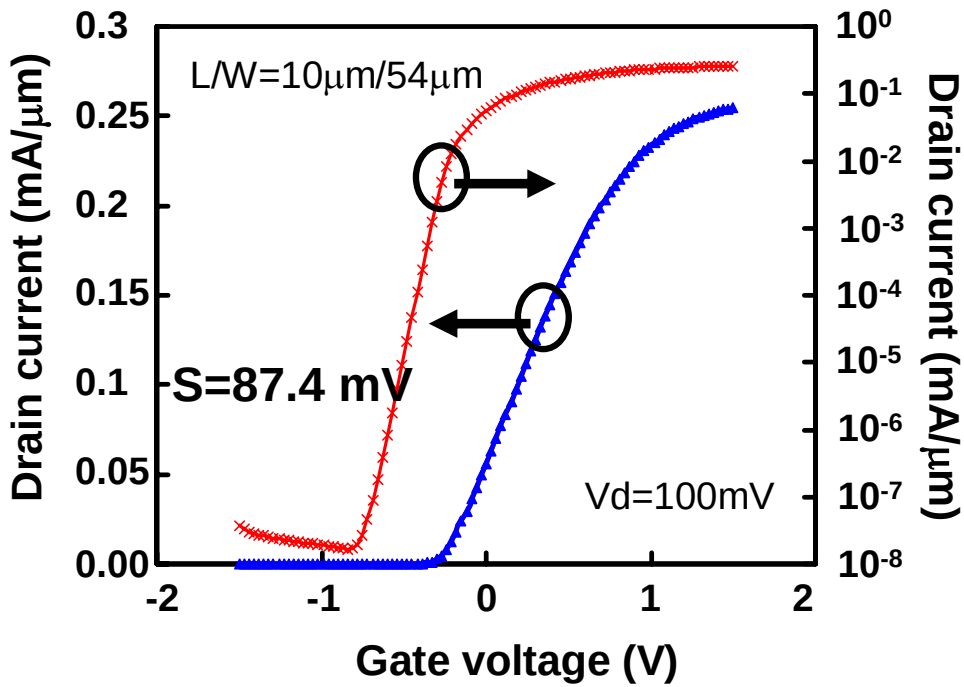
PMA@10min

Electrical Characteristics of La_2O_3 n-MOSFET

Al/La_2O_3/p-Si/Al

Process
- La_2O_3 300 °C deposition
- PDA N_2 300 °C 10 min





Good electrical characteristics can be obtained.

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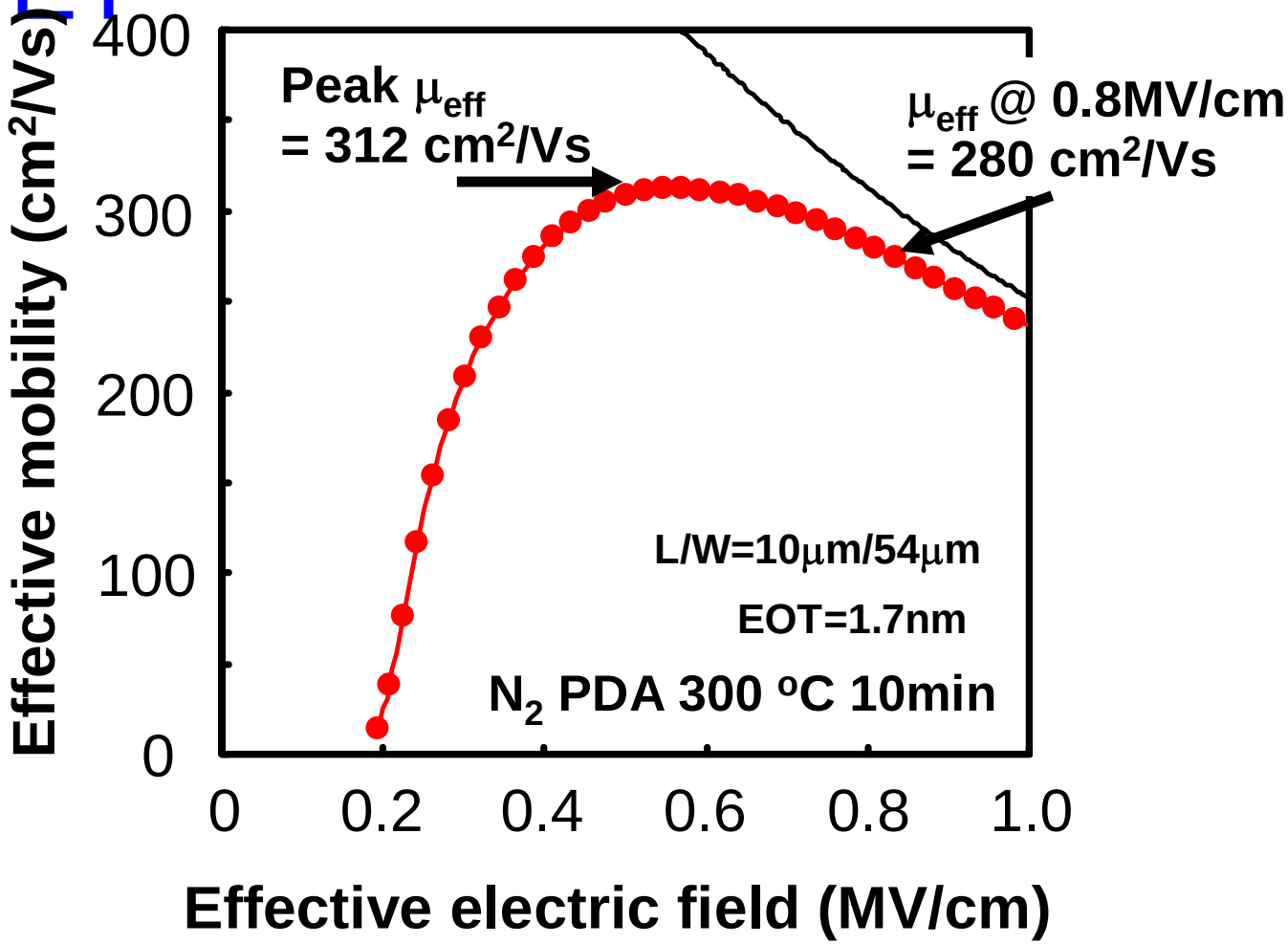
Effective Mobility of La_2O_3 MOSFET



High effective mobility of 312 cm²/Vs can be obtained with La_2O_3

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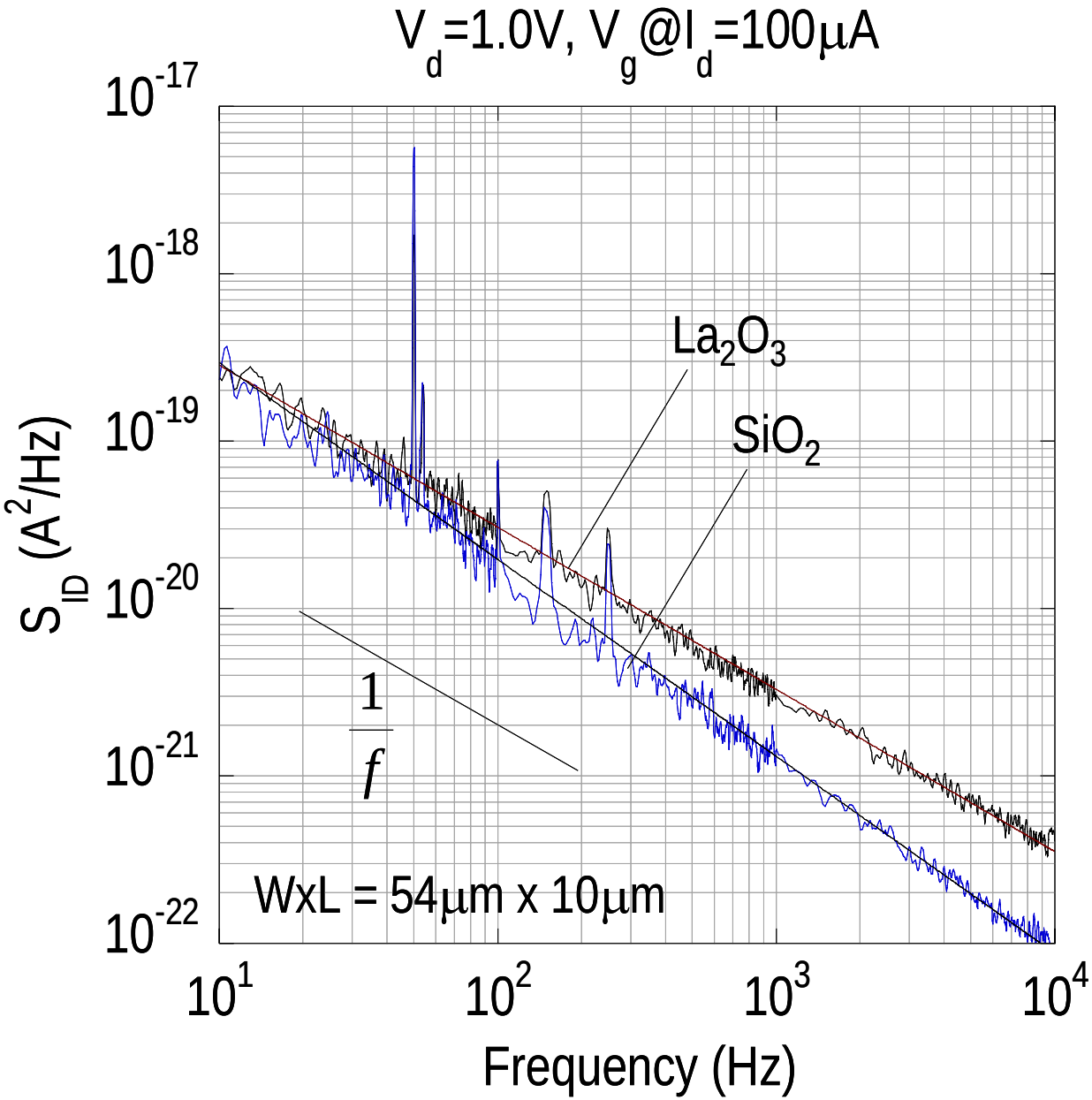
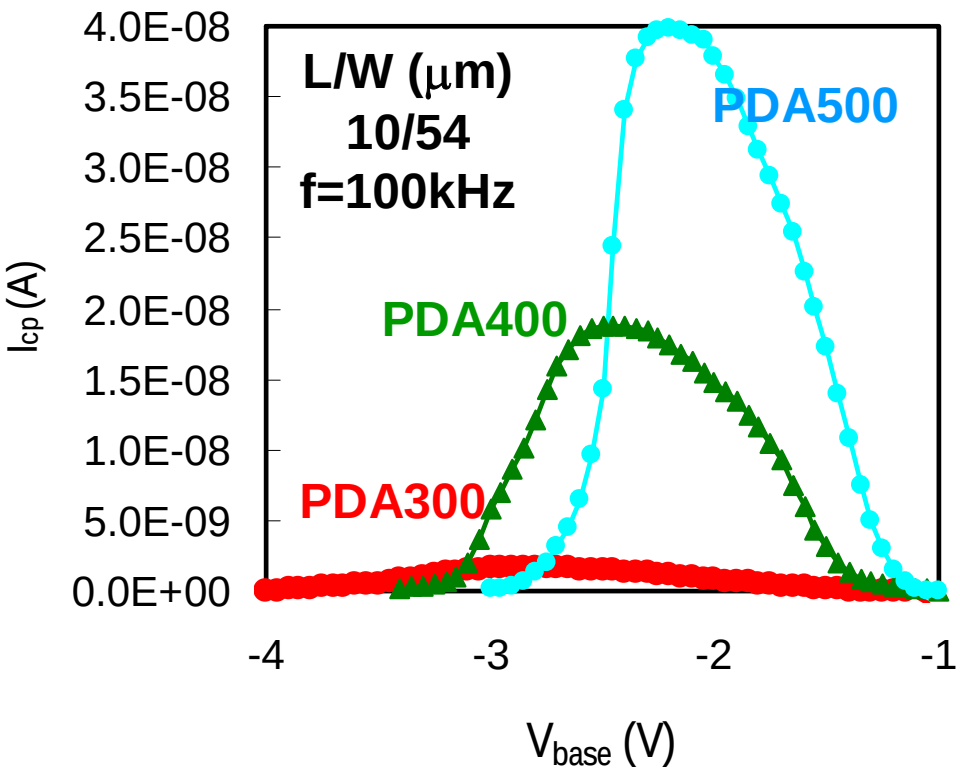
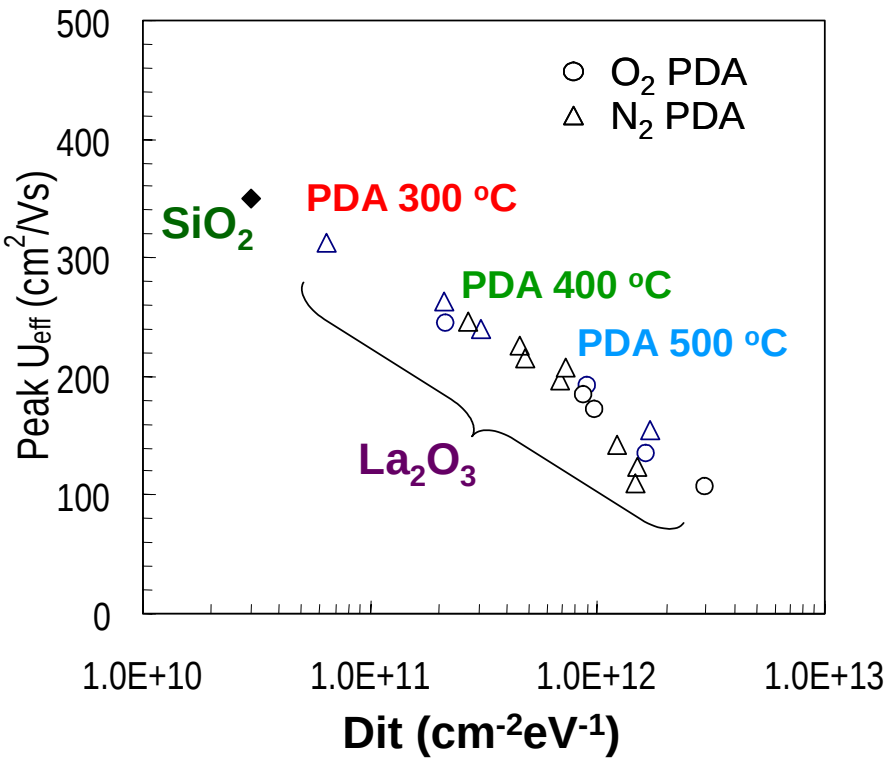
1/f noise in saturation region



Interfacial State Density





Interface state density increases at higher temperature annealing

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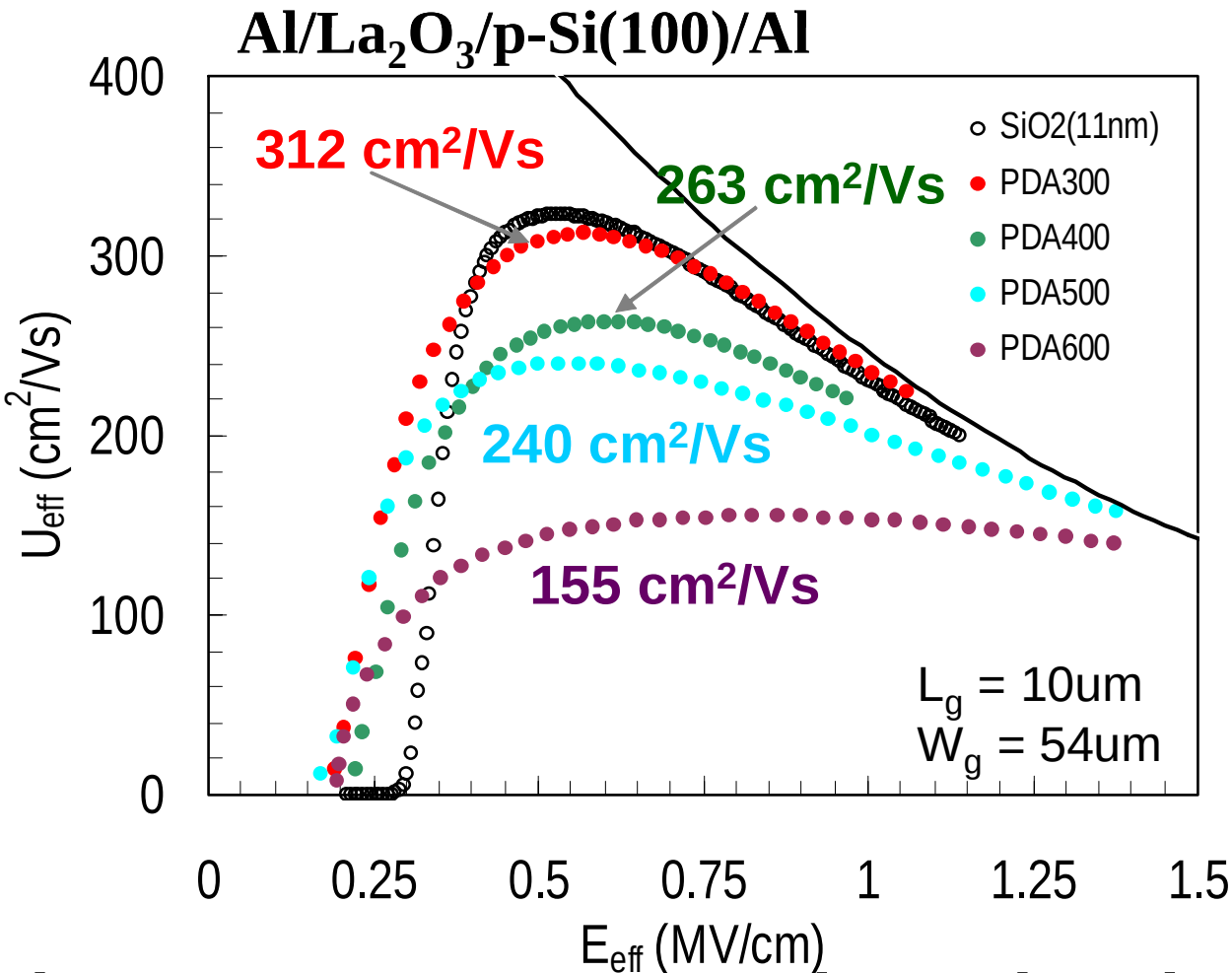
Effective Mobility of La2O3 MOSFET on PDA Temperature



Higher PDA temperature degrades the mobility

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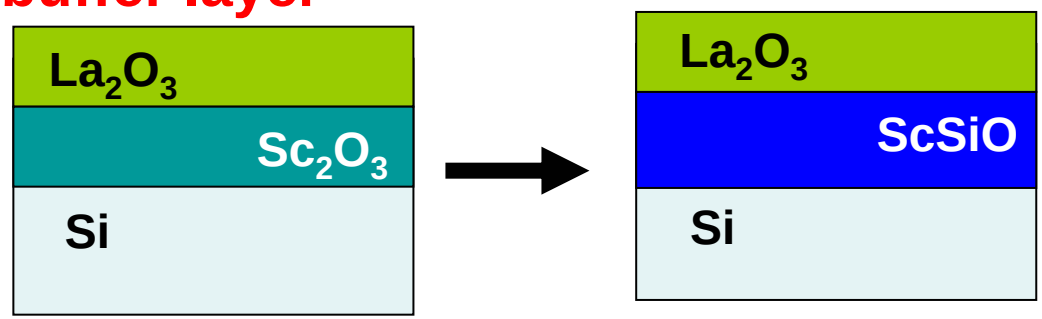
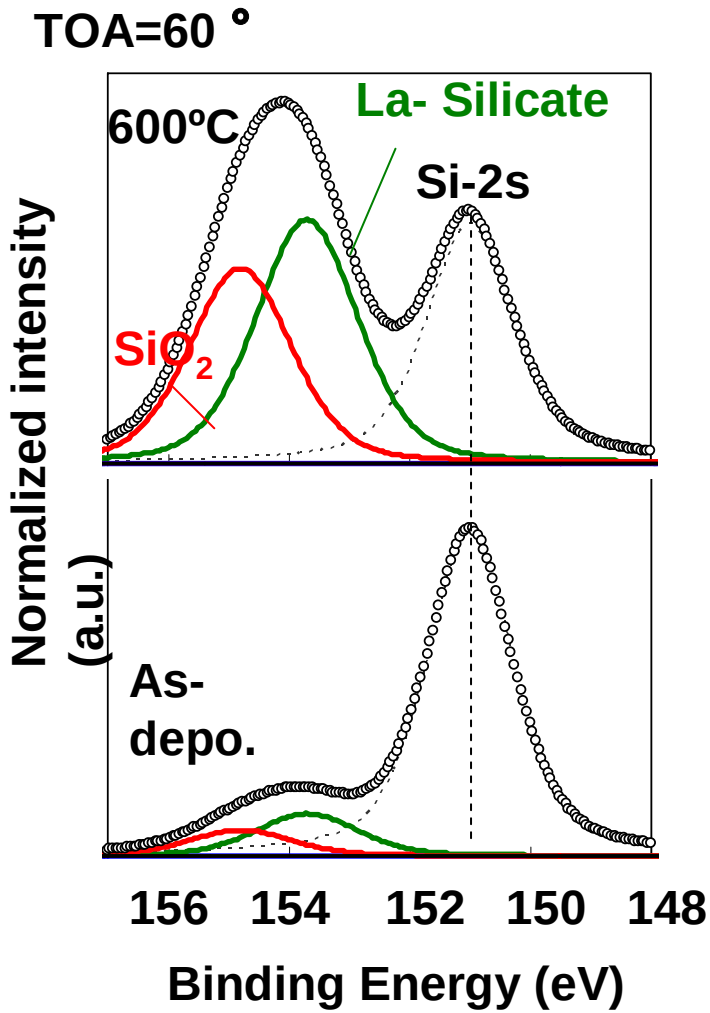
La_2O_3 Gate Insulator for High Temperature Process

High temperature annealing above 500°C

SiOx based interfacial layer formation
- **Increase in EOT**
- **Higher Dit**

Interfacial Layer Suppression using buffer layer





XPS analysis of La_2O_3/Si

Free Energy (kJ/mol)

Sc_2O_3 $\Delta G = -1901 + 0.287 * T$

Y_2O_3 $\Delta G = -1895 + 0.281 * T$

La_2O_3 $\Delta G = -1785 + 0.277 * T$

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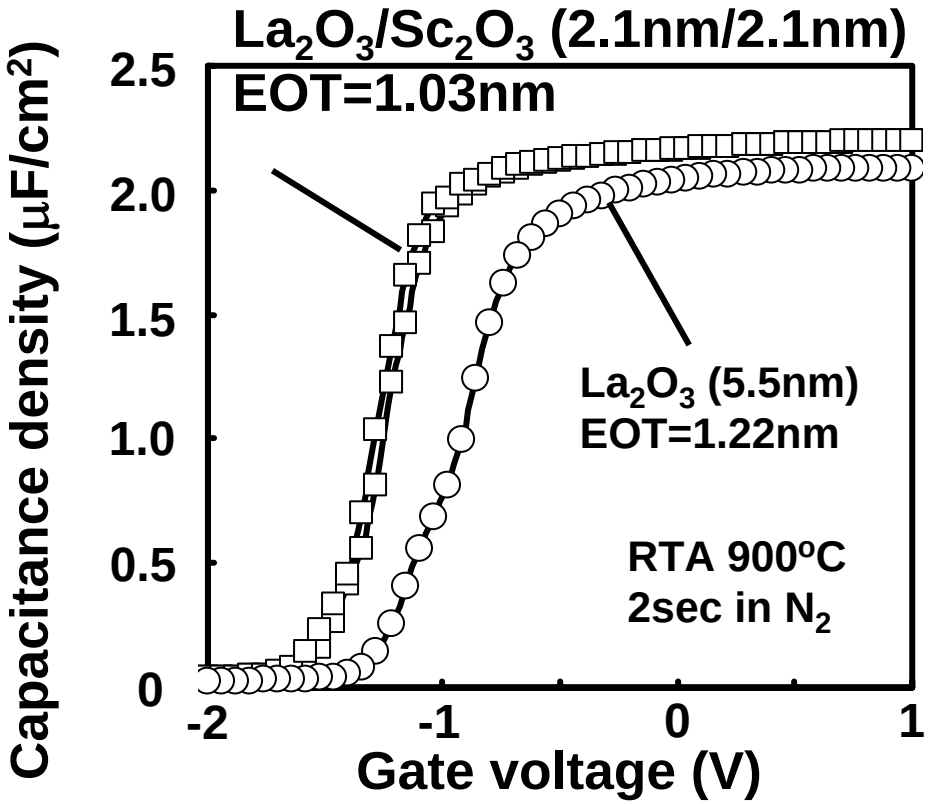
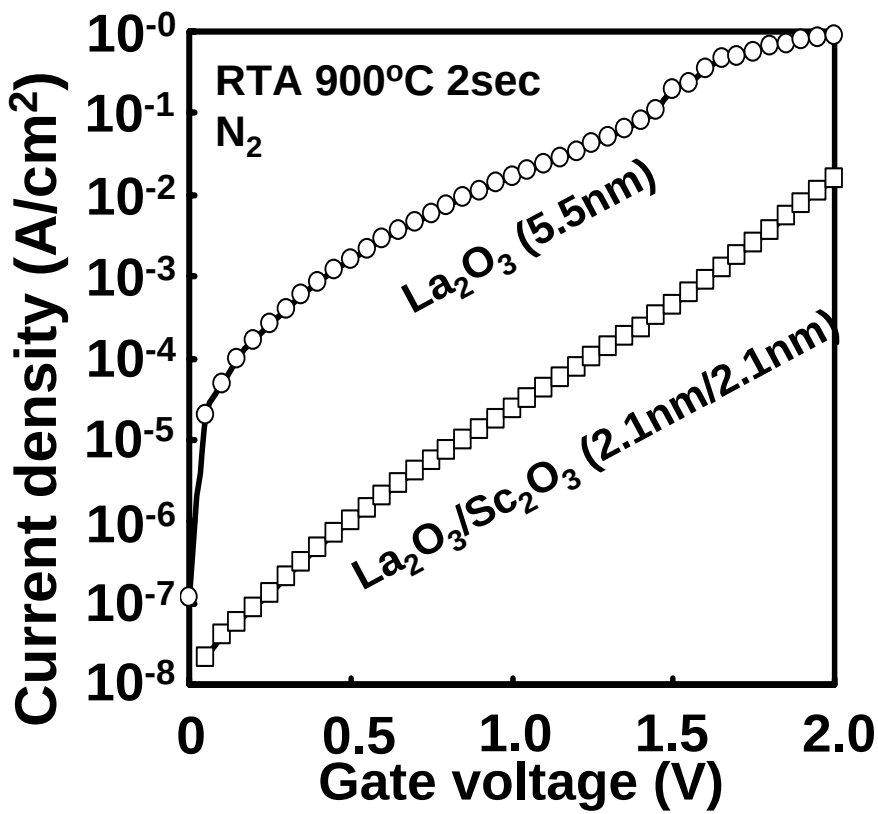
Sc_2O_3 Buffer Layer for High Temperature Process





Leakage current suppression without degrading the CV curve

High temperature stability can be obtained with Sc_2O_3 buffer layer

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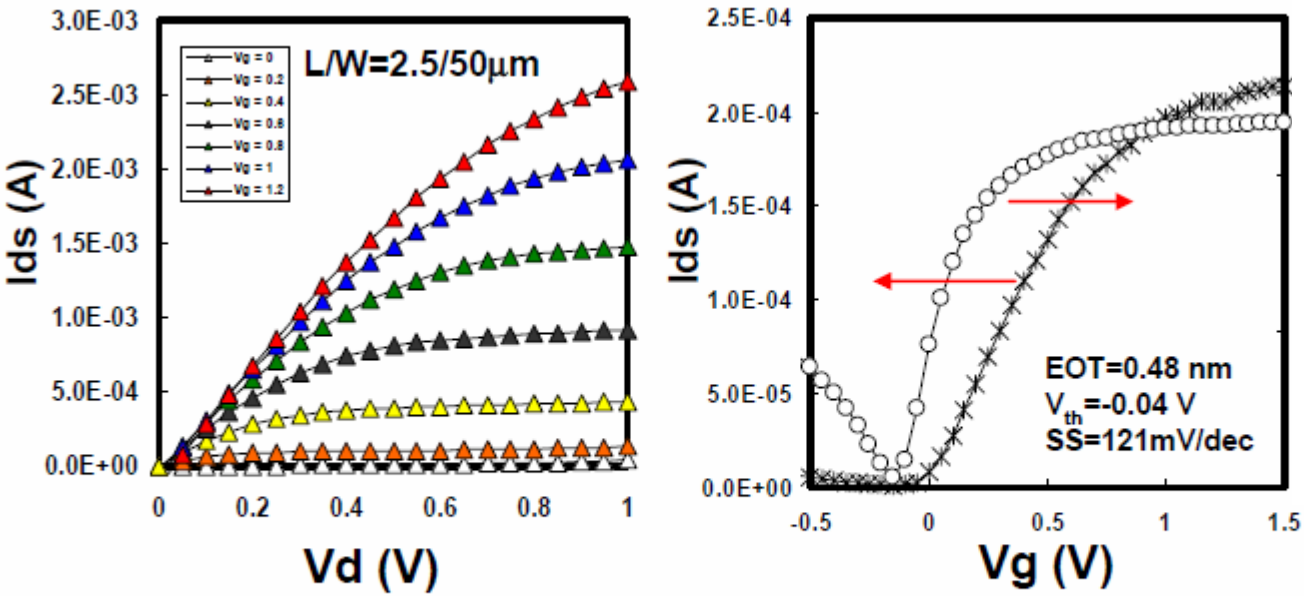
Submitted Symp. On VLSI, Yesterday



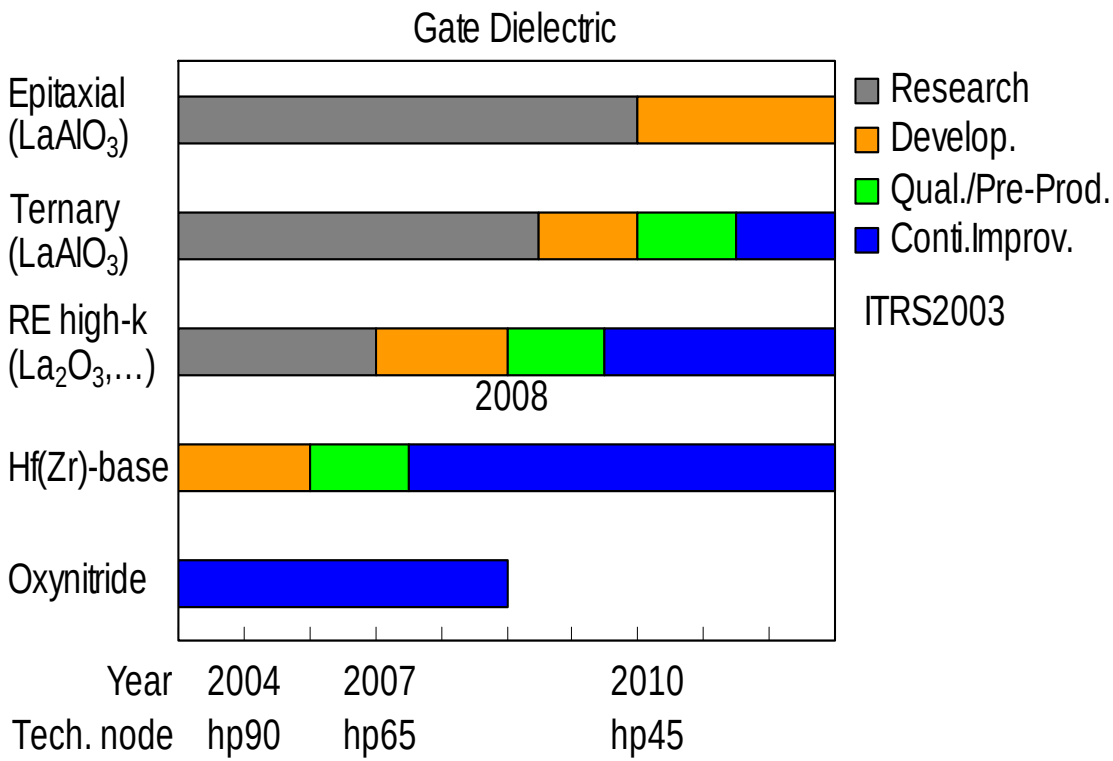
Electrical characteristics of W/La_2O_3 nFET with EOT=0.48 nm.

(a) W/La_2O_3, annealed at 300 °C (b)

Thinning EOT toward 0.5-0.7 nm

Keeping good mobility with thinning IL

→ **Searching new materials: La2O3 based**



ITRS 2003

Thank you!