Future Gate Stack Technology

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So far HfO_2 based gate dielectrics are being introduced to advanced logic integrated circuits from 45 nm commercial technology node, there are many issues for the high-k and metal gate stack for use for the next generation.

First of all, the current HfO_2 based oxides need intentionally grown interfacial layer in order to arrange a good interface between the silicon surface and the gate insulator, and hence to suppress the mobility degradation of the channel carrier of MOSFETs. This interfacial layer is typically made of SiO_xN_y and its typical EOT is 0.7 nm. Maybe the interfacial layer EOT could be reduced to around 0.5 nm. However, the SiO_xN_y interfacial layer will certainly prevent the total gate dielectric EOT reduction less than 0.7 nm almost impossible, and thus, direct contact of the high-k gate dielectrics with silicon would be inevitable. For the rare earth oxide material such as La_2O_3, we have already demonstrated very low interface state density of 6 X 10^{10} cm^{-2}, and nice peak mobility value of more than 300 $cm^2V^{-1}s^{-1}$ for channel electrons. However, this is supposed to be the hydrogen or maybe even OH termination effects of the dangling bonds at the Si surface. The hydrogen and OH are supposed to be introduced moisture absorption of water with the La_2O_3 exposure to air before the gate electrode deposition. The problem for this termination is that at least the interfacial concentration of the hydrogen decreases during the anneal at higher temperature above 300°C. Thus, the interface state density increases and the mobility degrades after higher temperature. Another problem is that higher temperature anneal around at 500°C make an interfacial silicate layer grow and this silicate layer increases the EOT of the gate oxide and interface state density. It is known that higher temperature annealing in hydrogen ambient decreases the interface state density, however the interfacial silicate layer formation is a problem.

Another way to improve the interfacial layer is to add other 3rd elements, such as Al. It seems that the Al repairs the oxygen vacancy and probably annihilates the interface states. We did confirm these effects but they are not sufficiently large at this moment and process optimization or maybe quest of more effective another 3rd element is necessary.

Further solution is to insert higher k interfacial layer than that of SiO_xN_y. Using Sc_2O_3 as the interfacial layer, we have achieved good suppression of the silicate interfacial layer growth at 500°C. However, interface state density between the Sc_2O_3 and Si is still necessary to be improved at this moment.

Fermi level pinning is another important factor to be considered. Eventually, the process temperature for the high-k will goes down to 400 ~ 500°C, as the gate stack process moves from ‘gate first’ to ‘gate last’ process and the Fermi level pinning effect will become less significant. However, it cannot be ignored. Addition of the 3rd element will be again a solution.

When, the EOT value of the gate insulator becomes less than 1 nm, the channel carrier mobility degradation due to the remote Coulomb and remote roughness scattering caused by the charge and roughness at the interface of high-k gate dielectrics and gate electrode becomes very significant. Thus, good mobility cannot be obtained without improving that interface.

For the middle and long term issues for the gate stack, we have to consider that the MOSFETs structure will change from planar to 3-dimensional structure, such as FinFET. Eventually, the FinFET will changes to nanowire MOSFETs, and maybe to CNT MOSFETs. Or maybe other semiconductor substrate such as GaAs or Ge could be used. Source and drain will be changed from semiconductor to metal. In the case of metal source drain, maybe process temperature could be decreased to 300~400oC, which would solve some critical issues of interfacial problems of high-k/semiconductor and high-k/metal gate. Some more details of gate stack for next 25 years will be explained.