Future of Silicon Integrated Circuit Technology

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Abstract:- CMOS technology has been developed into the sub-100 nm range. It is expected that the *nano-CMOS technology* will governed the IC manufacturing for at least another couple of decades. Though there are many challenges ahead, further down-sizing the device to a few nanometers is still on the schedule of International Technology Roadmap for Semiconductors (ITRS). Several technological options for manufacturing nano-CMOS microchips have been available or will soon be available. This paper reviews the challenges of nano-CMOS downsizing and manufacturing. We shall focus on the recent progress on the key technologies for the nano-CMOS IC fabrication in the next fifteen years.

1. Historical Review

Among numerous great inventions made in the 20th century, electronics is the most important one. According to a recent survey [1], "Electronic End Equipment' has become the base of all human political and economical activities staked a share of the world's total GDP of about 30,000 billion US dollars. Almost every thing related to human activities, such as power generation, transportation, entertainment, medical care, is now provided and controlled by electronics. Semiconductor, being the key component of the "Electronic End Equipment", is a strategically important technology for all countries (see Fig.1).

The electronic circuit development has been accomplished with the downscaling of component size since the replacement of vacuum tubes with transistors 40 years ago (see Fig.2) [2-3]. The circuit characteristics have benefited a lot from the downsizing. We are now able to integrate millions of *CMOS* transistors in the *nanoscale* in a silicon chip with few centimeters square. Right now the operation speed of the latest microprocessor has already reached 3 GHz and is expected to increase further [5] (see Fig.2), although recent trend indicates that the increase of the clock frequency may be gradually saturated. The CMOS integrated circuits as well as their core device technology are expected to evolve further for at least a couple of decades and their importance will be further increased in future intelligent society.

2. Challenges Ahead

The device dimensions have been reduced to a millionth at the production level in the past 100 years. Hundred years ago, no one could imagine that the mankind of our time is able to make some electronic circuits which consist of billions of electronic components with dimension smaller than bacteria and those circuits are controlling the operation of our society. Future scaling trends have been predicted by the International Technology Roadmap for Semiconductors (ITRS) [1] for 10 years up to 2018, when the physical gate length is expected to be 7 nm [2-4]. Gate oxide thickness should be two orders of magnitude smaller than that of the gate length. Right now we have 1.2-nm thick oxynitride film being used in production and it is expected the silicon dioxide equivalent thickness (EOT) will be reduced to 0.5 nm in 10 years later. Although it is demonstrated that a MOS transistor with 1.5 nm [6-7] and recently even 0.8 nm [8] oxynitride gate insulator is still functioning, many serious problems are anticipated when realizing a large scale integrated circuit with such a thin gate insulator. It is believed that the CMOS device downsizing is approaching the physical limit. The ultimate limit of the scaling is the distance of atoms in silicon crystals and that is about 0.3 nm [2-4] (see Fig.3).

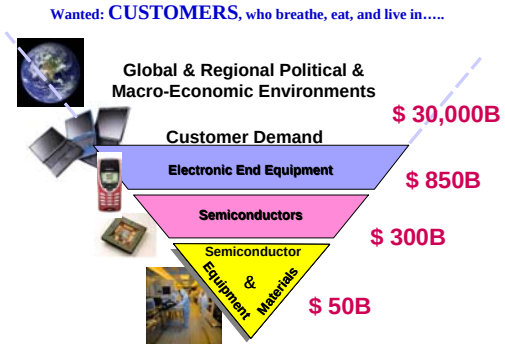


Fig.1 'Electronic End Equipment' is the base of all the human activities in the 'Global & Regional Political & Macro-Economic Environments' and 'Semiconductors' are the core components of these products.[1]

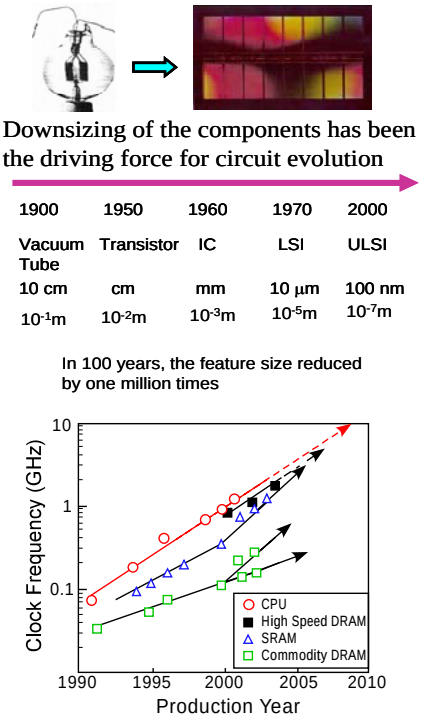


Fig.2 The downsizing trend of electronic components during the past century The device feature size has been reduced to a millionth since 1900 and the circuit has been developed from discrete circuits to the ULSI circuits with millions of transistors with operation speed over a couple of GHz.[2,5]

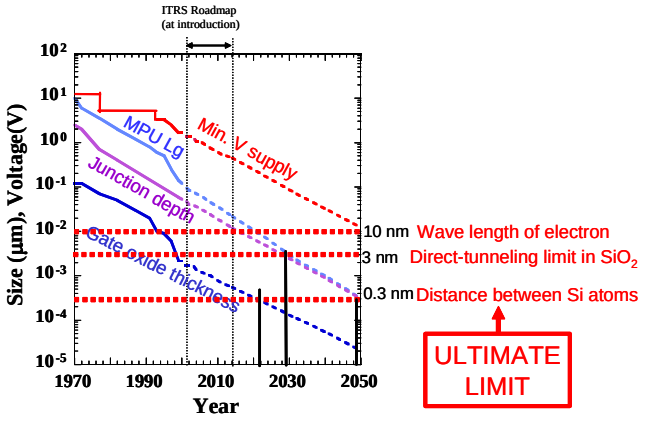


Fig.3 The downsizing trends on device parameters, possible constraints, and the ultimate limit of MOS transistors [2]

Performance Degradation: Device downsizing has benefited a lot in various aspects, such as speed, power, and cost, from downsizing of the MOS devices from 10 μm to the sub-100-nm range. When approaching the atomic scales, some performance degradations rather than improvements were reported. One of the major problems for performance degradation in the ultra-large scale circuits is the interconnect delay due to the increase in the resistance and the capacitance values of narrow and dense interconnection metal lines. Furthermore, the performance improvement is also questionable for the ultra-small MOSFET itself. According to the scaling theory, the drain current per unit gate width should stay constant. However, a significant reduction of the drain current value per unit gate width for sub-100 gate length MOSFETs was reported recently [2-4] (see Fig. 4). This phenomenon is due to the non-optimized MOSFET structure and process. On the other hand, the small drain current (of several tens of micro-Ampere per micrometer) at the scaled supply voltage becomes a major concern. Besides, the fringing capacitance of the gate electrode, and the inversion layer capacitance will also degrade the performance of the ultra-small MOSFETs [2-4] (see Fig.5). It is still doubtful at this moment for such a small MOSFET be used for high-speed devices. Hence, without new technology, further downscaling may only result in performance degradation [2].

New Technological Options: Performance enhancements can be achieved and further downscaling may be proceeded with the introduction of new technologies and materials at least for another 10 years and furthermore with that of three dimensional structures [1] (Fig.6). Several achievements in finding new materials and developing new process for sub-100 nm device manufacturing have been made recently. These processes or materials include the elevated source/drain [9-11], plasma doping with flash or laser annealing [12-14], NiSi silicide [15-16], strained Si channel for mobility enhancement [17-19], silicon on insulator (SOI) [20-22], three-dimensional structure [23-26] high dielectric constant (high-k) gate insulator [28-31], metal gate [33-34], and low dielectric constant (low-k) interlayer insulator for interconnects [35-36]. These measures are already on schedule for future technology nodes [37]. However, some unexpected device parameter degradations were reported with the new materials. High-k gate insulator is an example. Fortunately, scaling is not the only solution for performance improvement. The improved circuit structures and system architectures, such as parallel processing architecture and system-on-chip (SOC), optimized interconnect, can also make the integrated circuits to perform better. It is expected that the overall performance of our electronic system could be enhanced further at least down to the generation of 20 or 10 nm gate lengths as consequences of both the improved device technology and the new system structures.

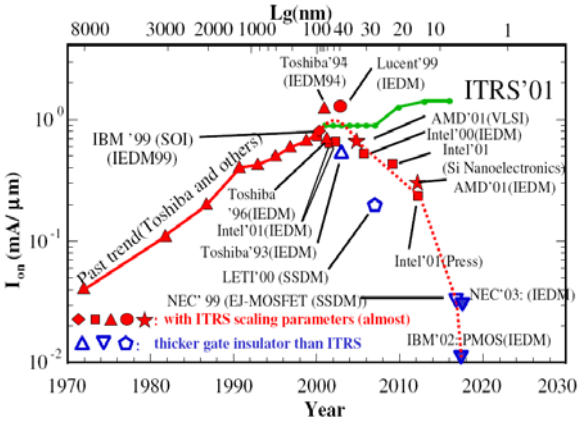


Fig.4 Significant reductions of the unit drain currents were reported in the sub-100 nm transistors which are diverged from the prediction of ITRS [1].

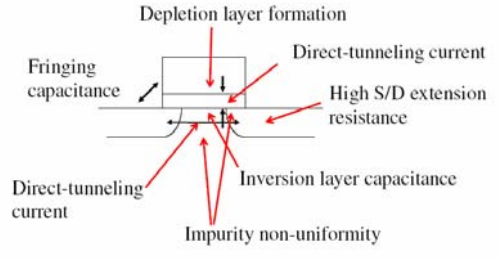


Fig.5 Challenging issues further downsizing of MOS transistor below sub-10 nm range [1].

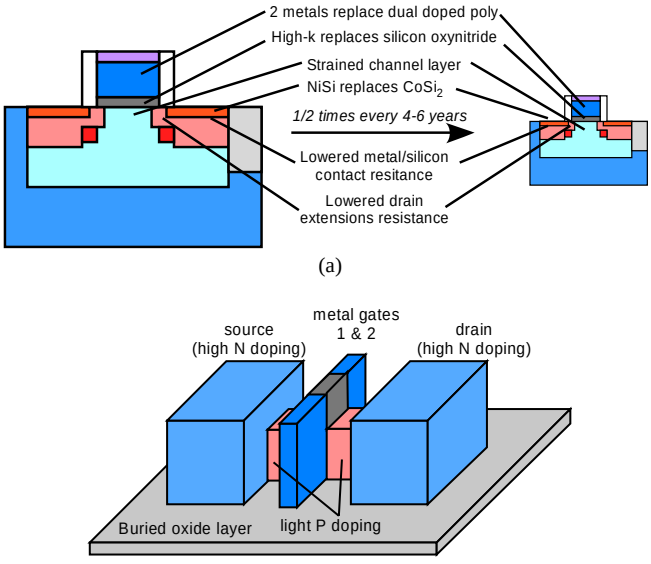


Fig.6 Scaling trend and challenges for some future technology node. The bulk MOS structure (a) can be further downscaled by introducing new materials. (b) Multiple gate or Fin-FET structure should be used to have a better control of the short-channel effects [1].

Options for Low Power: Increasing power consumption for high-performance logic integrated circuits is another serious problem. If the trends of the clock frequency and the chip density continue to increase, the power consumption of a high-performance MPU would reach 10 kW within several years and power density of the silicon chip surface may be as large as 1000 W/cm^2 which is equivalent to the level of a rocket nozzle surface [38]. The significant increase in power density is the consequences of the insufficient supply voltage reduction and the exponential increase in the transistor density. Low voltage technology (although is not easy) and appropriate control of the increase in chip density and chip size together with some new cooling technologies may partially solve this problem. In addition, some innovative system power management methods, such as variable clock frequency and variable voltage supply, will also help in this issue. On the other hand, the gate leakage current can be reduced by using a physically thicker high-k gate dielectrics and the subthreshold leakage current can be suppressed by using a three-dimensional (3D) structure, such as fin-FET [1] (see Fig.6)). Those measures would be introduced for low standby-power devices even earlier than the high performance logic units as soon as the reliability of the process and fabricated devices become established and the fabrication cost becomes reasonable.

3. IC Manufacturing in the Next 15 Years

Most technological options for manufacturing CMOS ICs with some 10-nm transistors are already available. We have EUV (Extremely Ultra Violet), e-beam lithography technologies for patterning gate length below 25 nm. Recently it was found that immersion with 193 nm wave length ArF laser can also be used for the 'commercial 32 nm' (HP45 nm) node [39]. We are able to fabricate sub-nanometer EOT gate dielectric film by using transition metal oxide or rare-earth metal oxide desipte it was found that the interface between the gate dielectric and silicon substrate is still quite poor.

The ultra-shallow junctions required for nano-CMOS can be achieved with low-energy plasma doping (PD) with flash or laser annealing. PD has several advantages such as high doping current, low implant energies, short process time, and low cost. In addition, the PD process is particularly suitable for ultra-shallow junction application [12,14].

Another concern for nano-CMOS fabrication is the increase of the contact resistance [40]. Nickel silicide can be readily formed with a simple single-step annealing at 400 to 600 ^{o}C will be a strong candidate for source and drian contacts of nano-CMOS. [15, 41-42]. In addition, it has advantages of less Si consumption and good ohmic contact.

Better device structures were also developed. To suppress the sub-threshold leakage current, introduction of SOI and double gate (DG) structures such as Fin- or Tri-gate FETs for the sub-20 nm gate length region [25-26] is highly possible. DG-FET or Fin-FET is considered as the ultimately scalable MOS device structure. It minimizes the short-channel effects with 2D or 3D conformed electric field. It relieves the channel doping level for punch-through control. Because of the reduced the channel doping the mobility in the DG-FET and Fin-FET can be theoretically enhanced. However, there are some technical problems which degrade the mobility and conductance of the fin-FET, such as non-strait etching and surface roughness of the fin, and higher source/drain resistance because of the narrow fin itself.

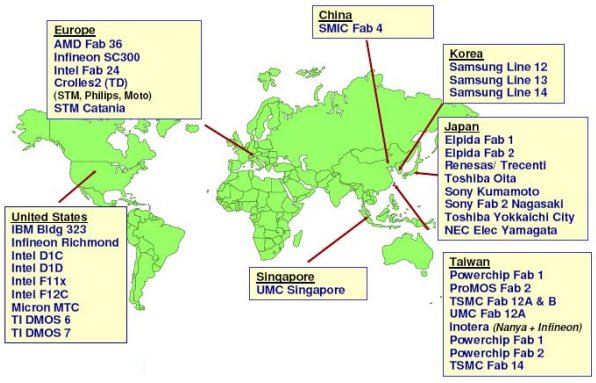
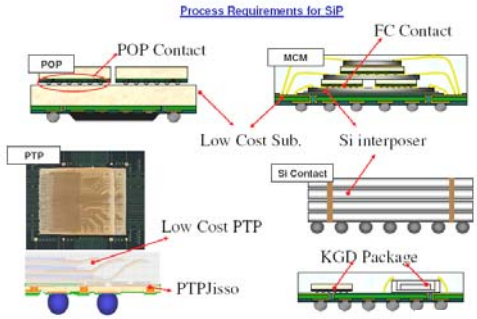
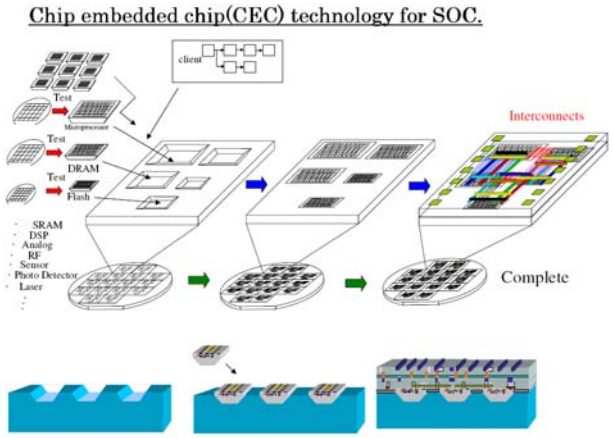


Fig.7 The global distribution of 300 mm Fabs. Number of Fabs is expected to increase in East and Southeast Asia and eventually dominates the world semiconductor manufacturing [19].



(a)



(b)

Fig.8 New packaging technologies such as system-in-package (a), chip-embedded-chip (b) will be the major driving force for performance booster for future large scale systems [1, 43].

Regarding the interconnect issue, introduction of lower-k materials for interlayers of interconnects should be a good solution in principle. However, it still faces some severe technical difficulties. The fundamental issues are the fragility, chemical resistance and the

pattenability of the low-k materials. Although there is a significant progress recently in achieving the effective-k value below 3 such as SiOC, polymer and porous films, the progress of low-k material application may lag behind the ITRS prediction.

Chip density up-scaling and interconnect complexity are other major issues for the next decade nano-CMOS technology. These issues can be solved with new packaging methods such as SOC (System-on-Chip) and/or SIP (System-in-Package) [43] (see Fig.8(a)). These techniques will be introduced after or even before the ultimate scaling limit because of better yield control and more cost effective. This approach will significantly reduce the signal delay between the chips because it can greatly reduce the large parasitic capacitances from bonding pads, bonding wires, and package pins. It saves power, reduces the wiring cost and increases the system performance.

4. Concluding Remarks

Silicon MOSFETs have been the smallest electronic device for several decades. Thirty five years ago, the gate oxide thickness was already in the nanoscale (120 nm) for commercial products. The gate oxide thickness is now 1.2 nm in production and 0.8 nm in research. The gate length used for high performance MPU and logic unit is 50 nm in production and 5 nm in research. Note that the 5-nm gate length is the distance of 18 atoms and 0.8-nm oxide thickness is two atomic layers only [8]. Si technology is no doubt the most successful nano-devices. We do not see that there is any realistic replacement for silicon devices. Even the Si devices reach the downsizing limit no matter 10 nm, 5 nm, or 1 nm, other emerging devices such as molecular transistors will also reach their limit of downsizing in similar dimensions.

It is a critical period for moving from 100-nm to 10-nm technology within this decade. Most of materials and the manufacturing processes used in the deep-submicron era are now pushing to their physical limits. New materials and technologies are required for further down-scaling the device to 10-nm technology and below. Immersion lithography for ultra fine patterning, strained channels, nickel salicide, high-k gate dielectric, low-k interlayer for interconnect, plasma doping, flash and laser annealing for source and drain doping, elevated source and drain and three-dimensional MOSFETs for controlling short-channel effects, would help to overcome the materials and technological constraints and improve the device performance in the ultra-small scale.

The final remark is a non-technical issue. We anticipate that this issue will be one of the most important issues for nano-CMOS technology development in the next 15 years. We are aware that most of the new mega-fabs being planned or under construction are in the East and Southeast Asia, and particularly the Mainland China. In 10 or 15-year's time, the distribution of semiconductor manufacturing sites in Asia (including Japan) will be quite substantial. Currently, Korea and Taiwan are in the first place for semiconductor memory manufacturing and semiconductor foundry, respectively. They also lead the technology development in Asia region. Mainland China seems to be another super power for semiconductor manufacturing. The share of China semiconductor manufacturing will keep fast growing with the support of booming IC design houses, constructing new fabs with remarkable increase in industrial investment, and will be the most important huge and rapidly expending market. As many other industries and other sectors of electronic products, Mainland China will eventually become "the factory of the world" in semiconductor manufacturing in 15 years or longer and will have great impact on the future nano-CMOS technology.

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