Future of Nano-CMOS Technology

June 4, 2007

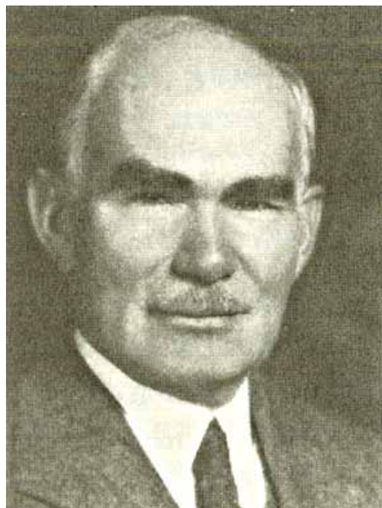
Tokyo Institute of Technology, Japan
Hiroshi IWAI

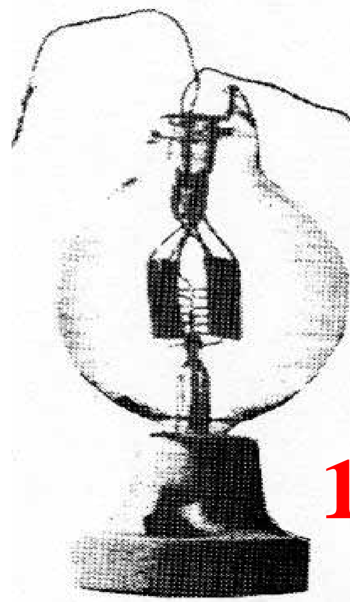
- Electronics is the

  Most important invention in the 20th century
- Electronics: Electronic Circuits or IC
- Electronic Circuits in 100 years

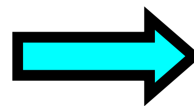
  Vacuum tube → ULSI

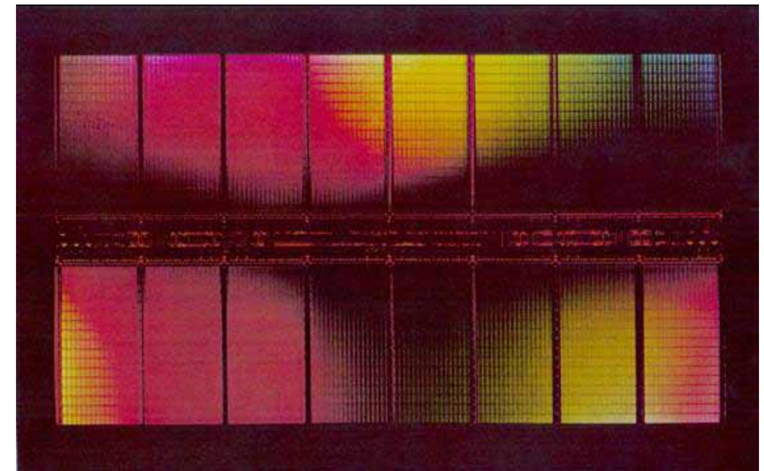
Last year was 100 year anniversary



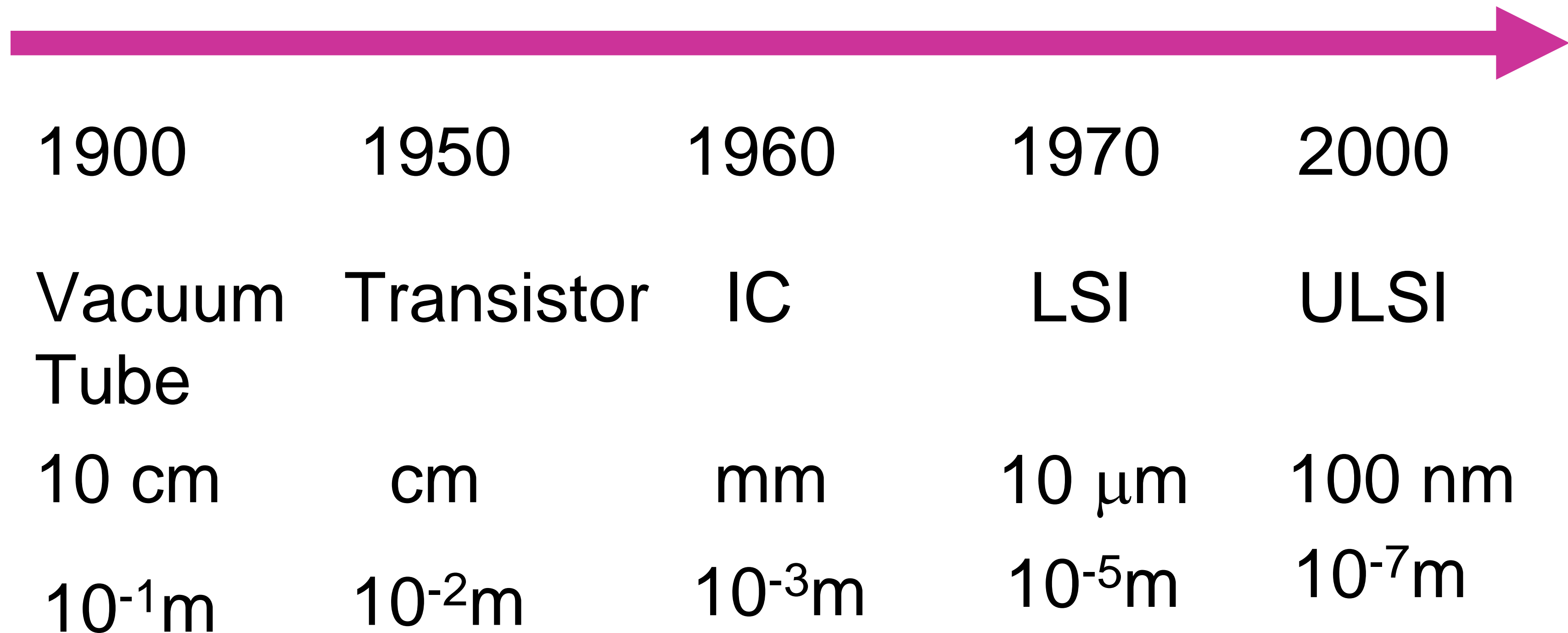


1906





Downsizing of the components has been the driving force for circuit evolution



In 100 years, the feature size reduced by one million times.
We have never experienced such a tremendous reduction in human history.

Downsizing

1. **Reduce Capacitance**

→ **Reduce switching time of MOSFETs**

Reduce power consumption

2. **Increase number of Transistors**

Increase functionality

→ Parallel processing

→ **Increase circuit operation speed**

Thus, downsizing of Si devices is the most important and critical issue.

Nano-CMOS:

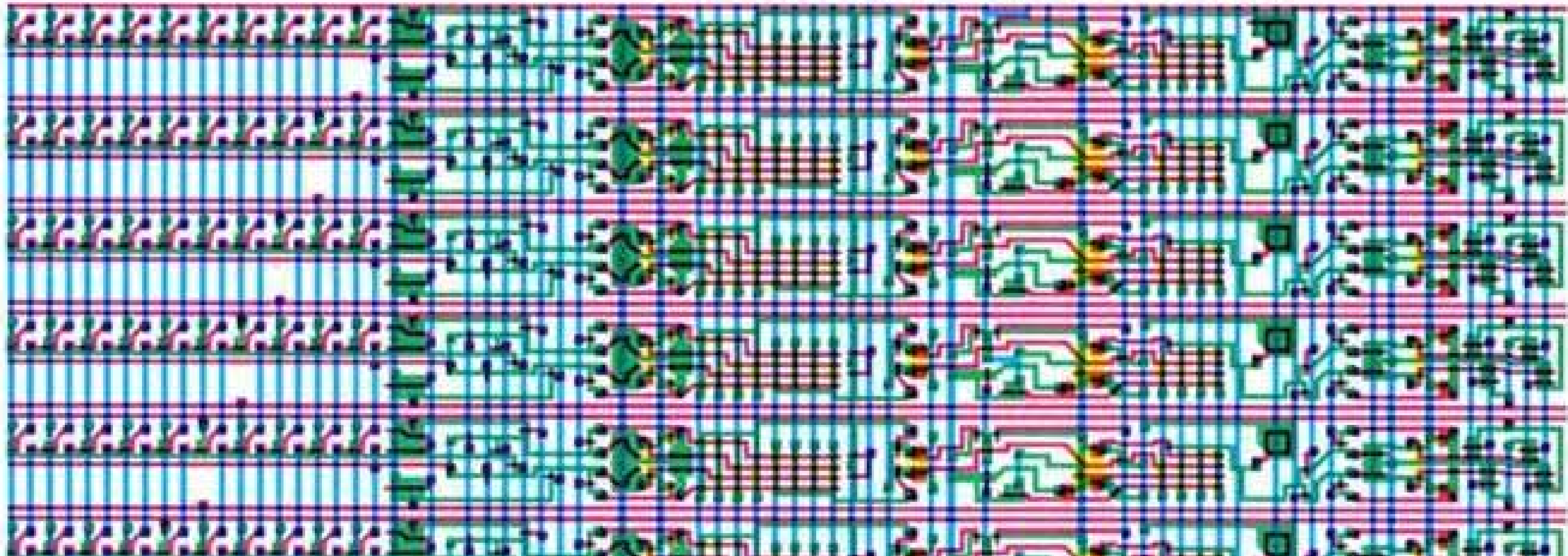
What would be the downsizing limit?

Many people wanted to say about the limit. Past predictions were not correct!!

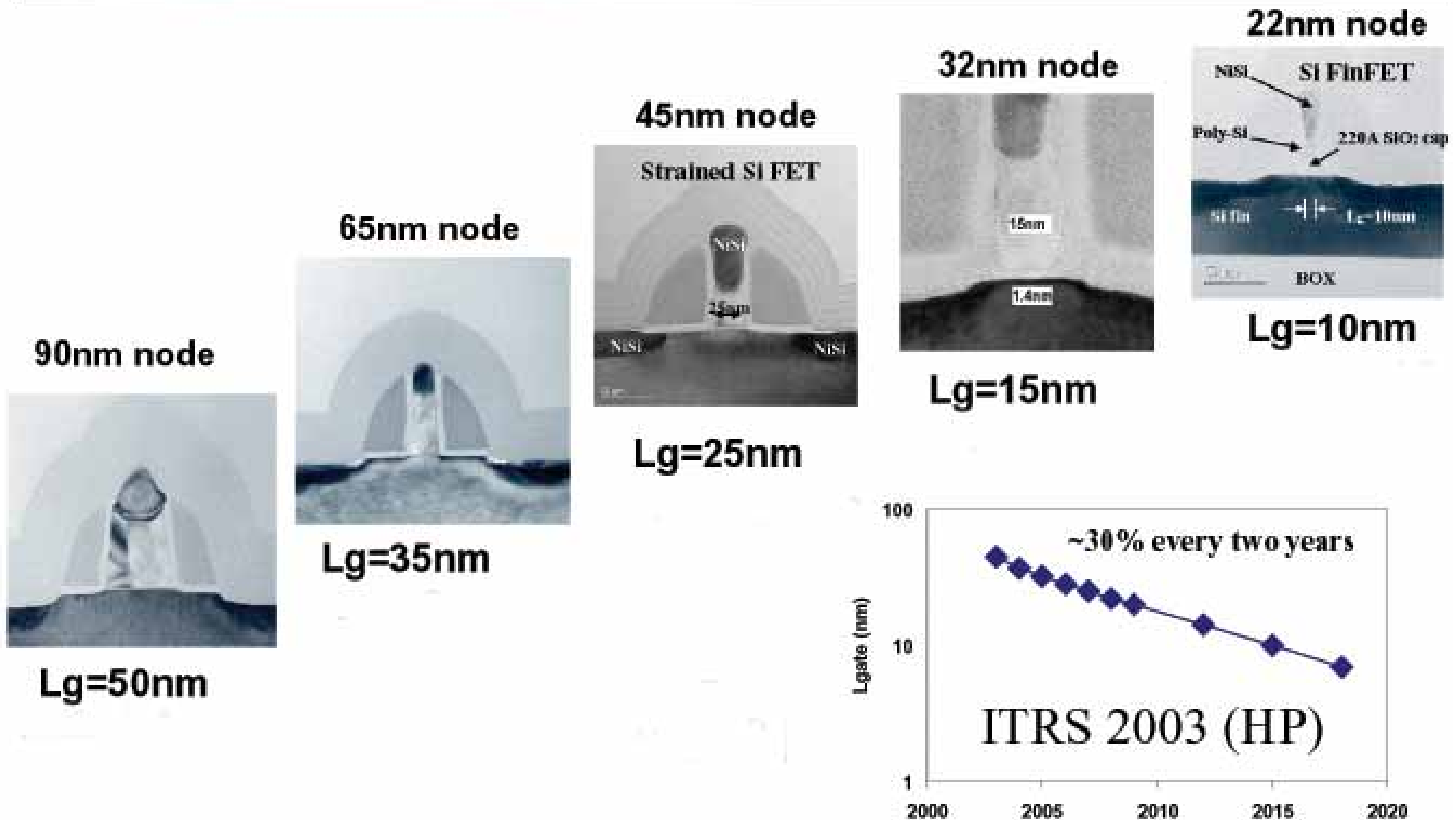
Period	Expected limit(size)	Cause
Late 1970's	1μm:	SCE
Early 1980's	0.5μm:	S/D resistance
Early 1980's	0.25μm:	Direct-tunneling of gate SiO_2
Late 1980's	0.1μm:	'0.1μm brick wall'(various)
2000	50nm:	'Red brick wall (various)
2000	10nm:	Fundamental?

Historically, many predictions of the limit of downsizing.

VLSI text book written 1979 predict that 0.25 micro-meter would be the limit because of direct-tunneling current through the very thin-gate oxide.



Transistor Scaling Continues

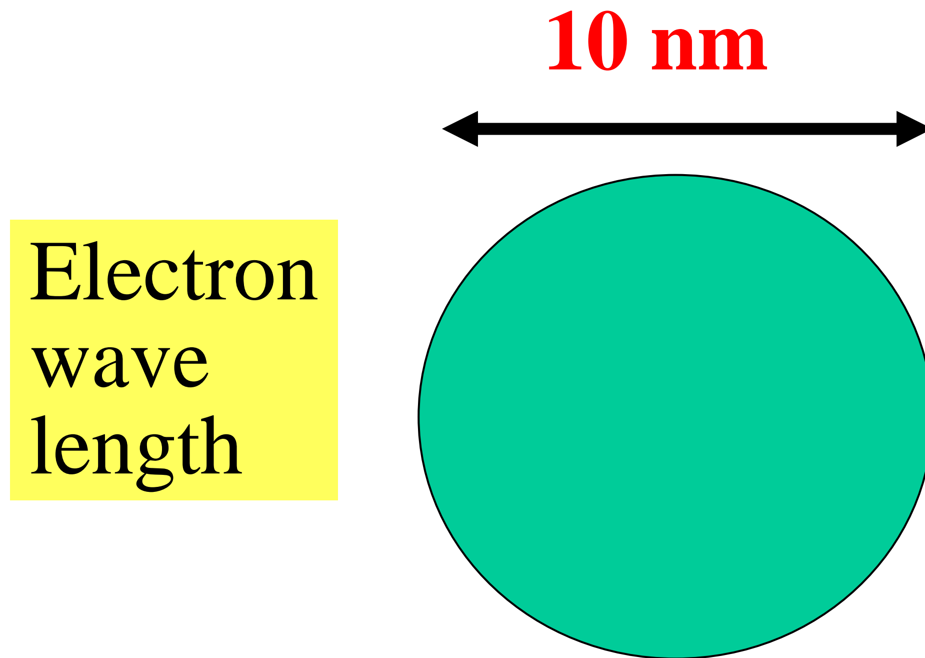


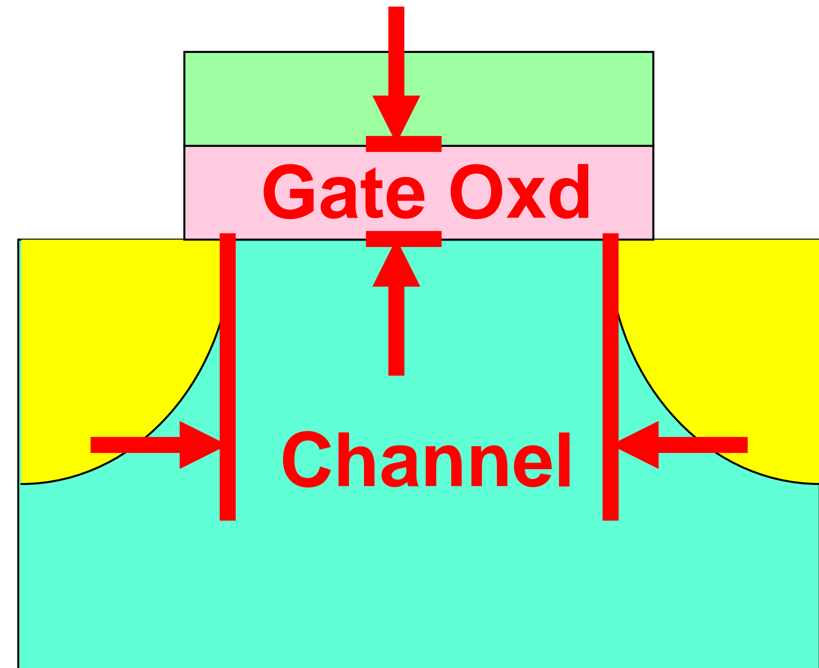
Qi Xinag, ECS 2004, AMD

Downsizing limit?

Channel length?

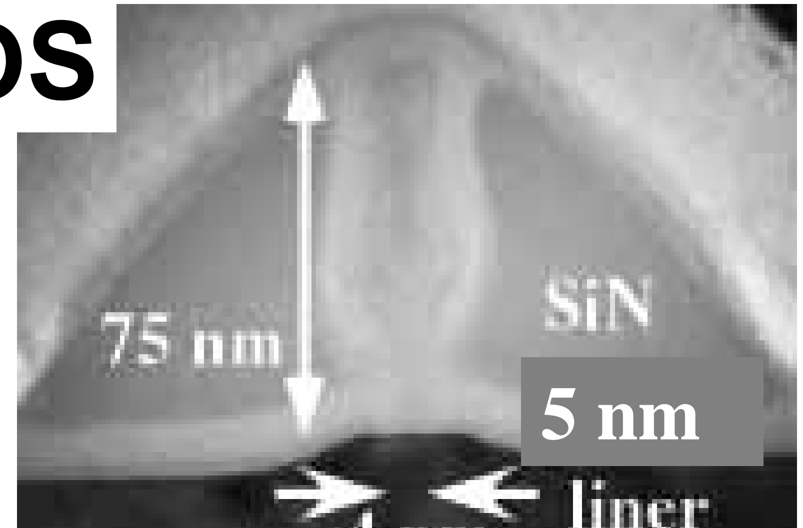
Electron wave length



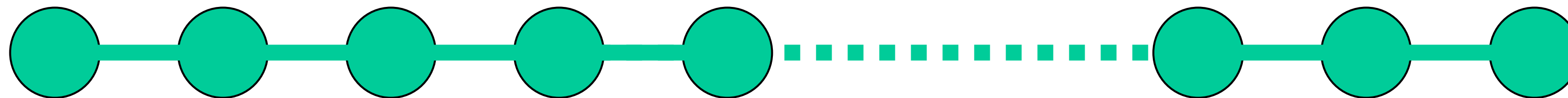


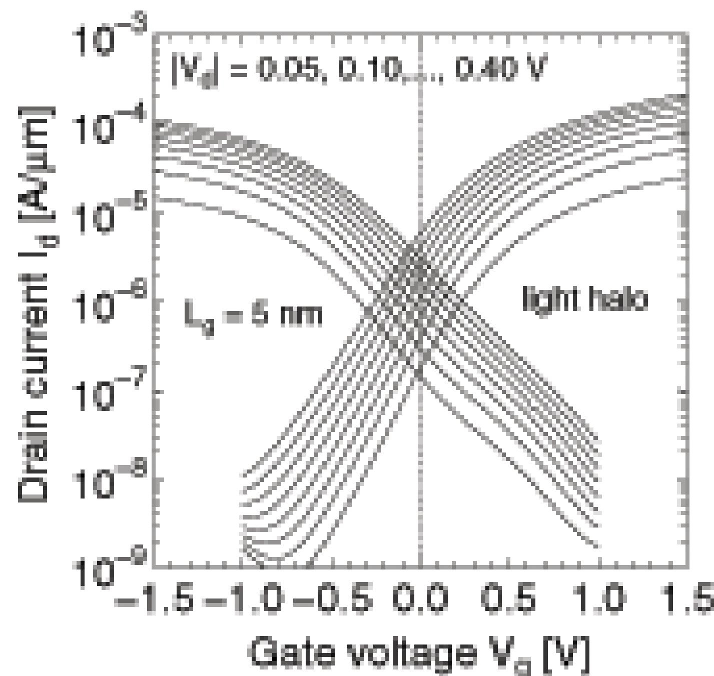
5 nm gate length CMOS

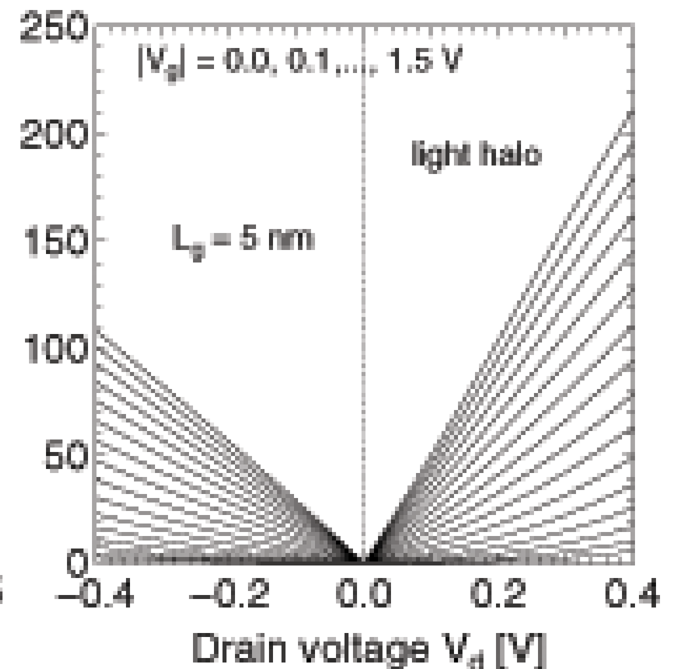
Is a Real Nano Device!!



Length of 18 Si atoms





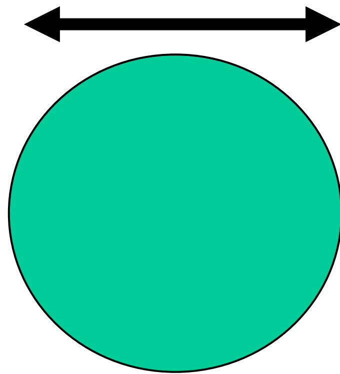


H. Wakabayashi et.al, NEC

IEDM, 2003

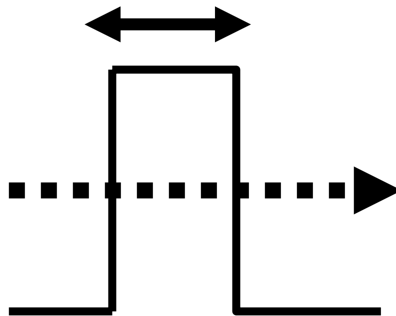
Electron wave length

10 nm



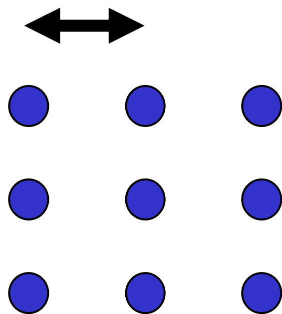
Tunneling distance

3 nm



Atom distance

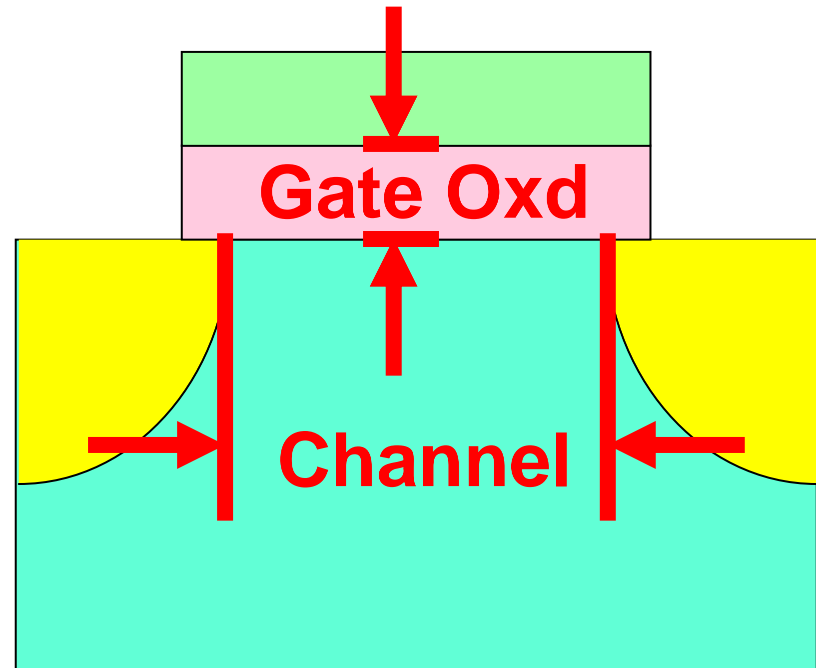
0.3 nm



Downsizing limit!

Channel length

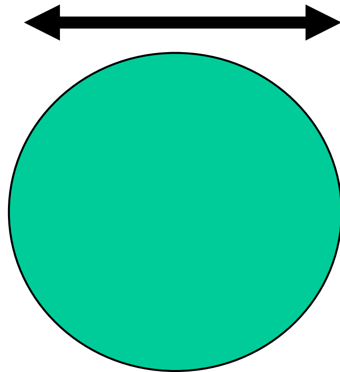
Gate oxide thickness



Prediction now!

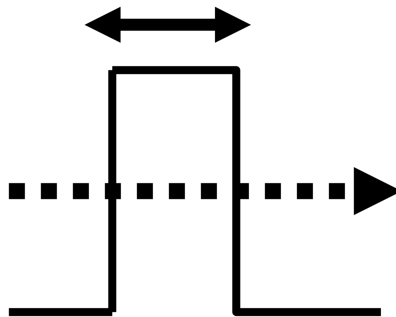
Electron wave length

10 nm



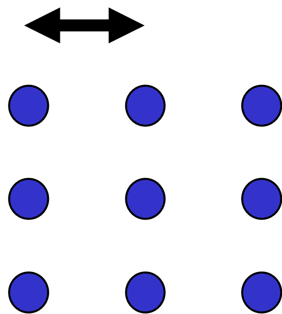
Tunneling distance

3 nm



Atom distance

0.3 nm



MOSFET operation

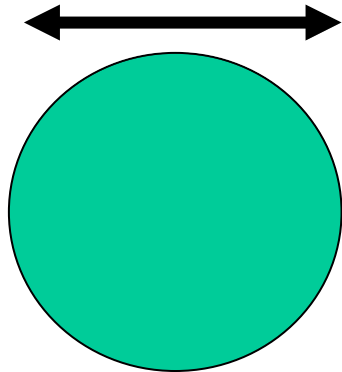
Lg = 2 ~ 1.5 nm?

But, no one knows future!

Prediction now!

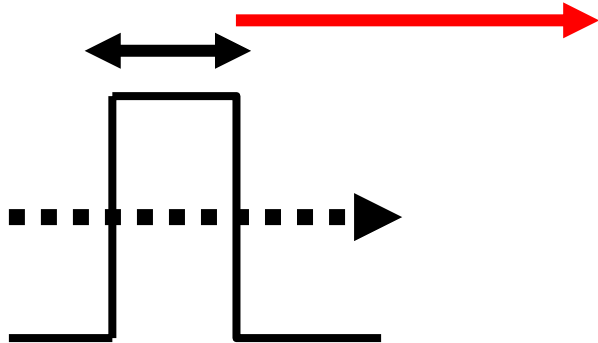
Electron wave length

10 nm



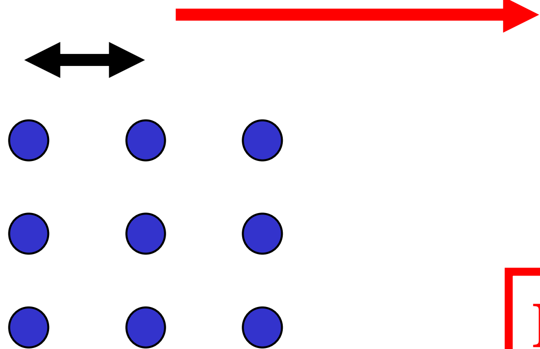
Tunneling distance

3 nm



Atom distance

0.3 nm



Gate length

Prediction at present

Practical limit because of off-leakage between S and D?

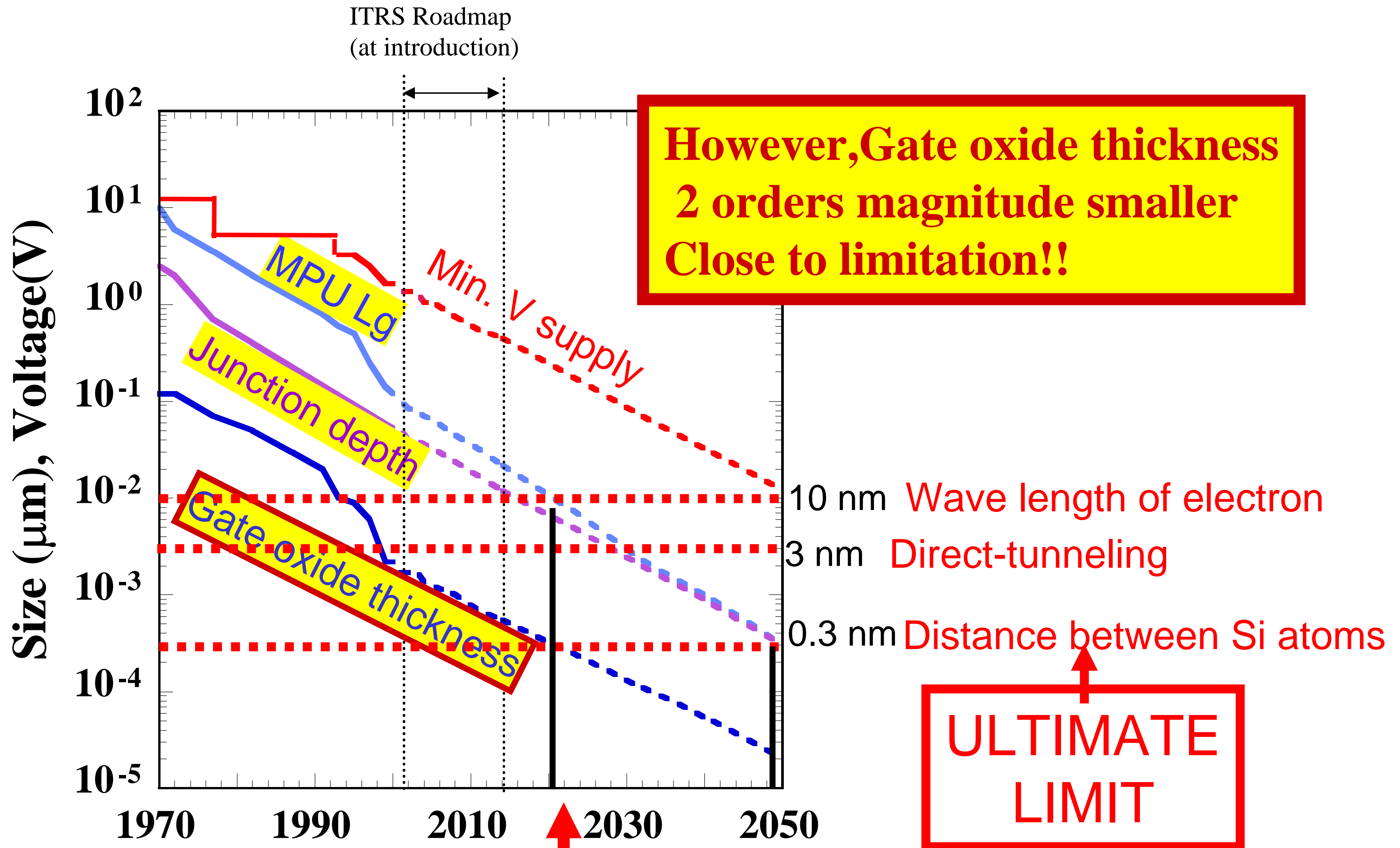
Lg = 5 nm?

MOSFET operation

Lg = 2 ~ 1.5 nm?

But, no one knows future!

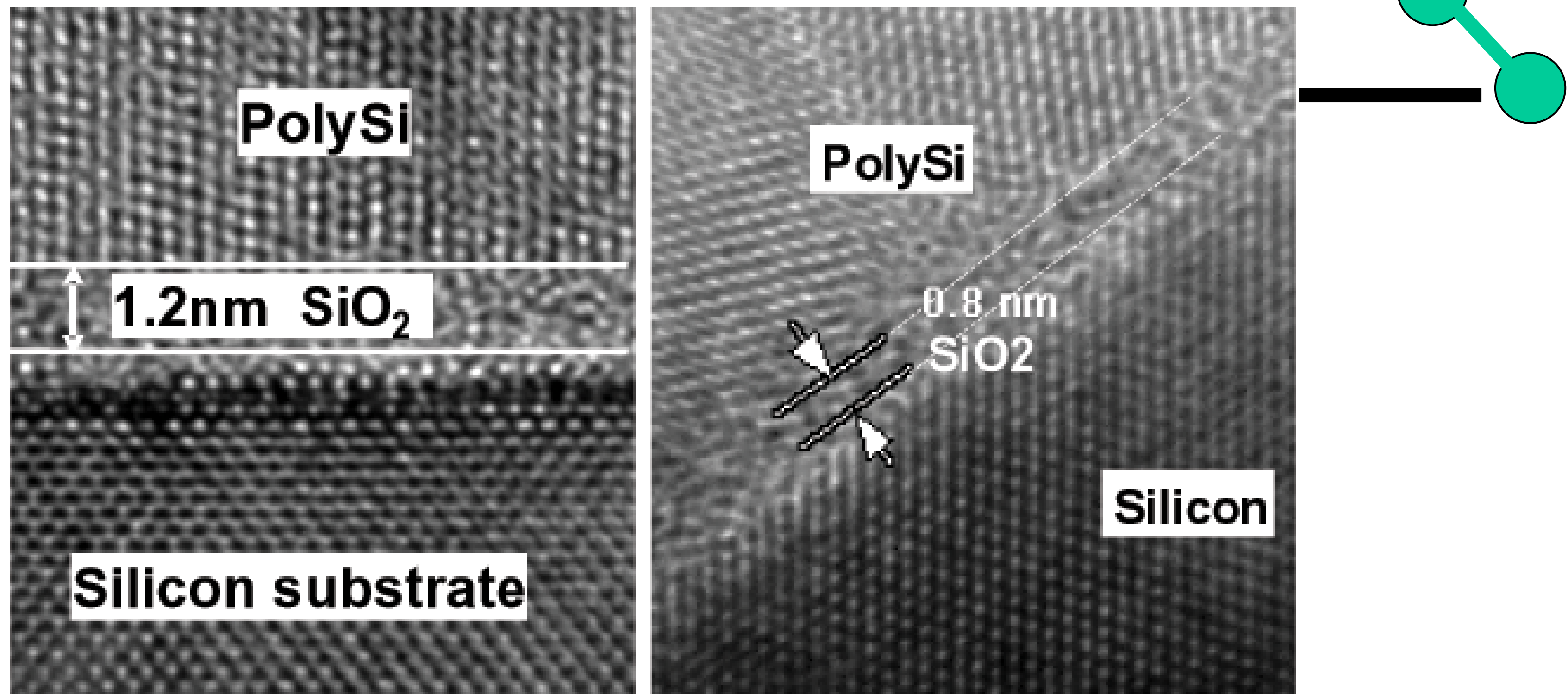
Ultimate limitation



Lg: Gate length downsizing will continue to another 10-15 years

0.8 nm Gate Oxide Thickness MOSFETs operates!!

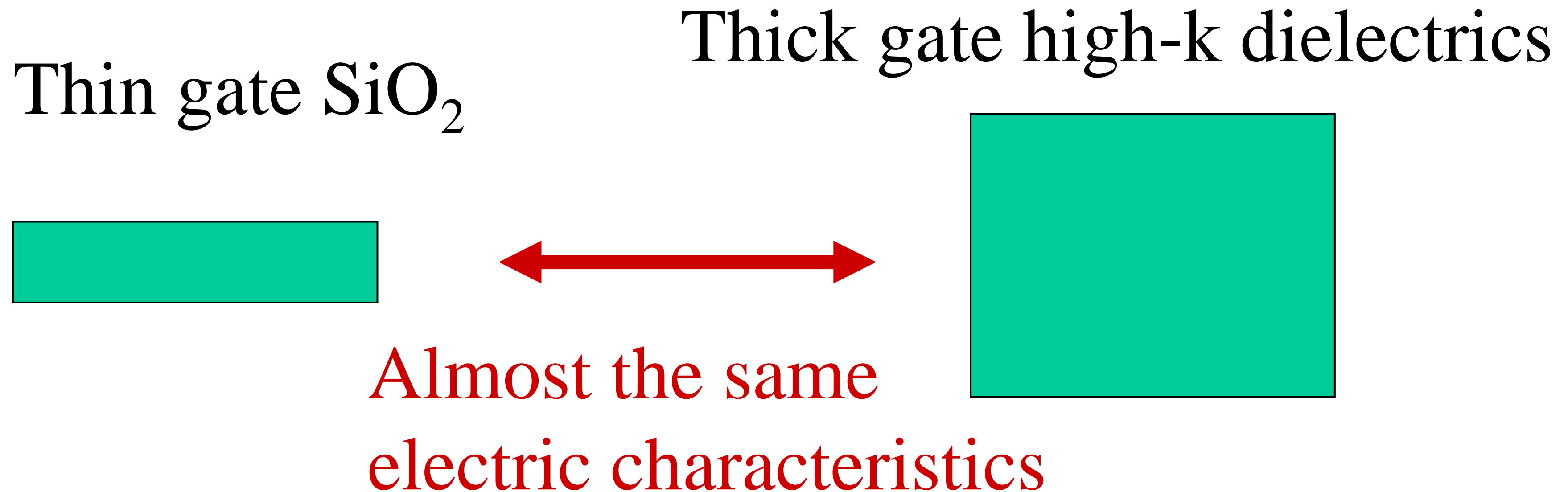
0.8 nm: Distance of 3 Si atoms!!



- 1.2nm physical SiO2 in production (90nm logic node)
- 0.8nm physical SiO2 in research transistors

By Robert Chau, IWGI 2003

There is a solution!
To use high-k dielectrics

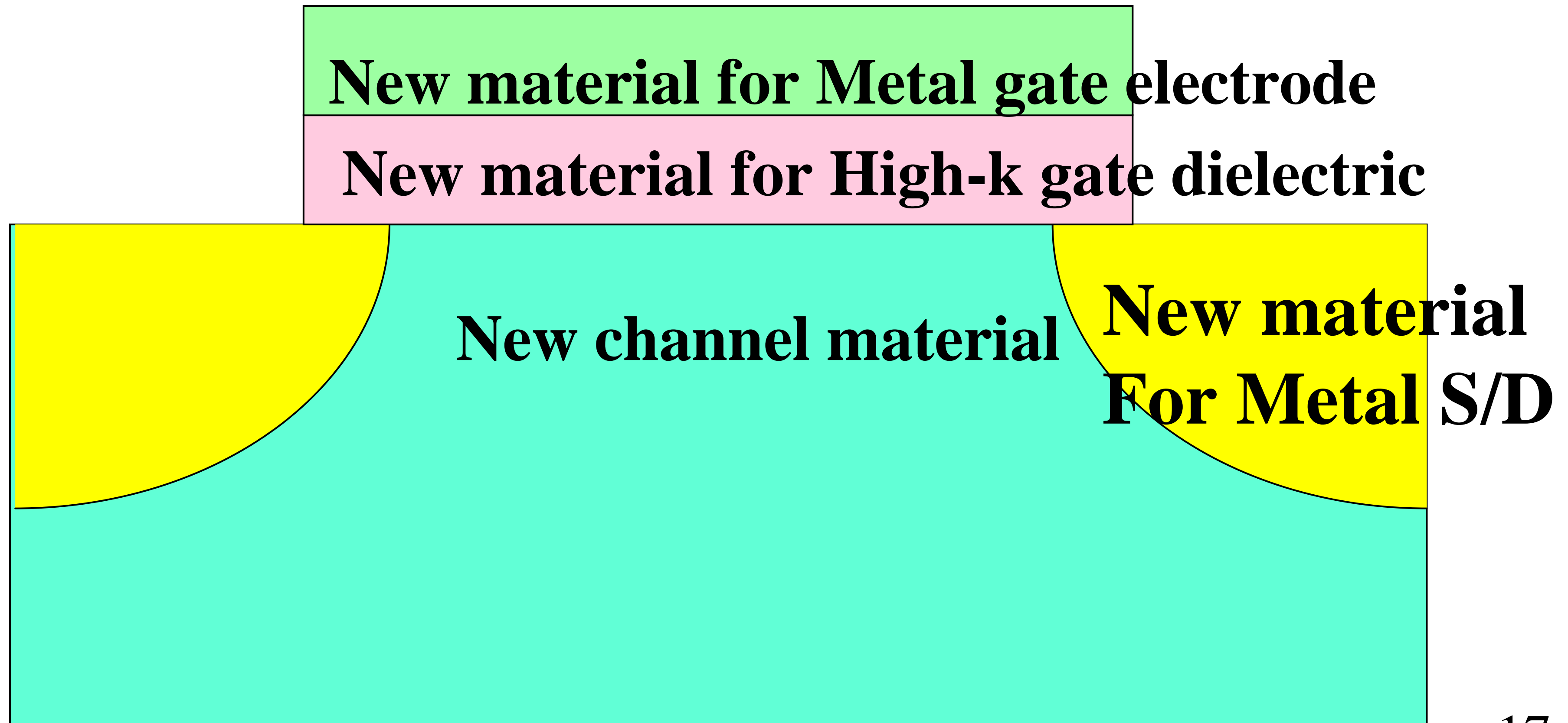


However, very difficult and big challenge!

Remember MOSFET had not been realized without Si/SiO_2!

New material research will give us many future possibilities and the most important for Nano-CMOS!

Not only for high-k!



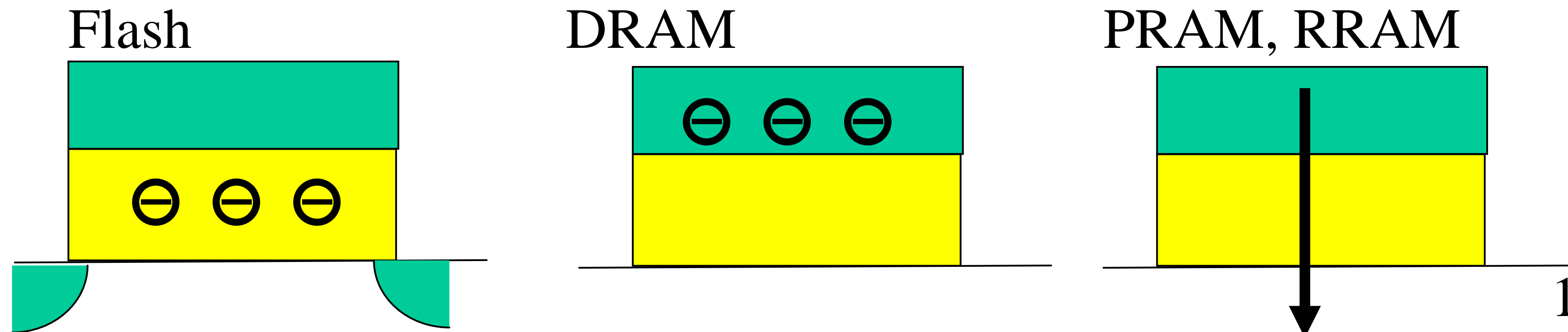
New materials are important for Not only nano-CMOS logic MOSFETs, But also for new memories!

Limit of high-density memories, such as flash, DRAM will be solved by new materials.

Flash: floating gate → gate insulator charge trap like SONOS, MNOS

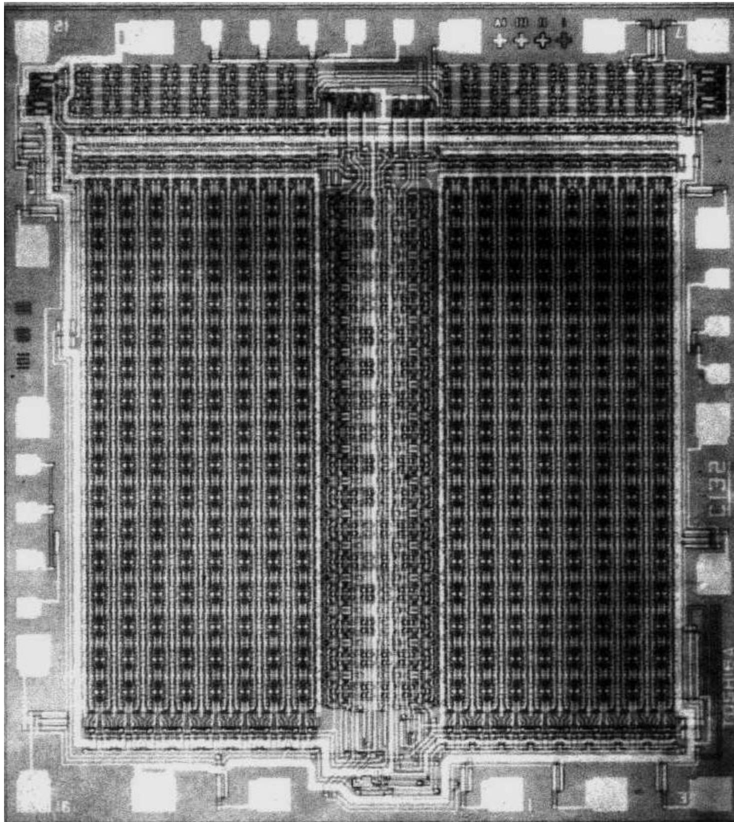
DRAM → New high-k insulator

New memory → PRAM, RRAM

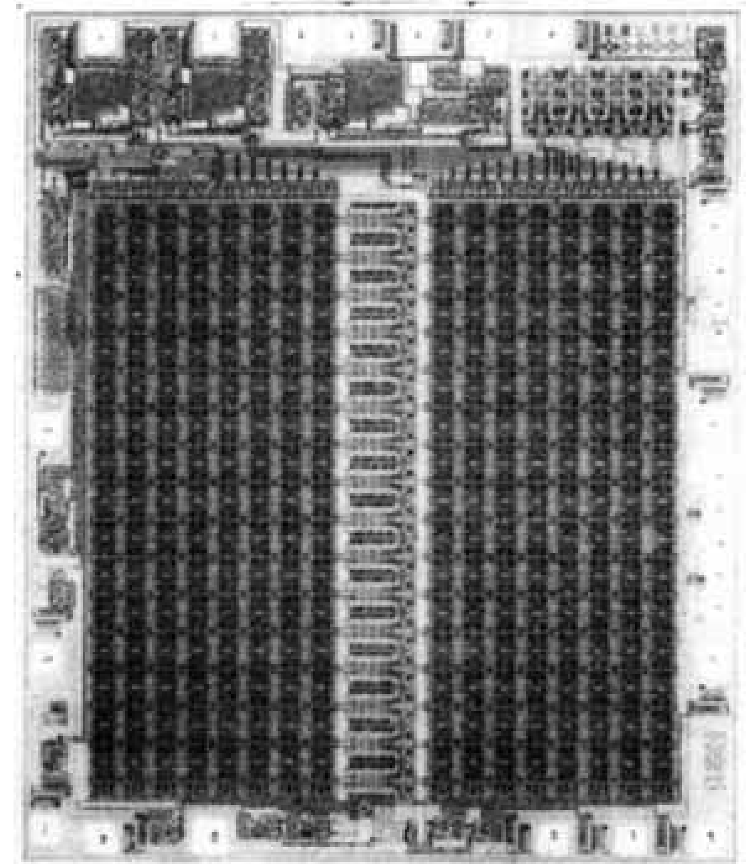


1970s: 10 years after single MOSFETs,

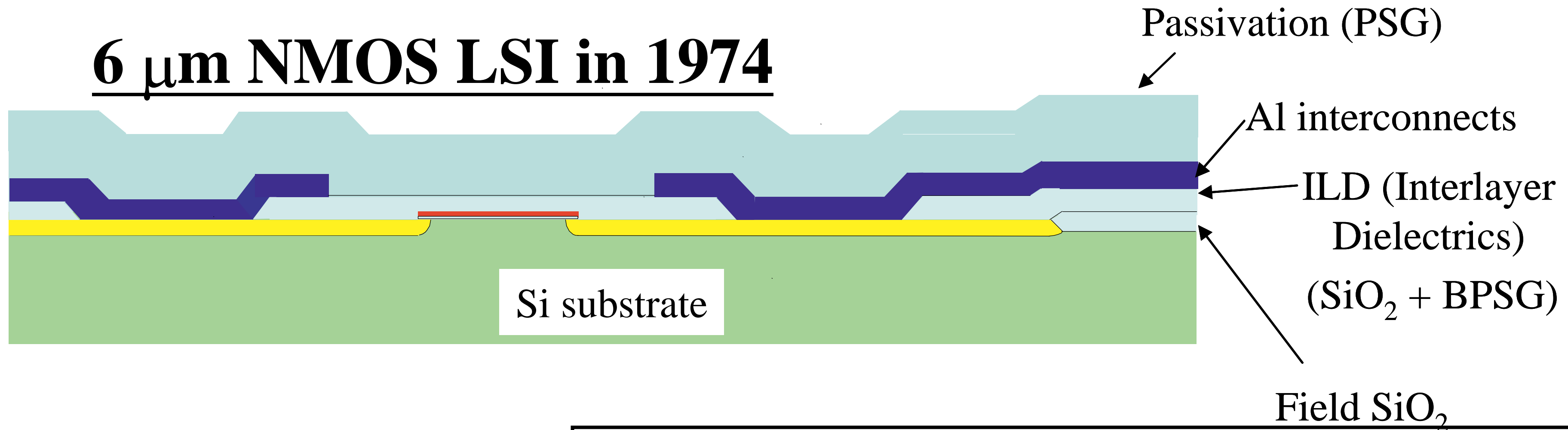
PMOS 1kbit DRAM Toshiba(1974)



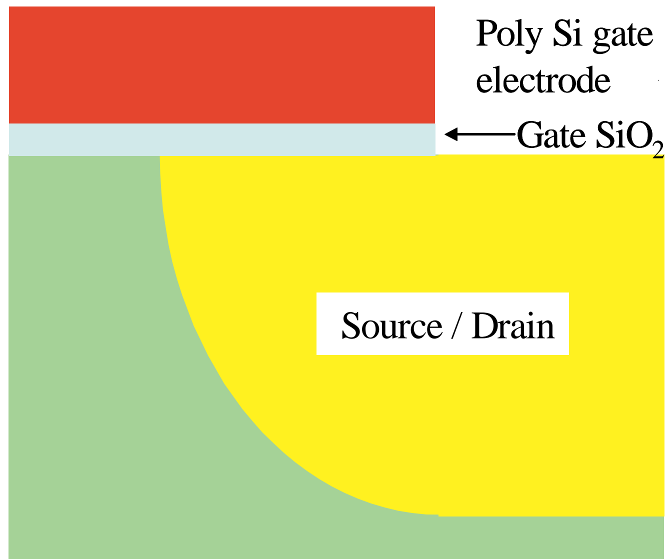
NMOS 1k bit SRAM Toshiba (1974)



6 μm NMOS LSI in 1974



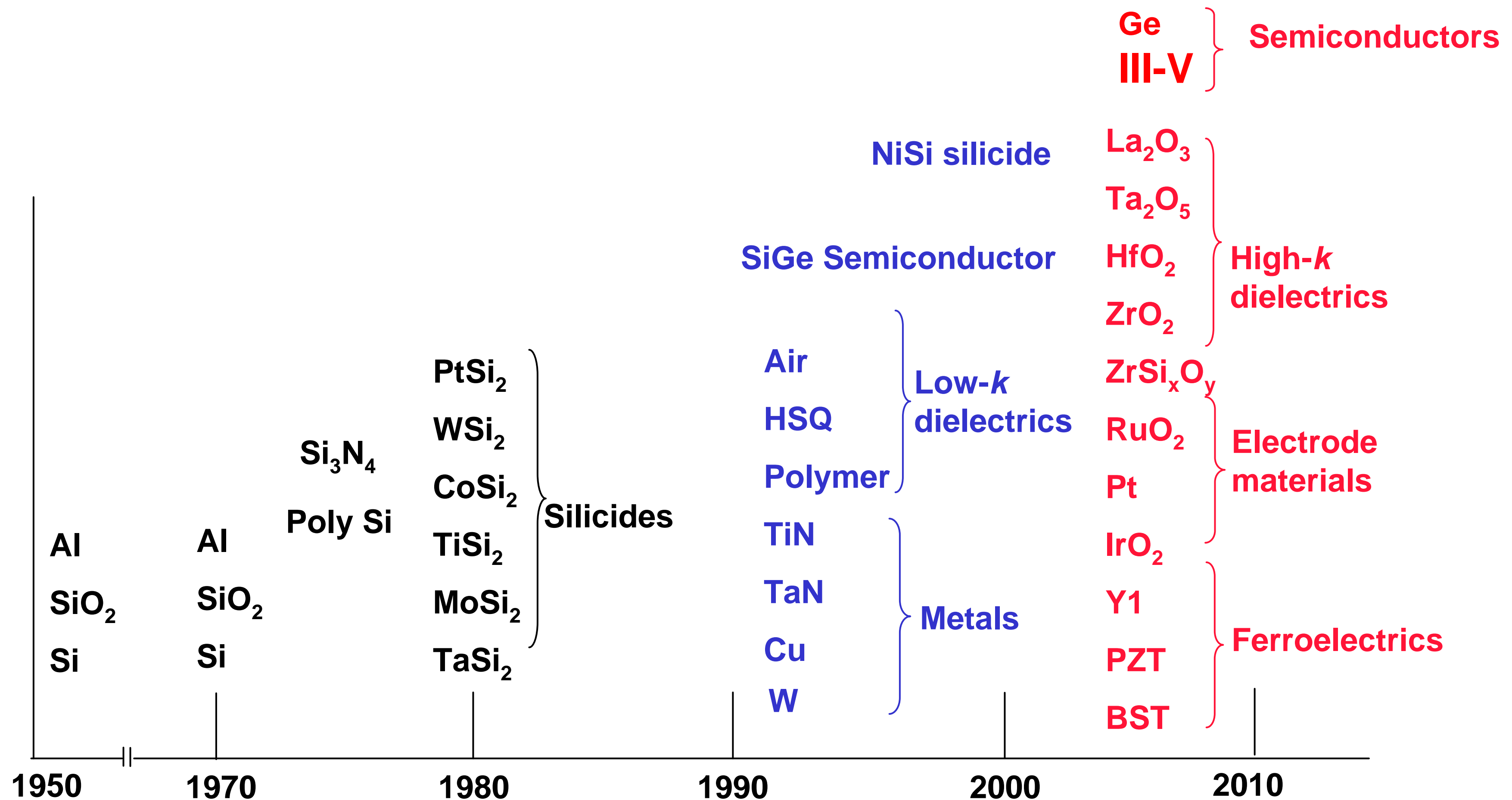
magnification



Layers	Materials	Atoms
1. Si substrate	1. Si	**1. Si**
2. Field oxide	2. SiO_2	**2. O**
3. Gate oxide	3. BPSG	**3. P**
4. Poly Si	4. Al	**4. B**
5. S/D	5. PSG	**5. Al**
6. Interlayer		**(H, N, Cl)**
7. Aluminum		
8. Passivation		

New materials

Just examples!
Many other candidates

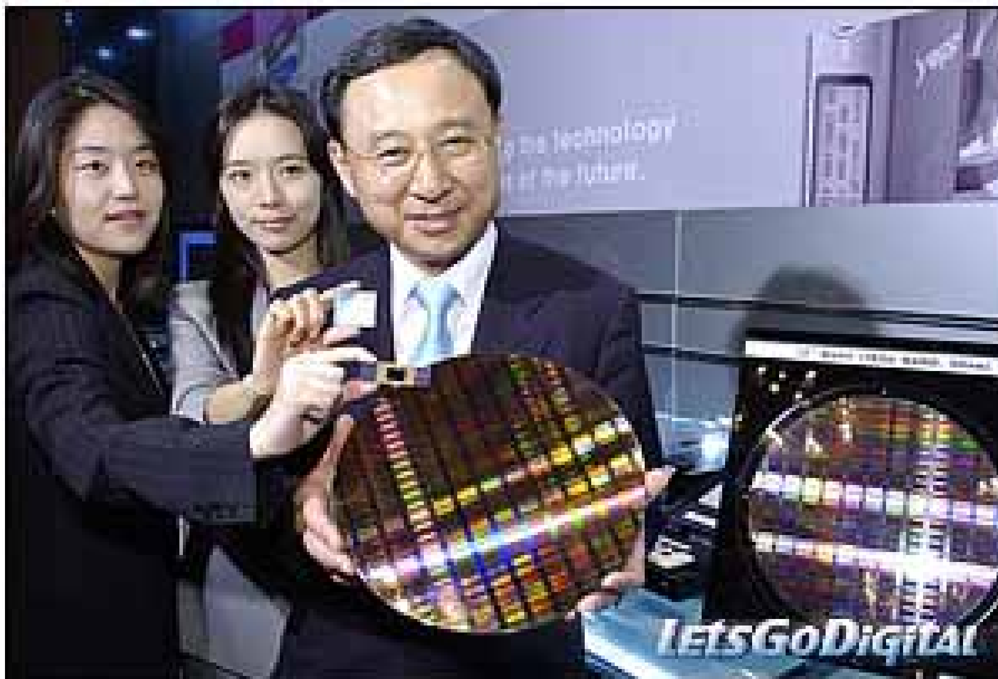


Y. Nishi, Si Nano Workshop, 2006,

(S. Sze, Based on invited talk at Stanford Univ., Aug. 1999)

Now: After 45 Years from the 1st single MOSFETs

32 Gb and 16Gb NAND, SAMSUNG



Samsung's NAND flash trend

Capacity	Node	Announcement	Product
512Mbit	120nm	2000	2001
1Gbit	100nm	2001	2002
2Gbit	90nm	2002	2003
4Gbit	70nm	2003	2004
8Gbit	60nm	2004	2005
16Gbit	50nm	2005	2006
32Gbit	40nm	2006	2007?
256Gbit	20nm	2010	2011?

Even Tbit is possible!

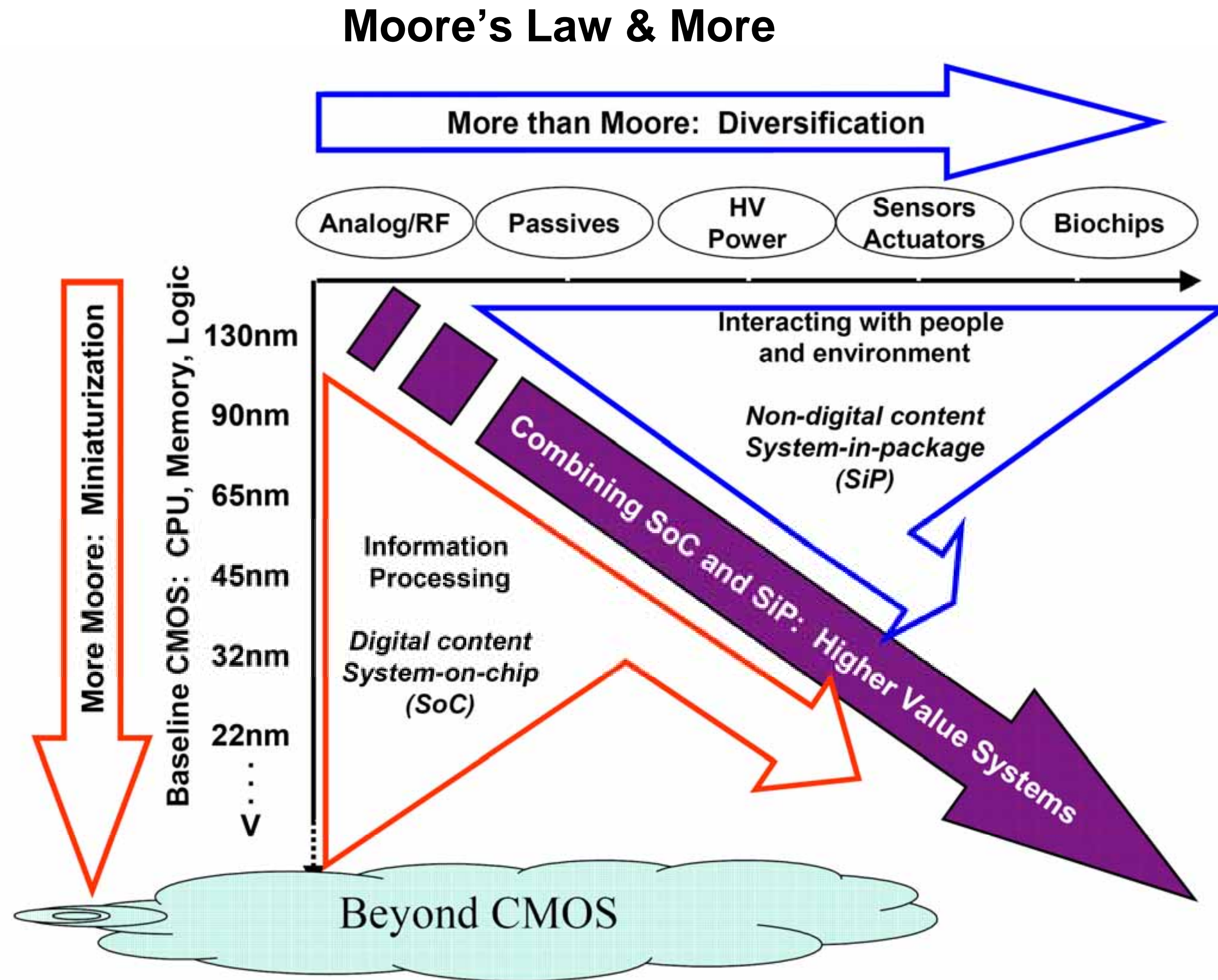
Already 32 Gbit:

larger than that of world population
comparable for the numbers of neurons
in human brain

Samsung announced 256 Gbit will be produced in 2010.
Only 4 years from now.
256Gbit: larger than those of # of stars in galaxies

What will be the roadmap after 2020?

More Moore and More than Moore



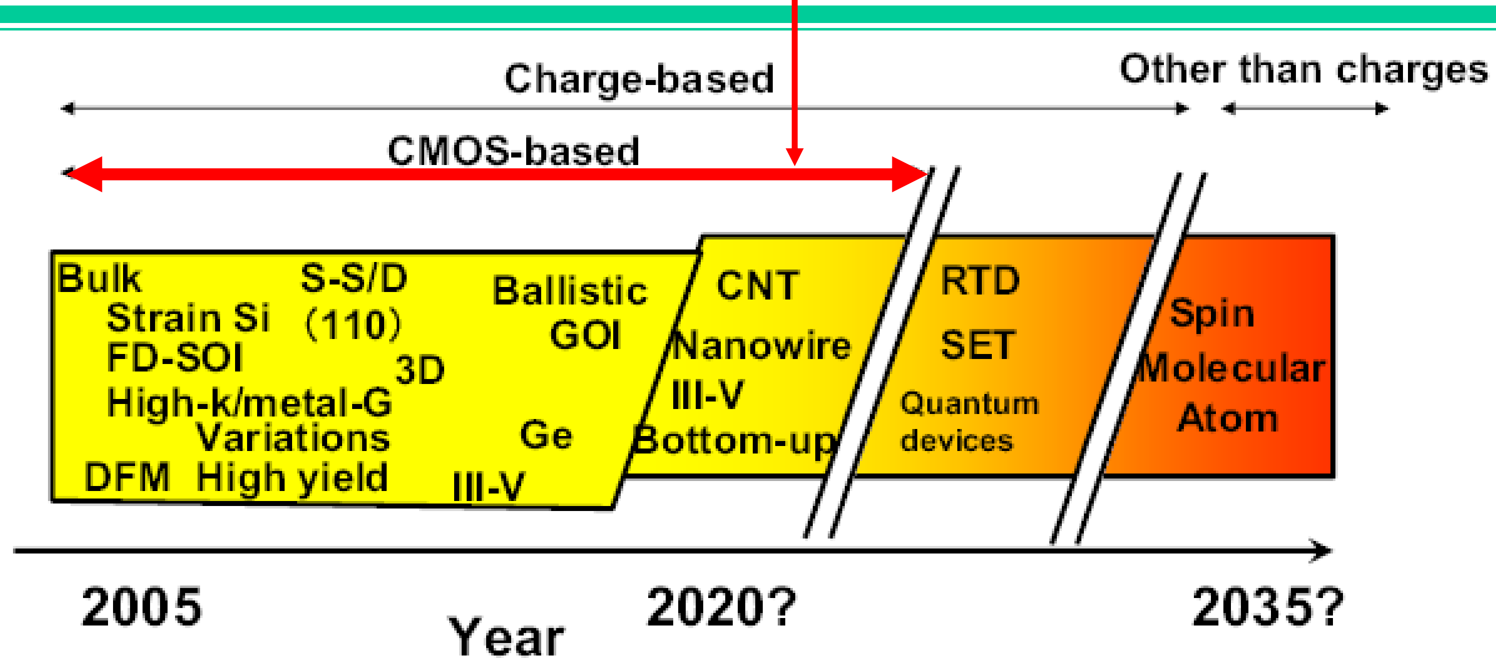
Question what is the other side of the cloud?

ITRS 2005 Edition

http://strj-jeita.elisasp.net/pdf_ws_2005nendo/9A_WS2005IRC_Ishiuchi.pdf

Question: Will CMOS end in 2020?

Three Stages in Silicon Nanoelectronics



1. CMOS Extension

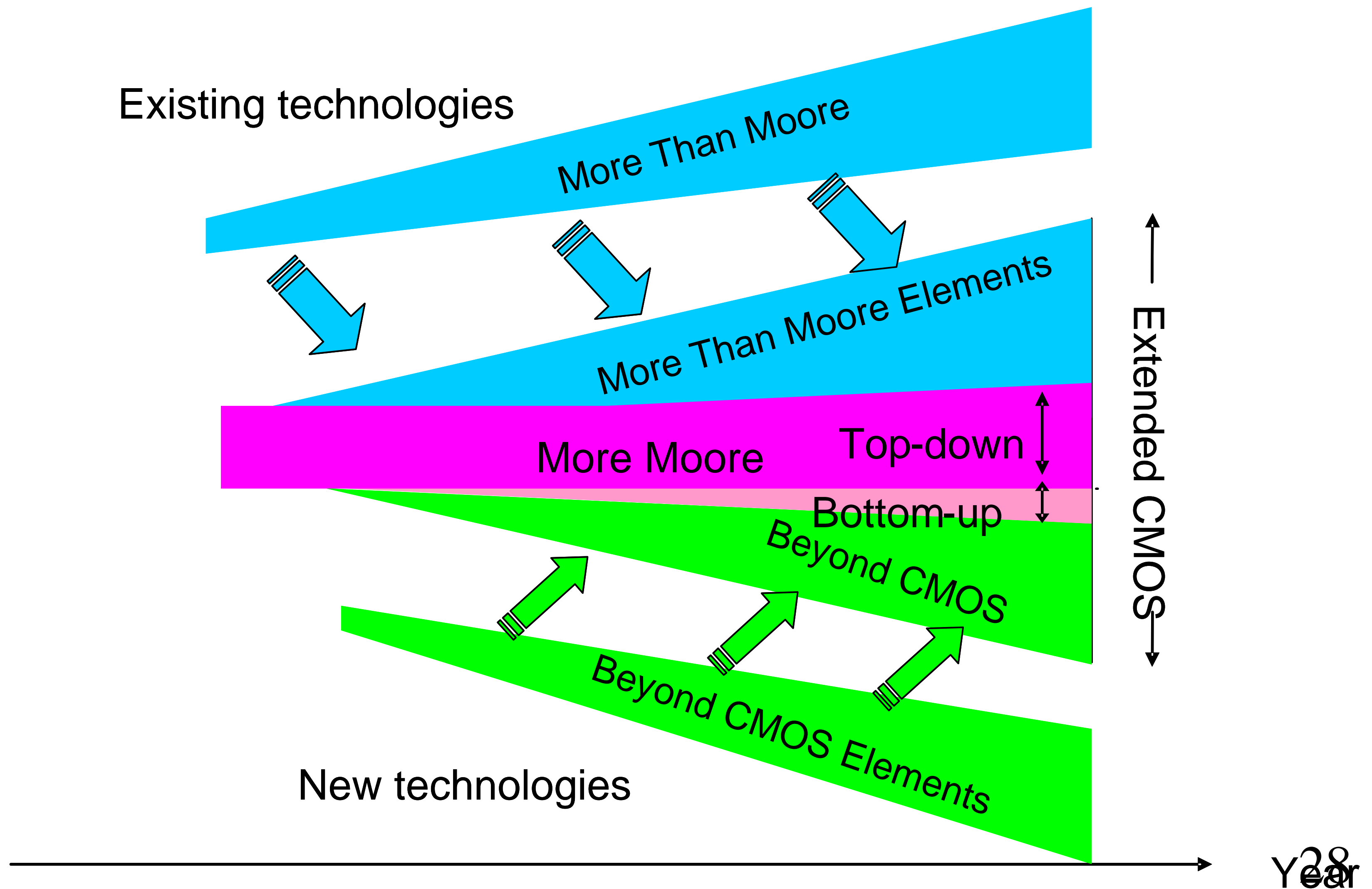
3. Beyond CMOS

2. New Functions Added to CMOS

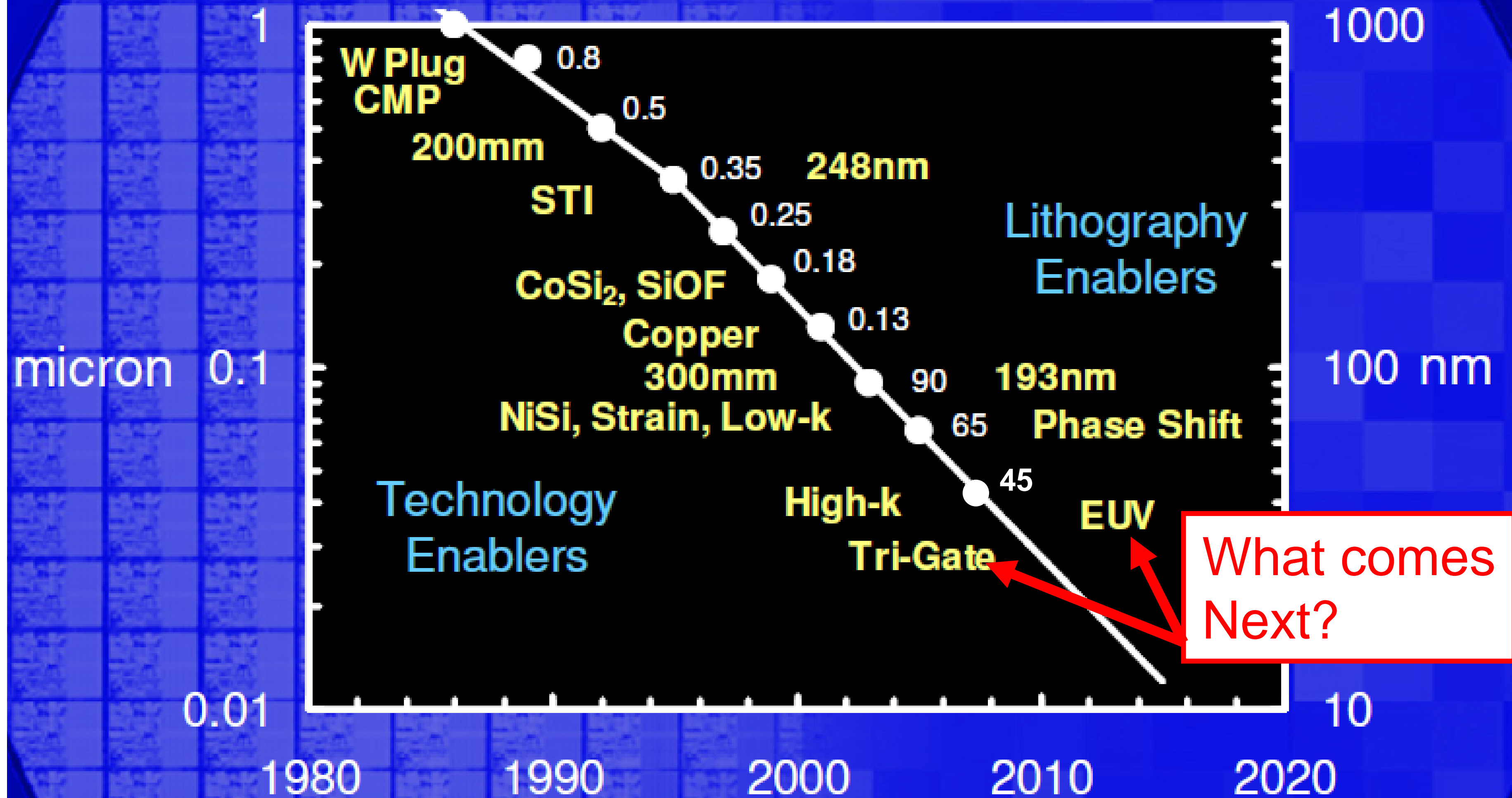
http://www.rcns.hiroshima-u.ac.jp/21coe/pdf/5th_WS/2-4-2_Hiramoto.pdf

New Concept for Roadmap

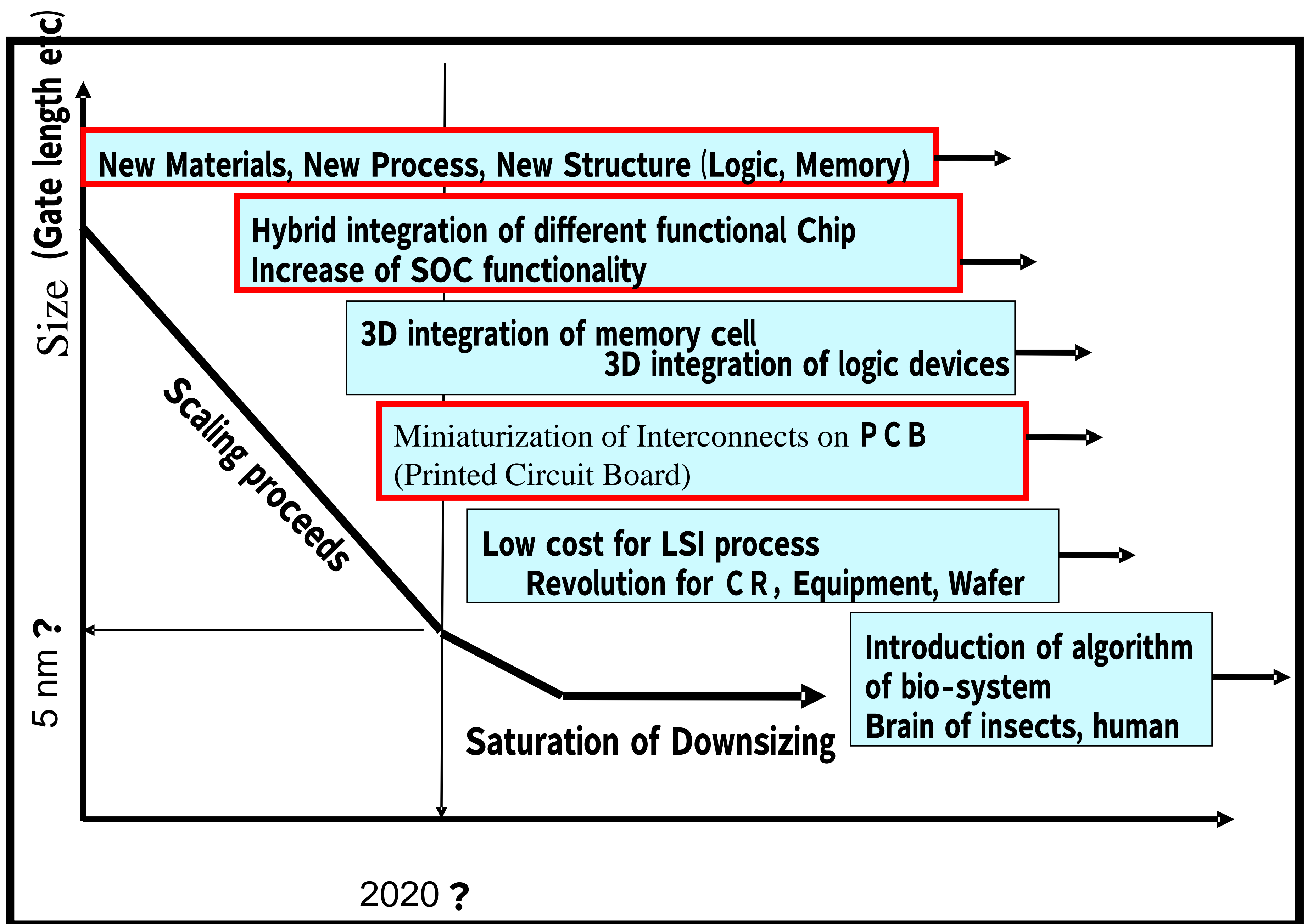
Evolution of Extended CMOS Continues!!



Scaling Gets Tougher at Smaller Dimensions



Intel continues to develop and implement new materials and structures to meet the challenge


Size (Gate length etc)
New Materials, New Process, New Structure (Logic, Memory)
Hybrid integration of different functional Chip
Increase of SOC functionality
3D integration of memory cell
3D integration of logic devices
Scaling proceeds
Miniaturization of Interconnects on PCB
(Printed Circuit Board)
Low cost for LSI process
Revolution for CR, Equipment, Wafer
5 nm ?
Introduction of algorithm
of bio-system
Brain of insects, human
Saturation of Downsizing
2020 ?

After 2020

There is no decrease in gate length around at 5 nm due to subthreshold leakage.

It is not useful to reduce the gate length any more for increasing the drain current, because the conduction is already semi-ballistic.

What is important for keeping Moore Law, then?

→ Increase drain current drive under low drain voltage in order to reduce the power consumption.

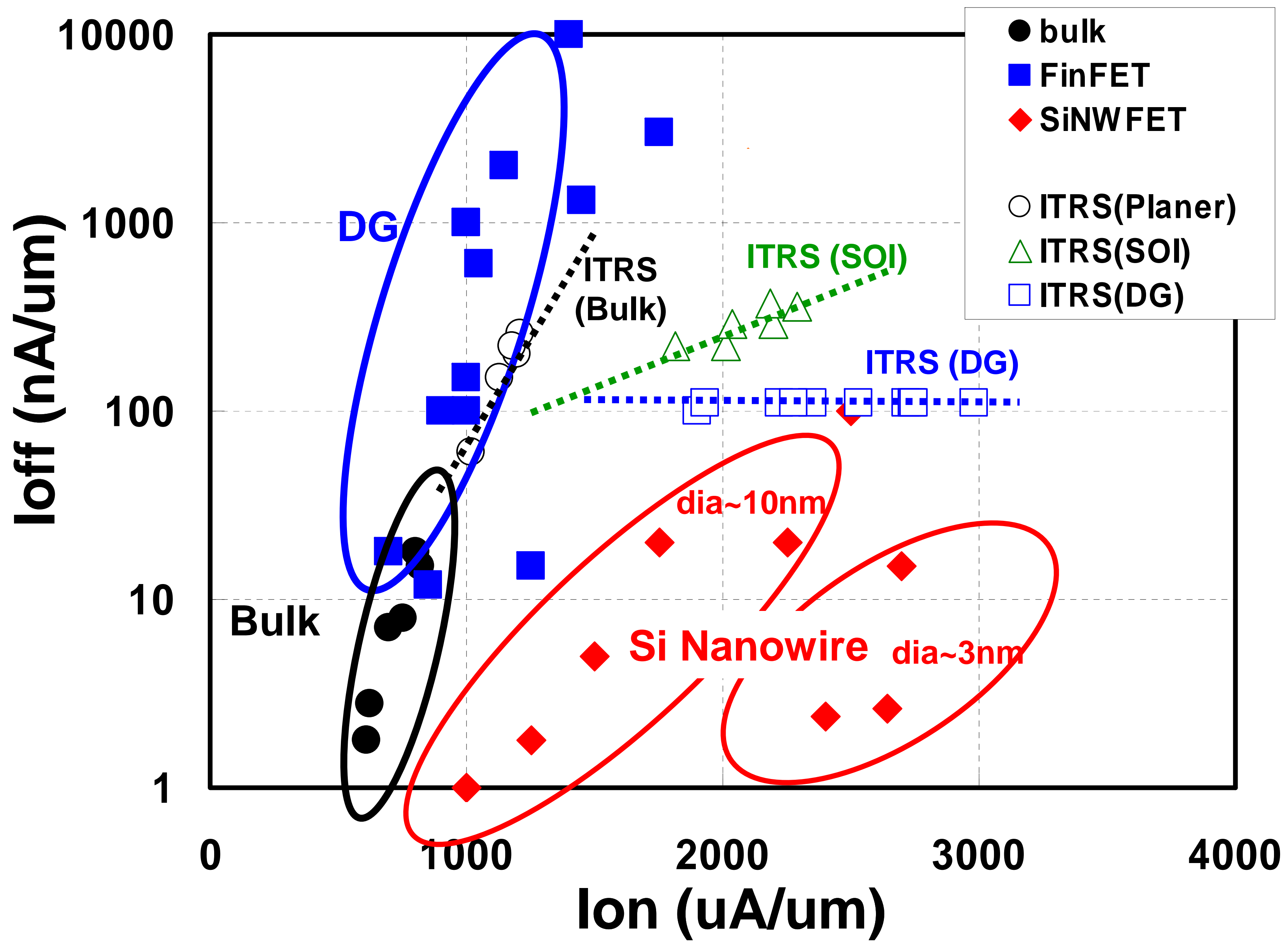
Selection of MOSFET structure

For suppression of Ioff, the structure will be Fin-FET type

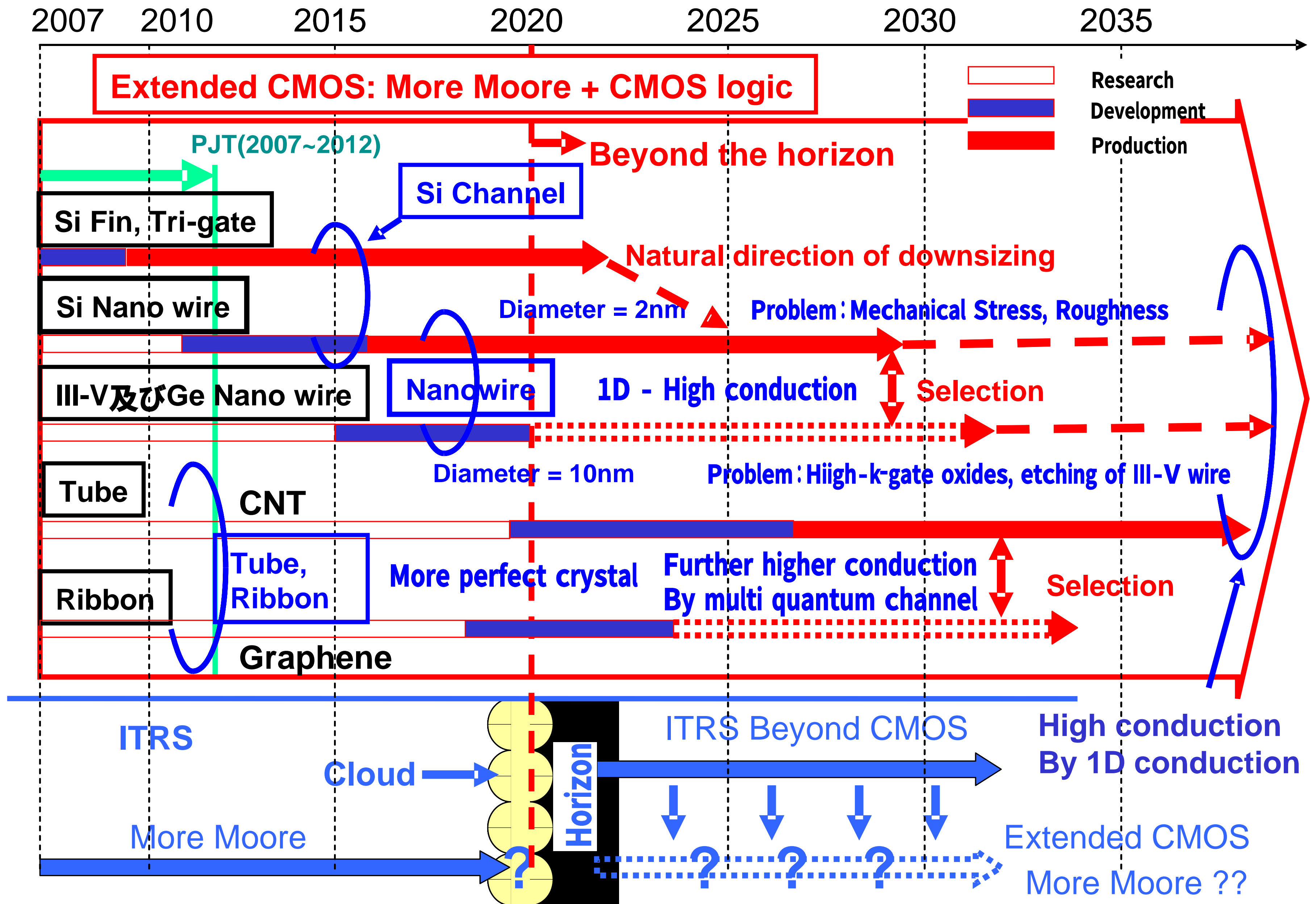
High-conduction at low voltage

1. 1D conduction → Nano-wire, Nano-tube FET
2. Increase number of quantum channel →
   Band engineering、CNT(Carbon Nano-tube Tnansistor)
3. Increase the number of wire or tube →
   3D integration of wires and tubes

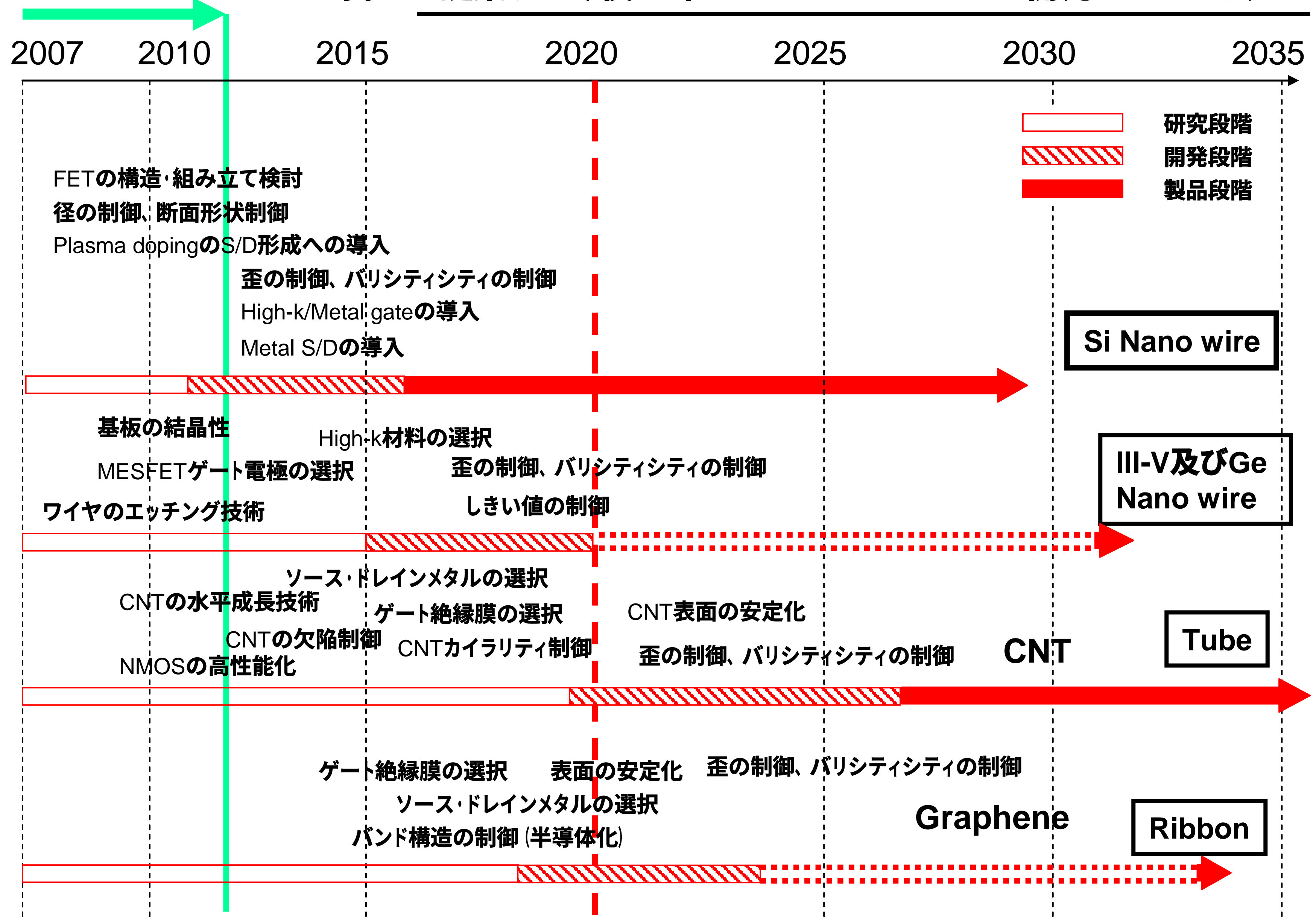
High-integration, low cost production,
no-small-geometry lithography → CNT



bulk
FinFET
SiNWFET
ITRS(Planer)
ITRS(SOI)
ITRS(DG)
10000
1000
100
10
1
Ioff (nA/um)
0
1000
2000
3000
4000
Ion (uA/um)
DG
ITRS (Bulk)
ITRS (SOI)
ITRS (DG)
Bulk
dia~10nm
Si Nanowire
dia~3nm



Our new roadmap
2007
2010
2015
2020
2025
2030
2035
Extended CMOS: More Moore + CMOS logic
Research
Development
Production
PJT(2007~2012)
Beyond the horizon
Si Channel
Si Fin, Tri-gate
Natural direction of downsizing
Si Nano wire
Diameter = 2nm
Problem：Mechanical Stress, Roughness
III-V及びGe Nano wire
Nanowire
1D - High conduction
Selection
Diameter = 10nm
Problem：Hiigh-k-gate oxides, etching of III-V wire
Tube
CNT
Tube,
Ribbon
More perfect crystal
Further higher conduction
By multi quantum channel
Selection
Ribbon
Graphene
ITRS
Cloud
Horizon
ITRS Beyond CMOS
High conduction
By 1D conduction
More Moore
Extended CMOS
More Moore ??

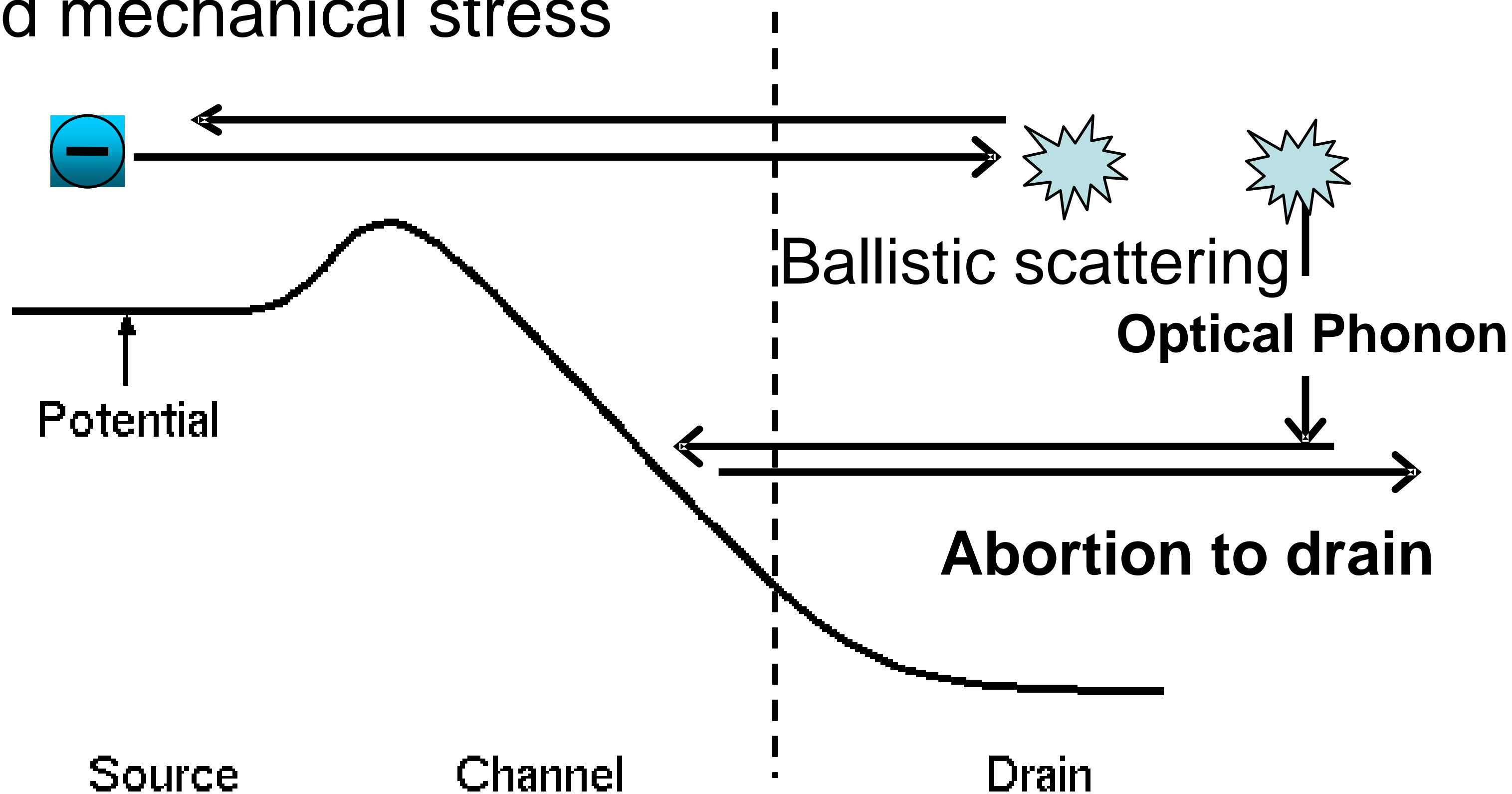

経産ナノエレPJT(2007~2012)
我々が提案する今後30年のExtended CMOSの開発のロードマップ
2007
2010
2015
2020
2025
2030
2035
研究段階
開発段階
製品段階
FETの構造･組み立て検討
径の制御、断面形状制御
Plasma dopingのS/D形成への導入
歪の制御、バリシティシティの制御
High-k/Metal gateの導入
Metal S/Dの導入
Si Nano wire
基板の結晶性
High-k材料の選択
MESFETゲート電極の選択
歪の制御、バリシティシティの制御
ワイヤのエッチング技術
しきい値の制御
III-V及びGe Nano wire
ソース･ドレインメタルの選択
CNTの水平成長技術
ゲート絶縁膜の選択
CNT表面の安定化
CNTの欠陥制御
CNTカイラリティ制御
歪の制御、バリシティシティの制御
NMOSの高性能化
CNT
Tube
ゲート絶縁膜の選択
表面の安定化
歪の制御、バリシティシティの制御
ソース･ドレインメタルの選択
バンド構造の制御 (半導体化)
Graphene
Ribbon

1D conduction per one quantum channel:

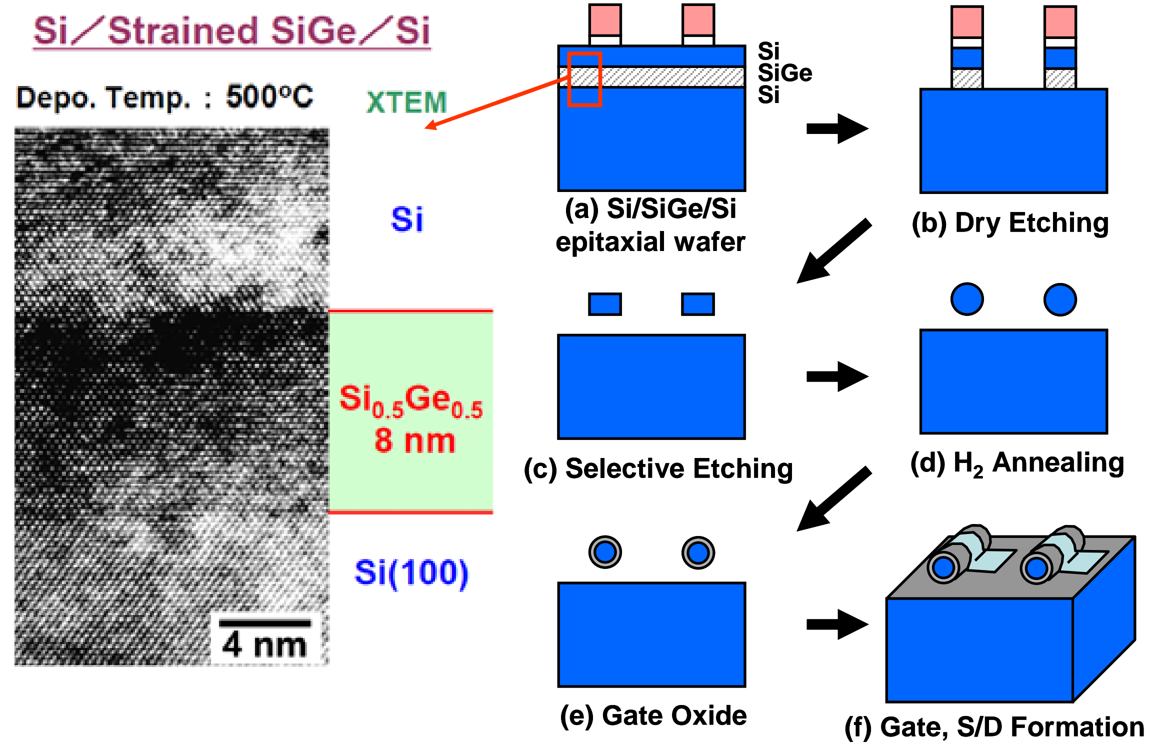
$G = 2e^2/h = 80\ \mu S$/wire or tube

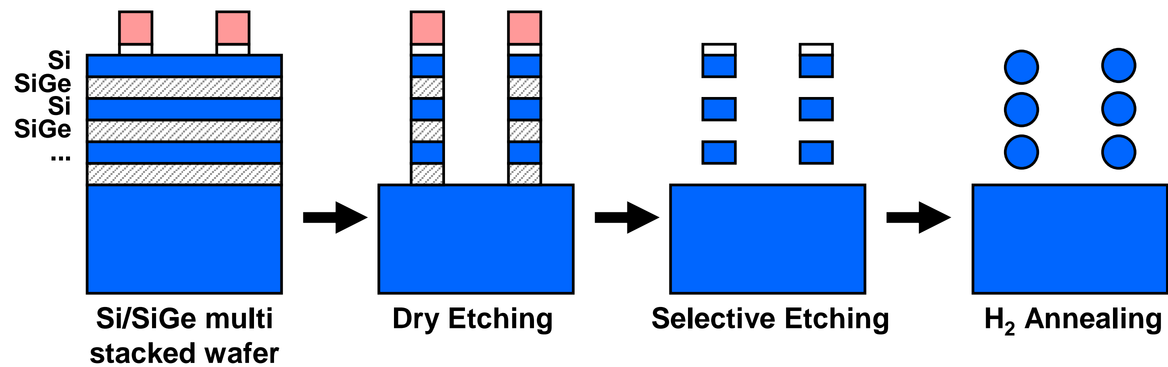
regardless of gate length and channel material

But this value has not been obtained yet,
due to reflection of carriers from drain, surface roughness and mechanical stress

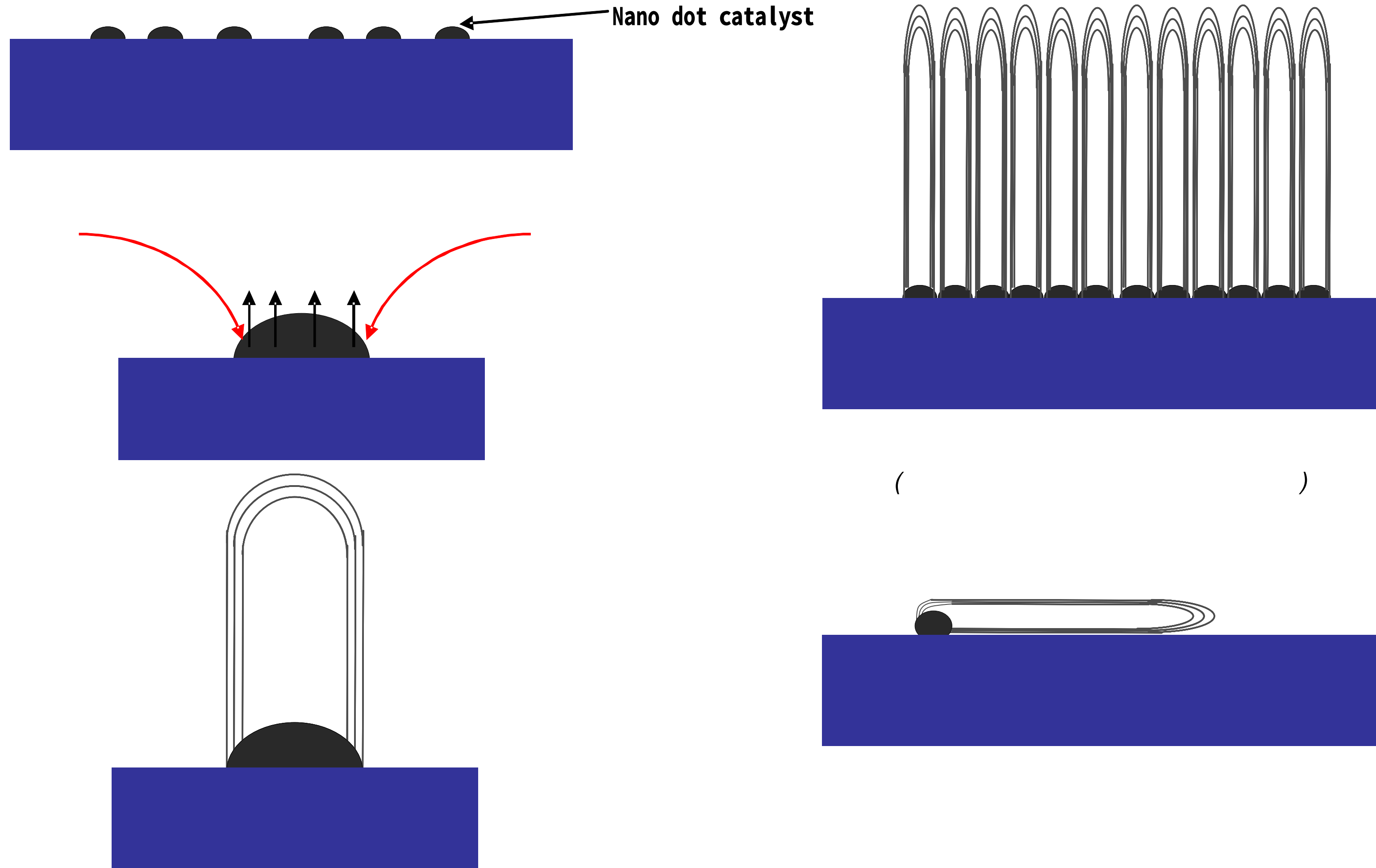


Increase the number of wires





Lateral growth of CNT



Thank you
for your attention!