

Recent Patent List

- [1] H. Iwai, Y. Nishi, "Method of manufacturing semiconductor devices" Unites States Patent 4,327,476, filed Nov. 28, 1980, patented May 4, 1982
- [2] H. Iwai, "Method of etching, refilling and etching dielectric grooves for isolating micron size regions," Unites States Patent 4,394,196, filed July 13, 1981, patented July 19, 1983
- [3] S. Sawada, H. Iwai, S. Maeda, , "Method for fabricating a semiconductor device," Unites States Patent 4,410,375, filed Oct. 2, 1981, patented Oct. 18, 1983
- [4] H. Iwai, "Semiconductor wafer with alignment marks and method for manufacturing semiconductor device," Unites States Patent 4,418,467, filed June 18, 1982, patented Dec. 6, 1983
- [5] H. Iwai, "Method for fabricating semiconductor device," Unites States Patent 4,419,813, filed Nov. 27, 1981, patented Dec. 13, 1983
- [6] H. Iwai, "Method of manufacturing a self-aligned U-MOS semiconductor device", United States Patent 4,455,740, filed Sept. 29, 1982, patented Jun. 26, 1984
- [7] H. Iwai, "Method for manufacturing a semiconductor device", United States Patent 4,491,486, filed Sept. 16, 1982, patented Jan. 1, 1985
- [8] H. Iwai, "Wafer exposure method and apparatus", United States Patent 4,500,615, filed Sept. 22, 1982, patented Feb. 19, 1985
- [9] M. Konaka, H. Iwai, Y. Nishi, "MOS Semiconductor device and method of manufacturing the same," Unites States Patent 4,523,213, filed July 9, 1982, patented June 11, 1985
- [10] H. Iwai, "Method of manufacturing a semiconductor device for forming a deep field region in a semiconductor substrate" Unites States Patent 4,532,696, filed Mar. 16, 1983, patented Aug. 6, 1985
- [11] S. Kameyama, S. Shinozaki, H. Iwai, "Method of manufacturing semiconductor device," Unites States Patent 4,532,701, filed Aug. 19, 1982, patented Aug. 6, 1985
- [12] S. Maeda, H. Iwai, "Semiconductor device and method of manufacturing the same," Unites States Patent 4,560,421, filed Oct. 2, 1981, patented Dec. 24, 1985
- [13] H. Iwai, H. Ohtsuka, "Treatment process for semiconductor wafer", United States Patent 4,575,466, filed Dec. 28, 1983, patented Mar. 11, 1986
- [14] H. Iwai, "Semiconductor substrate and method for manufacturing semiconductor device using the same", United States Patent 4,597,166, filed Feb. 8, 1983, patented July 1, 1986
- [15] H. Iwai, "Wafer exposure apparatus", United States Patent 4,613,230, filed Apr. 30, 1982, patented Sept. 23, 1986
- [16] S. Kameyama, S. Shinozaki, H. Iwai, "Method of forming isolation regions containing conductive patterns therein", United States Patent 4,615,103, filed May 28, 1985, patented Oct. 7, 1986
- [17] S. Kameyama, S. Shinozaki, H. Iwai, "Method of forming isolation regions containing conductive patterns therein", United States Patent 4,615,104, filed May 28, 1985, patented Oct. 7, 1986
- [18] H. Iwai, "Semiconductor device with self-aligned gate structure and manufacturing process thereof", United States Patent 4,737,831. filed Sept. 11, 1986, patented Apr. 12, 1988
- [19] S. Maeda, H. Iwai, "Semiconductor device having a semiconductor substrate with a high impurity concentration", United States Patent 4,755,863, filed Aug. 15, 1986, patented July 5, 1988
- [20] S. Maeda, H. Iwai, "Semiconductor device", United States Patent 4,872,042, filed July 13, 1984, patented Oct. 3, 1989
- [21] J. Tsujimoto, M. Matsui, H. Iwai, T. Ohtani, "Semiconductor memory device using partial decoders for redundancy, United States Patent 4,881,202. filed Dec. 29, 1987, patented Nov. 14, 1989
- [22] S. Maeda, H. Iwai," C-MOS device and a process for manufacturing the same", United States Patent 5,079,183, filed Jan. 6, 1989, patented Jan. 7, 1992
- [23] H. Iwai, T. Morimoto, H. Momose, K. Yamabe, Y. Ozawa, "Semiconductor device with

- nitrided gate insulating film”, United States Patent 5,237,188, filed November 27, 1991, patented Aug. 17, 1993
- [24] T. Yoshitomi, M. Saito, H. Momose, H. Iwai, Y. Ushiku, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, Y. Katsumata, “Semiconductor device and method of manufacturing the same”, United States Patent 5,434,440, filed May 28, 1993, patented July 18, 1995
- [25] H. Iwai, T. Morimoto, H. Momose, K. Yamabe, Y. Ozawa, “Method for fabricating semiconductor device in which threshold voltage shift and charge-pumping current are improved”, United States Patent 5,489,542, filed July 16, 1993, patented Feb. 6, 1996
- [26] H. Nakajima, Y. Katsumata, H. Iwai, T. Iinuma, K. Inou, M. Kitagawa, K. Morizuka, A. Nakagawa, I. Omura, “Semiconductor device and method of manufacturing the same”, United States Patent 5,510,647, filed March 15, 1994, patented Apr. 23, 1996
- [27] H. Nakajima, Y. Katsumata, H. Iwai, T. Iinuma, K. Inou, M. Kitagawa, K. Morizuka, A. Nakagawa, I. Omura, “Semiconductor device and method of manufacturing the same”, United States Patent 5,637,909, filed Jan. 2, 1994, patented Jun. 10, 1997
- [28] T. Yoshitomi, M. Saito, H. Momose, H. Iwai, Y. Ushiku, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, Y. Katsumata, T. Ooguro, C. Fiegna” MOSFET with Solid Phase Diffusion”, United States Patent 5,698,881, filed Dec. 2, 1994, patented Jun. 16, 1998
- [29] T. Yoshitomi, M. Saito, H. Momose, H. Iwai, Y. Ushiku, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, Y. Katsumata, “Semiconductor device and method of manufacturing the same”, United States Patent 5,766,965, filed Dec. 5, 1995, patented Jun. 16, 1998
- [30] T. Yoshitomi, H. Iwai, M. Saito, H. Momose, T. Ohguro, M. Ono, “Semiconductor device with side wall conductor film”, United States Patent 5,780,901, filed Jun. 30, 1995, patented Jul. 14, 1998
- [31] T. Yoshitomi, M. Saito, H. Momose, H. Iwai, Y. Ushiku, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, Y. Katsumata, “Semiconductor device having solid phase diffusion sources”, United States Patent 5,898,203, filed Jul. 30, 1997, patented April. 27, 1999
- [32] T. Yoshitomi, M. Saito, H. Momose, H. Iwai, Y. Ushiku, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, Y. Katsumata, T. Ooguro, C. Fiegna” MOSFET with Solid Phase Diffusion Source”, United States Patent 5,903,027, filed Aug. 13, 1997, patented May 11, 1999
- [33] T. Yoshitomi, H. Iwai, M. Saito, H. Momose, T. Ohguro, M. Ono, “Semiconductor device and manufacturing thereof”, United States Patent 5,995,761, filed Apr. 30, 1998, patented Sept. 21, 1999
- [34] H. Momose, H. Iwai, S. Saito, T. Ohguro, M. Ono, T. Yoshitomi, S. Nakamura, “MOSFET with a thin gate insulating film”, United States Patent 5,990,516, filed Sep. 13, 1995, patented Nov. 23, 1999
- [35] H. Momose, H. Iwai, S. Saito, T. Ohguro, M. Ono, T. Yoshitomi, S. Nakamura, “MOSFET with a thin gate insulating film”, United States Patent 6,229,164, filed Nov. 16, 1999, patented May. 8, 2001
- [36] H. Momose, H. Iwai, S. Saito, T. Ohguro, M. Ono, T. Yoshitomi, S. Nakamura, “MOSFET with a thin gate insulating film”, United States Patent 6,410,952, filed Apr. 9, 2001, patented Jun. 25, 2002

Publication List

Research Papers:

- [1] T. Inoue, S. Horiuchi, H. Iwai, H. Shimizu, and T. Ishida, "Micro-probe Auger analysis of Si migration in Al metallization for LSI," Japan J. Appl. Phys., vol.15 pp.63-69, 1976
- [2] K. Natori, M. Ogura, H. Iwai, K. Maeguchi, and S. Taguchi, "A 64k bit MOS dynamic random access memory," IEEE J. Solid-State Circuits, vol. 14, pp.482-485, 1979
- [3] M. Konaka, H. Iwai, and Y. Nishi, "Suppression of anomalous drain current in short channel MOSFET," Japan J. Appl. Phys. vol.18, Suppl. 18-1, pp.27-33, 1979
- [4] L. M. Dang, H. Iwai, Y. Nishi, and S. Taguchi, "P-channel versus N-channel in MOS-ICs of submicron channel lengths," Japan J. Appl. Phys.vol.19, Suppl. 19-1, pp.107-112, 1980

- [5] L. M. Dang and H. Iwai, "Modeling of the impurity profile in an ion-implanted layer of an IGFET for the calculation of threshold voltages," IEEE Trans. Electron Devices, vol.28, pp.116-117, 1981
- [6] K. Taniguchi, M. Kashiwagi, and H. Iwai, "Two-dimensional computer simulation models for MOSLSI fabrication processes," IEEE Trans. on Electron Devices, vol.28, pp.574-580 , 1981
- [7] H. Otsuka, K. Watanabe, H. Nishimura, H. Iwai, and H. Nihira, "The effect of substrate materials on holding time degradation in MOS dynamic RAM," IEEE Electron Device Letters, vol. EDL-3, No.7, pp.182-184, 1982
- [8] H. Iwai, K. Taniguchi, M. Konaka, S. Maeda, and Y. Nishi, "Two-dimensional nature of diffused layers and certain limitations in scaling-down coplanar structure," IEEE Trans. Electron Devices, vol.29, pp.625-630 ,1982
- [9] H. Iwai and S. Kohyama, "On-chip capacitance measurement circuits in VLSI structures," IEEE Trans. Electron Devices, vol. 29, pp. 1622-1626 ,1982
- [10] J. Oristian, H. Iwai, J. Walker, and R. W. Dutton, "Small geometry MOS transistor capacitance measurement method using simple on-chip circuits," IEEE Electron Device Letters, vol.EDL-5, No.10, pp.395-397, October, 1984.
- [11] H. Iwai, H. Otsuka, Y. Matsumoto, K. Hisatomi, and K. Aoki, "Comparison of intrinsic gettering and epitaxial wafers in terms of soft error endurance and other characteristics of 64k bit dynamic RAM," IEEE Trans. Electron Devices, vol.31, pp.1149-1151 ,1984
- [12] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian, and R. W. Dutton, "Velocity saturation effect on short channel MOS transistor capacitance," IEEE Electron Device Letters, vol.EDL-6, No.3, pp.120-122, March, 1985
- [13] J. Oristian, H. Iwai, J. Walker, and R. W. Dutton, "A reply to "Comments to 'Small geometry MOS transistor capacitance measurement method using simple on-chip circuits,'" IEEE Electron Device Letters, vol.EDL-6, No.1, pp., January, 1985.
- [14] H. Iwai, J. E. Oristian, J. T. Walker, and R. W. Dutton, "A scaleable technique for measurement of intrinsic MOS capacitance with atto Farad resolution," IEEE Trans. Electron Devices, vol. ED-32, pp.344-356 ,1985
- [15] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian, and R. W. Dutton, "Analysis of velocity saturation and other effects on short channel MOS transistor capacitances," IEEE Trans. Computer-Aided Design, vol.6, pp.173-184 ,1987
- [16] M. Matsui, T. Ohtani, J. Tsujimoto, H. Iwai, A. Suzuki, K. Sato, M. Isobe, K. Hashimoto, M. Saitoh, H. Shibata, H. Sasaki, T. Matsuno, J. Matsunaga, and T. Iizuka, "A 25-ns 1-Mbit CMOS SRAM with loading-free bit lines," IEEE J. Solid-State Circuits, vol.22, pp.733-740, 1987
- [17] Y. Hiruta, H. Iwai, F. Matsuoka, K. Hama, K. Maeguchi, and K. Kanzaki, "Interface state generation under long term positive bias temperature stress for a p+ poly gate MOS structure," IEEE Trans. Electron Devices, vol.36, pp.1732-1739 , 1989
- [18] Matsuoka, H. Iwai, K. Hama, H. Itoh, R. Nakata, T. Nakakubo, K. Maeguchi, and K. Kanzaki, "Electromigration reliability for tungsten filled via hole structure," IEEE Trans. Electron Devices, vol.37, pp.562-568 , 1990
- [19] F. Matsuoka, H. Iwai, H. Hayashida, K. Hama, Y. Toyoshima, and K. Maeguchi, "Analysis of hot carrier induced degradation mode on PMOSFETs," IEEE Trans. Electron Devices, vol. 37, pp.1487-1495 , 1990
- [20] Y. Toyoshima, H. Iwai, F. Matsuoka, H. Hayashida, K. Maeguchi, and K. Kanzaki "Analysis of gate oxide thickness dependence of hot carrier induced degradation in thin gate oxide nMOSFETs," IEEE Trans. Electron Devices, vol.37, pp.1496-1503 , 1990
- [21] **Invited Paper:** M. Norishima, H. Iwai, Y. Niitsu, and K. Maeguchi, "Impurity diffusion behaviors of bipolar transistor under low-temperature furnace annealing and high-temperature RTA and its optimization for 0.5 μ m Bi-CMOS process," IEEE Trans. Electron Devices, vol.39, pp.33-40, January , 1992
- [22] B. Baccus, T. Wada, N. Shigyo, M. Norishima, H. Nakajima, K. Inou, T. Iinuma, and H. Iwai, "A study of non-equilibrium diffusion modeling; Application to rapid thermal annealing and advanced bipolar technologies," IEEE Trans. Electron Devices, vol.ED-39, no.3, pp.648-661,

March, 1992.

- [23] T. Iijima, A. Nishiyama, Y. Ushiku, T. Ohguro, I. Kunishima, K. Suguro, and H. Iwai, "A new contact plug technique for deep-submicron ULSIs employing selective nickel silicidation of polysilicon with a titanium nitride stopper," IEEE Trans. Electron Devices, vol. 40, pp.371-377 , 1993
- [24] M. Tsuchiaki, H. Hara, T. Morimoto, and H. Iwai, "New Charge Pumping Method for Determining the Spatial Distribution of Hot-Carrier-Induced Fixed Charge in p-MOSFET's," IEEE Trans. Electron Devices, vol. 40, pp.1768-1779 , 1993
- [25] M. Saito, T. Yoshitomi, H. Hara, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, H. S. Momose, Y. Katsumata, and H. Iwai, "P-MOSFET's with Ultra-Shallow Solid-Phase-Diffused Drain Structure Produced by Diffusion from BSG Gate-Sidewall," IEEE Trans. Electron Devices, vol.ED-40, no.12, pp.2264-2272 , 1993
- [26] S. Matsuda, N. Itoh, C. Yoshino, Y. Tsuboi, Y. Katsumata, and H. Iwai, "Mechanical Stress Analysis of Trench Isolation Using a Two-Dimensional Simulation," IEICE Trans. Electron., vol.E77-C, pp.124-128 , 1993
- [27] Y. Tsuboi, C. Fiegna, E. Sangiorgi, B. Ricco, T. Wada, Y. Katsumata, and H. Iwai, "Monte Carlo Analysis of Velocity Overshoot Effects in Bipolar Devices with and without an i-Layer," IEICE Trans. Electron., vol.E77-C, pp.174-178 , 1993
- [28] H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, "Electrical Characteristics of Rapid Thermal Nitride-Oxide Gate n- and p-MOSFET's with Less Than 1 Atom% Nitrogen Concentration," IEEE Trans. Electron Devices, vol. 41, pp.546-552 , 1994
- [29] H. S. Momose, and H. Iwai, "Analysis of the Temperature Dependence of Hot-Carrier-Induced Degradation in Bipolar Transistors for Bi-CMOS," IEEE Trans. Electron Devices, vol. 41, pp.978-987 , 1994
- [30] C. Fiegna, H. Iwai, T. Wada, M. Saito, E. Sangiorgi, and B. Ricco, "Scaling the MOS transistor below 0.1 μ m: methodology, device structures and technology requirements," IEEE Trans. Electron Devices, vol. 41, pp.941-951 , 1994
- [31] T. Ohguro, S. Nakamura, M. Koike, T. Morimoto, A. Nishiyama, Y. Ushiku, T. Yoshitomi, M. Ono, M. Saito, and H. Iwai, "Analysis of Resistance Behavior in Ti- and Ni- Salicided Polysilicon Films," IEEE Trans. Electron Devices, vol. 41, pp.2305-2317 , Dec. 1994
- [32] T. Iinuma, N. Itoh, H. Nakajima, K. Inou, A. Matsuda, C. Yoshino, Y. Tsuboi, Y. Katsumata, and H. Iwai, "Sub-20 ps High-Speed ECL Bipolar Transistor with Low Parasitic Architecture," IEEE Trans. Electron Devices, vol. 42, pp.399-405 , Mar. 1995
- [33] H. S. Momose, T. Morimoto, Y. Ozawa, K. Yamabe, and H. Iwai, "An Improvement of Hot-Carrier Reliability in the Stacked Nitride-Oxide Gate n- and p-MISFET's," IEEE Trans. Electron Devices, vol. 42, pp.704-712 ,Apr. 1995
- [34] T. Morimoto, T. Ohguro, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, "Self-Aligned Nickel-Mono-Silicide Technology for High-Speed Deep Submicrometer Logic CMOS ULSI," IEEE Trans. Electron Devices, vol. 42, pp.915-922 , May 1995
- [35] H. Iwai, H. S. Momose, M. Saito, M. Ono, and Y. Katsumata "The future of ultra-small-geometry MOSFETs beyond 0.1 micron," Microelectronic Engineering, vol.28 pp.147-154 , Jun. 1995
- [36] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, H. S. Momose, and H. Iwai, "Fabrication of sub-50-nm gate length n-metal-oxide semiconductor field effect transistors and their electrical characteristics," J. Vac. Sci. Technol., vol.B13, pp.1740-1743, JUL-AUG 1995
- [37] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, H. S. Momose, and H. Iwai, "A Study of Hot Carrier Effects on n-MOSFET's Under High Substrate Impurity Concentration," IEEE Trans. Electron Devices, vol. 42, pp.1510-1521 ,Aug. 1995
- [38] M. Ono, M. Saito, T. Yoshitomi, C. Fiegna, T. Ohguro, and H. Iwai, "A 40 nm gate length n-MOSFET," IEEE Trans. Electron Devices, vol. 42, pp.1822-1830 , Oct. 1995
- [39] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, M. Saito, and H. Iwai, "Realization of High-Performance MOSFETs with gate lengths of 0.1 μ m or Less," Electronics and Communication in Japan, Part 2, vol.79, pp.67-76 , Oct. 1996

- [40] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, and H. Iwai, "1.5 nm Direct-Tunneling Gate Oxide Si MOSFET's," IEEE Trans. Electron Devices, vol. 43, pp.1233-1242, Aug. 1996
- [41] H. S. Momose, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, and H. Iwai, "Prospects for Low-power, High-speed MPUs Using 1.5 nm Direct-tunneling Gate Oxide MOSFETs," Solid-State Electronics Vol.41, pp. 707-714, May 1997
- [42] H. Iwai and H. S. Momose, "Technology towards low power / low voltage and scaling of MOSFETs" Microelectronic Engineering, vol.39 pp.7-30, Dec. 1997
- [43] T. Yoshitomi, M. Saito, T. Ohguro, M. Ono, H. S. Momose, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, "A hot-carrier degradation mechanism and electrical characteristics in of S⁴D n-MOSFETs," IEEE Trans. Electron Devices, vol. 44, pp.2053-2058, Nov. 1997
- [44] R. Fujimoto, S. Otaka, H. Iwai, and H. Tanimoto, "A 1.5GHZ CMOS low noise amplifier" IEICE Trans. on Fundamentals, vol.E81-A, pp.382-388, Mar. 1998
- [45] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto and H. Iwai, "Study of the manufacturing feasibility of 1.5-nm direct-tunneling gate oxide MOSFET's: Uniformity, reliability, and dopant penetration of the gate oxide," IEEE Trans. Electron Devices, vol. 45, pp.691-700, 1998
- [46] T. Ohguro, N. Sugiyama, S. Imai, K. Usuda, M. Saito, T. Yoshitomi, M. Ono, H. Kimijima, H. S. Momose, Y. Katsumata, and H. Iwai, "Undoped epitaxial Si channel n-MOSFET grown by UHV-CVD with preheating," IEEE Trans. Electron Devices, vol. 45, pp.710-716, 1998
- [47] T. Ohguro, K. Yamada, N. Sugiyama, S. Imai, K. Usuda, T. Yoshitomi, C. Fiegna, M. Ono, M. Saito, H. S. Momose, Y. Katsumata, and H. Iwai, "0.15- μ m buried-channel p-MOSFET's with ultrathin boron-doped epitaxial Si layer," IEEE Trans. Electron Devices, vol. 45, pp.717-721, March 1998
- [48] M. Saito, M. Ono, R. Fujimoto, H. Tanimoto, N. Ito, T. Yoshitomi, T. Ohguro, H. S. Momose, and H. Iwai, "0.15- μ m RF CMOS technology compatible with logic CMOS for low-voltage operation" IEEE Trans. Electron Devices, vol. 45, pp.737-742, March 1998
- [49] D. Esseni, H. Iwai, M. Saito, and B. Ricco, "Non-scaling of MOSFETs linear resistance in deep submicrometer regime," IEEE Electron Device Letters, vol.19, pp.131-133, Apr. 1998
- [50] **Invited Paper:** H. Iwai, "Downsizing of silicon MOSFETs beyond 0.1 μ m," Microelectronics Journal, vol.29, pp.671-678, Oct. 1998
- [51] T. Yoshitomi, M. Saito, T. Ohguro, M. Ono, H. S. Momose, E. Morifuji, T. Morimoto, Y. Katsumata, and H. Iwai, "High performance of silicided silicon-sidewall source and drain (S⁴D) structure," IEEE Trans. Electron Devices, vol. 45, pp.1295-1299, Jun. 1998
- [52] H. S. Momose, S. Nakamura, Y. Katsumata, and H. Iwai, "Application of direct-tunneling gate oxides to high-performance CMOS," Microelectronics Reliability, vol.38, pp.1413-1423, Sep. 1998
- [53] **Invited Paper:** H. Iwai, "CMOS Technology – Year 2010 and beyond", IEEE Journal of Solid-State Circuits, vol.34, pp.357-366, Mar. 1999
- [54] H. Nii, C. Yoshino, S. Yoshitomi, K. Inoh, H. Furuya, H. Nakajima, H. Sugaya, H. Naruse, Y. Katsumata, and H. Iwai, "An 0.3- μ m Si epitaxial base BiCMOS technology with 37-GHz f_{max} and 10-V BV_{ceo} for RF telecommunication," IEEE Trans. Electron Devices, vol. 46, no.4, pp.712-721, Apr. 1999
- [55] T. Ohguro, H. Naruse, H. Sugaya, E. Morifuji, S. Nakamura, T. Yoshitomi, T. Morimoto, H. Kimijima, H. S. Momose, Y. Katsumata, and H. Iwai, "An 0.18- μ m CMOS for Mixed Digital and Analog Applications with Zero-Volt-V_{th} Epitaxial-Channel MOSFET's", IEEE Transactions on Electron Devices, vol.46, no.6 pp.1378-1383, Jul. 1999
- [56] **Invited Paper:** H. Iwai, "Outlook of MOS Devices into Next Century", Microelectronic Engineering, vol.48, pp.7-14 September, 1999
- [57] T. Yoshitomi, M. Saito, T. Ohguro, M. Ono, H. S. Momose, E. Morifuji, T. Morimoto, Y. Katsumata, H. Iwai, "Single-gate 0.15 and 0.12 μ m CMOS with Co salicide technology", Solid State Electronics, vol.43 no.3, pp.543-546, Mar. 1999
- [58] T. Yoshitomi, H. Oguma, T. Ohguro, E. Morifuji, T. Morimoto, H. S. Momose, H. Kimijima, Y. Katsumata, H. Iwai, "A high performance 0.15 μ m buried channel pMOSFET with

- extremely shallow counter doped channel region using solid phase diffusion", Solid State Electronics, vol.43 no.7, pp.1209-1214, Jul. 1999
- [59] T. Yoshitomi, H. Kimijima, S. Ishizuka, Y. Miyahara, T. Ohguro, E. Morifuji, T. Morimoto, H. S. Momose, Y. Katsumata, H. Iwai, "A study of self-aligned doped channel MOSFET structure for low power and low 1/f noise operation", Solid State Electronics, vol.43 no.7, pp.1219-1224, Jul. 1999
- [60] H. Iwai, T. Ikoma, Y. Kado, "Overview of the ULSI Session and Chapter", International Journal of High Speed Electronics and Systems, vol.10 no.1, pp.171-173, 2000
- [61] T. Ohguro, M. Saito, E. Morifuji, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "Thermal Stability of CoSi₂ Film for CMOS Salicide", IEEE Transactions on Electron Devices, Vol.47, No.11, pp.2208-2213, November 2000
- [62] T. Ohguro, M. Saito, E. Morifuji, K. Murakami, K. Matsuzaki, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "Power Si-MOSFET Operating with High Efficiency Under Low Supply Voltage", IEEE Transactions on Electron Devices, Vol.47, No.12, pp.2385-2391, December 2000
- [63] J.-S. Goo, C.-H. Choi, F. Danneville, E. Morifuji, H. S. Momose, Z. Yu, H. Iwai, T. H. Lee, and R. W. Dutton, "An Accurate and Efficient High Frequency Noise Simulation Technique for Deep Submicron MOSFETs", IEEE Transactions on Electron Devices, Vol.47, No.12, pp.2410-2419, December 2000
- [64] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata, H. Iwai, "Hot-carrier reliability of ultra-thin gate oxide CMOS", Solid-State Electronics 44, pp.2035-2044, Nov. 2000
- [65] H. S. Momose, T. Ohguro, E. Morifuji, H. Sugaya, S. Nakamura, and H. Iwai, "Ultrathin Gate Oxide CMOS with Nondoped Selective Epitaxial Si Channel Layer," IEEE Transactions on Electron Devices, Vol.48, No.6, pp.1136-1144, June 2001
- [66] H. S. Momose, E. Morifuji, T. Yoshitomi, T. Ohguro, M. Saito, and H. Iwai, "Cutoff Frequency and Propagation Delay Time of 1.5-nm Gate Oxide CMOS," IEEE Transactions on Electron Devices, Vol.48, No.6, pp.1165-1174, June 2001
- [67] **Invited Paper:** H. Iwai, T. Ohguro, and H. Ohmi, "NiSi salicide technology for scaled CMOS", Microelectronic Engineering 60, pp.157-169, February 2002
- [68] **Invited Paper:** H. Iwai and S. Ohmi, "Silicon integrated circuit technology from past to future," Microelectronics Reliability, vol.42, pp.465-491, April, 2002
- [69] H. Iwai, S. Ohmi, "Trend of CMOS downsizing and its reliability" Microelectronics Reliability, vol.42, No.9-11, pp.1251-1258, Sep-Nov, 2002
- [70] H. S. Momose, T. Ohguro, S. Nakamura, Y. Toyoshima, H. Ishiuchi, H. Iwai, "Ultrathin Gate Oxide CMOS on (111) Surface-Oriented Si Substrate", IEEE Transactions on Electron Devices, Vol.49, No.9, pp.1597-1605, September, 2002
- [71] J.O.Borland, V.Moroz, H.Wang, W.Maszara and H.Iwai, "High-tilt implant and diffusion-less activation for lateral graded S/D engineering" SolidState Technology, Vol.2003-06, pp.52-58, 2003
- [72] F. Lime, K. Oshima, M. Casse, G. Ghibaudo, S. Cristoloveanu, B. Guillaumot, H. Iwai, "Carrier mobility in advanced CMOS devices with metal gate and HfO₂ gate dielectric" Solid-State Electronics, Vol.47, pp.1617-1621, Oct. 2003
- [73] J.Tonotani, T.Iwamoto, F.Sato, K.Hattori, S.Ohmi, and H.Iwai, "Dry etching characteristics of TiN film using Ar/CHF₃, Ar/Cl₂, and Ar/BCl₃ gas chemistries in an inductively coupled plasma" Journal of Vacuum Science & Technology B (JVST B), Second Series, Vol.21, No.5, pp.2163-2168, September/October 2003
- [74] H.Iwai, "CMOS downsizing toward sub-10nm", SolidState Electronics 48, pp.497-503, September 2003
- [75] C.Ohshima, J.Taguchi, I.Kashiwagi, H.Yamamoto, S.Ohmi, H.Iwai, "Effect of surface treatment of Si substrates and annealing condition on high-k rare earth oxide gate dielectrics" Applied Surface Science, 216 pp. 302-306, Jun. 2003
- [76] H.Nohira, T.Shiraishi, T.Nakamura, K.Takahashi, M.Takeda, S.Ohmi, H.Iwai, T.Hattori, "Chemical and electronic structures of Lu₂O₃/Si interfacial transition layer" Applied Surface

- Science 216, pp. 234-238, Jun. 2003
- [77] S.Ohmi, C.Kobayashi, I.Kashiwagi, C.Ohshima, H.Ishiwara, H.Iwai, “Characterization of La₂O₃ and Yb₂O₃ Thin Films for High-k Gate Insulator Application” Journal of The Electrochemical Society, 150 (7), F134-F140, Jul. 2003
 - [78] J. O. Borland, H. Iwai, W. Maszara, H. Wang, “Extending the life of planar CMOS with multigate CMOS devices”, Solid State Technology, Vol.46, pp.26, March, 2003
 - [79] T.Hattori, T.Yoshida, T.Shiraishi, K.Takahashi, H.Nohira, S.Joumori, K.Nakajima, M.Suzuki, K.Kimura, I.Kashiwagi, C.Ohshima, S.Ohmi, H.Iwai, “Composition, chemical structure, and electronic band structure of rare earth oxide/Si(100) interfacial transition layer” Microelectronic Engineering 72 pp.283-287, Apr. 2004
 - [80] S.Ohmi, H.Yamamoto, J.Taguchi, K.Tsutsui, H.Iwai, “Effects of Post Dielectric Deposition and Post Metallization Annealing Processes on Metal/Dy₂O₃/Si(100) Diode Characteristics” Japanese Journal of Applied Physics Vol.43, No.4B, pp. 1873-1878, Apr. 2004
 - [81] S.Ohmi, M.Takeda, H.Ishiwara, H. Iwai, “Electrical Characteristics for Lu₂O₃ Thin Films Fabricated by E-Beam Deposition Method” Journal of The Electrochemical Society, 151(4), pp.G279-283, 2004
 - [82] H. Iwai “The Future of CMOS Downscaling” Future Trends in Microelectronics The Nano, the Giga, and Ultra, pp.23-33, The Institute of Electrical and Electronics Engineers, Inc., New York, 2004
 - [83] H. Nohira, T. Shiraishi, K. Takahashi, T. Hattori, I. Kashiwagi, C. Ohshima, S. Ohmi, H. Iwai, S. Joumori, K. Nakajima, M. Suzuki, K. Kimura, “Atomic-scale depth profiling of composition, chemical structure and electronic band structure of La₂O₃/Si(100) interfacial transition layer, Applied Surface Science, 234, pp.493-496, Jul. 2004
 - [84] K. Oshima, S. Cristoloveanu, B. Guillaumot, S. Deleonibus, H. Iwai, “SOI MOSFETs with Buried Alumina : Thermal and Electrical Aspects”, Journal of The Electrochemical Society, 151(4), pp.G257-G261, 2004
 - [85] K. Oshima, S. Cristoloveanu, B. Guillaumot, H. Iwai, S. Deleonibus, “Advanced SOI MOSFETs with buried alumina and ground plane : self-heating and short-channel effects”, Solid-State Electronics 48, pp.907-917, Jun. 2004
 - [86] Y. Kim, K. Miyauchi, S. Ohmi, K. Tsutsui, and H. Iwai, “Electrical properties of vacuum annealed La₂O₃ thin films grown by e-beam evaporation”, Microelectronics Journal, 36/1, pp.41-49 Jan. 2005.
 - [87] Y. Kim, S. Ohmi, K. Tsutsui, H. Iwai “Analysis of variation in leakage currents of Lanthana thin films” Solid-State Electronics 49, pp. 825-833, May 2005
 - [88] J.A.Ng, Y. Kuroki, N. Sugii, K. Kakushima, S.-I. Ohmi, K. Tsutsui, T. Hattori, H. Iwai, H. Wong “Effects of low temperature annealing on the ultrathin La₂O₃ gate dielectric; comparison of post deposition annealing and post metallization annealing” Microelectronic Engineering 80, pp. 206-209, Jun. 2005
 - [89] Y. Sasaki, C.G.Jin, K. Okashita, H. Tamura, H. Ito, B. Mizuno, H. Sauddin, R. Higaki, T. Satoh, K. Majima, Y. Fukagawa, K. Takagi, I. Aiba, K. Tsutsui, H. Iwai “New method of Plasma doping with in-situ Helium pre-amorphization” Nuclear Instruments and Methods in Physics Research B237, pp.41-45, Aug. 2005
 - [90] A. Kuriyama, S. Ohmi, K. Tsutsui, H. Iwai, “Effect of Post-Metallization Annealing on Electrical Characteristics of La₂O₃ Gate Thin Films,” Japanese Journal of Applied Physics Vol. 44, No.2, pp.1045-1051, Feb. 2005
 - [91] Y. Kim, S. Ohmi, K. Tsutsui, H. Iwai, “Space-Charge-Limited Currents in La₂O₃ Thin Films Deposited by E-Beam Evaporation after Low Temperature Dry-Nitrogen Annealing” Japanese Journal of Applied Physics Vol. 44, No.6A, pp.4032-4042, Jun. 2005
 - [92] H. Wong, H. Iwai, “The Road to Miniaturization” Physics World Vol. 18 No.9 September, pp.40-44, Sep. 2005
 - [93] D. Misra, H. Iwai, and H. Wong, “ High-k Gate Dielectrics” Interface vol.14 No.2 Summer, 2005
 - [94] H. Nohira, T. Yoshida, H. Okamoto, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, Ng Jin Aun, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, K. Kobayashi, Y. Takata, T. Hattori,

- “Thermal Stability of Lanthanum Oxide / Si (100) Interfacial Transitionlayer” Physics and Chemistry of SiO₂ and the SiO₂Interface-5 Vol. 1 No. 1, pp.87-95, 2005
- [95] E.Miranda J.Molina, Y.Kim, H. Iwai, “Effects of high-field electrical stresses on the conduction properties of ultra-thin La₂O₃ Films” Applied Physics Letters 86, 232104, Jun. 2005
- [96] E.Miranda J.Molina, Y.Kim, H. Iwai “Degradation of High-K La₂O₃ Gate Dielectrics Using Progressive Electrical Stress” Microelectronics Reliability, 45, pp. 1365-1369, Sep-Nov 2005
- [97] N. Bresson, S. Cristoloveanu, C. Mazure, F. Letertre, H. Iwai, “Integration of buried insulators with high thermal conductivity in SOI MOSFETs: Thermal properties and short channel effects”, SOLID-STATE ELECTRONICS, Vol.49, pp.1522-1528, Sep. 2005
- [98] C. G. Jin, Y. Sasaki, K. Okashita, H. Tamura, H. Ito, B. Mizuno, K. Tsutsui, S. Ohmi, H. Iwai, “Ultra shallow p⁺/n junction formation by plasma doping (PD) and long pulse all solid-state laser annealing (ASLA) with selective absorption modulation” Nuclear Instruments and Methods in Physics Research B237, pp.58-61, Aug. 2005
- [99] K. Tsutsui, R. Higaki, Y. Sasaki, T. Sato, H. Tamura, K. Okashita, B. Mizuno, H. Iwai, “Doping effects from neutral B₂H₆ gas phase on plasma pretreated Si substrates as a possible process in plasma doping” Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers, Vol.44, 6A, pp.3903-3907, Jun., 2005
- [100] J. Tonotani, S. Ohmi, H. Iwai, “Dry etching of Cr₂O₃/Cr stacked film during resist ashing by oxygen plasma”, Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers, Vol.44, 1A, pp.114-117, Jan., 2005
- [101] E.Miranda, J.Molina, Y.Kim, H. Iwai, “ Tunneling in sub-5nm La₂O₃ Deposited by E-beam Evaporation” Journal of Non-Crystalline Solids, Vol. 352 , pp.92-97, Jan. 2006
- [102] J.A.Ng, N. Sugii, K. Kakushima, P. Ahmet, K. Tsutsui, T. Hattori, H. Iwai “Effective Mobility and Interface-state Density of La₂O₃ nMisFETs after post deposition annealing” IEICE 2006 Electronics Express Vol.3, No.13, pp. 316-321, Jul. 2006
- [103] H. Nohira, T. Yoshida, H. Okamoto, S. Shinagawa, W. Sakai, K. Nakajima, M. Suzuki, K. Kimura, N.J. Aun, Y. Kobayashi, S. Ohmi, H. Iwai, E. Ikenaga, Y. Tanaka, K. Kobayashi, T. Hattori, “Thermal stability of Gd₂O₃/Si(100) interfacial transition layer”, JOURNAL DE PHYSIQUE IV, Vol.132, pp.273-277, Mar. 2006
- [104] H. Wong, H. Iwai “On the scaling issues and high - k replacement of ultrathin gate dielectrics for nanoscale MOS transistors ” Microelectronic Engineering 83, pp.1867-1904, Oct. 2006
- [105] K. Kakushima, H. Wong, H. Iwai “Challenges for Future Semiconductor Manufacturing” International Journal of High Speed Electronics and Systems Vol.16,No.1, pp.43-81, 2006
- [106] Y. Kuroki, J.A.Ng, K. Kakushima, N.Sugii, K.Tsutsui, H. Iwai “Al/La₂O₃Analysis of Post Metallization Annealed MISFETs by XPS” ECS Transactions, Vol.1, No.5, pp.239-247, 2006
- [107] J. Molina, K. Kakushima, P.Ahmet, N. Sugii, K. Tsutsui, H. Iwai “Breakdown and Reliability of Metal Gate- La₂O₃ Thin Films After Post-Deposition Annealing In N₂” ECS Transactions, Vol.1, No.5, pp.757-765, 2006
- [108] H. Wong, H. Iwai, “Modeling and characterization of direct-tunneling current in dual-layer ultrathin-gate dielectric films” J. Vac. Sci. Technol. B 24(4), Jul/Aug, 2006
- [109] K. Kakushima, Kazuo Tsutsui, Sun-Ichiro Ohmi, Parhat Ahmet and H. Iwai “Rare Earth Oxides in Microelectronics” Rare Earth Oxide Thin Films, Topics in Applied Physics 106, pp.345-365, 2007
- [110] Banani Sen, Hei Wong, J.Molina, H. Iwai, J.A.Ng, K.Kakushima, C.K.Sarkar “Trapping Characteristics of lanthanum oxide gate dielectric film explored from temperature dependent current-voltage and capacitance-voltage measurements” Solid-State Electronics 51, pp.475-480, Mar. 2007
- [111] J.Song, K.Kakushima, P.Ahmet, K.Tsutsui, N.Sugii, T.Hattori, H.Iwai, “CHARACTERISTICS of Ultrathin Lanthanum Oxide Films on Germanium Substrate: Comparison with Those on Silicon Substrate” Japanese Journal of Applied Physics, Vol.46, No.16, pp.L376-L378, Apr. 2007
- [112] N.Umezawa, K.Shiraishi, S.Sugino, A.Tachibana, K.Ohmori, K.Kakushima, H.Iwai,

- T.Chikyow, T.Ohno, Y.Nara, and K.yamada “Suppression of Oxygen Vacancy Formation in Hf-based High-k Dielectrics by Lanthanum Incorporation” Sep. 2007
- [113] E.Miranda, H.Iwai “ Postbreakdown Conduction in Ultrathin La_2O_3 Gate Dielectrics”, IEEE Transactions on Device and Materials Reliability, Vol.7, No.2, pp.333-339, June 2007
- [114] Y. Kobayashi, C. Raghunathan Manoj, K. Tsutsui, Venkanarayan Hariharan, K. Kakushima, V. Ramgopal Rao, P. Ahmet and H. Iwai “Parasitic Effects in Multi-Gate MOSFETs” IEICE TRANS. ELECTRON., Vol.E90-C, No.10, pp.2051-2056, October 2007
- [115] A. Kuriyama, J. Mitard, O. Faynot, L. Brevard, L. Lclerc, A. Tozzo, V. Vidal, S. Deleonibus, H. Iwai , S.Cristoloveanu, “A systematic investigation of work function in advanced metal gate-HfO₂-SiO₂ structures with bevel oxide” , SOLID-STATE ELECTRONICS, Vol.51, pp.1515-1522, Nov-Dec 2007
- [116] B. Sen, B. L. Yang, H. Wong, P. K. Chu, A. Huang, K. Kakushima, and H. Iwai, “Aluminium incorporation in lanthanum oxide films by using plasma immersion ion implantation”, Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits 2007, Taiwan, vol. 1, pp. 173.
- [117] B. Sen, B. L. Yang, H. Wong, C. W. Kok, M. K. Bera, P. K. Chu, A. Huang, K. Kakushima, and H. Iwai, “Electrical stability improvement for lanthanum oxide films by nitrogen incorporation using plasma immersion ion implantation”, Proceedings of IEEE Conference on Electron Devices and Solid-State Circuits 2007, Taiwan, vol. 2, pp. 6
- [118] S. Sato, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Thermal-stability improvement of LaON thin film formed using nitrogen radicals” Microelectronic Engineering 84, pp.1894-1897, Sep-Oct 2007
- [119] J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Improvement of interfacial properties with interfacial layer in La_2O_3 / Ge structure”, Microelectronic Engineering 84, pp.2336-2339, Sep-Oct 2007
- [120] T. Kawanago, K.Tachi, J.Song, K. Kakushima, P. Ahmet, K.Tsutsui, N. Sugii, T. Hattori, H.Iwai, “Electrical characterization of directly deposited La-Sc oxides complex for gate insulator application” Microelectronic Engineering 84, pp.2335-2338, Sep-Oct 2007
- [121] Y.C.Ong, D.S.Ang, K.L.Pey, S.J.O’Shea, K.E.J.Goh, C.Troade, C.H.Thung, T. Kawanago, K. Kakushima, H. Iwai, “Bilayer gate dielectric study by scanning tunneling microscopy”, APPLIED PHYSICS LETTERS 91, 102905, Sep. 2007
- [122] J. Molina, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Carrier separation and V_{th} measurements of W-La₂O₃ gated MOSFET structures after electrical stress” IEICE Electronics Express, Vol.4, No.6, pp.185-191, Mar. 2007
- [123] J. Molina, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Effects of N₂-Based Annealing on the Reliability Characteristics of Tungsten/ La_2O_3 /Silicon Capacitors” Journal of The Electrochemical Society, 154(5), pp.G110-G116, Mar. 2007
- [124] K. Doi, Y. Mikazuki, S. Shinya, T. Doi, P. Szarek, M. Senami, K. Shiraishi, H. Iwai, N. Umezawa, T. Chikyo, K. Yamada, A. Tachibana, “Electronic structure study of local dielectric properties of lanthanoid oxide, clusters”, JAPANESE JOURNAL OF APPLIED PHYSICS Vol. 47, pp.205-211, Jan. 2008
- [125] K. Kakushima, K. Okamoto, K. Tachi, J. Song, S. Sato, T. Kawanago, K. Tsutsui, N. Sugii, P. Ahmet, T. Hattori, H. Iwai, “Observation of band bending of metal/high-k Si capacitor with high energy x-ray photoemission spectroscopy and its application to interface dipole measurement” JOURNAL OF APPLIED PHYSICS, Volume104, No.10, Article Number: 104908, Nov. 2008
- [126] P. Ahmet, T. Shiozawa, K. Nagahiro, T. Nagata, K. Kakushima, K. Tsutsui, T. Chikyow, H. Iwai, “Thermal stability of Ni silicide films on heavily doped n⁺ and p⁺ Si substrates” MICROELECTRONIC ENGINEERING, Volume 85, pp 1642-1646, Jul. 2008
- [127] K. Kakushima, K. Okamoto, M. Adachi, K. Tachi, J. Song, S. Sato, T. Kawanago, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Band bending measurement of HfO₂/SiO₂/Si capacitor with ultra-thin La_2O_3 insertion by XPS”, APPLIED SURFACE SCIENCE, Volume254, pp 6106-6108, Jul. 2008
- [128] D. S. Ang, Y. C. Ong, S. J. O’Shea, K. L. Pey, C. H. Tung, T. Kawanago, K. Kakushima, H.

- Iwai, "Polarity dependent breakdown of the high-kappa/SiO_x gate stack: A phenomenological explanation by scanning tunneling microscopy" APPLIED PHYSICS LETTERS, Volume 92, Article Number 192904, May 2008
- [129] Y. C. Ong, D. S. Ang, K. L. Pey, Z. R. Wang, S. J. O'Shea, C. H. Tung, T. Kawanago, K. Kakushima, H. Iwai, "Electronic trap characterization of the Sc₂O₃/La₂O₃ high-kappa gate stack by scanning tunneling microscopy" APPLIED PHYSICS LETTERS, Volume 92, Article Number 022904, Jan. 2008
- [130] K. Kakushima, K. Okamoto, M. Adachi, K. Tachi, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Origin of flat band voltage shift in HfO₂ gate dielectric with La₂O₃ insertion", SOLID-STATE ELECTRONICS, Volume 52, pp. 1280-1284, Sep. 2008
- [131] N. Urushihara, S. Iida, N. Sanada, M. Suzuki, D. F. Paul, S. Bryan, Y. Nakajima, T. Hanajiri, K. Kakushima, P. Ahmet, K. Tsutsui, H. Iwai, "Three dimensional image construction and spectrum extraction from two dimensional elemental mapping in Auger electron spectroscopy", JOURNAL OF VACUUM SCIENCE & TECHNOLOGY A, Volume 26, pp. 668-672, Jul-Aug 2008
- [132] J. Molina, A. Torres, W. Calleja, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Degradation and breakdown of W-La₂O₃ stack after annealing in N₂", JAPANESE JOURNAL OF APPLIED PHYSICS, Volume 47, No.9, pp. 7076-7080, Sep. 2008
- [133] K. Tsutsui, Ruifei Xiang, K. Nagahiro, T. Shiozawa, P. Ahmet, Y. Okuno, M. Matsumoto, M. Kubota, K. Kakushima, H. Iwai, "Analysis of irregular increase in sheet resistance of Ni silicides on transition from NiSi to NiSi₂", Microelectronic Engineering, vol.85, pp.315-319, Feb. 2008
- [134] K. Tsutsui, T. Shiozawa, K. Nagahiro, Y. Ohishi, K. Kakushima, P. Ahmet, N. Urushihara, M. Suzuki, and H. Iwai, "Improvement of Thermal Stability of Ni Silicide on N⁺-Si by Direct Deposition of Group III Element (Al, B) Thin Film at Ni/Si Interface", Microelectronic Engineering, vol.85, pp.2000-2004, Oct. 2008
- [135] K. Tsutsui, T. Matsuda, M. Watanabe, Cheng-Guo Jin, Y. Sasaki, B. Mizuno, E. Ikenaga, K. Kakushima, P. Ahmet, T. Maruizumi, H. Nohira, T. Hattori and H. Iwai, "Activated Boron and its Concentration Profiles in Heavily Doped Si Studied by Soft X-ray Photoelectron Spectroscopy and Hall Measurements", Journal of Applied Physics, vol.104, 093709, Nov. 2008
- [136] P. Ahmet, K. Nakagawa, K. Kakushima, H. Nohira, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Electrical characteristics of MOSFETs with La₂O₃/Y₂O₃ gate stack" Microelectronics Reliability 48, 1769–1771, Nov-Dec 2008
- [137] D.S.Ang, Y.C.Ong, S.J. O'Shea, K.L.Pey, K.Kakushima, and H.Iwai "Study of trap generation in the Sc₂ O₃/La₂O₃/SiO_xgate dielectric stack by scanning tunneling microscopy" APPLIED PHYSICS LETTERS, Volume 93, Article Number 242904, Dec. 2008
- [138] H.Iwai "Roadmap for 22nm and beyond", Microelectronic Engineering, vol. 86, pp.1520-1528, Jul-Sep 2009
- [139] J. Song, K. Kakushima, P.Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Post metallization annealing study in La₂O₃/Ge MOS structure", Microelectronic Engineering, vol. 86, pp.1638-1641, Jul-Sep 2009
- [140] T. Kawanago, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Experimental Study for High Effective Mobility with directly deposited HfO₂/La₂O₃ MOSFET", Microelectronic Engineering, vol. 86, pp.1629-1631, Jul-Sep 2009
- [141] B. Sen, H.Wong, B. L. Yang, P. K. Chu, K. Kakushima and H. Iwai, "Effects of nitrogen incorporation into lanthana film by plasma immersion ion implantation", Solid-State Electronics, vol.53, pp.355-358, Mar. 2009.
- [142] S.-L. Siu, H. Wong, W.-S. Tam, K. Kakushima, H. Iwai, "Subthreshold parameters of radio-frequency multi-finger nanometer MOS transistors", Microelectronics Reliability, vol.49, pp.387391, Apr. 2009.
- [143] T. Koyanagi, K. Tachi, K. Okamoto, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Electrical Characterization of La₂O₃-Gated Metal Oxide Semiconductor Field Effect Transistor with Mg Incorporation" Japanese Journal of Applied Physics 48, May

2009

- [144] H. Wong, C. K. Wong, J. Liu, and H. Iwai, "Growth of Dielectric-Embedded Silicon Nanocrystallites for Light-Emitting Device Application" *Journal of Nanoscience and Nanotechnology*, 2009.
- [145] K. Kakushima, K. Tachi K, J. Song, S. Sato, H. Nohira, E. Ikenaga, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai , "Comprehensive x-ray photoelectron spectroscopy study on compositional gradient lanthanum silicate film", *JOURNAL OF APPLIED PHYSICS*, Vol.106, Dec. 2009
- [146] K. Kakushima, K. Okamoto, T. Koyanagi, M. Kouda, K. Tachi, T. Kawanago, J. Song, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai, "Selection of rare earth silicates for highly scaled gate dielectrics", *Microelectronic Engineering*, doi:10.1016/j.mee.2009.11.001, ,2009
- [147] H. Wong, H. Iwai, K. Kakushima, B.L. Yang and P. K. Chu, "XPS Study of the Bonding Properties of Lanthanum Oxide/Silicon Interface with a Trace Amount of Nitrogen Incorporation," *Journal of Electrochemical Society*, 2010.
- [148] Y. Kobayashi, K. Kakushima, P. Ahmet, V. Ramgopal Rao, K. Tsutsui, H. Iwai, "Analysis of dependence of short-channel effects in double-gate MOSFETs on channel thickness", *Microelectronics Reliability* 50, pp.332-337, March, 2010
- [149] K. Kakushima, K. Okamoto, T. Koyanagi, M. Kouda, K. Tachi, T. Kawanago, J. Song, P. Ahmet, H. Nohira, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "SrO capping effect for La₂O₃/Ce-Silicate gate dielectrics", *Microelectronics Reliability* 50, pp.356-359, March, 2010
- [150] Y. Kobayashi, K. Tsutsui, K. Kakushima, P. Ahmet, V. Ramgopal Rao, H. Iwai, "Analysis of Threshold Voltage Variation in Fin Field Effect Transistors (FinFETs) Separating Role of Short Channel Effects", *Japanese Journal of Applied Physics* 49, pp.044201-1-044201-6, April, 2010
- [151] H. Shimomura, K. Kakushima, H. Iwai, "Effect of High Frequency Noise Current Sources on Noise Figure for Sub-50 nm Node MOSFETs", *IEICE TRANSACTIONS on Electronics* Vol. E93-C No.5, pp.678-684, May 2010
- [152] K. Kakushima, M. Nakagawa, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai, "Radio-frequency performance of a sub-100 nm metal-oxide field-effect transistor with high-k gate dielectric", *Semiconductor Science and Technology*, Vol. 25, No. 4, 045029, ,2010
- [153] A. Uedono, K. Tsutsui, S. Ishibashi, H. Watanabe, S. Kubota, Y. Nakagawa, B. Mizuno, T. Hattori, H. Iwai, "Vacancy-Boron Complexes in Plasma Immersion Ion-Implanted Si Probed by a Monoenergetic Positron Beam", *Japanese Journal of Applied Physics* 49, 051301, May 2010
- [154] M. K. Bera, J. Song, P. Ahmet, K. Kakushima, N. Sugii, T. Hattori, H. Iwai, "Yttrium-scandium oxide as high-k gate dielectric for germanium metal-oxide-semiconductor devices", *Semiconductor Science and Technology* , Vol.25, No. 6, 065008 ,May 2010
- [155] Y. Lee, K. Natori, H. Iwai, K. Kakushima, K. Shiraishi, "Size-Dependent Properties of Ballistic Silicon Nanowire Field Effect Transistors", *Journal of Applied Physics*, Vol.107, No.11, pp.113705, June 2010
- [156] S. Inamoto, J. Yamasaki, E. Okunishi, K. Kakushima, H. Iwai, and N. Tanaka, "Annealing effects on a high-k lanthanum oxide film on Si(001) analyzed by aberration-corrected transmission electron microscopy/scanning transmission electron microscopy and electron energy loss spectroscopy", *Journal of Applied Physics*, Vol.107, 124510, June ,2010
- [157] K. Kakushima, K. Tachi, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Advantage of further scaling in gate dielectrics below 0.5 nm of equivalent oxide thickness with La₂O₃

- gate dielectrics”, *Microelectronics Reliability*, Vol.50(6), pp.790-793, June, 2010
- [158] Y. Lee, K. Kakushima, K. Shiraishi, K. Natori, H. Iwai, “Trade-off between density of states and gate capacitance in size-dependent injection velocity of ballistic n-channel silicon nanowire transistors”, *Applied Physics Letters*97(3), Art. No. 032101, July 19,2010
- [159] K. Kakushima, T. Koyanagi, K. Tachi, J. Song, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Characterization of flatband voltage roll-off and roll-up behavior in La₂O₃/silicate gate dielectric”, *Solid-State Electronics*, Vol. 54(7), pp. 720-723, July,2010
- [160] K. Kakushima, K. Tachi, M. Adachi, K. Okamoto, S. Sato, J. Song, T. Kawanago, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Interface and electrical properties of La-silicate for direct contact of high-k with silicon”, *Solid-State Electronics*, Vol. 54, pp. 715-719, July, 2010
- [161] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada, H. Iwai, “Electrical characterization of Si nanowire field-effect transistors with semi gate-around structure suitable for integration”, *Solid-State Electronics*, Vol. 54(9), pp. 925-928, Sep. 2010
- [162] H. Shimomura, K. Kakushima, H. Iwai, “Equivalent Noise Temperature Representation for Scaled MOSFETs”, *IEICE TRANSACTIONS on Electronics*, Vol. E93-C, No.10, pp.1550-1552, Oct. 2010
- [163] K. Kakushima, K. Okamoto, T. Koyanagi, M. Kouda, K. Tachi, T. Kawanago, J. Song, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Selection of rare earth silicates for highly scaled gate dielectrics”, *Microelectronic Engineering*, Vol.87(10), pp.1868-1871, Oct. 2010
- [164] H. Wong, CK Wong, J. Liu, H. Iwai, “Growth of Dielectric-Embedded Silicon Nanocrystallites for Light-Emitting Device Application”, *JOURNAL OF NANOSCIENCE AND NANOTECHNOLOGY*, Vol.10(11), Sp. Iss. SI, pp.7244-7249, Nov. 2010

International Conferences:

- [1] T. Inoue, S. Horiuchi, H. Iwai, H. Shimizu, and T. Ishida, "Micro-probe Auger analysis of Si migration in Al metallization for LSI," *Proceedings of the 7th Conference on Solid State Devices*, 1975, Tokyo
- [2] M. Konaka, H. Iwai, and Y. Nishi, "Suppression of anomalous drain current in short channel MOSFET," *Proceedings of the 10th Conference on Solid State Devices*, 1978, Tokyo
- [3] H. Nihira, M. Konaka, H. Iwai, and Y. Nishi, "Anomalous drain current in N-MOSFET's and its suppression by deep ion implantation," *IEDM Tech. Dig.* pp.487-491, 1978
- [4] L. M. Dang, H. Iwai, Y. Nishi, and S. Taguchi, "P-channel versus N-channel in MOS-ICs of submicron channel lengths," *Proceedings of the 11th Conference on Solid State Devices*, 1979, Tokyo
- [5] H. Iwai and S. Kohyama, "Capacitance measurement technique in high density MOS structures," *IEDM Tech. Dig.* pp.235-238, 1980
- [6] H. Iwai, K. Taniguchi, M. Konaka, S. Maeda, and Y. Nishi, "Two dimensional nature of diffused line capacitance in coplanar structures," *IEDM Tech. Dig.* pp.728-731, 1980
- [7] S. Onga, M. Konaka, K. Taniguchi, H. Iwai and L. M. Dang, "SUBMODAN -a composite process/device simulation system for short-channel MOSFETs," *Proceedings of the 4th International Symposium on Silicon Materials Science and Technology*, vol 81-5, pp.1020-1028, 1981
- [8] H. Otsuka, K. Watanabe, H. Nishimura, H. Iwai, and H. Nihira, "Effect of intrinsic gettering on MOS dynamic charge storage characteristics," *Extended Abstracts, Electrochemical Society Fall Meeting, Denver*, vol. 81-2, pp.962-964, 1981
- [9] S. Sawada, S. Maeda, Y. Matsumoto, H. Iwai, H. Nihira and O. Ozawa, "Degradation of thin gate oxide under process induced electrical stress," *162nd ECS Fall Meeting, Detroit*, Recent

Newspapers, October, 1982

- [10] J. Oristian, H. Iwai, J. Walker, and R. Dutton, "Small geometry MOS intrinsic and extrinsic capacitance measurement test structure for VLSI," IEEE Workshop on VLSI Test Chip structure, San Diego, February, 1984
- [11] H. Iwai, J. Oristian, J. Walker, and R. Dutton, "Small geometry MOS transistor measurements and observed short and narrow channel effects," Digest of Technical Papers, VLSI Symposium on Technology, San Diego, pp.78-79, June, 1984
- [12] M. Pinto, R. Dutton, H. Iwai, and C. Rafferty, "Computer-aids for analysis and scaling of extrinsic devices," IEDM Tech. Dig. pp.288-291, December, 1984
- [13] H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian, and R. W. Dutton, "Analysis of short channel effects on MOS transistor capacitance by two-dimensional simulation," VLSI Process/Device Modeling Workshop, Kobe, May, 1985
- [14] Y. Niitsu, S. Taguchi, H. Fuji, Y. Shimamune, H. Iwai, and K. Kanzaki, "Latch-up free CMOS structure using shallow trench isolation," IEDM Tech. Dig. pp.509-512, December, 1985
- [15] T. Ohtani, K. Hashimoto, M. Matsui, J. Tsujimoto, H. Iwai, M. Saitoh, H. Shibata, H. Sasaki, M. Isobe, J. Matsunaga, T. Iizuka, "A 25ns 1Mb CMOS SRAM," ISSCC Digest of Technical Papers, pp.264-265, February, 1987
- [16] H. Iwai, Y. Niitsu, G. Sasaki, M. Norishima, K. Shino, Y. Sugimoto, and K. Kanzaki, "1.2 mm high performance direct ion-implanted emitter Bi-CMOS technology in comparison with poly emitter," ECS Spring Meeting, Recent Newspapers, Philadelphia, May, 1987
- [17] H. Iwai, Y. Niitsu, G. Sasaki, M. Norishima, K. Shino, Y. Unno, K. Tsugaru, H. Hara, Y. Sugimoto, and K. Kanzaki, "1.2 μ m Bi-CMOS technology with high performance ECL," 17th European Solid State Device Research Conference, pp.29-32, Bologna, 1987 : also in Solid State Devices, edited by E. Soncini and P. U. Calzolari, Elsevier Science Publishers B. V. (North-Holland), pp.199-202, 1988
- [18] H. Iwai, G. Sasaki, Y. Unno, Y. Niitsu, M. Norishima, Y. Sugimoto, and K. Kanzaki, "0.8 μ m Bi-CMOS technology with high fT ion-implanted emitter bipolar transistor," IEDM Tech. Dig. pp.28-31, December, 1987
- [19] Y. Hiruta, F. Matsuoka, K. Hama, H. Iwai, K. Maeguchi, and K. Kanzaki, "+BT instability in P+ poly gate MOS structure," IEDM Tech. Dig. pp.28-31, December, 1987
- [20] Y. Toyoshima, F. Matsuoka, H. Hayashida, H. Iwai, and K. Kanzaki, "A study on gate oxide thickness dependence of hot carrier induced degradation for n-MOSFETs," Digest of Technical Papers, Symposium on VLSI Technology, San Diego, pp.39-40, May, 1988
- [21] F. Matsuoka, K. Hama, H. Itoh, R. Nakata, H. Iwai, and K. Kanzaki, "Elecromigration and related resistance increase phenomenon on a tungsten filled via hole structure," Proc. IEEE VLSI Multilevel Interconnection Conference, Santa Clara, pp.491-497, June, 1988
- [22] F. Matsuoka, H. Hayashida, K. Hama, Y. Toyoshima, H. Iwai, and K. Maeguchi, "Drain avalanche hot hole injection mode on PMOSFETs", in IEDM Tech. Dig. pp.18-21, December, 1988
- [23] H. Hara, Y. Sugimoto, M. Noda, T. Nagamatsu, Y. Watanabe, H. Iwai, Y. Niitsu, G. Sasaki, and K. Maeguchi, "A 350 ps 50K 0.8 μ m BiCMOS gate array with shared bipolar cell structure," IEEE CICC, pp.8.5.1-8.5.4, May, 1989, San Diego, U.S.A
- [24] H. Hayashida, Y. Toyoshima, Y. Suizu, K. Mitsuhashi, H. Iwai, and K. Maeguchi, "Dopant redistribution in dual gate W-polycide CMOS and its improvement by RTA," Digest of Technical Papers, VLSI Symposium on Technology, pp.29-30, May, 1989, Kyoto, Japan
- [25] J. Wenstrand, H. Iwai, M. Norishima, G. Sasaki, Y. Niitsu, H. Tanimoto, and T. Wada, "A manufacturing-oriented design environment for fabrication process," in Work Note, 6h VLSI Process/Device Modeling Workshop, pp.27-28, May, 1989, Osaka, Japan
- [26] Y. Hiruta, H. Oyamatsu, H. S. Momose, H. Iwai, and K. Maeguchi, "Gate oxide thickness dependence of hot carrier induced degradation on pMOSFETs," 19th European Solid State Device Conference, pp.732-735, September, 1989, Berlin, Germany
- [27] Y. Niitsu, M. Norishima, G. Sasaki, H. Iwai, and K. Maeguchi, "Comparison between poly emitter bipolar characteristics with and without native oxide layers under various processes," IEEE Bipolar Circuit and Technology Meeting, pp.48-51, September, 1989, Mineapolis, U.S.A

- [28] H. S. Momose, Y. Niitsu, H. Iwai, and K. Maeguchi, "Temperature dependence of emitter-base reverse stress degradation and its mechanism analyzed by MOS structure," IEEE Bipolar Circuit and Technology Meeting, pp.98-101, September, 1989, Mineapolis, U.S.A.
- [29] K. Tsugaru, M. Noda, G. Sasaki, H. Iwai, Y. Sugimoto, and Y. Suwa, "A 10bit 40MHz ADC using 0.8 μ m Bi-CMOS technology," IEEE Bipolar Circuit and Technology Meeting, pp.140-143, September, 1989, Mineapolis, U.S.A.
- [30] J. Wenstrand, H. Iwai, R. W. Dutton, "A manufacturing-oriented environment for synthesis of fabrication processes," in Dig. Tech. IEEE International Conference on Computer-Aided Design (ICCAD), pp.376-379, November, 1989, Santa Clara, U.S.A.
- [31] M. Norishima, Y. Niitsu, H. Iwai, and K. Maeguchi, "Bipolar transistor design for low process-temperature 0.5 μ m Bi-CMOS," IEDM Tech. Dig. pp.231-240, December, 1989
- [32] H. S. Momose, S. Kitagawa, K. Yamabe, and H. Iwai, "Hot carrier related phenomena for n- and p-channel MOSFETs with nitrided gate oxide by RTA," IEDM Tech. Dig. pp.267-270, December, 1989
- [33] H. S. Momose, S. Takagi, S. Kitagawa, K. Yamabe, and H. Iwai, "Field dependent mobilities at RT and 77K for n- and p-MOSFETs with nitrided gate oxide by RTP," 20th IEEE Semiconductor Interface Specialists Conference, p.I.5, December, 1989, Ft. Lauderdale, Florida, U.S.A.
- [34] H. Iwai, F. Matsuoka, H. Oyamatsu, H. S. Momose, K. Hama, Y. Toyoshima, and H. Hayashida, "BT Reliability for thin gate oxide n+ and p+ poly MOSFETs," 20th IEEE Semiconductor Interface Specialists Conference, p.II.5, December, 1989, Ft. Lauderdale, Florida, U.S.A.
- [35] J. Wenstrand, H. Iwai, M. Norishima, H. Tanimoto, T. Wada, and R. W. Dutton, "Intelligent simulation for optimization of fabrication process," Workshop on Numerical Modeling of Process and Devices for Integrated Circuits: NUPAD III, pp.15-16, June, 1990, Honolulu, Hawaii, U.S.A.
- [36] H. Iwai, H. S. Momose, S. Takagi, T. Morimoto, S. Kitagawa, S. Kambayashi, K. Yamabe, and S. Onga, "Analysis of an ONO gate film effect on n- and p-MOSFET mobilities," Digest of Technical Papers, VLSI Symposium on Technology, pp.131-132, June, 1990, Honolulu, Hawaii, U.S.A.
- [37] H. S. Momose, T. Morimoto, S. Takagi, K. Yamabe, S. Onga, and H. Iwai, "Mechanical stress induced threshold voltage shifts for nitrided oxide gate n- and p-MOSFETs," International Conference on Solid State Device and Materials, pp.279-283, August, 1990, Sendai, Japan
- [38] T. Morimoto, H. S. Momose, K. Yamabe, and H. Iwai, "Ultra thin nitride gate MISFET operating with tunneling gate current," International Conference on Solid State Device and Materials, pp.361-364, August, 1990, Sendai, Japan,
- [39] H. Iwai, H. S. Momose, T. Morimoto, S. Takagi, and K. Yamabe, "Comparison of hot carrier degradations for n- and p-MOSFETs with various nitride-oxide gate films", ESSDERC 90, pp.287-290, September, 1990, Nottingham, England,
- [40] H. S. Momose, T. Morimoto, S. Takagi, K. Yamabe, S. Onga, and H. Iwai, "New short-channel effects on nitrided oxide gate MOSFETs," ESSDERC 90, pp.149-152, September, 1990, Nottingham, England
- [41] T. Morimoto, H. S. Momose, K. Yamabe, and H. Iwai, "Prevention of boron penetration from pt poly gate by RTP produced thin gate oxide," ESSDERC 90, pp.73-76, September, 1990, Nottingham, England,
- [42] H. S. Momose, T. Morimoto, K. Yamabe, and H. Iwai, "Relationship between mobility and residual-mechanical-stress as measured by Raman spectroscopy for nitrided-oxide-gate MOSFETs," IEDM Tech. Dig. pp.65-68, December, 1990
- [43] H. Iwai, H. S. Momose, T. Morimoto, Y. Ozawa, and K. Yamabe, "Stacked-nitride oxide gate MISFET with high hot-carrier-immunity," IEDM Tech. Dig. pp.235-238, December, 1990
- [44] T. Morimoto, H. S. Momose, Y. Ozawa, K. Yamabe, and H. Iwai, "Effects of boron penetration and resultant limitations in ultra thin pure-oxide and nitrided-oxide gate-films," IEDM Tech. Dig. pp.429-432, December, 1990
- [45] **Invited Talk:** H. Iwai, "Hot carrier induced degradation mode in thin gate insulator dual gate

- MISFETs," Workshop on "The Physics of Hot-Carrier Degradation in Silicon MOSFETs" in 1991 INFOS, Liverpool, UK, April, 1991: also Edited by W. Eccleston and M. Uren, "Insulating Films on Semiconductors 1991," pp.83-92, 1991, Adam Hilger, Bristol, Philadelphia and New York
- [46] M. Tsuchiaki, H. S. Momose, T. Morimoto, and H. Iwai, "New charge pumping method for direct measurement of spatial distribution of fixed charge," Digest of Technical Papers, VLSI Symposium on Technology, pp.19-20, May, 1991, Oiso, Japan
- [47] T. Morimoto, H. S. Momose, Y. Ozawa, K. Yamabe, and H. Iwai, "Limits on gate insulator thickness for MISFET operation in pure-oxide and nitrided-oxide gate cases," International Conference on Solid State Device and Materials, pp.23-25, Yokohama, Japan, August, (1991)
- [48] Y. Katsumata, I. Katakabe, N. Itoh, E. Tsukioka, Y. Yoshino, and H. Iwai, "Stress analysis around trench isolation for bipolar LSIs," IEEE Bipolar Circuit and Technology Meeting, pp.271-274, September, 1991, Mineapolis, U.S.A
- [49] B. Baccus, T. Wada, N. Shigyo, M. Norishima, and H. Iwai, "Impact of ion-implantation damage and transient enhanced diffusion on advanced bipolar technologies - comparisons between experiments and non-equilibrium diffusion modeling", IEEE Bipolar Circuit and Technology Meeting, pp.275-278, September, 1991, Mineapolis, U.S.A.
- [50] H. S. Momose, T. Morimoto, Y. Ozawa, M. Tsuchiaki, M. Ono, K. Yamabe, and H. Iwai, "Very lightly nitrided oxide gate MOSFETs for deep-sub-micron CMOS devices," IEDM Tech. Dig. pp.359-362, December, 1991
- [51] T. Morimoto, H. S. Momose, T. Iinuma, I. Kunishima, K. Suguro, H. Okano, I. Katakabe, H. Nakajima, M. Tsuchiaki, M. Ono, Y. Katsumata, and H. Iwai, "A NiSi salicide technology for advanced logic devices," IEDM Tech. Dig. pp.653-656, December, 1991
- [52] T. Iizima, A. Nishiyama, Y. Ushiku, T. Ohguro, I. Kunishima, K. Suguro, and H. Iwai, "A novel selective Ni₃Si contact plug technique for deep-submicron ULSIs," VLSI Symposium on Technology, pp.70-71, June, 1992, Siattle, Washington, U.S.A.
- [53] T. Iinuma, K. Inou, H. Nakajima, S. Matsuda, I. Kunishima, K. Suguro, Y. Katsumata, and H. Iwai, "A self-aligned emitter base NiSi electrode technology for advanced high speed bipolar LSIs," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.92-95, October, 1992, Mineapolis, U.S.A
- [54] N. Itoh, Yoshino, S. Matsuda, Y. Tsuboi, K. Inou, Y. Katsumata, and H. Iwai, "Optimization of shallow and deep trench isolation structures for ultra-high-speed bipolar LSIs," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.104-107, October, 1992, Mineapolis, U.S.A.
- [55] K. Inou, M. Kondo, N. Itoh, Y. Tsuboi, Y. Yoshino, H. Nakajima, Y. Katsumata, and H. Iwai, "Analysis of process margins for emitter-base self-aligned structures by combination of simulation and experiment," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.113-116, October, 1992, Mineapolis, U.S.A.
- [56] M. Saito, T. Yoshitomi, M. Ono, Y. Akasaka, H. Nii, S. Matsuda, H. S. Momose, Y. Katsumata, Y. Ushiku, and H. Iwai, "An SPDD p-MOSFET structure suitable for 0.1 and sub 0.1 micron channel length and its electrical characteristics," in IEDM Tech. Dig. pp.897-900, December, 1992, San Francisco, U.S.A.
- [57] **Invited Talk:** H. Iwai, "Application of T-CAD to Advanced Silicon Devices: Its Usage," Requirements and Problem, in Symposium on Semiconductor Modeling and Simulation Tech. Dig., pp.11-14, March, 1993, Taipei, Taiwan, ROC
- [58] C.Fiegna, H. Iwai, T. Kimura, S.Nakamura, E.Sangiorgi, and B.Riccò, "Monte Carlo Analysis of Hot Carrier Effects in Ultra Small Geometry MOSFETs," International Workshop on VLSI Process and Device Modeling:VPAD, pp.102-103, May,1993. Nara, Japan.
- [59] Y.Tsuboi, C. Fiegna, E.Sangiorgi, B.Riccò, T.Wada, Y.Katsumata, and H. Iwai, "Analysis of Collector Signal Delay in Bipolar Devices Using a Monte Carlo Method," International Workshop on VLSI Process and Device Modeling:VPAD,pp.98-99,May,1993, Nara, Japan
- [60] S.Matsuda N.Itoh, C.Yoshino, Y.Tsuboi, Y.Katsumata, and H. Iwai, "Analysis of Mechanical Stress Associated with Trench Isolation Using a Two-Dimensional Simulation," International Workshop on VLSI Process and Device Modeling: VPAD, pp.64-65,May,1993 Nara, Japan

- [61] Y.Ushiku, H.Ono, T.Iijima, N.Ninomiya, A.Nishiyama, H.Iwai, and H.Hara, "Planarized Silver Interconnect Technology with a Ti Self-Passivation Technique for Deep Sub-micron ULSIs, "Digest of Technical Papers, Symposium on VLSI Technology, pp.121-122, May, 1993, Kyoto, Japan,
- [62] T.Yoshitomi, M.Saito, H.Oguma, Y.Akasaka, M.Ono, H.Nii, Y.Ushiku, H.Iwai, and H.Hara, "Ultra-Shallow Buried-Channel P-MOSFET with Extremely High Transconductance, "Digest of Technical Papers, Symposium on VLSI Technology, pp.99-100, May, 1993, Kyoto, Japan
- [63] S.Matsuda, N.Itoh, H.Nakajima, K.Inou, T.Iinuma, C.Yoshino, Y.Tsuboi, Y.Katsumata, H.Hara, and H.Iwai, "A Low Stress Trench Isolation Structure and Its Electrical Characteristics of 20 ps High-Speed ECL, "Digest of Technical Papers, Symposium on VLSI Technology, pp.73-74, May, 1993, Kyoto, Japan
- [64] C.Fiegna, H.Iwai, T.Wada, T.Saito, E.Sangiorgi, and B.Riccò, "A New Scaling Methodology for the 0.1-0.25 μ m MOSFET." Digest of Technical Papers, Symposium on VLSI Technology , pp.33-34, May, 1993, Kyoto, Japan
- [65] T.Ohguro, T.Morimoto, Y.Ushiku, and H.Iwai, "Analysis of Anomalously Large Junction Leakage Current of Nickel Silicided N-Type Diffused Layer and Its Improvement," International Conference on Solid State Devices and Materials, pp.192-194, August, 1993, Chiba, Japan
- [66] T.Iijima, H.Ono, N.Ninomiya, Y.Ushiku, T.Hatanaka, A.Nishiyama, and H.Iwai, "Analysis of Ti Self-Passivation on Silver Interconnects for ULSIs Applications. "International Conference on Solid State Devices and Materials, pp.183-185, August, 1993, Chiba, Japan
- [67] N.Itoh, Y.Katsumata, and H.Iwai, "Noise figure degradation under emitter-base reverse stress for high-frequency bipolar ICs, "ESSDERC 93, pp. 727-730, September, 1993, Grenoble, France,
- [68] C.Fiegna, H.Iwai, E.Sangiorgi, and B.Ricco, "Analysis of Carrier Transport and Heating in Ultra-Small SOI N-MOSFETs," ESSDERC 93, pp. 675-678, September, 1993, Grenoble, France,
- [69] **Invited Talk:** H.Iwai, "CMOS Device Architecture and Technology for the 0.25 Micron to 0.025 Micron Generation," "ESSDERC 93, pp. 513-520, September, 1993, Grenoble, France,
- [70] T.Ohguro, T.Morimoto, A.Nishiyama, Y.Ushiku, and H.Iwai, "Comparison of Ti and Ni silicide as regards the electrical conductance of silicided films," ESSDERC 93, pp. 481-484, September, 1993, Grenoble, France
- [71] Y.Katsumata, N.Itoh, H.Nakajima, K.Inou, T.Iinuma, S.Matsuda, C.Yoshino, Y.Tsuboi, and H.Iwai, "Sub-20 ps ECL Bipolar Technology with High Breakdown Voltage, " ESSDERC 93, pp. 133-136, September, 1993, Grenoble, France
- [72] M.Ono, M.Saito, T.Yoshitomi, C.Fiegna, T.Ohguro, and H.Iwai, "Sub-50 nm Gate Length N-MOSFETs with 10nm phosphorus Source and Drain Junction," in IEDM Tech.Dig.pp.119-122, December, 1993.
- [73] T.Ohguro, K.Yamada, N.Sugiyama, K.Usuda, Y.Akasaka, T.Yoshitomi, C.Fiegna, M.Ono, M.Saito, and H.Iwai, "Tenth Micron P-MOSFET's with Ultra-Thin Epitaxial Channel Layer Grown by Ultra-High Vacuum CVD," in IEDM Tech.Dig.pp.433-436, December, 1993.
- [74] M.Ono, M.Saito, T.Yoshitomi, C.Fiegna, T.Ohguro, H.S.Momose, and H.Iwai, "Influence of High Substrate Doping Concentration on the Hot-Carrier and Other Characteristics of Small-Geometry CMOS Transistors Down to the 0.1 μ m Generation, "Digest of Technical Papers, Symposium on VLSI Technology, pp.147-148, June, 1994, Honolulu, Hawaii, U.S.A.
- [75] **Invited Talk:** H.Iwai, Y.Katsumata, S.Matsuda, and C.Yoshino, "Local Stress Analysis of Semiconductor Devices, "Proceedings of 22nd Symposium on ULSI Ultra Clean Technology, pp.252-264, August, 1994.
- [76] K.Inou, S.Matsuda, N.Nakajima, N.Sugiyama, K.Usuda, S.Imai, Y.Kawaguchi, K.Yamada, Y.Katsumata, and H.Iwai, "52 GHz Epitaxial Base Bipolar Transistor with High Early Voltage of 26.5V with Box-like Base and Retrograded Collector Impurity Profiles, "IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.217-220, October, 1994, Minneapolis, U.S.A.
- [77] N.Nakajima, N.Itoh, K.Inou, T.Iinuma, S.Matsuda, C.Yoshino, Y.Katsumata, and H.Iwai,

- “0.5 μ m Silicon Bipolar Transistor Technology for Analog Applications,” IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.213-216, October,1994, Minneapolis, U.S.A.
- [78] N.Itoh, Y.Yoshida, S.Watanabe, Y.Katsumata, and H.Iwai, “The Analysis of Silicon Bipolar Transistor Scaling-Down Scheme for Low Noise and Low Power Analog Application,” IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.60-63, October,1994, Minneapolis, U.S.A.
- [79] **Invited Talk:** H.Iwai, Y.Katsumata, and M.Saito, “Solid-Phase Diffusion Technique,” Technical Proceedings, SEMI Technology Symposium, pp.80-88, November,1994.
- [80] C.Fiegna, H.Iwai, M.Saito, E.Sangiorgi, “Application of Semiclassical Device Simulation to Trade-Off Studies Sub-0.1 μ m MOSFETs,” in IEDM Tech.Dig.pp.347-350, December, 1994.
- [81] S.Matsuda, C.Yoshino, H.Nakajima, K.Inou, T.Yoshitomi, Y.Katsumata, and H.Iwai, “Tree-Dimensional Mechanical Stress Analysis of Trench Isolation along{111}Gliding Planes,” in IEDM Tech.Dig.pp.885-888, December, 1994.
- [82] H.S.Momose, M.Ono, T.Yoshitomi, T.Ohguro, S.Nakamura, M.Saito, and H.Iwai, “Tunneling gate oxide approach to ultra-high current drive in small-geometry MOSFETs,” in IEDM Tech.Dig.pp.593-596, December, 1994.
- [83] M.Ono, M.Saito, T.Yoshitomi, C.Fiegna, T.Ohguro, and H.Iwai, “Fabrication of Sub-50nm Gate Length n-MOSFETs and their Electrical Characteristics,” Twenty-second Annual Conference on the Physics and Chemistry of Semiconductor Interfaces, p.SU1940, January, 1995
- [84] T.Ohguro, M.Saito, K.Endo, M.Kakumoto, T.Yoshitomi, M.Ono, H.S.Momose, and H.Iwai, “A High Frequency 0.35 μ m Gate Length Power Silicon NMOSFET Operating with Breakdown Voltage of 13 V,” Proceeding of 1995 International Symposium on Power Semiconductor Devices & Ics, pp.114-118, May, 1995, Yokohama, Japan,
- [85] **Invited Talk:** H.Iwai, H.S.Momose, and Y.Katsumata, , “Si-MOSFET Scaling Down to Deep-Sub 0.1-Micron Range and Future of Silicon LSI,” Proceeding of Technical Papers, International Symposium on VLSI Technology, Systems, and Applications, pp.262-267, May, 1995, Taipei, Taiwan, ROC
- [86] C.Yoshino, K.Inou, S.Matsuda, H.Nakajima, Y.Tsuboi, H.Naruse, H.Sugaya, Y.Katsumata, and H.Iwai, “A 62.8 GHz fmax LP-CVD Epitaxially Grown Silicon Base Bipolar Transistor with Extremely High Early Voltage of 85.7 V,” Digest of Technical Papers, Symposium on VLSI Technology, pp.131-132, June, 1995, Kyoto, Japan
- [87] M.Saito, M.Ono, R.Fujimoto, C.Takahashi, H.Tanimoto, N.Ito, T.Ohguro, T.Yoshitomi, H.S.Momose, and H.Iwai, “ Advantage of Small Geometry MOSFETs for High-Frequency Analog Applications under Low Power Supply Voltage of 0.5 V, ” Digest of Technical Papers, Symposium on VLSI Technology, pp.71-72, June, 1995, Kyoto, Japan
- [88] T.Ohguro, N.Sugiyama, K.Imai, K.Usuda, M.Saito, T.Yoshitomi, M.Ono, H.S.Momose, and H.Iwai, “ The influence of oxygen at epitaxial Si/Si substrate interface for 0.1 μ m epitaxial Si channel N-MOSFETs grown by UHV-CVD, ”Digest of Technical Papers, Symposium on VLSI Technology, pp.21-22, June, 1995, Kyoto, Japan
- [89] T.Yoshitomi, M.Saito, T.Ohguro, M.Ono, H.S.Momose, and H.Iwai, “ Silicided Silicon-Sidewall Source and Drain (S⁴D) structure for high-performance 75-nm gate length pMOSFETs, ” Digest of Technical Papers, Symposium on VLSI Technology, pp.11-12, June, 1995, Kyoto, Japan
- [90] **Invited Talk:** H.Iwai, H.S.Momose, M.Saito, M.Ono, and Y.Katsumata, “ The future of ultra-small-geometry MOSFETs beyond 0.1 micron, ” in 1995 INFOS, Villard-de-Lans, June, 1995, France : also Edited by S. Cristoloveanu and N.Gillemot, “ Insulating Films on Semiconductors 1995, ” pp.147-154, 1995
- [91] T.Yoshitomi, M.Saito, T.Ohguro, M.Ono, H.S.Momose, and H.Iwai, “ A High Performance 0.15 μ m Single Gate CMOS Technology, ”International Conference on Solid State Devices and Materials, pp.222-224, August,1995, Osaka, Japan,

- [92] K.Inou, Y.Katsumata, S.Matsuda, H.Naruse, H.Sugaya, and H.Iwai, "Improvement of Narrow Emitter Bipolar Transistor Performance by In-situ Highly Doped Arsenic Polysilicon Technique," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp.93-96, September, 1995, Minneapolis, U.S.A.
- [93] T.Ohguro, S.Nakamura, E.Morifuji, M.Ono, T.Yoshitomi, M.Saito, H.S.Momose, and H.Iwai, "Nitrogen-doped nickel monosilicide technique for deep submicron CMOS salicide" in IEDM Tech. Dig. pp.453-546, December, 1995
- [94] **Invited Talk:** H.Iwai, "Si-MOSFET downsizing into deep-sub-0.1 μm regime and images of future silicon LSIs towards 2010s" FUET '96, International Symposium on the Basic of Future Electronics technology, pp.57-64, February, 1996, Oiso, Japan
- [95] **Plenary Invited Talk:** H.Iwai, W.Fichtner, and R.W.Dutton, "TCAD for Sub-0.1 Micrometer Era – Present Status & Future - , " 1996 Semiconductor Technology CAD Workshop & Exhibition, pp.1-42, May, 1996, Taiwan, ROC
- [96] T.Ohguro, E.Morifuji, M.Saito, M.Ono, T.Yoshitomi, H.S.Momose, N.Ito, and H.Iwai, "0.2 μm analog CMOS with very low noise figure at 2 GHz operation," Digest of Technical Papers, Symposium on VLSI Technology, pp.132-133, June, 1996, Honolulu, Hawaii, U.S.A.
- [97] T.Yoshitomi, T.Ohguro, M.Saito, M.Ono, E.Morifuji, H.S.Momose, and H.Iwai, "High Performance 0.15 μm Single Gate Co Salicide CMOS," Digest of Technical Papers, Symposium on VLSI Technology, pp.34-35, June, 1996, Honolulu, Hawaii, U.S.A.
- [98] **Invited Talk:** H.Iwai, "Ultra-small MOSFET Limits and Device Prospects for the Year 2010," IEEE Silicon Nanoelectronics Workshop, June, 1996, Honolulu, Hawaii, U.S.A.
- [99] T.Yoshitomi, M.Saito, T.Ohguro, M.Ono, H.S.Momose, and H.Iwai, "Hot-Carrier Reliability of S^4D n-MOSFETs," ESSDERC '96, pp.65-68, September, 1996, Bologna, Italy
- [100] **Plenary Invited Talk:** H.Iwai, "Recent advances and future trends of ULSI technologies," ESSDERC'96, pp.46-52, September, 1996, Bologna, Italy,
- [101] H.S.Momose, S.Nakamura, Y.Katsumata, and H.Iwai, "Thin Gate Dielectrics for future CMOS Applications," 27th IEEE Semiconductor Interface Specialists Conference, 8.1, December, 1996, San Diego, California, U.S.A.
- [102] H.S.Momose, E.Morifuji, T.Yoshitomi, T.Ohguro, M.Saito, T.Morimoto, Y.Katsumata, and H.Iwai, "High-frequency AC Characteristics of 1.5 nm Gate Oxide MOSFETs," in IEDM Tech. Dig. pp.105-108, December, 1996
- [103] T.Ohguro, M.Saito, E.Morifuji, K.Murakami, K.Matsuzaki, T.Yoshitomi, T.Morimoto, H.S.Momose, Y.Katsumata, and H.Iwai, "High efficiency 2 GHz power Si-MOSFET design under low supply voltage down to 1V," in IEDM Tech. Dig. Pp.83-86, December, 1996
- [104] **Invited Talk:** H.Iwai, "Future High Performance Technologies for Sub-0.1 μm Devices," Semiconductor Technology Symposium, SEMICON Korea 97, pp.IV 30-39, February, 1997, Korea
- [105] T.Ohguro, S.Nakamura, E.Harakawa, E.Morifuji, T.Yoshitomi, T.Morimoto, H.S.Momose, Y.Katsumata, and H.Iwai, "Salicide Technology for Advanced CMOS Devices," Semiconductor technology Symposium, SEMICON Korea 97, pp. 57-66, February, 1997, Korea
- [106] T.Ohguro, S.Nakamura, M.Saito, M.Ono, H.Harakawa, E.Morifuji, T.Yoshitomi, T.Morimoto, H.S.Momose, Y.Katsumata, and H.Iwai, "Ultra-shallow Junction and Salicide Techniques for Advanced CMOS Devices," in Proceedings of the Sixth International Symposium on Ultralarge Scale Integration Science and Technology, Electrochemical Society, pp.275-295, May, 1997
- [107] H.S.Momose, S.Nakamura, Y.Katsumata, and H.Iwai, "Ultra-thin Gate Oxide Technology for High Performance CMOS," in Proceedings of the Sixth International Symposium on Ultralarge Scale Integration Science and Technology, Electrochemical Society, pp.235-246, May, 1997
- [108] **Invited Talk:** H.Iwai, "RF CMOS Technology," Symposium on ULSI Technology & Systems, May, 1997, Hsinchu, Taiwan, ROC

- [109] H.S.Momose, S.Nakamura, T.Ohguro, Y.Katsumata, and H.Iwai, "Uniformity and Reliability of 1.5nm direct tunneling gate oxide MOSFETs," Symposium on VLSI Technology, pp.15-16, June, 1997, Kyoto, Japan,
- [110] T.Ohguro, S.Nakamura, E.Morifuji, Y.Katsumata, and H.Iwai, "0.25mm CoSi₂ salicide technology thermally stable upto 1000C with high TDDDB reliability," Symposium on VLSI Technology, pp.102-103, June, 1997, Kyoto, Japan
- [111] H.S.Momose, and H.Iwai, "Low power, low voltage integrated circuit," Internal Summer School on Advanced Microelectronics, June, 1997, Grenoble, France
- [112] H.Iwai, "Silicon MOSFET scaling beyond 0.1mm" International Microelectronics Conference, pp.11-18, Nis, September, 1997, Yugoslavia,
- [113] H.S.Momose, S.Nakamura, Y.Katsumata, and H.Iwai, "Tunnelling gate oxide MOSFET technology" European Solid State Device Research Conference (ESSDERC), pp.133-143, September, 1997, Ludwigberg, Germany
- [114] H.Iwai, "CMOS Scaling beyond 0.1mm" IEEE EDS Distinguished Lecture Univ. of Florida, September, 1997, Gainesville, FL, USA
- [115] H.Nii, C.Yoshino, H.Nakajima, Y.Katsumata, and H.Iwai, "0.3mm BiCMOS technology for mixed analog/digital application systems" IEEE bipolar/BiCMOS Circuit and Technology Conference(BCTM), pp.68-71, September, 1997, Minneapolis, MN, U.S.A.
- [116] H.Iwai, "CMOS downsizing and future concept of Si-LSI" International Conference on VLSI and CAD, pp.162-167, November, 1997, Seoul, Korea
- [117] H.S.Momose, S.Nakamura, T.Ohguro, Y.Katsumata and H.Iwai, "A study of hot-carrier degradation in n- and p-MOSFETs with ultra-thin gate oxide in the direct-tunneling regime" IEEE International Electron Devices Meeting (IEDM), pp.453-456, December, 1997, Washington DC, U.S.A.
- [118] T.Ohguro, H.Naruse, H.S.Momose, Y.Katsumata and H.Iwai, "0.18mm low voltage / low power RF CMOS with zero V_{tn} analog MOSFETs made by undoped epitaxial channel technique" IEEE International Electron Devices Meeting (IEDM), pp.837-840, December, 1997, Washington DC, U.S.A.
- [119] **Invited Talk:** H. Iwai, "The downsizing of silicon devices and the impact on computers and communications," International Conference on Computers and Devices for Communications (CODEC'98), pp.4-13, January, 1998, Calcutta, India
- [120] H.Iwai, "CMOS scaling below 0.1mm" IEEE Distinguished Lecture" IEEE Distinguished Lecture, January, 1998, Singapore,
- [121] **Invited Talk:** H. Iwai, "Scaling CMOS below 0.1μm," A Workshop Honoring of the Career of Robert H. Dennard on the Occasion of the 320th Anniversary of the 1-Transistor DRAM Memory Cell, May, 1998, Yorktown Heights, NY, U.S.A.
- [122] H. Iwai, "CMOS - year 2010 and beyond ; from technological side," IEEE Custom Integrated Circuit Conference (CICC'98), pp.141 – 148, May, 1998, Santa Clara, U.S.A.
- [123] **Invited Talk:** Y. Unno and H. Iwai, "Future trends in semiconductor technologies, -- from industrial view point," 1998 Advanced Research Workshop, Future Trends in Microelectronics: Off the Beaten Path, May 31- June 5, 1998, Ike des Embiez, France
- [124] H. S. Momose, S. Nakamura, Y. Katsumata, and H. Iwai, "Study of direct-tunneling gate oxides for CMOS applications," 3rd International Symposium on Plasma-Induced Damage, pp.30-33, June, 1998, Honolulu, Hawaii, U.S.A.
- [125] T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "High performance RF characteristics of raised gate/source/drain CMOS with Co salicide," Dig. Tech., Symp on VLSI Tech., pp.136-137, June, 1998, Honolulu, Hawaii, U.S.A.
- [126] T. Yoshitomi, H. Kimijima, S. Ishizuka, Y. Miyahara, T. Ohguro, E. Morifuji, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "A study of self-aligned doped channel structure for low power and low 1/f noise operation," Dig. Tech., Symp on VLSI Tech., pp.98-99, June, 1998, Honolulu, Hawaii, U.S.A

- [127] H. Momose, R. Fujimoto, S. Otaka, E. Morifuji, T. Ohguro, T. Yoshitomi, H. Kimijima, S. Nakamura, T. Morimoto, Y. Katsumata, H. Tanimoto, and H. Iwai, "RF noise in 1.5 nm gate oxide MOSFETs and the evaluation of NMOS LNA circuit integrated on a chip," Dig. Tech., Symp on VLSI Tech., pp.96-97, June, 1998, Honolulu, Hawaii, U.S.A.
- [128] E. Morifuji, C. E. Biber, W. Bachtold, T. Ohguro, T. Yoshitomi, H. Kimijima, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "RF noise study of small gate width Si-mOSFETs up to 8 GHz applications," International Conference on Solid State Devices and Materials, pp.80-81, September, 1998, Hiroshima, Japan,
- [129] **Plenary Invited Talk:** H. Iwai, "Current status and future of advanced CMOS technologies – digital and analog aspects --," Int Conf. on Advanced Semiconductor Devices and Microelectronics (ASDAM'98), pp.1-10, October, 1998, Smolenice, Slovakia
- [130] **Invited Talk:** H. Iwai, "CMOS Scaling toward its limits," Int. Conf. on Solid-State and Integrated Circuit Technology (ICSICT'98), pp.31-34, October, 1998, Beijing, China
- [131] **Invited Talk:** H. Iwai, "Thin film technology for CMOS downsizing towards its limit", International Workshop on Development of Thin Film for Future ULSI's, p.17, 1998
- [132] **Invited Talk:** H. Iwai and H. S. Momose, "Ultra-thin gate oxide – performance and reliability", Dig. Tech., pp.163-166, December, 1998, San Francisco, U.S.A.
- [133] E. Morifuji, T. Ohguro, T. Yoshitomi, H. Kimijima, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "Process induced damage on RFCMOS," Tech. Dig. IEDM, Dig. Tech., pp.956-968, December, 1998, San Francisco, U.S.A.
- [134] T. Ohguro, H. Naruse, H. Sugaya, H. Kimijima, E. Morifuji, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, H. Iwai, "0.12 μ m Raised Gate/source/Drain Epitaxial Channel NMOS Technology" Tech. Dig. IEDM, Dig. Tech., pp.927-930, December, 1998, San Francisco, U.S.A.
- [135] H. S. Momose, H. Kimijima, S. Ishizuka, Y. Miyahara, T. Ohguro, T. Yoshitomi, E. Morifuji, S. Nakamura, T. Morimoto, Y. Katsumata, and H. Iwai, "A study of flicker noise in n- and p-OSFETs with ultra-thin gate oxides in the direct-tunneling regime," Tech. Dig. IEDM, Dig. Tech., pp.923-926, December, 1998, San Francisco, U.S.A.
- [136] T. Yoshitomi, Y. Sugawara, E. Morifuji, T. Ohguro, H. Kimijima, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "On-chip spiral inductors with diffused shields using channel-stop implant," Tech. Dig. IEDM, Dig. Tech., pp.540-543, December, 1998, San Francisco, U.S.A.
- [137] Y. Katsumata, T. Ohguro, H. S. Momose, E. Morifuji, and H. Iwai, "RF CMOS technology," 1998 Asa-Pacific Microwave Conference, Workshop, WS2. Leading Edge Silicon Devices and Their Applications to Microwave/Millimeter-Wave Circuits, pp.3-20, December, 1998, Yokohama, Japan,
- [138] **Plenary Invited Talk:** H. Iwai, "RF CMOS technology," Int. Electron Devices and Material Symposia (IEDMS'98), pp.1-01, December, 1998, Tainan, Taiwan, ROC
- [139] H. Iwai, "Downsizing of CMOS Towards Deep Sub-0.1 Micro-Meter and its Limitation", The 6th Korean Conference on Semiconductors, pp.1-4, February, 1999, Korea
- [140] H. Kimijima, T. Ohguro, B. Evans, B. Acker, J. Bloom, H. Mabuchi, D.-L. Kwong, E. Morifuji, T. Yoshitomi, H.S. Momose, M. Kinugawa, Y. Katsumata, and H. Iwai, "Improvement of 1/f noise by using VHP (Vertical High Pressure) oxynitride gate insulator for deep-sub micron RF and analog CMOS", 1999 Symposium on VLSI Technology, pp. 119-120, June, 1999, Kyoto, Japan
- [141] J.-S. Goo, C.-H. Choi, E. Morifuji, H.S. Momose, Z. Yu, H. Iwai, T.H. Lee, and W. Dutton, "RF Noise Simulation for Submicron MOSFET's Based on Hydrodynamic Model", 1999 Symposium on VLSI Technology, pp.153-154, June, 1999, Kyoto, Japan
- [142] E. Morifuji, H.S. Momose, T. Ohguro, T. Yoshitomi, H. Kimijima, F. Matsuoka, M. Kinugawa, Y. Katsumata, and H. Iwai, "Future perspective and scaling down roadmap for RF CMOS", 1999 Symposium on VLSI Technology, pp.163-164, June, 1999, Kyoto, Japan
- [143] E. Morifuji, T. Ohguro, H. Kimijima, T. Yoshitomi, H. S. Momose, Y. Katsumata, K. Ishimaru, F. Matsuoka, M. Kinugawa, H. Iwai, "RF modeling for 0.1 μ m gate length MOSFETS", 29th European Solid-State Device Research Conference, pp.656-659, September, 1999, Leuven, Belgium

- [144] **Invited Talk:** H. Iwai, "Scaling laws of CMOS How this can be driven?", in Litho Workshop, A path towards sub-100nm lithography, IMEC, pp.1-14, September, 1999, Leuven, Belgium
- [145] **Invited Talk:** H. Iwai, Y. Katsumata, T. Ohguro, E. Morifuji, H.S. Momose, K. Inoh, H. Nii, "Advanced Silicon BIPOLAR, BICMOS and CMOS technologies for RF Applications", EUMW (European Microwave)-Workshop 1999, Silicon and SiGe Technologies and Circuits, pp.4-7, October 1999, Munich, Germany
- [146] T. Yoshitomi, Y. Ebuchi, H. Kimijima, T. Ohguro, E. Morifuji, H. S. Momose, K. Kasai, K. Ishimaru, F. Matsuoka, Y. Katsumata, M. Kinugawa and H. Iwai, "High Performance MIM Capacitor for RF BiCMOS/CMOS LSIs", Proceedings of the 1999 BIPOLAR/BiCMOS Circuits and Technology Meeting (BCTM), pp.133-136, September, 1999, Minneapolis, Minnesota, U.S.A.
- [147] **Invited Talk:** H. Iwai, T. Ohguro, E. Morifuji, T. Yoshitomi, H. Kimijima, H. S. Momose, K. Inoh, H. Nii, Y. Katsumata, "Advanced RF CMOS Technology", Proceedings of SPIE (The International Society for Optical Engineering)-Electronics and Structures for MEMS, pp.10-20, October, 1999, Queensland, Australia
- [148] T. Ohguro, H. Naruse, H. Sugaya, S. Nakamura, N. Sugiyama, E. Morifuji, H. Kimijima, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata and H. Iwai, "Silicon Epitaxy and Its Application to RFIC's", The First Symposium on ULSI Process Integration, Electrochemical Society Proceedings, vol.99-18, pp.123-141 in the 196th Meeting of the Electrochemical Society, pp.123-141, October 1999, Honolulu, Hawaii, U.S.A.
- [149] **Invited Talk:** H. Iwai, "Sub-100nm MOSFET technologies", International Symposium on Surface Science for Micro-and Nano-Device Fabrication, pp.,5, November. 1999, Tokyo, Japan
- [150] **Plenary Invited Talk:** H. Iwai, "Problems for downsizing of CMOS below 0.1 μm and attempts for solution by introduction of new materials, structures and planarization", International CMP Symposium '99, November, 1999, Tokyo, Japan
- [151] **Invited Talk:** H. Iwai, "Next-generation RF silicon device technology for mobile telecommunication", 1999 The 20th Modern Engineering and Technology Symposium, December, 1999, Taipei, Taiwan, ROC
- [152] H.S.Momose, E.Morifuji, H.Sugaya, S.Nakamura, T.Yoshitomi, H.Kimijima, T.Morimoto, F.Matsuoka, Y.Katsumata, H.Ishiuchi and H.Iwai, "Improvement of direct-tunneling gate leakage current in ultra-thin gate oxide CMOS with TiN gate electrode using non-doped selective epitaxial Si channel technique", International Electron Devices Meeting 1999, pp.819-822, December. 1999, Washington DC, U.S.A.
- [153] H. Iwai, "Source Drain and Wells" in Sub-100nm CMOS, 1999 IEDM Short Course, pp.1-95, December, 1999, Washington DC, U.S.A.
- [154] **Invited Talk:** H. Iwai, "Sub-100nm MOSFET Technologies", ISSS 2000, February, 2000, India
- [155] **Invited Talk:** H. Iwai, T. Ohguro, E. Morifuji, T. Yoshitomi, H. Kimijima, H. S. Momose, S. Ohmi, K. Inoh, H. Nii, Y. Katsumata, "CMOS Technologies for High Frequencies", GHz2000 Symposium, pp.41-45, March, 2000, Göteborg, Sweden,
- [156] **Plenary Invited Talk:** H. Iwai, H. S. Momose, S. Ohmi, "Ultra-thin gate SiO₂ technology", proceedings of The Fourth International Symposium on The Physics and Chemistry of SiO₂ Interface, Electrochemical Society, pp.3-17, also in the Meeting Abstracts, the 197th Meeting of the Electrochemical Society, vol.2000-1, p.443, May14-18, 2000, Toronto, Canada,
- [157] **Invited Talk:** H. Iwai, "CMOS Technology for RF Application", presented at the 22nd International Conference On Microelectronics (MIEL 2000), pp.27-34, May 2000, Niš, Yugoslavia,
- [158] **Invited Talk:** H. Iwai, "High-speed low-power CMOS technology", conference proceedings of the SEMICON Kansai 2000, Session 3, pp.42-51, June 1-2, 2000
- [159] **Invited Talk:** H. Iwai, S. Ohmi, "Future CMOS Technology below 0.1 μm ", SBMicro2000, pp.2-17, September 18-24, 2000, Manaus, Amazonas, Brazil

- [160] **Plenary Invited Talk:** H. Iwai, S. Ohmi, "Problems and solutions for downsizing CMOS below 0.1 μm ", Proceedings for 2000 IEEE International Conference on Semiconductor Electronics (ICSE2000), pp.1-19, November 13-15, 2000, Malaysia
- [161] **Invited Talk:** H. Iwai, "Gate Oxide Film and Small-Geometry MOS Devices", Abstracts, Joint Workshop of 29th IUVSTA International Workshop on Selective and Functional Film Deposition Technologies as Applied to ULSI Technology, and 2nd International Workshop on Development of Thin Films for Future ULSI's and Nano-Scale Process Integration, Ise-Shima, pp.108-122, November 19-24, 2000, Mie, Japan
- [162] R. Fujimura, K.Sato, M. Takeda, S. Ohmi, H. Ishiwara, H. Iwai, "The relation between dielectric constant and short-channel effects for high-k gate insulator film's MOSFETs down to sub 50nm", Abstracts, Joint Workshop of 29th IUVSTA International Workshop on Selective and Functional Film Deposition Technologies as Applied to ULSI Technology, and 2nd International Workshop on Development of Thin Films for Future ULSI's and Nano-Scale Process Integration, Ise-Shima, pp.165-169, November 19-24, 2000, Mie, Japan
- [163] K. Osima, E. Tokumitsu, S. Ohmi, H. Iwai, and H. Ishiwara, "Electrical Characteristics of High Dielectric Constant ZrO₂ Thin Films Prepared by Ultra High Vacuum-Electron Beam Evaporation Method", Abstracts, Joint Workshop of 29th IUVSTA International Workshop on Selective and Functional Film Deposition Technologies as Applied to ULSI Technology, and 2nd International Workshop on Development of Thin Films for Future ULSI's and Nano-Scale Process Integration, Ise-Shima, pp.323-326, November 19-24, 2000, Mie, Japan
- [164] **Invited Talk:** H. Iwai, "Silicon Technology-Miniaturization from past to future," Inauguration Workshop of the Microtechnology Center at Chalmers, MC2, March 1, 2001 Göteborg, Sweden
- [165] **Invited Talk:** H. Iwai, T. Ohguro, S. Ohmi, "NiSi Salicide Technology for Scaled CMOS," Abstract, European Workshop Materials for Advanced Metallization (MAM2001), p.07.5, March 5-7, 2001, Sigtuna, Sweden
- [166] **Plenary Invited Talk:** H. Iwai and S. Ohmi, "ULSI Process Integration for 2005 and beyond," ULSI Process Integration II, Electrochemical Society Proceedings Volume 2001-2, pp.3-33, 2001, also Abstract No.395, Meeting Abstracts, The 199th Meeting of The Electrochemical Society, March 25-29, 2001
- [167] R. Fujimura, M. Takeda, K. Sato, S. Ohmi, H. Ishiwara, and H. Iwai, "Enhanced short-channel effects of sub-50nm gate length MOSFETs with high-k gate insulator films," ULSI Process Integration II, Electrochemical Society Proceedings Volume 2001-2, pp.313-323, 2001, also Abstract No.421, Meeting Abstracts, The 199th Meeting of The Electrochemical Society, March 25-29, 2001
- [168] H. S. Momose, T. Ohguro, S. Nakamura, Y. Toyoshima, H. Ishiuchi and H. Iwai, "Study of 0wafer orientation dependence on performance and reliability of CMOS with direct-tunneling gate oxide," 2001 Symposium on VLSI Technology, Kyoto, Digest of Technical Papers, pp.77-78, June 12-14, 2001
- [169] H. Iwai and S. Ohmi, "Gate dielectrics for deep sub-0.1 μm CMOS," FTM 2001 Poster Presentations, Scientific Program, 2001 Advanced Research Workshop, Future Trends in Microelectronics: The Nano Millennium, pp.45, June 25-29, 2001, Ile de Bendor, France
- [170] **Keynote Invited Talk:** H. Iwai, "Direction of Silicon Technology from Past to Future," Keynote address, 8th International Symposium on the Physical & Failure Analysis of Integrated Circuits, IPFA 2001, Proceedings, pp.1-35, July 9-13, 2001, Singapore
- [171] **Invited Talk:** H. Iwai and S. Ohmi, "Problems and expected solutions for the gate oxide thinning in miniaturized CMOS ULSI devices," International Workshop on Device Technology, Alternatives to SiO₂ as Gate Dielectric for Future Si-Based Microelectronics, pp.16, September 3-5, 2001, Porto Alegre, Brazil, also 2001 MRS Workshop Series, pp.1-12, 2001
- [172] S. Ohmi, C. Kobayashi, E. Tokumitsu, H. Ishiwara and H. Iwai, "Low Leakage La₂O₃ Gate Insulator Film with EOTs of 0.8-1.2 nm", the 2001 International Conference on Solid State Devices and Materials, pp.496-497, 2001
- [173] S. Ohmi, S. Akama, A. Kikuchi, I. Kashiwagi, C. Ohshima, J. Taguchi, H. Yamamoto, C.

- Kobayashi, K. Sato, M. Takeda, K. Oshima, H. Ishiwara and H. Iwai, "Rare Earth Metal Oxide Gate Thin Films Prepared by E-beam Deposition," International Workshop on Gate Insulator 2001, pp200-204, November 2001, Tokyo Japan
- [174] **Invited Talk:** H. Iwai, "Silicon technology trend from past to future," IEEE Electron Devices and Solid-State Circuits Society Bangalore Chapter, March 2002, India
- [175] **Invited Talk:** H. Iwai, S. Ohmi, "CMOS Downsizing and High-k Gate Insulator Technology", Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, pp.D049_1-8, April 17-19, 2002, Aruba
- [176] S. Ohmi, S. Akama, A. Kikuchi, I. Kashiwagi, C. Ohshima, J. Taguchi, H. Yamamoto, K. Sato, M. Takeda, H. Ishiwara, H. Iwai, " Rare earth metal oxides for high-k gate insulator," 201st ECS Meeting, abstracts vol.2002-1, pp.585, May 12-17 2002, Philadelphia U.S.A., also Proc. of the Ninth International Symposium on Silicon Material Science and Technology, Semiconductor Silicon 2002, pp. 376-383
- [177] H. Iwai: Advanced Device Technologies for sub-65nm Node FEOL; Varian semiconductor equipment vTech 2002, July 2002
- [178] S. Ohmi, M.Takeda, H.Ishiwara and H. Iwai: Characterization of Lu₂O₃ High-k Thin Films on Si(100) Fabricated by E-beam Deposition Method; Abstract of ISTC2002, September 2002
- [179] S.Ohmi, I.Kashiwagi, C.Ohshima, J.Taguchi, H.Yamamoto, J.Tonotanim H.Ishiwara and H.Iwai: Electrical Characteristics of Rare Earth Gate Oxides Improved by Chemical Oxide and Long Low Temperature Annealing; Abstracts of the 2002 International Conference on SSDM, pp.718-719, September 2002
- [180] T.Shiraishi, T.Nakamura, K.Takahashi, I.Kashiwagi, C.Ohshima, H.Nohira, S.Ohmi, H.Iwai and T.Hattori: Depth Profiling of High-K Dielectric/Si Interfacial Transition Layer; abstracts of international conference of SSDM, pp.758-759, September 2002
- [181] C. Ohshima, I. Kashiwagi, S. Ohmi and H. Iwai, "Electrical Characteristics of Gd₂O₃ thin film deposited on Si substrate" Proceedings of ESSDERC2002, pp.415-418, September 2002
- [182] S. Akama, A. Kikuchi, J. Tonotani, S. Ohmi, and H. Iwai: "Stability of High-k Thin Films in Moisture Ambience - The Effect of Dissolution Gas from Acryl Apparatus-" Proceedings of ESSDERC2002, pp.587-590, September 2002
- [183] J. Taguchi, H. Yamamoto, J. Tonotani, S. Ohmi and H. Iwai, "Annealing Condition Dependence of Electrical Characteristics for Dy₂O₃/Si(100) Structures" Proceedings of ESSDERC2002, pp.591-594, September 2002
- [184] **Invited Talk:** H.Iwai, S.Ohmi, "Trend of CMOS downsizing and its reliability", Proceedings of ESREF2002, pp.1251-1258, October 2002
- [185] H. Yamamoto, J. Taguchi, S. Ohmi and H. Iwai, "Electrical Characteristics Improvement of Dy₂O₃ Thin Films by In-situ Vacuum Anneal", abstracts of ECS 202nd Meeting, October 2002
- [186] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, I. Kashiwagi, A. Kikuchi, J. Taguchi, H. Yamamoto, I. Ueda, A. Kuriyama, J. Tonotani, Y. Kim, Y. Yoshihara and H. Ishiwa, "High Dielectric Constant Gate Insulator Technology using Rare Earth Oxides" abstracts of ECS 202nd Meeting, October 2002
- [187] A. Kikuchi, S. Akama, S. Ohmi and H. Iwai, "Stability of High-k Thin Films for Wet Process" abstracts of ECS 202nd Meeting, October 2002
- [188] I. Kashiwagi, C. Ohshima, S. Ohmi and H. Iwai, "Characteristics of High-k Gd₂O₃ Films Deposited on Different Orientation of Si Substrate" abstracts of ECS 202nd Meeting, October 2002
- [189] H. Yamamoto, J. Taguchi, S. Ohmi, and H. Iwai, "The Effect of In-situ Vacuum Anneal for High-Dielectric Dy₂O₃ Thin Films" abstracts of μ E-ED 2002, pp.16-17, October 2002
- [190] I. Kashiwagi, C. Ohshima, Y. Kim, S. Ohmi, K. Tsutsui and H. Iwai, "Dependence of Gd₂O₃ Thin Film Properties on Si Substrate Orientation" abstracts of μ E-ED 2002, pp.14-15, October 2002
- [191] A.Kikuchi, S. Akama, S. Ohmi, K. Tsutsui and H. Iwai, "High-k Gate Insulator Endurance against Moisture Ambience and Wet Process" abstracts of IEEE μ E-ED 2002, pp.12-13, October 2002
- [192] H. Iwai, "CMOS Downscaling Towards Its Limit" abstracts of IEEE μ E-ED 2002, pp.4-5,

October 2002

- [193] H. Iwai, "CMOS Scaling and Requested New Technologies" Proceedings of SISC2002, December, 2002
- [194] H. Nohira, T. Shiraishi, T. Nakamura, K. Takahashi, M. Takeda, S. Ohmi, H. Iwai and T. Hattori, "Chemical and Electronic Structures of Lu_2O_3 /Si Interfacial Transition Layer" abstracts of 4th ISCSI, October 2002
- [195] C. Ohshima, J. Taguchi, I. Kashiwagi, H. Yamamoto, S. Ohmi and H. Iwai, "Effect of Surface Treatment of Si substrates and Annealing Condition on High-k Rare Earth Oxide Gate Dielectrics" abstracts of 4th ISCSI, October 2002
- [196] H. Iwai, "Advanced CMOS Technology for Sub-70 nm and further below", 1st WIMNACT, pp.3-98, November 2002
- [197] F.Lime, K.Oshima, M.Cassé, G.Ghibaud, S.Cristoloveanu, B.Guillaumot, H.Iwai, "Electrical Characterization of Advanced CMOS Devices with Metal Gate and HfO_2 Gate Dielectric", Proceedings WoDIM 2002, pp.81-84, November 2002
- [198] **Plenary Invited Talk:** H.Iwai, "CMOS Scaling and Requested New Technologies", 33rd IEEE SISC 2002, December 2002
- [199] **Invited Talk:** H.Iwai, S.Ohmi, S.Akama, C.Ohshima, A.Kikuchi, I. Kashiwagi, J.Taguchi, H.Yamamoto, J.Tonotani, Y.Kim, I.Ueda, A.Kuriyama, and Y.Yoshihara, "Advanced Gate Dielectric Materials for Sub-100nm CMOS", IEDM 2002, pp.625-628, December 2002
- [200] H.Iwai, "CMOS Downsizing toward sub-10 nm", ULIS 2003, pp7-10, March 2003
- [201] **Invited Talk:** H.Iwai, "Prospects and Challenges for Advanced Gate-Stack Materials in Sub-65 nm CMOS", 2003 MRS Spring Meeting, Abstracts pp.90, April 2003
- [202] **Keynote Invited Talk:** H.Iwai, "CMOS down scaling and process induced damages", 2003 8th International Symposium on Plasma- and Process- Induced Damage, pp1-11, April 2003
- [203] K.Oshima, S.Cristoloveanu, B.Guillaumot, G.le Carval, H.Iwai, C. Mazure, M.S.Kang, Y.H.Bae, M.W.Kwon, J.H.Lee and S.Deleonibus, "Replacing the BOX with Buried Alumina: Improved Thermal Dissipation in SOI MOSFETs" 203rd ECS Meeting, Vol.2003-01, Abstract No.815, 2003
- [204] J.O.Borland, H.Iwai, W.Masazara and H.Wang, "Extending the Life of Planar Single-Gate CMOS & the Realization of Double-Gate/Multi-Gate CMOS Devices", 203rd ECS Meeting, Vol.2003-01, Abstract No.976, 2003
- [205] T.Hattori, T.Yoshida, T.Shiraishi, K.Takahashi, H.Nohira, S.Joumori, K.Nakajima, M.Suzuki, K.Kimura, I.Kashiwagi, C.Ohshima, S.Ohmi and H.Iwai, "Composition, Chemical Structure and Electronic Band Structure of Rare Earth Oxide/Si(100) Interfacial Transition Layer", INFOS 2003-Barcelona, WS1-9, June 2003
- [206] H.Iwai, "The Future of CMOS Downscaling", FTM(Future Trends in Microelectronics)-2003, Corsica, France, p46, June 2003
- [207] J.O.Borland, H.Iwai, W.Masazara and H.Wang, "Extending Planar Single-Gate CMOS & Accelerating the Realization of Double-Gate/Multi-Gate CMOS Devices" ULSI Process Integration III, Vol.2003-06, pp.330-345, 2003
- [208] **Plenary Invited Talk:** H.Iwai, "Advanced High K Dielectrics", ESSDERC 2003, pp. 15, September 2003, Estoril, Portugal
- [209] R.Higaki, K.Tsutsui, Y.Sasaki, S.Akama, B.Mizuno, S.Ohmi and H.Iwai, "Effects of gas phase absorption into Si substrates on plasma doping process", ESSDERC 2003, pp.231-234, September 2003, Estoril, Portugal
- [210] Y.Kim, A.Kuriyama, I.Ueda, S. Ohmi, K.Tsutsui and H.Iwai, "Analysis of Electrical Characteristics of La_2O_3 Thin Films Annealed in Vacuum and Others", ESSDERC 2003, pp.569-572, September 2003, Estoril, Portugal
- [211] S.Ohmi, H.Yamamoto, J.Taguchi, K.Tsutsui and H.Iwai, "Effect of Vacuum Annealing on High-k Dy_2O_3 Thin Films Deposited on Si(100)", SSDM 2003, pp.510-511, September 2003, Tokyo, Japan
- [212] **Plenary Invited Talk:** H.Iwai, "CMOS Downscaling", IUMRS-ICAM 2003, pp.110, October 8-13, 2003, Yokohama, Japan
- [213] I.Ueda, S.Ohmi and H.Iwai, "Electrical Characteristics of High-K Stack Gate Dielectric Thin

- Films with La_2O_3 as Buffer Layer” 204th ECS Meeting Orlando, Abs.545, October12-16, 2003, Florida, U.S.A.
- [214] H.Sauddin, Y.Yoshihara, S.Ohmi, K.Tsutsui and H.Iwai, “Low-Frequency Noise Characteristics of MISFET’s with La_2O_3 Gate Dielectrics” 204th ECS Meeting Orlando, Abs.546, October12-16, 2003, Florida, U.S.A.
- [215] A.Kuriyama, S.Ohmi, K.Tsutsui and H.Iwai, “Effect of Post Metallization Annealing for La_2O_3 Gate Thin Films on Electrical Characteristics” 204th ECS Meeting Orlando, Abs.564, October12-16, 2003, Florida, U.S.A.
- [216] Y.Kim, S.Ohmi, K.Tsutsui and H.Iwai, “Electrical Characteristics of High-k La_2O_3 Thin Film Deposited by E-Beam Evaporation Method”, 204th ECS Meeting Orlando, Abs.582, October12-16, 2003, Florida, U.S.A.
- [217] S.Ohmi, I.Ueda, Y.Kobayashi, K.Tsutsui and H.Iwai, “Electrical Characteristics of rare-earth oxides stacked-layer structures”, IWGI 2003 Tokyo, pp.28-31, November6-7,2003, Tokyo, Japan
- [218] **Invited Talk:** H.Iwai “CMOS Scaling toward sub-10nm regime” EDMO2003, pp.30-34, November 17-18,2003, Orlando, Florida, U.S.A.
- [219] **Plenary Invited Talk:** H.Iwai “Scaling of Advanced CMOS”, IWPSD2003, pp.13-18, December 2003, Chennai, India
- [220] **Plenary Invited Talk:** H.Iwai “CMOS Scaling Challenge to sub-10 nm”, CODEC-04, January 1-3,2004, Kolkata, India
- [221] **Plenary Invited Talk:** H.Iwai “CMOS Scaling for sub-90 nm to sub-10 nm”, VLSI2004, pp.30-35, January 5-9, 2004, Mumbai, India
- [222] K.Tsutsui, R.Higaki, Y.Sasaki, T.Sato, H.Tamura, B.Mizuno and H.Iwai, “Contribution and Control of Neutral Gas Absorption Effects in the Plasma Doping of Boron into Si”, IWJT-2004 pp.46-49, March 15-16,2004, Shanghai, China
- [223] C.G.Jin, Y.Sasaki, K.Tsutsui, H.Tamura, B.Mizuno, R.Higaki, T.Satoh, K.Majima, H.Sauddin, K.Takagi, S.Ohmi and H.Iwai, “Estimation of Ultra-Shallow Plasma Doping (PD) Layer’s Optical Absorption Properties by Spectroscopic Ellipsometry (SE)” IWJT-2004 pp.102-103 March 15-16,2004, Shanghai, China
- [224] K.Tsutsui, Y.Sasaki, C.G.Jin, H.Tamura, B.Mizuno, R.Higaki, T.Sato, K.Majima, S.Ohmi, H.Iwai, “Ultra Shallow p +/n Junctions Fabricated by Plasma Doping and All Solid State Laser Annealing” Proceedings of the International Symposium, 205th Meeting of The Electrochemical Society, Proceeding Volume 2004-01, pp.106-111, May 2004, San Antonio, U.S.A
- [225] **Plenary Talk:** H.Iwai “FUTURE CMOS SCALING” Proceeding of the 11th International Conference, Mixed Design of integrated circuits and systems, pp.19-23, MIXEDS 2004, June 24-26, 2004, Szczecin, Poland
- [226] Y.Sasaki, C.G.Jin, H.Tamura, B.Mizuno, R.Higaki, T.Satoh, K.Majima, H.Sauddin, K.Takagi, S.Ohmi, K.Tsutsui, H.Iwai, “B₂H₆ Plasma Doping with “In-situ He Pre-amorphization” 2004 Symposium on VLSI Technology Digest of Technical Papers, pp.180-181, June 15-17, 2004, Honolulu, U.S.A.
- [227] **Invited Talk:** H.Iwai “RF CMOS Technology” 2004 Asia-Pacific Radio Science Conference Proceedings, pp.296-298, August 24-27,2004, Qingdao, China
- [228] **Invited Talk:** H. Iwai “Future of CMOS Technology” 2004 Semiconductor Manufacturing Technology workshop Proceedings, pp.5-8, Sep.9-10, 2004, Taiwan, ROC
- [229] Y.Kim, S. Ohmi, K.Tsutsui, H.Iwai, “Space-Charge-Limited Current Conductions in La_2O_3 Thin Films Deposited by E-Beam Evaporation after Low Temperature Dry-Nitrogen Annealing” ESSDERC 2004, Proceeding of the 34th European Solid-State Device Research Conference, 21-23 September 2004, pp.81-84, 2004, Leuven, Belgium
- [230] T. Sato, R. Higaki, H. Tamura, Y. Sasaki, B. Mizuno, K. Tsutsui, H. Iwai “Effects of Wet Cleaning Treatment on Dose of Impurity after Plasma Doping” ESSDERC 2004, Proceeding of the 34th European Solid-State Device Research Conference, 21-23 September 2004, pp.149-152, 2004
- [231] J.Ng, S.Ohmi, K.Tsutsui, H.Iwai “A Study of Aluminum Gate La_2O_3 nMISFET with Post Metallization Anneal” Dielectrics for Nanosystems: Materials Science, Processing, Reliability,

- and Manufacturing, 206th Meeting of The Electrochemical Society, Proceedings Volume 2004-04, pp.369-380, Hawaii, October 2004, Leuven, Belgium
- [232] Y. Kim, S. Ohmi, K. Tsutsui, H. Iwai, "Electrical Conduction Processes in Lanthana Thin Films prepared by E-Beam Evaporation" Dielectrics for Nanosystems: Materials Science, Processing, Reliability, and Manufacturing, 206th Meeting of The Electrochemical Society, Proceedings Volume 2004-04, pp.452-463, October 2004, Hawaii, U.S.A.
- [233] B. Mizuno, Y. Sasaki, C. Jin, H. Tamura, K. Okashita, H. Ito, K. Tsutsui, H. Iwai, "Plasma Doping" 7th International Conference on Solid-State and Integrated Circuits Technology, Proceedings October 18-21, 2004, ICSICT 2004, Volume I pp.423-427, Beijing, China
- [234] K. Tsutsui, R. Higaki, T. Sato, Y. Sasaki, H. Tamura, B. Mizuno, H. Iwai, "Effects of Surface Conditions on Dose Controllability of Plasma Doping Process" 7th International Conference on Solid-State and Integrated Circuits Technology, Proceedings October 18-21, 2004, ICSICT 2004, Volume I pp.439-444, Beijing, China,
- [235] **Invited Talk:** H. Iwai, "CMOS Technology Future" ICCDCS pp.179-182, 3-5 November 2004, Punta Cana, Dominican Republic
- [236] C.G. Jin, Y. Sasaki, K. Okashita, H. Tamura, H. Ito, B. Mizuno, K. Tsutsui, S. Ohmi, H. Iwai, "Ultra Shallow p+/n Junction Formation by Plasma Doping (PD) and All Solid-State Laser Annealing (ASLA) with Selective Absorption Modulation" the 15th International Conference on Ion Implantation Technology, IIT2004, October 25-29, 2004, Taipei, Taiwan, ROC
- [237] Y. Sasaki, C.G. Jin, K. Okashita, H. Tamura, H. Ito, B. Mizuno, R. Higaki, T. Satoh, K. Majima, H. Sauidin, K. Takagi, S. Ohmi, K. Tsutsui, H. Iwai, "New Method of Plasma Doping with In-Situ Helium Pre-Amorphization" the 15th International Conference on Ion Implantation Technology, IIT2004, October 25-29, 2004, Taipei, Taiwan, ROC
- [238] **Plenary Talk:** Hiroshi Iwai "Future Semiconductor Manufacturing – Challenges and Opportunities" 2004 IEEE International Electron Devices Meeting, December 13-15, 2004, pp.11-16, San Francisco Hilton and Towers, San Francisco, U.S.A.
- [239] Hiroshi Iwai "Future of Si integrated devices and its manufacturing" WOFE 2004 Advanced Workshop on Frontiers Electronics, J. E. Irausquin Blvd 77 Palm Beach, December 18-22, pp.72, 2004, Aruba
- [240] Kunihiro Miyauchi, Kenichiro Nakagawa, Kazuo Tsutsui, Hiroshi Iwai "La2O3/Y2O3 Stack High-K Gate Insulator Technique" WOFE 2004 Advanced Workshop on Frontiers Electronics, J. E. Irausquin Blvd 77 Palm Beach, December 18-22, 2004, pp.14, Aruba,
- [241] H. Iwai "New Technology Study for Future Downscaling CMOS: High-k and Plasma Doping" 6th Workshop and IEEE EDS Mini-colloquia on Nanometer CMOS Technology, National Chiao Tung University, January 21-22, 2005, pp.1-1, Taiwan, ROC
- [242] **Invited Talk:** H. Iwai, "Challenges for the CMOS roadmap and nanotechnology beyond CMOS" Workshop on Semiconductors and Micro & Nano-Technology SEMANTEC 2005, pp.1-4, March 4, 2005, Campinas, Brazil
- [243] Y. Kobayashi, R. Xiang, K. Tsutsumi, H. Iwai "Formation of heat resistant Ni silicide by additional Hf layers." Materials for Advanced Metallization (MAM2005), March 6-9, 2005, Dresden, Germany,
- [244] I. Aiba, Y. Sasaki, K. Okashita, H. Tamura, Y. Fukagawa, K. Tsutsui, H. Ito, K. Kakushima, B. Mizuno, H. Iwai "Feasibility Study of Plasma Doping on Si Substrates with Photo-Resist Patterns" International Workshop on Junction Technology (IWJT), pp.71-72, June 7-8, 2005, Osaka, Japan
- [245] K. Tsutsui, K. Majima, Y. Fukagawa, Y. Sasaki, K. Okashita, H. Tamura, K. Kakushima, H. Ito, B. Mizuno, H. Iwai "Analysis of Conductivity in Ultra-shallow p+ Layers Formed by Plasma Doping" International Workshop on Junction Technology (IWJT), pp.73-74, June 7-8, 2005, Osaka, Japan
- [246] H. Sauidin, H. Tamura, K. Okashita, Y. Sasaki, H. Ito, B. Mizuno, K. Kakushima, K. Tsutsui, H. Iwai "Reverse Current of Plasma Doped p+/n Ultra-Shallow Junction" International Workshop on Junction Technology (IWJT), June 7-8, 2005, Osaka, Japan pp.75-76
- [247] **Tutorial:** H. Iwai "High-K Gate Stack Technology" ESSDERC 2005, Sept. 12-16, 2005, Grenoble, France

- [248] K. Nakagawa, K. Miyauchi, K. Kakushima, T. Hattori, K. Tsutsui, H. Iwai “ The Effect of Y_2O_3 Buffer Layer for La_2O_3 Gate Dielectric Film ” ESSDERC 2005, pp.387-389, Sept. 12-16, 2005, Grenoble, France
- [249] S. Yoshizaki, Woei Yuan Chong, M. Nakagawa, Y. Nara, M. Yasuhira, F. Ohtsuka, T. Arikado, K. Nakamura, K. Kakushima, K. Tsutsui, H. Aoki, H. Iwai “ RF Modeling of Sub 100 nm CMOS ” ESSDERC 2005, Sept. 12-16, 2005, Grenoble, France
- [250] **Keynote Address:** H. Iwai “ Silicon Integrated Circuit Technology and MANUFACTURING Innovations for the Past and the Next 30 Years ” 22nd International VLSI Multilevel Interconnection Conference,, pp.25-27, Oct. 4-6, 2005, Fremont, U.S.A
- [251] E.Miranda J.Molina, Y.Kim, H.Iwai “Degradation of High-K La_2O_3 gate Dielectrics using Progressive Electrical Stress” the 16th European Symposium on Reliability of Electron Devices, October 12, 2005, Bordeaux, France
- [252] H. Iwai “CMOS Scaling and its Future towards Downsizing Limit ” IEEE EDS WIMNACT-9,2005, Oct. 25, 2005, Yokohama, Japan,
- [253] **Invited Talk:** H. Iwai “Future of CMOS Scaling and Its Manufacturing” IWPSD-2005, pp.55-66, Dec.13-17, 2005, New Delhi, India
- [254] **Distinguished Lecture:** H.Iwai, “Future of CMOS and Its Manufacturing” IEEE LEOS Chapter& EDS Chapter, Jan.3, 2006, Kolkata, India
- [255] **Invited Talk:** H. Iwai “Future CMOS Technology and Manufacturing” EPMDs-2006, vol.1-1, Jan.4-6, 2006, Kolkata, India
- [256] H. Iwai, “Recent Status an Nano CMOS and Future Direction” IWNC2006, pp.1-5, Jan. 30-31, 2006, Mishima, Japan
- [257] K. Tsutsui, Y. Sasaki, K. Majima, Y. Futagawa, I. Aiba, R. Higaki, C. Jin, H. Ito, B. Mizuno, J.A.Ng, K. Tachi, J. Song, Y. Shiino, K. Kakushima, P. Ahmet, H. Iwai, “Ultra-shallow Junction and High-k dielectric for Nano CMOS” IWNC2006, pp.56-68, Jan. 30-31, 2006, Mishima, Japan
- [258] H. Wong, K. Kakushima, H. Iwai, “Material and Interface Instabilities of High-k MOS Gate Dielectric Films” IWNC2006, pp.169-174, Jan. 30-31, 2006, Mishima, Japan
- [259] Manoj C. R., A. Mangal, V. R. Rao, K. Tsutsui, H. Iwai, “Parasitics Effects in Multi Gate MOSFETs” IWNC2006, pp.255-260, Jan. 30-31, 2006, Mishima, Japan
- [260] I. Aiba, Cheng - Guo Jinm, Y. Sasaki, K. Tsutsui, H. Tamura, K. Okashita, H. Kakushima, H. Iwai “Photo Resist Removal Process UUsing Wet Treatment After Plasma Doping” ISTC-2006, Mar. 21-22, 2006, Shanghai, China, vol.1 pp.295-296
- [261] K. Tsutsui, Y. Sasaki, Cheng - Guo Jin, H. Tamura, K. Okashita, H. Ito, B. Mizuno, H. Sauddin, K. Majima, T. Satoh, Y. Fukagawa, K. Kakushima, H. Iwai “Formation of Ultra-shallow Junctions by Plasma Doping” ISTC-2006, vol. 1 pp.232-241, Mar. 21-22, 2006, Shanghai, China
- [262] A. Fukuyama, K. Kakuashima, P. Ahmet, A.N.Chandorkar, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “ Analysis of Voltage Coefficient and Leakage Current of La_2O_3 Mim Capacitor” ISTC-2006, vol.1 pp.225-231, Mar. 21-22, 2006, Shanghai, China
- [263] Ruifei Xiang, K. Nagahiro, T. Shiozawa, P. Ahmet, K. Tsusui, Y. Okuno, M. Matsumoto, M. Kubota, K. Kakushima, H. Iwai “Irregular Increase in Sheet Resistance of Ni Silicides at Transition Temperature Range from NiSi to NiSi₂ Depending on Annealing Time” ISTC-2006, Mar. 21-22, 2006, Shanghai, China
- [264] P. Ahmet, T. Nagata, D. A. Kukuruznyak, K. Ohmori, K. Kakushima, K. Tsutsui, T.Chikyow, H.Iwai “Combinatorial Fabrication and Phase Diagramming of Ternary Composition Spreads” ISTC-2006, vol.1 pp.215-224, Mar. 21-22, 2006, Shanghai, China
- [265] **Invited Talk:** H.Iwai “CMOS Scaling and Future Manufacturing” 2006-IWNE, pp.3-47, Apr.21, 2006, Tainan, Taiwan
- [266] **Keynote Speech:** H.Iwai “Semiconductor Manufacturing Technology in the 21st Century” 2006VLSI-TSA, pp.1-17, Apr.24-26, 2006, Hsinchu, Taiwan
- [267] K. Shiraiishi, T.Nakayama, Y.Akasaka, S.Miyazaki, T.Nakaoka, K.Ohmori, P.Ahmet, K.Torii, H.Watanabe, T.Chikyow, Y.Nara, H.Iwai, K.Yamada “New Theory of Effective Work Functions at Metal/High-k Dielectric Interfaces-Application to Metal/High-k HfO_2 And La_2O_3

- Dielectric Interfaces—" 2006ECS, vol. 2 pp.25-40, May 7-12, 2006, Denver, U.S.A
- [268] P.Ahmet, T.Nagata, D.A.Kukuruznyak, K.Ohmori, K.Kakushima, K.Tsutsui, T.Chikyow and H.Iwai "Combinatorial Fabrication and Characterization of Oxide and Metal Thin Film Composition Spreads" 2006ECS, vol. 2 pp.79-90, May 7-12, 2006, Denver, U.S.A
- [269] K.Kakushima, P.Ahmet, N.Sugii, K.Tsutsui, T.Hattori and H.Iwai "Lanthanum Oxides for Gate Insulator Application" 2006ECS, vol.2 pp.115-127, May 7-12, 2006, Denver, U.S.A
- [270] T.Hattori, K.Kakushima, K.Nakajima, H.Nohira, K.Kimura and H.Iwai "Angle-Resolved Photoelectron Spectroscopy Study on Gate Insulators" 2006ECS, vol. 2 pp.275-286, May 7-12, 2006, Denver, U.S.A
- [271] J.A.Ng, N.Sugii, K.Kakushima, P.Ahmet, T.Hattori, K.Tsutsui and H.Iwai "Mobility Degradation Analysis for La_2O_3 nMOSFET" 2006ECS, vol. 2 pp.329-338, May 7-12, 2006, Denver, U.S.A
- [272] K.Tsutusi, R.Xiang, K.Nagahiro, T.Shiozawa, P.Ahmet, Y.Okuno, M.Matsumoto, M.Kubota, K.Kakushima and H.Iwai "Irregular Increase in sheet Resistance of Ni Sicicides at Temperature Range of Transition from NiSi to NiSi_2 " IWJT-2006, pp.188-191, May 15-16, 2006, Shanghai, China
- [273] **Invited Talk:** H. Iwai, " La_2O_3 Gate Oxide Technology for MOSFETs" The-E-MRS 2006 Spring Meeting, May 29, 2006, Nice, France
- [274] J.Song, A.Fukuyama, K.Kakushima, P.Ahmet, K.Tsutsui, T.Hattori and H.Iwai "Characteristics of $\text{La}_2\text{O}_3/\text{Ge}$ MIS Capacitors on Annealing Condition" The-E-MRS 2006 Spring Meeting, vol. 1-1, May 29, 2006, Nice, France,
- [275] **Distinguished Lecture:** H.Iwai, "Future CMOS Scaling and Its Manufacturing" AdCom & ExCom Meeting Mini-Colloquia, June 1, 2006, Napoli, Italy
- [276] K.Kakushima, P.Ahmet, J.A.Ng, J.Molina, H.Saoudin, Y.Kuroki, K.Nakagawa, A.Fukuyama, K.Tachi, Y.Shiino, J.Song, K.Tsutsui, N.Sugii, T.Hattori and H.Iwai "Study of La_2O_3 Gate Dielectric Suitability for Future MIM and MOSFETs" 2006 IEEE Si Nanoelectronics Workshop, pp.113, June 12, 2006, Honolulu Hawaii
- [277] **Poster Presentation:** H.Iwai, "Future of nano CMOS and its manufacturing" FTM, pp.47, June 27, 2006, Heraklion, Crete
- [278] **Distinguished Lecture:** H.Iwai, "High Dielectric Constant Gate Insulator Technology" WIMNACT Mini-Colloquium, July 4, 2006, Singapore
- [279] **Keynote Speech:** H.Iwai, "Future of Nano-CMOS Technology and Its Production" IPFA2006, pp.1-17, July 5, 2006, Singapore
- [280] E.Miranda and H.Iwai "Modeling of the Leakage Current in Ultrathin La_2O_3 Films Using a Generalized Power Law Equation" IPFA2006, pp.306-310, July 7, 2006, Singapore
- [281] **Distinguished Lecture:** H.Iwai, "Nano-CMOS and Its Manufacturing", EDS Tsinghua Student Chapter Opening Ceremony, Jul. 10 2006, Beijing, China
- [282] **Invited Talk:** H. Iwai, "Historical Trends and Future Perspectives of Silicon Technology Scaling" SINANO Summer School 2006, Bologna, Italy
- [283] A.Kuriyama, O. Faynot, L. Brevard, A. Tozzo, L.Clerc, J.Mitard, V. Vidal, S. Deleonibus, S.Cristoloveanu and H. Iwai "Precise Extraction of Metal Gate Work Function from Bevel Structures" Solid State Devices and Materials Yokohama 2006, pp.210-211, September 13-15, 2006, Japan
- [284] K. Ohmori, P.Ahmet, K. Shiraishi, K. Yamabe, H. Watanabe, Y. Akasaka, N. Umezawa, K. Nakajima, M.Yoshitake, T. Nakayama, K.-S. Chang, K. Kakushima, Y. Nara, M.L. Green, H.Iwai, K. Yamada, T. Chikyow "Wide Controllability of Flatband Voltage in La_2O_3 Gate Structures-Remarkable Advantages of La_2O_3 over HfO_2 " Solid State Devices and Materials Yokohama 2006, pp.432-433, September 13-15, 2006, Japan
- [285] **Keynote Talk:** H. Iwai, "Academia-Industry collaborations in Japan in the field of Nanoelectronics" ENIAC-MEDEA+ Workshop, ESSDERC/ESSCIRC 2006, September 22, 2006, Montreux, Switzerland
- [286] **Invited Talk:** H. Iwai, "CMOS for next 15 years as the mainstream of nano device technology: problems, solutions and beyond that", SINANO Workshop, ESSDERC/ESSCIRC 2006, September 22, 2006, Montreux, Switzerland

- [287] M. Nakagawa, J. Song, Y. Nara, M. Yasuhira, F. Ohtsuka, T. Akikado, K. Nakamura, K. Kakushima, P. Ahmet, K. Tsutsui, and H. Iwai, "High Frequency Model of Sub-100nm High-k RF CMOS" Satellite workshop to ESSDERC/ESSCIRC 2006, September 22, 2006, Montreux, Switzerland
- [288] A. Kuriyama, O. Faynot, L. Brevard, A. Tozzo, L. Clerc, S. Deleonibus, J. Mitard, V. Vidal, S. Cristoloveanu and H. Iwai "Work Function Investigation in Advanced Metal Gate-HfO₂-SiO₂ Systems with Bevel Structures" ESSDERC 2006, pp.109-112, September 19, 2006, Montreux, Switzerland
- [289] K. Tsutsui, Y. Sasaki, C-G. Jin, H. Sauddin, K. Majima, Y. Fukagawa, I. Aiba, H. Ito, B. Mizuno, K. Kakushima, P. Ahmet, H. Iwai "Ultra-Shallow Junction Formation By Plasma Doping And Flash Lamp Annealing" RTP-2006, Oct.11, 2006, Kyoto, Japan
- [290] A.N. Chandorkar, Ch. Ragunandan, P. Agashe, D. Sharma, H. Iwai "Impact of Process variations on Leakage Power in CMOS Circuits in Nano Era" ICSICT-2006, Vo.2 pp.1248-1251, Oct.23-26, 2006, Shanghai, China
- [291] K. Shiraishi, H. Takeuchi, Y. Akasaka, T. Nakayama, S. Miyazaki, T. Nakaoka, A. Ohta, H. Watanabe, N. Umezawa, K. Ohmori, P. Ahmet, K. Toii, T. Chikyow, Y. Nara, T-J. King Liu, H. Iwai, and K. Yamada "Physics of Interfaces between gate electrodes and high-k dielectrics" ICSICT-2006, pp.384-387, Oct.23-26, 2006, Shanghai, China
- [292] P. Ahmet, K. Kakushima, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "La-based oxides for High-k Gate Dielectric Application" ICSICT-2006, pp.408-411, Oct.23-26, Shanghai, China
- [293] K. Nagahiro, K. Tsutsui, T. Shiozawa, R. Xiang, P. Ahmet, K. Kakushima, Y. Okuno, M. Matsumoto, M. Kubota, H. Iwai "Thermal Stability of NiSi Controlled by Post Silicidation Metal Doping Method" ICSICT-2006, pp.466-469, Oct.23-26, 2006, Shanghai, China
- [294] H. Sauddin, Y. Sasaki, H. Ito, B. Mizuno, P. Ahmet, K. Kakushima, N. Sugii, K. Tsutsui, and H. Iwai "Leakage Current Characteristics of Ultra-Shallow Junctions Formed by B₂H₆ Plasma Doping" ECS 210th Meeting, Vol.3 No.2 pp.57-65, Oct 29 – Nov.3, 2006, Cancun, Mexico
- [295] H. Nohira, T. Matsuda, K. Tachi, Y. Shiino, J. Song, Y. Kuroki, Ng Jin Aun, P. Ahmet, K. Kakushima, K. Tsutsui, E. Ikenaga, K. Kobayashi, H. Iwai, T. Hattori "Effect of Deposition Temperature on Chemical Structure of Lanthanum Oxide/Si Interface Structure" ECS 210th Meeting, Vol.3 No.2 pp.169-173, Oct 29 – Nov.3, 2006, Cancun, Mexico
- [296] T. Nakayama, K. Shiraishi, S. Miyazaki, Y. Akasaka, T. Nakaoka, K. Torii, A. Ohta, P. Ahmet, K. Ohmori, N. Umezawa, H. Watanabe, T. Chikyow, Y. Nara, H. Iwai, K. Yamada "Physics of Metal/High-k Interfaces" ECS 210th Meeting, Vol.3 No.3 pp.129-140, Oct 29 – Nov.3, 2006, Cancun, Mexico
- [297] K. Ohmori, P. Ahmet, K. Shiraishi, K. Yamabe, H. Watanabe, Y. Akasaka, N. Umezawa, K. Nakajima, M. Yoshitake, T. Nakayama, K.-S. Chang, K. Kakushima, Y. Nara, M. L. Green, H. Iwai, K. Yamada, T. Chikyow "Wide Controllability of Flatband Voltage in La₂O₃ Gate Stack Structures – Remarkable Advantages of La₂O₃ over HfO₂." ECS 210th Meeting, Vol.3 No.3 pp.351-363, Oct 29 – Nov.3, 2006, Cancun, Mexico
- [298] K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Effect of Oxygen for Ultra-Thin La₂O₃ Film Deposition" ECS 210th Meeting, Vol.3 No.3 pp.425-434, Oct 29 – Nov.3, 2006, Cancun, Mexico
- [299] Y. Shiino, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "La₂O₃ Gate Dielectric Thin Film with Sc₂O₃ Buffer Layer for High Temperature Annealing" ECS 210th Meeting, Oct 29 – Nov.3, Vol.3 No.3 pp.511-519, 2006, Cancun, Mexico
- [300] **Invited Talk:** Hiroshi Iwai, Hei Wong "Nano-CMOS Technology for Next Fifteen Years", The IEEE TENCON Nanoscale CMOS Technology, pp.9, Nov.14-17, 2006, Hong Kong
- [301] **Distinguished Lecture:** H. Iwai "Miniaturization of Semiconductor Devices for Integrated Circuits" University of Chile, UTFSM., University of Bio Bio, Nov. 20-24, 2006, Chile
- [302] **Invited Plenary Talk:** Hiroshi Iwai, "Nano CMOS Manufacturing", The Conference on Optoelectronic and Microelectronic Materials and Devices, Dec.6-8 2006, Perth, Western Australia
- [303] **Invited Plenary Talk:** Hiroshi Iwai, "Nano CMOS Manufacturing", The International Conference on Computers and Devices for Communication (CODEC)2006, pp.5, Dec.18-20

- 2006, Kolkata, India
- [304] **Keynote Speech:** Hiroshi Iwai, "Nano CMOS Technology and Manufacturing", The 4th International Conference on Electrical & Computer Engineering, pp.20, Dec. 19-21 2006, Dhaka, Bangladesh
- [305] **Distinguished Lecture:** H. Iwai "Electron Devices for Human Society" Inaugural Ceremony of IEEE Electron Devices Society Bangladesh Chapter, Dec 19, 2006, Dhaka, Bangladesh
- [306] **Distinguished Lecture:** Hiroshi Iwai, "Miniaturization of Semiconductor Devices for Integrated Circuits" IEEE EDS Mini-Colloquium on Microelectronics & VLSI, pp.5-8, Jan. 3 2007, Bhubaneswar, India
- [307] **Distinguished Lecture:** Hiroshi Iwai, "Past and future of Si integrated circuit technology" Jan. 9, 11 2007, Kashgar Pedagogical Institute, Kashgar & Hotan Pedagogical College, Hotan, China
- [308] **Distinguished Lecture:** Hiroshi Iwai, "Past and future of Si integrated circuit technology" Jan.11 2007, Hotan Pedagogical College, Hotan, China
- [309] **Distinguished Lecture:** Hiroshi Iwai, "Past and future of Si integrated circuit technology" Jan.16 2007, Xinjian University, Urumuqi, China
- [310] **Distinguished Lecture:** Hiroshi Iwai, "Nano-CMOS Technology and Its Beyond" Feb. 5, 2007, National Chiao Tung University, Taiwan
- [311] **Distinguished Lecture:** Hiroshi Iwai, "Nano-CMOS and High-k/metal Gate Technology" Feb.6, 2007, UMC, Taiwan
- [312] **Invited Talk:** Hiroshi Iwai, "Future of Silicon Integrated Circuit Technology" The 2007 Nano and Giga Challenges Conference, pp.97, Mar. 14 2007, Phoenix, U.S.A.
- [313] T. Shiozawa, K. Nagahiro, K. Tsutsui, P. Ahmet, K. Kakushima, and H. Iwai, "Improvement of Thermal Stability of Ni Silicide by Al Interlayer Deposition", The ECS ISTC 2007, Mar. 20, 2007, pp.43-47, Shanghai, China
- [314] Y. Kobayashi, K. Tsutsui, K. Kakushima, V. Hariharan, V. R. Rao, P. Ahmet, H. Iwai "Parasitic Effects Depending on Shape of Spacer Region on FinFETs" ECS 211th Meeting, Vol.6 No.4 pp.83-87, May 8, 2007, Chicago, U.S.A.
- [315] **Distinguished Lecture:** H. Iwai, "Future of Nano CMOS Technology", WIMNACT/MQ 1 & IEDST, June 4, 2007, Tsinghua University, Beijing, China
- [316] J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Improvement of interfacial properties with interfacial layer in $\text{La}_2\text{O}_3/\text{Ge}$ Structure", INFOS2007, Microelectronic Engineering, pp.2336-2339, June 20-23 2007, Glyfada Athens Greece
- [317] S. Sato, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, and H. Iwai "Thermal-Stability Improvement of LaON Thin Film Formed Using Nitrogen Radicals", INFOS2007, Microelectronic Engineering, pp.1894-1897, June 20-23 2007, Glyfada Athens Greece
- [318] T. Kawanago, K. Tachi, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, "Electrical Characterization of Directly Deposited La-Sc Oxides Complex for Gate Insulator Application", INFOS2007, Microelectronic Engineering, pp.2235-2238, June 20-23 2007, Glyfada Athens Greece
- [319] **Invited Talk:** Hiroshi Iwai, "Future of Silicon Integrated Circuit Technology", Second International Conference on Industrial and Information systems, 8-11 Aug. 2007, University of Paradeniya, Sri Lanka
- [320] H. Iwai "Past and Future of Silicon Integrated Circuit Technology", School of Physics, 7 Sep. 2007, Xinjiang University, Xinjiang, China
- [321] Koichi Okamoto, Manabu Adachi, Kuniyuki Kakushima, Parhat Ahmet, Nobuyuki Sugii, Kazuo Tsutsui, Takeo Hattori, Hiroshi Iwai "Effective Control of Flat-band Voltage in HfO_2 Gate Dielectric with La_2O_3 Incorporation" ESSDERC 2007, 11-13 September 2007, Munich, Germany
- [322] Y.C.Ong, D.S.Ang, S.J.O'Shea, K.L.Pey, T.Kawanago, K.Kakushima, H.Iwai "Characterization of the $\text{Sc}_2\text{O}_3/\text{La}_2\text{O}_3$ High-k Gate Stack by STM" SSDM TSUKUBA 2007, 19-21 September 2007, Tsukuba, Japan
- [323] **Keynote Speech:** H. Iwai "Gate stack technology for next 25 years", 4th International

- Symposium on Advanced Gate Stack Technology, 26 September 2007, Dallas, Texas, USA
- [324] K. Tsutsui, K. Nagahiro, T. Shiozawa, P. Ahmet, K. Kakushima, H. Iwai "Improvement of Thermal Stability of Ni Silicide by Additive Metals with Specific Introduction Processes" ECS 212th Meeting, Vol.11 No.6 pp.207-213, Oct. 7– Oct.12, 2007, Washington, USA
- [325] K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Improvement of Interface of W/La₂O₃/Si MOS Structure Using Al Capping Layer" ECS 212th Meeting, Vol.11 No.4 pp.191-198, Oct. 7– Oct.12, 2007, Washington, USA
- [326] M. Adachi, K. Okamoto, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Control of Flat Band Voltage by Partial Incorporation of La₂O₃ or Sc₂O₃ into MfO₂ in Metal/MfO₂/SiO₂/Si MOS Capacitors" ECS 212th Meeting, Vol.11 No.4 pp.157-167, Oct. 7– Oct.12, 2007, Washington, USA
- [327] **Distinguished Lecture:** H. Iwai, "Future Gate Stack Technology" Mini-Colloquium at IBM East Fishkill, Dec. 7, 2007, New York, USA
- [328] **Distinguished Lecture:** H. Iwai, "High-k/Metal Gate Technology" Indian Institute of Technology, Bombay, Jan. 9, 2008, Bombay, India
- [329] **Golden Jubilee Distinguished Lecture:** H. Iwai, "Past and Future Half-Centuries for Semiconductor Device Development" Indian Institute of Technology, Bombay, Jan. 11, 2008, Bombay, India
- [330] H. Iwai, "Advanced Logic Technologies with New Materials and Structures" Indian Institute of Science, Jan. 18, 2008, Bangalore, India
- [331] **Distinguished Lecture:** H. Iwai, "Past and Future for Micro-and Nano-Electronics Focusing on Si Integrated Circuits Technology" Narula Institute of Technology, Feb. 29, 2008, Kolkata, India
- [332] H. Iwai, "Past and future for micro-and nano-electronics, focusing on Si integrated circuits technology" Workshop and IEEE EDS Mini-colloquia on Nanometer CMOS Technology (WIMNACT), Mar. 6-7, 2008, Sikkim, India
- [333] K. Tsutsui, T. Shiozawa, K. Nagahiro, Y. Ohishi, K. Kakushima, P. Ahmet, N. Urushihara, M. Suzuki, and H. Iwai, "Improvement of Thermal Stability of Ni Silicide on N+-Si by Direct Deposition of Group III Element (Al, B) Thin Film at Ni/Si Interface", MAM2008, pp.63-64, Mar.2-5, Dresden, Germany
- [334] Y. Ohishi, K. Noguchi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai "Schottky Barrier Height Modulation of Ni Silicide/Si Contacts by Insertion of Thin Er or Pt Layers" The ECS ISTC 2008, pp.459-462, Mar. 16, 2008, Shanghai, China
- [335] Y. Morozumi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, K. Natori, H. Iwai "Properties of Ballistic current in MOSFETs studied by RT model" The ECS ISTC 2008, pp.129-132, Mar. 16, 2008, Shanghai, China
- [336] **Keynote Speech:** H. Iwai "CMOS Technology after Reaching the Scale Limit" IWJT-2008, pp.1-2, May 15-16, 2008, Shanghai, China
- [337] K. Tsutsui, M. Watanabe, Y. Nakagawa, K. Sasaki, T. Kai, Cheng-Guo Jin, Y. Sasaki, K. Kakushima, P. Ahmet, B. Mizuno, T. Hattori, H. Iwai "Profiling of Carrier Properties for Shallow Junctions Using a New Sub-nanometer Step-by-step Etching Technique" IWJT-2008, pp.58-61, May 15-16, 2008, Shanghai, China
- [338] K. Kakushima, K. Okamoto, K. Tachi, S. Sato, T. Kawanago, J. Song, P. Ahmet, N. Sugii, K. Tsutsui, T. Hattori, H. Iwai "Impact of Thin La₂O₃ Insertion for MfO₂ MOSFET" ECS 213th Meeting, May 19, 2008, Phoenix, USA
- [339] K. Tsutsui, T. Shinozawa, K. Nagahiro, Y. Ohishi, K. Kakushima, P. Ahmet, N. Urushihara, N. Suzuki, H. Iwai "Effects of B Al Interface Layers on Thermal Stability of Ni Silicide on Si" ECS 213th Meeting, May 21, 2008, Phoenix, USA
- [340] K. Tsutsui, T. Shinozawa, K. Nagahiro, Y. Ohishi, K. Kakushima, P. Ahmet, N. Urushihara, N. Suzuki, H. Iwai "Effects of B Al Interface Layers on Thermal Stability of Ni Silicide on Si" ECS 213th Meeting, May 21, 2008, Phoenix, USA
- [341] **Distinguished Lecture:** H. Iwai, "Past and future for micro-and nano-electronics, focusing on Si integrated circuits technology" IEEE EDS Committee, AdCom & ExCom Meeting Mini-Colloquium, Jun. 2, 2008, National Technical University at Athens, Greece

- [342] **Distinguished Lecture:** H.Iwai, “Past and future for micro- and nano-electronics, focusing on Si integrated circuits technology” Mini-Colloquia, Sabanci University, Jun. 4, 2008, Istanbul, Republic of Turkey
- [343] **Distinguished Lecture:** H.Iwai, “Future of Nano-CMOS after Scaling Limit” Mini-Colloquia, Pontificia Universidad Javeriana, Mini-Colloquium, Sept. 8, 2008, Bogota, Colombia
- [344] Y. Kobayashi, K. Tsutsui, K. Kakushima, P. Ahmet, V. R. Rao and H. Iwai “ Analysis of Threshold Voltage Variations of FinFETs : Separation of Short Channel Effects and Space Charge Effects” Int. Conf. on Solid State Devices and Materials (SSDM2008), Sept., 2008, Tsukuba, Japan
- [345] K. Kakushima, K. Okamoto, K. Tachi, S. Sato, J. Song, T. Kawanago, P. Ahmet, N. Sugii, K. Tsutsui, T. Hattori, H. Iwai “Interfacial Dipole Measurement of Dielectric/Silicon Interface by X-ray Photoelectron Spectroscopy” PRIME 2008: Joint International Meeting, Oct.14, 2008, Honolulu, Hawaii, USA
- [346] H. Nohira, Y. Takenaga, K. Kakushima, P. Ahmet, K. Tsutsui, H. Iwai “Annealing-temperature Dependence of Compositional Depth Profile and Chemical Structures of LaOx/ScOx/Si and ScOx/LaOx/Si Interfacial Transition Layer” PRIME 2008: Joint International Meeting, vol.16 No.5 pp.171-176, Oct.14, 2008, Honolulu, Hawaii, USA
- [347] K. Okamoto, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, A. N. Chandorkar, T. Hattori, H. Iwai “0.5 nm EOT MOS structure with TaSi_x/W stacked gate electrode” PRIME 2008: Joint International Meeting, vol.16 No.5 pp.203-212, Oct.14, 2008, Honolulu, Hawaii, USA
- [348] K. Noguchi, W. Hosoda, K. Matano, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, A. N. Chandorkar, T. Hattori, H. Iwai “ Schottky Barrier Height Modulation by Er Insertion and Its Application to SB-MOSFETs” PRIME 2008: Joint International Meeting, Oct.14, 2008, Honolulu, Hawaii, USA
- [349] Y. Lee, T. Nagata, K. Kakushima, K. Shiraishi, H. Iwai “Electronic Structure Analysis of Silicon Nanowires for High Conductivity in n- and p-channel Nanowire-FET” PRIME 2008: Joint International Meeting, Oct.14, 2008, Honolulu, Hawaii, USA
- [350] Y. Kobayashi, A. Sachid, K. Tsutsui, K. Kakushima, P. Ahmet, V. Rao, H. Iwai “Analysis of Threshold Voltage Variations of FinFETs Relating to Short Channel Effects” PRIME 2008: Joint International Meeting, Oct.14, 2008, Honolulu, Hawaii, USA
- [351] M. Kouda, K. Tachi, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, A. Chandorkar, T. Hattori, H. Iwai “Electric Properties of CeOX /La2O3 Stack as Gate Dielectric in Advanced MOSFET Technology”, PRIME 2008: Joint International Meeting, vol.16 No.5 pp.153-160, Oct.14, 2008, Honolulu, Hawaii, USA
- [352] J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai “Effect of Ultrathin Si Passivation Layer for Ge MOS Structure with La2O3 Gate Dielectric”, PRIME 2008: Joint International Meeting, vol.16 No.5 pp.285-293, Oct.14, 2008, Honolulu, Hawaii, USA
- [353] M. Hino, K. Nagata, T. Yoshida, D. Kosemura, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, A. Ogura, T. Hattori, H. Iwai “Study on Stress Memorization by Argon Implantation and Annealing” PRIME 2008: Joint International Meeting, vol.16 No.10 pp.117-124, Oct.14, 2008, Honolulu, Hawaii, USA
- [354] K. Kakushima, K. Tachi, M. Adachi, K. Okamoto, S. Sato, T. Kawanago, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Advantage of La₂O₃ Gate Dielectric over HfO₂ for Direct Contact and Mobility Improvement” ESSDERC 2008, pp. 126-129, Oct. 15-19, 2008, Scotland, UK
- [355] K. Tsutsui, M. Watanabe, Y. Nakagawa, T. Matsuda, T. Yoshida, E. Ikenaga, K. Kakushima, P. Ahmet, H. Nohira, T. Maruzumi, A. Ogura, T. Hattori, H. Iwai, “New Analysis of Heavily Doped Boron and Arsenic in Shallow Junctions by X-ray Photoelectron Spectroscopy” ESSDERC 2008, pp. 142-145, Oct. 15-19, 2008, Scotland, UK
- [356] P. Ahmet, T. Shiozawa, K. Nagahiro, K. Kakushima, K. Tsutsui, T. Chikyow, H. Iwai “Ni silicidation on Heavily Doped Si Substrates” ICSICT2008, Vol.2 pp.1304-1307, Oct. 20 – Oct. 23, 2008, Beijing, China
- [357] H. Iwai, “Past and future for micro- and nano-electronics, focusing on Si integrated circuits

- technology” Changchun University of Science and Technology, Mini-Colloquium, Oct. 24, 2008, Changchun, China
- [358] H. Iwai, “Technology Scaling and Roadmap for 22nm CMOS logic and beyond” Dalian University of Technology, Mini-Colloquium, Oct. 27, 2008, Dalian, China
- [359] H. Iwai, “Future of Nano-CMOS after Scaling Limit” Shenyang University of Technology, Mini-Colloquium, Oct. 28, 2008, Shenyang, China
- [360] **Invited Talk:** H. Iwai, “Introduction of new materials into Si-integrated Circuits” C-MRS, Nov. 23, 2008, South China University of Technology, Guangzhou, China
- [361] H. Iwai, “Past and Future of Si integrated Circuit Technology” Xiangtan University, Nov. 24, 2008, Xiangtan, China
- [362] H. Iwai, “Introduction of new materials into Si integrated circuits” Hunan University, Nov. 27, 2008, Changsha, China
- [363] H. Iwai, “Past and future of Si integrated circuit technologies” Nanjing University, Nov. 28, 2008, Nanjing, China
- [364] H. Iwai, “Technology Scaling and Roadmap” 2008 IEDM Short Course : 22nm CMOS Technology, Dec. 14, 2008, San Francisco, USA
- [365] H. Iwai, “Downsizing of transistors towards its Limit” NIT Calicut, Jan. 5, 2009, Calicut, India
- [366] **Distinguished Lecture:** H. Iwai, “Roadmap for 22nm Logic CMOS and Beyond” IIT Bombay, Jan. 21, 2009, Bombay, India
- [367] **Distinguished Lecture:** H. Iwai, “Roadmap for 22nm Logic CMOS and Beyond” Bengal Engineering Science University, Mar. 5, 2009, Bengal, India
- [368] **Distinguished Lecture:** H. Iwai, “Downsizing of transistors towards its Limit” Bengal Institute of Technology & Management, Mar. 6, 2009, Bengal, India
- [369] **Distinguished Lecture:** H. Iwai, “Roadmap for 22nm Logic CMOS and Beyond” Heritage Institute of Technology, Mar. 9, 2009, Heritage, India
- [370] **Distinguished Lecture:** H. Iwai, “Technology Scaling and Roadmap for 22nm and beyond”, Kyungpook National University, Mini-Colloquium, Mar. 13, 2009, Daegu, Korea
- [371] H. Fujisawa, A. Srivastava, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori¹, C. K. Sarkar, H. Iwai, “Electrical Characterization of W/HfO₂ MOSFETs with La₂O₃ Incorporation”, ISTC /CSTIC2009, pp.53, Mar. 19, 2009, Shanghai, China
- [372] H. Kamimura, H. Arai, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai, “Evaluation of Lateral Ni Diffusion in Si Nanowire Schottky Contact”, ISTC /CSTIC2009, pp.58, Mar. 19, 2009, Shanghai, China
- [373] **Distinguished Lecture:** H. Iwai, “Technology Scaling and Roadmap for 22nm CMOS and beyond” University College of Dublin, EDS Mini-Colloquium on Advanced Electron Devices modeling and Technology, May 1, 2009, Dublin, Ireland
- [374] **Distinguished Lecture:** H. Iwai, “Past and Future of Integrated Circuits Technology” University of Manchester, May 5, 2009, Manchester, UK
- [375] **Invited Talk:** H. Iwai, “Technology Roadmap for 22nm CMOS and Beyond”, IEEE/2nd IEEE International Workshop On Electron Devices And Semiconductor Technology, June 1, 2009, Indian Institute of Technology Bombay, Mumbai, India
- [376] H. Iwai, “Past and Future of Integrated Circuits Technology”, International Conference on Frontiers of Physics (ICFP 2009), pp.60, June 2-5, 2009, Kathmandu, Nepal
- [377] K. Tachi, T. Ernst, C. Dupre, A. Hubert, S. Becu, H. Iwai, S. Cristoloveanu, O. Faynot “Transport Optimization with Width Dependence of 3D-stacked GAA Silicon Nanowire FET with High-k/Metal Gate Stack”, 2009 Silicon Nanoelectronics Workshop, June 13, 2009, Kyoto, Japan
- [378] **Poster Presentation:** H. Iwai, “Nono-CMOS Technology after Reaching Its Scaling Limit” Future Trends in Microelectronics (FTM-2009) Workshop, June 16, Sardinia, Italy
- [379] **Poster Presentation:** P. Ahmet, T. Nagata, K. Kakushima, K. Tsutsui, T. Chikyow, H. Iwai, “On the thermal stability of nickel silicides” Future Trends in Microelectronics (FTM-2009) Workshop, June 16, Sardinia, Italy
- [380] M. Kouda, N. Umezawa, K. Kakushima, P. Ahmet, K. Shiraishi, T. Chikyow, K. Yamada, H. Iwai, “Charged defects reduction in gate insulator with multivalent materials”, 2009 Symposium on

- VLSI Technology Digest of Technical Papers, pp.200-201, June 17, 2009, Kyoto, Japan
- [381] **Plenary Invited Talk:** H.Iwai “Roadmap for 22nm and beyond, INFOS2009, June 29, 2009, Clare College, Cambridge, UK
- [382] J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Post metallization annealing study in $\text{La}_2\text{O}_3/\text{Ge}$ MOS structure” INFOS2009, Microelectronic Engineering, vol. 86, pp.1638-1641, June 28-July 1, 2009, Cambridge University, UK
- [383] T. Kawanago, J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Experimental Study for High Effective Mobility with directly deposited $\text{HfO}_2/\text{La}_2\text{O}_3$ MOSFET” INFOS2009, Microelectronic Engineering, vol. 86, pp.1629-1631, June 28-July 1, 2009, Cambridge University, UK
- [384] H.Iwai, “Si Nanowire experiment”, G-COE Workshop on Nanoelectronics, July 3, 2009, University of Cambridge, UK
- [385] K.Kakushima, H.Iwai, “High-k Experiment below 0.5-nm EOT”, G-COE Workshop on Nanoelectronics, July 3, 2009, Cambridge University, UK
- [386] **Keynote Speech:** H.Iwai “Logic LSI Technology Roadmap for 22nm and Beyond” IPFA2009, July 8, Suzhou, China
- [387] H.Iwai, “Future nanoelectronic device technologies –high-k, nanowire and alternative channel-”, NSC-JST Nano Device Workshop, July 23, 2009, National Nano Device Laboratories, Hsinchu, Taiwan
- [388] S. Sato, H. Kamimura, H. Arai, K. Kakushima, P. Ahmet, K. Ohmori, K. Yamada, H. Iwai “High-Performance Si Nanowire FET with a Semi Gate-Around Structure Suitable for Integration”, ESSDERC 2009, 39th European Solid-State Device Research Conference, pp.249-252, September 14-18, 2009, Athens, Greece.
- [389] K. Kakushima, K. Okamoto, T. Koyanagi, K. Tachi, M. Kouda, T. Kawanago, J. Song, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori, H. Iwai “Selection of Rare Earth Silicate with SrO Capping for EOT Scaling below 0.5 nm”, ESSDERC 2009, 39th European Solid-State Device Research Conference, pp.403-406, September 14-18, 2009, Athens, Greece.
- [390] H.Iwai, “Roadmap for Nano-CMOS”, ECS 216th Meeting, Vol.25 No.7 pp.67-76, Oct.7, 2009, Vienna, Austria
- [391] K.Kakushima, P.Ahmet, H. Iwai “Overwhelming the 0.5 nm EOT Level for CMOS Gate Dielectric”, ECS 216th Meeting, Vol.25 No.7 pp.171-75, Oct. 4– Oct.9, 2009, Vienna, Austria
- [392] M.Mamatrishat, M.Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, K. Natori, T. Hattori, H. Iwai “Analysis of Remote Coulomb Scattering Limited Mobility in MOSFETs with $\text{CeO}_2/\text{La}_2\text{O}_3$ Gate Stacks”, ECS 216th Meeting, Vol.25 No.7 pp.253-257, Oct. 4– Oct.9, 2009, Vienna, Austria
- [393] H.Arai, H.Kamimura, S.Sato, K.Kakushima, P. Ahmet, K.Tsutsui, N.Sugii, K.Natori, T.Hattori, H.Iwai “Annealing Reaction for Ni Silicidation of Si Nanowire”, ECS 216th Meeting, Vol.25 No.7 pp.447-454, Oct. 4– Oct.9, 2009, Vienna, Austria
- [394] T.Koyanagi, K.Okamoto, K.Kakushima, P.Ahmet, K.Tsutsui, A. Nishiyama, N.Sugii, K.Natori, T.Hattori, H.Iwai “Impact of Alkali Earth Elements Incorporation on Electrical Characteristics of La_2O_3 Gated MOS Device”, ECS 216th Meeting, Vol.25 No.6 pp.17-22, Oct. 4– Oct.9, 2009, Vienna, Austria
- [395] M.K.Bera, J.Song, K.Kakushima, P.Ahmet, K.Tsutsui, N.Sugii, T.Hattori, H.Iwai “Electrical Properties of Lanthanum-scandate Gate Dielectric Directly Deposited on Ge”, ECS 216th Meeting, Vol.25 No.6 pp.67-77, Oct. 4– Oct.9, 2009, Vienna, Austria
- [396] K.Funamizu, Y.C.Lin, K.Kakushima, P.Ahmet, K.Tsutsui, N.Sugii, E.Y.Chang, T.Hattori, H.Iwai “Electrical Characteristics of HfO_2 and La_2O_3 Gate Dielectrics for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Structure” ECS 216th Meeting, Vol.25 No.6 pp.265-270, Oct. 4– Oct.9, 2009, Vienna, Austria
- [397] H.Nohira, Y.Kon, K.Kitamura, M.Kouda, K.Kakushima, H.Iwai “Annealing-temperature Dependence of Compositional Depth Profiles and Chemical Bonding States of $\text{CeO}_x/\text{LaO}_x/\text{Si}$ and $\text{LaO}_x/\text{CeO}_x/\text{Si}$ Structure”, ECS 216th Meeting, Vol.25 No.6 pp.321-326, Oct. 4– Oct.9, 2009, Vienna, Austria
- [398] H.Nakayama, K.Kakushima, P.Ahmet, E.Ikenaga, K.Tsutsui, N.Sugii, T.Hattori, H.Iwai “Crystallographic Orientation Dependent Electrical Characteristics of La_2O_3 MOS Capacitors”,

- ECS 216th Meeting, Vol.25 No.6 pp.339-345, Oct. 4– Oct.9, 2009, Vienna, Austria
- [399] Y. Lee, K. Kakushima, K. Shiraishi, K. Natori, and H. Iwai, “Systematic Study on Size Dependences of Transport Parameters for Ballistic Nanowire-FET with Effective Mass Approximation”, 2009 International Conference on Solid State Devices and Materials, E-7-5, October 2009, Sendai Kokusai hotel, Miyagi, Japan
- [400] H. Iwai “Miniaturization and future prospects of Si devices”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [401] **Poster Presentation:** M. K. Bera, J. Song, P. Ahmet, K. Kakushima, K. Tsutsui, A. Nishiyama, N. Sugii, T. Hattori, H. Iwai: “Rare-earth based mixed oxide as high-k gate dielectrics for Ge MOSFET”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [402] **Poster Presentation:** J. Song, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai: “Effect of Ultrathin Si Passivation Layer for $\text{La}_2\text{O}_3/\text{Ge}$ MOS structure”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [403] **Poster Presentation:** T. Kawanago, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai: “Experimental Investigation of V_{FB} shift and Effective Mobility in La_2O_3 MOS Devices”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [404] **Poster Presentation:** Soshi Sato, Hideaki Arai, Kuniyuki Kakushima, Parhat Ahmet and Hiroshi Iwai: “Evaluation of Channel Potential Profile of Si Nanowire Field Effect Transistor”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [405] **Poster Presentation:** M. Mamatrishat, M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, K. Natori, T. Hattori, H. Iwai: “Study on Remote Coulomb Scattering Limited Mobility in MOSFETs with $\text{CeO}_2/\text{La}_2\text{O}_3$ Gate Stacks”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [406] **Poster Presentation:** A. Abudukelimu, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai: “Current-Voltage Characteristics of Ballistic Nanowire MOSFET by Numerical Analysis”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [407] **Poster Presentation:** M. Kouda, N. Umezawa, K. Kakushima, H. Nohira, P. Ahmet, K. Shiraishi, T. Chikyow, K. Yamada, H. Iwai: “Charged defects reduction in gate insulator with multivalent materials”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [408] **Poster Presentation:** Yeonghun Lee, Kuniyuki Kakushima, Kenji Shiraishi, Kenji Natori and Hiroshi Iwai: “Size-Dependent Transport Characteristics of Ballistic Silicon Nanowire FETs”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [409] **Poster Presentation:** H. Nakayama, K. Kakushima, P. Ahmet, E. Ikenaga, K. Tsutsui, N. Sugii, T. Hattori and H. Iwai: “Crystallographic Orientation Dependent Electrical Characteristics of La_2O_3 MOS Capacitors”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [410] **Poster Presentation:** H. Arai, H. Kamimura, S. Sato, K. Kakushima, P. Ahmet, A. Nishiyama, K. Tsutsui, N. Sugii, K. Natori, T. Hattori and H. Iwai: “Annealing Reaction for Ni Silicidation of Si Nanowire”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [411] **Poster Presentation:** K. Funamizu, T. Kanda, Y.C. Lin, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, E.Y. Chang, K. Natori, T. Hattori and H. Iwai: “Electrical Characteristics of HfO_2 and La_2O_3 Gate Dielectrics for $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ MOS Structure”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [412] **Poster Presentation:** W. Hosoda, K. Ozawa, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama,

- N.Sugii, K.Natori, T.Hattori, and H.Iwai: “A Study of Schottky Barrier Height Modulation of NiSi by Interlayer Insertion and Its Application to SOI SB-MOSFETs”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [413] **Poster Presentation:** K. Matano, K. Kakushima, P. Ahmet, N. Sugii, K. Tsutsui, T. Hattori, and H. Iwai: “Threshold Voltage Control in p-MOSFET with High-k Gate dielectric”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [414] **Poster Presentation:** T. Koyanagi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai: “Influence of Alkali Earth Elements Capping on Electrical Characteristics of La₂O₃ Gated MOS Device”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [415] **Poster Presentation:** Y. Kobayashi, K. Kakushima, P. Ahmet, V. Ramgopal Rao, K. Tsutsui and H. Iwai: “Short-channel effects on FinFETs induced by inappropriate fin widths”, G-COE PICE International Symposium on Silicon Nano Devices, October 13-14, 2009, Tokyo Institute of Technology, Japan
- [416] **Distinguished Lecture:** H. Iwai “Recent Our Activities in Si FET Research” IIT Madras, November 3, 2009, Chennai, India
- [417] **Keynote Speech:** H. Iwai “Past and future of Micro/Nano-electronics”, IEEE EDS & SKP Workshop 2009, November 4, 2009, SKP Engineering College, Tiruvannamalai, India
- [418] **Distinguished Lecture:** H. Iwai “Past and future of Micro/Nano-electronics” IEEE EDS Mini Colloquia, November 9, 2009, Government Engineering College, Port Blair, India
- [419] K. Tachi, M. Casse, D. Jang, C. Dupre, A. Hubert, N. Vulliet, C. Maffini-Alvaro, C. Vizioz, C. Carabasse, V. Delaye, J.M.Hartmann, G. Ghibaudo, H. Iwai, S. Cristoloveanu, O. Faynot, and Ernst “Relationship between mobility and high-k interface properties in advanced Si and SiGe nanowires”, IEDM 2009, December 8, 2009, Baltimore, USA
- [420] **Plenary Invited Talk:** H. Iwai “Si MOSFET Roadmap for 22nm and beyond”, CODEC 2009, December 14, 2009, Hyatt Regency, Kolkata, India
- [421] H. Iwai “Past and Future of Silicon Electronic Devices”, National Symposium on “Science and Technology and the Young (Career, Creativity and Excitement)” Organized by National Academy of Science, December 15, 2009, Calcutta University, Kolkata, India
- [422] H. Iwai “Si MOSFET Roadmap for 22nm and beyond”, December 16, 2009, Jadavpur University, Kolkata, India
- [423] **Distinguished Lecture:** H. Iwai “Future nanoelectronic device technologies - high-k, nanowire and alternative channel”, IEEE AP & ED Joint MQ, January 13, 2010, IIT Bombay, Bombay, India
- [424] K. Matano, K. Funamizu, M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai “Electrical Characteristics of Rare Earth (La, Ce, Pr and Tm) Oxides/Silicates Gate Dielectric”, China Semiconductor Technology International Conference, pp.1129-1134, March 18-19, 2010, Shanghai, China
- [425] W. Hosoda, K. Ozawa, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai “Fabrication of SB-MOSFETs on SOI Substrate Using Ni Silicide Containing Er Interlayer” China Semiconductor Technology International Conference, pp.1105-1110, March 18-19, 2010, Shanghai, China
- [426] A. Abudukelimu, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai “Performance of Silicon Ballistic Nanowire MOSFET with Diverse Orientations and Diameters” China Semiconductor Technology International Conference, pp.1111-1116, March 18-19, 2010, Shanghai, China
- [427] H. Iwai, “Si Nanoelectronic Device Technology”, March 10, 2010, University of Science and Technology of China, Hefei, China
- [428] H. Iwai, “Past and Future of Integrated Circuits Technology”, March 15, 2010, Jiangxi University of Finance and Economics, Nanchang, China

- [429]H Iwai, "Past and Future of Integrated Circuits Technolog", March 16, 2010, East China Jiaotong University, Nanchang, China
- [430]**Distinguished Lecture:**H. Iwai, "Beyond the definition of classical devices & communication technology", IEEE EDS DL Siliguri Institute of Technology, March 29, 2010, Siliguri Institute of Technology, Siliguri, India
- [431]**Distinguished Lecture:**H. Iwai, "Si Nanoelectronic Device Technology", IEEE EDS WIMNACT 23, April 2, 2010, IIT Guwahati, Guwahati, India
- [432]**Distinguished Lecture:**H. Iwai, "Si Nanoelectronic Device Technology", IEEE EDS WIMNACT 23, April 5, 2010, North-Eastern Hill University, Shillong, India
- [433]**Distinguished Lecture:**H. Iwai, "Si Nanoelectronic Device Technology", IEEE EDS WIMNACT 23, April 8, 2010, NIT Silchar, Silchar, India
- [434]**Distinguished Lecture:**H. Iwai, "Nanoelectronic Device Technology", IEEE EDS WIMNACT 23, April 9, 2010, Heritage Institute of Technology, Kolkata, India
- [435]P. Ahmet, K. Kakushima, H. Iwai, "Towards the Ultimate Scaling of MOSFET Gate Dielectrics - Direct Contact of High-k and Silicon-", ECS 217th, Vancouver, April 26, 2010, Canada
- [436]P. Ahmet, W. Hosoda, K. Noguchi, Y. Ohishi, K. Kakushima, K. Tsutsui, H. Iwai, "Er Inserted Ni Silicide Metal Source/Drain for Schottky MOSFETs", IEEE IWJT 2010 Extended Abstracts 2010 International Workshop on Junction Technology, pp.62-64, May 11, 2010, Shanghai, China
- [437]A. Uedono, K. Tsutsui, S. Ishibashi, H. Watanabe, S. Kubota, K. Tenjinbayashi, Y. Nakagawa, B. Mizuno, T. Hattori, H. Iwai, "Vacancy-Type Defects in Ultra-Shallow Junctions Fabricated Using Plasma Doping Studied by Positron Annihilation", IEEE IWJT 2010 Extended Abstracts 2010 International Workshop on Junction Technology, pp.149-154, May 11, 2010, Shanghai, China
- [438]K. Tsutsui, N. Hoshino, Y. Nakagawa, M. Tanaka, H. Nohira, K. Kakushima, P. Ahmet, Y. Sasaki, B. Mizuno, T. Hattori, H. Iwai, "Depth Profiling of Chemical Bonding States of Impurity Atoms and Their Correlation with Electrical Activity in Si Shallow Junctions", IEEE IWJT 2010 Extended Abstracts 2010 International Workshop on Junction Technology, pp.174-177, May 11, 2010, Shanghai, China
- [439]**Poster Presentation:**K. Tsutsui, Y. Kobayashi, K. Kakushima, P. Ahmet, V. R. Rao, H. Iwai, "Analysis of Threshold Voltage Variation in Double-gate MOSFETs(FinFETs), International Symposium on technology Evolution for Silicon Nano-Electronics(ISTESNE), pp.53, June 4, 2010, Tokyo Institute of Technology, Tokyo, Japan
- [440]**Distinguished Lecture:**H. Iwai, "Past and future of Si integrated circuit device technologies", IEEE EDS Mini Colloquium, June 7, 2010, Institute for Microelectronics Stuttgart(IMS-CHIPS), Stuttgart, Germany

- [441] K. Kakushima, T. Koyanagi, D. Kitayama, M. Kouda, J. Song, T. Kawanago, M. Mamatrishat, K. Tachi, M. K. Bera, P. Ahmet, H. Nohira, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, K. Yamada, H. Iwai, "Direct Contact of High-k/Si Gate Stack for EOT below 0.7 nm using LaCe-silicate Layer with V_{fb} controllability", 2010 Symposium on VLSI Technology, pp.69-70, June 15, 2010, Honolulu, USA
- [442] **Keynote Speech:** H. Iwai, "Future perspective for the mainstream CMOS technology and their contribution to green technologies", 2010 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices, July 1, 2010, Tokyo Institute of Technology, Japan
- [443] H. Iwai, "Nanoelectronic Device Technology – Future perspective for the mainstream CMOS technology-", July 15, 2010, Xinjiang University, Xinjiang, China
- [444] **Invited Talk:** H. Iwai, "Si Nanowire Device and its Modeling", International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), September 6, 2010, Bologna, Italy
- [445] T. Kawanago, Y. Lee, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, "Optimized Oxygen Annealing Process for V_{th} Tuning of p-MOSFET with High-k/Metal Gate Stacks", ESSDERC 2010, 40th European Solid-State Device Research Conference, September 15, 2010, Seville, Spain
- [446] S. Sato, Y. Lee, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, H. Iwai, "Gate Semi-Around Si Nanowire FET Fabricated by Conventional CMOS Process with Very High Drivability", ESSDERC 2010, 40th European Solid-State Device Research Conference, September 16, 2010, Seville, Spain
- [447] K. Tachi, N. Vulliet, S. Barraud, B. Guillaumot, V. Maffini-Alvaro, C. Vizios, C. Arvet, Y. Campidelli, P. Gautier, J.M. Hartmann, T. Skotnicki, S. Cristoloveanu, H. Iwai, O. Faynot, T. Ernst, "3D Source/Drain Doping Optimization in Multi-Channel MOSFET", ESSDERC 2010, 40th European Solid-State Device Research Conference, September 16, 2010, Seville, Spain
- [448] H. Iwai, "Future Silicon Nanoelectronic Technology", Shandong University, September 21, 2010, Jinan, China
- [449] **Invited Talk:** H. Iwai, "High-k Gate Stack Technology Beyond 0.5 nm EOT", 11th IUMRS International Conference in Asia, September 28, 2010, Qingdao, China
- [450] T. Koyanagi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, "Impact of Alkali-Earth-Elements Incorporation on V_{fb} Roll-Off Characteristics of La_2O_3 Gated MOS Device", ECS 218th Meeting, October 11, 2010, Las Vegas, USA
- [451] M. Bera, P. Ahmet, K. Kakushima, K. Tsutsui, N. Sugii, A. Nishiyama, T. Hattori, H. Iwai, "Electrical Properties of Yttrium-Titanium Oxide High-k Gate Dielectric on Ge", ECS 218th

Meeting, October 11, 2010, Las Vegas, USA

- [452] M. Mamatrishat, M. Kouda, T. Kawanago, K. Kakushima, P. Ahmet, A. Aierken, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, H. Iwai, "Effect of Remote-Surface –Roughness Scattering on Electron Mobility in MOSFETs with High-k Dielectrics", ECS 218th Meeting, October 11, 2010, Las Vegas, USA
- [453] N. Shigemori, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, "Suppression of Lateral Encroachment of Ni Silicide into Si Nanowires using Nitrogen Incorporation", ECS 218th Meeting, October 11, 2010, Las Vegas, USA
- [454] D. Kitayama, T. Koyamagi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, "TiN Capping Effect on High Temperature Annealed RE-Oxide MOS Capacitors for Scaled EOT", ECS 218th Meeting, October 11, 2010, Las Vegas, USA
- [455] Y. Wu, N. Shigemori, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, A. Nishiyama, K. Natori, T. Hattori, H. Iwai, "Observation of Tunneling FET operation in MOSFET with NiSi/Si Schottky source/channel interface", ECS 218th Meeting, October 11, 2010, Las Vegas, USA
- [456] H. Iwai, "Past and Future of Micro/Nano CMOS Devices", ICSICT(International Conference on Solid-State and Integrated Circuit Technology)2010 EDS-Mini Colloquia & Tutorials, November 1, 2010, Shanghai, China
- [457] K. Tsutsui, M. Tanaka, N. Hoshino, H. Nohira, K. Kakushima, P. Ahmet, Y. Sasaki, B. Mizuno, T. Muro, T. Kinoshita, T. Hattori, H. Iwai, "Soft X-ray Photoelectron Spectroscopy Study of Activation and Deactivation of Impurities in Shallow Junctions", ICSICT(International Conference on Solid-State and Integrated Circuit Technology)2010, November 3, 2010, Shanghai, China
- [458] A. Abudukelimu, K. Kakushima, P. Ahmet, M. Geni, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, "The Effect of Isotropic and Anisotropic Scattering in Drain Region of Ballistic Channel Diode", ICSICT(International Conference on Solid-State and Integrated Circuit Technology)2010, November 3, 2010, Shanghai, China
- [459] P. Ahmet, D. Kitayama, T. Kaneda, T. Suzuki, T. Koyanagi, M. Kouda, M. Mamatrishat, T. Kawanago, K. Kakushima, H. Iwai, "Scaling of EOT Beyond 0.5nm", ICSICT(International Conference on Solid-State and Integrated Circuit Technology)2010, November 4, 2010, Shanghai, China
- [460] K. Ozawa, M. Kouda, Y. Urabe, T. Yasuda, K. Kakushima, P. Ahmet, H. Iwai, "La₂O₃ insulators prepared by ALD using La(iPrCp)₃ source: self-limiting growth conditions and electrical properties", ICSICT(International Conference on Solid-State and Integrated Circuit Technology)2010, November 4, 2010, Shanghai, China
- [461] H. Iwai, "Si Nanowire FET Modeling and Technology", Institute of Microelectronics Chinese

Academy of Sciencee, November 8, 2010, Beijing, China

- [462] K. Tachi, M. Casse, S. Barraud, C. Dupre, A. Hubert, N. Vulliet, M.E. Faivre, C. Vizioz, C. Carabasse, V. Delaye, J.M. Hartmann, H. Iwai, S. Cristoloveanu, O. Faynot, T. Ernst, “Experimental study on carrier transport limiting phenomena in 10 nm width nanowire CMOS transistors”, 2010 IEDM, December 8, 2010, San Francisco, USA
- [463] T. Nakayama, K. Kakushima, O. Nakatsuka, Y. Machida, S. Sotome, T. Matsuki, K. Ohmori, H. Iwai, S. Zaima, T. Chikyow, K. Shiraishi, K. Yamada, “Theory of Workfunction Control of Silicides by Doping for Future Si-Nano-Devices based on Fundamental Physics of Why Silicides Exist in Nature”, 2010 IEDM, December 8, 2010, San Francisco, USA
- [464] H. Iwai, “Past and Future of Micro/Nano-Electronics”, IEEE EDS MINI-COLLOQUIUM on “Nanoelectronics”, Gandhi Institute of Technology and Management, December 28, 2010, Bhubaneshwar, Orissa, India
- [465] H. Iwai, “Si Nanowire FET Modeling and Technology”, IEEE EDS MINI-COLLOQUIUM on “Nanoelectronics”, National Institute of Science and Technology, December 30, 2010, Berhampur, Orissa, India
- [466] H. Iwai, “Past and Future of Micro/Nano-Electronics”, Muthayammal Engineering, January 7, 2011, Rasipuram, Tamilnadu, India
- [467] M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Rare earth oxide capping effect on La₂O₃ gate dielectrics toward EOT of 0.5nm”, 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [468] **Poster Presentation:** M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Preparation and electrical characterization of CeO₂ films for gate dielectrics application: comparative study of CVD and ALD processes”, 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [469] **Poster Presentation:** Y. Lee, K. Kakushima, K. Natori, H. Iwai, “Cross-sectional distribution of phonon-limited electron mobility in rectangular silicon nanowire field effect transistors” 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [470] **Poster Presentation:** D. Hassanzadeh, T. Takashi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Effects of In_{0.53}Ga_{0.47}As Surface Preparation on MOS Device Electrical Characterization” 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [471] **Poster Presentation:** M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Preparation and electrical characterization of CeO₂ films for gate dielectrics application: comparative study of CVD and ALD processes”, 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [472] **Poster Presentation:** Y. Lee, K. Kakushima, K. Natori, H. Iwai, “Cross-sectional distribution of phonon-limited electron mobility in rectangular silicon nanowire field effect transistors” 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11), January 20, 2011, Tokyo, Japan
- [473] **Poster Presentation:** D. Hassanzadeh, T. Takashi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Effects of In_{0.53}Ga_{0.47}As Surface

- Preparation on MOS Device Electrical Characterization” 2011 International Workshop on Dielectric Thin Films for Future ULSI Devices: Science and Technology(IWDTF-11) , January 20, 2011, Tokyo, Japan
- [474]**Introductory Talk:** H. Iwai, “Future of Nano CMOS Technology” IEEE EDS Mini-colloquium on Nanometer CMOS Technology (WIMNACT 26), February 9, 2011, Tokyo, Japan
- [475]H. Iwai, K. Kakushima, E. Y. Chang, Yueh-Chin Lin, “III-V MOSFETs for Next Generation – Fabrication of III-V MOS Capacitors” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [476]**Poster Presentation:** H. Iwai, “High-K Gate Dielectronics for Future III-V FET” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [477]**Poster Presentation:** K. Tachi, K. Kakushima, H. Iwai, S. Cristoloveanu, T. Ernst, “Characterization of carrier transport in vertically-stacked Si nanowire FETs ”Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [478]**Poster Presentation:** S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, H. Iwai, “Influence of the cross-sectional shape for Si nanowire FETs” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [479]**Poster Presentation:** Y. Lee, K. Kakushima, K. Natori, H. Iwai, “Corner Effects on Phonon-Limited Mobility in Rectangular Si Nanowire MOSFETs ”Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [480]**Poster Presentation:** A. Abudukelimu, K. Kakushima, P. Ahmet, K. Natori, H. Iwai, “Influence of Phonon Generation of Hot Electrons in Drain Region on Ballistic Transport” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [481]**Poster Presentation:** N. Shigemori, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “An effective suppression process for Ni silicide encroachment into Si nanowire” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [482]**Poster Presentation:** M. Koyama, N. Shigemori, H. Arai, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Lateral encroachment of Ni silicide into silicon nanowire” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [483]**Poster Presentation:** K. Nakajima, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Interface State Density Measurement of Three Dimensional Silicon Structures by Charge Pumping Method” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [484]**Poster Presentation:** T. Kawanago, T. Suzuki, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “An effective process for oxygen defect suppression for La-based oxide gate dielectric” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [485]**Poster Presentation:** T. Koyanagi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Flatband Voltage Shift of La-based Gate Oxides with Alkali-earth-elements Incorporation” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [486]**Poster Presentation:** T. Kaneda, M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Effect of rare earth oxide capping for La-based gate oxides” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [487]**Poster Presentation:** M. Mamatrishat, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, H. Iwai, “Remote-surface-roughness scattering-limited electron, mobility in ultrathin high-k gate stacked MOSFETs” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan
- [488]**Poster Presentation:** D. Kitayama, T. Kubota, T. Koyanagi, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “Precise Control of Silicate Reaction with La₂O₃ Gate Dielectrics towards Equivalent Oxide Thickness of 0.5 nm ” Taiwan-Japan Workshop on “Nano Devices”, March 3, 2011, Tokyo, Japan

- [489] T. Kanda, D. Zade, Y. -C. Lin, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, E. Y. Chang, K. Natori, T. Hattori, and H. Iwai, “Annealing Effect on the Electrical Properties of $\text{La}_2\text{O}_3/\text{InGaAs}$ MOS Capacitors”, CSTIC2011, March 13, 2011, Shanghai, China
- [490] T. Kawanago, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai, “Metal Inserted Poly-Si Stacks with La_2O_3 Gate Dielectrics for Scaled EOT and V_{FB} Control by Oxygen Incorporation”, CSTIC2011, March 13, 2011, Shanghai, China
- [491] S. Sato, K. Kakushima, P. Ahmet, K. Ohmori, K. Natori, K. Yamada, H. Iwai, “Structural Effects of Channel Cross-section on a Gate Capacitance of Silicon Nanowire Field-Effect Transistors”, CSTIC2011, March 14, 2011, Shanghai, China
- [492] P. Ahmet, D. Kitayama, T. Kaneda, T. Suzuki, T. Koyanagi, M. Kouda, M. Mamatrishat T. Kawanago, K. Kakushima, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, H. Iwai, “ $\text{TiN}/\text{W}/\text{La}_2\text{O}_3/\text{Si}$ High-k Gate Stack for EOT below 0.5nm”, CSTIC2011, March 14, 2011, Shanghai, China
- [493] ***Distinguished Lecture***: H. Iwai, “Past and Future of Micro/Nano-Electronic Devices”, One day National Workshop on Electronic Devices, April 7, 2011, Mizoram University Aizawl, Mizoram, India
- [494] H. Iwai, “Past and Future of Micro/Nano-Electronic Devices”, ISDMISC 2011, April 12, 2011, Sikkim Manipal Institute of Technology, Sikkim, India

Distinguished Lecture

- [1] “CMOS Scaling and its Future towards Downsizing Limit,” IEEE EDS WIMNACT-9, 2005, Yokohama, Japan, Oct. 2005. pp. 55-66.
- [2] “Recent Status an Nano CMOS and Future Direction,” IWNC, Mishima, Japan, Jan. 2006, pp. 2-3.
- [3] “Future of CMOS and Its Manufacturing” IEEE LEOS Chapter & EDS Chapter, Jan.3, 2006, Kolkata, India
- [4] “Future CMOS Scaling and Its Manufacturing”, IEEE Mini-Colloquia, Jun. 1, 2006, Naples, Italy
- [5] “High Dielectric Constant Gate Insulator Technology”, WIMNACT IEEE Mini-Colloquia Singapore, Jul. 4 2006, Singapore
- [6] “Nano-CMOS and Its Manufacturing”, EDS Tsinghua Student Chapter Opening Ceremony, Jul. 10 2006, Beijing, China
- [7] “Miniaturization of Semiconductor Devices for Integrated Circuits” University of Chile, UTFSM., University of Bio Bio, Nov. 20-24, Chile
- [8] “Electron Devices for Human Society” Inaugural Ceremony of IEEE Electron Devices Society Bangladesh Chapter, Dec 19, 2006, Dhaka, Bangladesh
- [9] "Miniaturization of Semiconductor Devices for Integrated Circuit " Jan. 3 2007, Bhubaneswar, India
- [10] “Past and future of Si integrated circuit technology” Jan. 9, 11 2007, Kashgar Pedagogical Institute, Hotan, China
- [11] “Past and future of Si integrated circuit technology” Jan.11 2007, Hotan Pedagogical College, Hotan, China
- [12] “Past and future of Si integrated circuit technology” Jan.16 2007, Xinjian University, Urumuqi, China
- [13] "Nano-CMOS Technology and Its Beyond" Feb. 5, 2007, National Chiao Tung University, Taiwan
- [14] "Nano-CMOS and High-k/metal Gate Technology" Feb.6, 2007, UMC, Taiwan
- [15] "Future of Nano CMOS Technology”, WIMNACT/MQ 1 & IEDST, June 4, 2007, Tsinghua University, Beijing, China
- [16] “Future Gate Stack Technology” Mini-Colloquium at IBM East Fishkill, Dec. 7, 2007, New York, USA

- [17] “High-k/Metal Gate Technology” Indian Institute of Technology, Bombay , Jan. 9 , 2008, Bombay, India
- [18] Past and Future for Micro-and Nano-Electronics Focusing on Si Integrated Circuits Technology” Narula Institute of Technology , Feb. 29, 2008, Kolkata, India
- [19] “Roadmap for 22nm Logic CMOS and Beyond” IIT Bombay, Jan. 21, 2009, Bombay, India
- [20] “Roadmap for 22nm Logic CMOS and Beyond” Bengal Engineering Science University, Mar. 5 , 2009, Bengal, India
- [21] “Downsizing of transistors towards its Limit” Bengal Institute of Technology&Management, Mar. 6 , 2009, Bengal, India
- [22] “Roadmap for 22nm Logic CMOS and Beyond” Heritage Institute of Technology, Mar. 9 , 2009, Heritage, India
- [23] “Technology Scaling and Roadmap for 22nm CMOS and beyond” University College of Dublin, EDS Mini-Colloquium on Advanced Electron Devices modeling and Technology, May 1, 2009, Dublin, Ireland
- [24] “Past and Future of Integrated Circuits Technology” University of Manchester, May 5, 2009, Manchester, UK
- [25] “Recent Our Activities in Si FET Research” IIT Madras, November 3, 2009, Chennai, India
- [26] “Past and future of Micro/Nano-electronics” IEEE EDS Mini Colloquia, November 9, 2009, Government Engineering College, Port Blair, India
- [27] “Si MOSFET Roadmap for 22nm and beyond”, December 16, 2009, Jadavpur University, Kolkata, India
- [28] “Future nanoelectronic device technologies - high-k, nanowire and alternative channel”, January 13, 2010, IEEE AP & ED Joint MQ, IIT Bombay, Bombay, India
- [29] H. Iwai, "Beyond the definition of classical devices & communication technology", March 29, 2010, IEEE EDS DL Siliguri Institute of Technology, Siliguri Institute of Technology, Siliguri, India
- [30] H. Iwai, "Si Nanoelectronic Device Technology", April 2, 2010, IEEE EDS WIMNACT 23, IIT Guwahati, Guwahati, India
- [31] H. Iwai, "Si Nanoelectronic Device Technology", April 5, 2010, IEEE EDS WIMNACT 23, North-Eastern Hill University, Shillong, India
- [32] H. Iwai, "Si Nanoelectronic Device Technology", April 8, 2010, IEEE EDS WIMNACT 23, NIT Silchar, Silchar, India
- [33] H. Iwai, "Nanoelectronic Device Technology", April 9, 2010, IEEE EDS WIMNACT 23, Heritage Institute of Technology, Kolkata, India
- [34] H. Iwai, "Past and future of Si integrated circuit device technologies", June 7, 2010, IEEE EDS Mini Colloquium, Institute for Microelectronics Stuttgart(IMS-CHIPS), Stuttgart, Germany
- [35] H. Iwai, “Past and future trends of integrated Circuit Technology”, October 25, 2010, Nano Devices and Material Technology, Tribhuvan University, Pokhara, Nepal
- [36] H. Iwai, “Si Nanowire FET Modeling and Technology”, November 8, 2010, Peking University IEEE EDS DL Talk, Peking, China
- [37] H. Iwai, “Past and Future of Micro/Nano-Electronics”, IEEE EDS MINI-COLLOQUIUM on “Nanoelectronics”, Gandhi Institute of Technology and Management, December 28, 2010, Bhubaneswar, Orissa, India
- [38] H. Iwai, “Si Nanowire FET Modeling and Technology”, IEEE EDS MINI-COLLOQUIUM on “Nanoelectronics”, National Institute of Science and Technology, December 30, 2010, Berhampur, Orissa, India
- [39] H. Iwai, “Short Presentation and Discussion for Future of Micro/Nano-Electronics”, January 8, 2011, SKP Engineering College, India

- [40] H. Iwai, "Past and Future of Micro/Nano-Electronic Devices", April 9, 2011, IEEE EDS DL, North Eastern Regional Institute of Science and Technology Nirjuli, (Itanagar), Arunachal Pradesh, India
- [41] H. Iwai, "Past and Future of Micro/Nano-Electronic Devices", April 14, 2011, IEEE EDS DL Seminar, Nanocenter of Calcutta University, Calcutta, India
- [42] H. Iwai, "Past and Future of Micro/Nano-Electronic Devices", April 7, 2011, One day National Workshop on Electronic Devices, Mizoram University Aizawl, Mizoram, India

Seminar

- [1] H Iwai "Past and Future of Silicon Electronic Devices", Seminar, December 24, 2009, Xian Jiaotong University, Xian, China
- [2] H Iwai "Future nanoelectronic device technologies - high-k, nanowire and alternative channel", Seminar, December 24, 2009, Xian Jiaotong University, Xian, China
- [3] H Iwai "Past and Future of Silicon Electronic Devices", Seminar, December 29, 2009, Northwestern Polytechnical University, Xian, China

Books:

- [1] H. Iwai, "Hot carrier induced degradation mode in thin gate insulator dual gate MISFETs," Edited by W. Eccleston and M. Uren, "Insulating Films on Semiconductors 1991," Adam Hilger, Bristol, Philadelphia and New York, pp.83-92, 1991
- [2] Y.katsumata, T.Ohguro, K.Inoh, E.Morifuji, T.Yoshitomi, H.Kimijima, H.Nii, T.Morimoto, H.S.Momose, K.Yoshikawa, H.Ishiuchi and H.Iwai, "CMOS/BiCMOS Technology" in The VLSI Handbook, Chapter 2, edited by Prof. Wai-Kai Chen, Univ. of Illinois, Chicago, Illinois, 1999
- [3] Y.Unno, H.Iwai, "Future Trend in Large-Scale Integrated Circuit Technologies from an Industrial Perspective" edited by J.Xu et al. in "Future Trends in Microelectronics, The Road Ahead", published by John Wiley & Sons, Inc., pg.196, 1999
- [4] H. Iwai and S. Ohmi, "Trends and Projections for the Future of Scaling and Future Integration Trends", The Computer Engineering Handbook, pp1_1-1_29, February 2002
- [5] Hei Wong, Kenji Shiraishi, Kuniyuki Kakushima and Hiroshi Iwai, "High-K Gate Dielectrics" Electronic Device Architectures for the Nano-CMOS Era, pp.105-140, 2009

Panel Discussions:

- [1] **Panel Discussion:** H.Iwai, M.Hiratani, M.Takayanagi, H.Kitajima, H.Kang, T.Horikawa, K.Torii, Y.Tsunashima, J.Yugami, S.De Gendt, H.Niimi, M.Fischetti, and R.Chau, "Development Strategy of Gate Dielectrics: Ultra-thin Oxynitride versus High-k materials", IWGI 2003, pp.194, November6-7,2003, Tokyo,
- [2] **Evening Panel Discussion:** J.N.Burghartz, D.Harame, T.Stetzler, H.Iwai, M.Tiebout and V.Ilderem, "When Will CMOS Replace HBTs for RF?", p.593, SESSION25, IEDM2003, , December8-10,2003, Washington DC, USA,
- [3] **Evening Discussion Session ME2:** W.J. Dally, J. Emer, F. Fox, W-M. Hwu, H. Iwai, F. Pollack, and F. Weber, "Where will processor performance come from in the next ten years?" pp.118-119, Dig. Tech. ISSCC, 2000
- [4] **Panel Discussion:** K.Shimohigashi, K.Kyuma, H.Iwai, K.Asada, Innovation Japan2007

pp19,September12-14, Tokyo

- [5] **Panel Discussion:** H. Iwai, S. Oda, S. Sze, G. Bacarani, N. Sano, T. Kanayama, K. Natori, S. Deleonibus, T. Hiramoto, C. Claeys, S. Takagi, Y. Miyamoto, W. Milne, K. Banerjee, N. Koshida, K.Uchida, S. Sugano, K. Kimura, K. Yamada, K. Shiraishi, D-L.,Kwong, S. Sugawara, “Silicon nano-devices in 2030” , Global COE International Symposium, October 14, 2009, Tokyo

Short Course:

- [1] H. Iwai, “Source Drain and Wells,” Short Course A: Sub-100NM CMOS, IEDM Short Course, December, 1999
- [2] H. Iwai, “Advanced Device Technologies,” Key Technology Challenges for sub-70nm VLSI, Symp. on VLSI Tech., June, 2002
- [3] H. Iwai, “High-k Dielectrics,” Short Course 1) New process and device concepts, ESSDERC, September, 2005
- [4] H.Iwai,“Technology Scaling and Roadmap,” Short Course: 22nm CMOS Technology,IEDM 2008, December, 2008

Others:

- [1] H. Iwai “Transistor Level Modeling for Analog/RF IC Design” 2006 Springer
- [2] H. Iwai and W. Maszara, “Advanced materials and IC process technologies,” Proc. of the Ninth International Symposium on Silicon Material Science and Technology, Semiconductor Silicon 2002, pp. 325-327