Interface reaction and formation of La-silicate gate dielectrics on SiC substrates

Tokyo institute of technology
Department of electrical and electronic Engineering
Dissertation for degree of Master of Engineering

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ABSTRACT

As a wide band-gap semiconductor, Silicon Carbide (SiC) is a promising candidate for next generation power devices, the ability to grow silicon dioxide (SiO₂) by thermal oxidation is a unique advantage over other wide band-gap semiconductor material. However, the properties of thermal oxidation grown SiO₂ on SiC still suffer from a lot problems. One issue is that, the SiC MOSFET using SiO₂ gate dielectric facing low electron mobility problem, which should be attributed to the high interface state density near SiC/ SiO₂ interface. Recently a passivation of interface trap on SiC has been found by forming LaSiOₓ interface layer on SiC substrate. For further improvement of the gate dielectric, investigation of the reaction and formation of La-silicate is critical important.

In this research, the reaction and formation of La-silicate gate dielectrics on SiC substrates has been investigated using multiple physical analyses method. An enhanced oxidation of SiC substrate has been found by La₂O₃ capped annealing in 5%O₂ ambient through ATR-FITR. Ten times of oxidation rate has been obtained compared with dry thermal oxidation at the same temperature. However, oxidation variation has been found and agglomeration of La-silicate grain has been observed by TEM at the SiC/SiO₂ interface after La₂O₃ capped annealing.

To improve the interface properties, a SiN buffer layer has been used to prohibit the facet oxidation from SiC substrate. The reaction of SiN with La₂O₃ after annealing above 950°C in 5%O₂ ambient has been confirmed by ATR-FTIR. Although a rough surface of formed gate dielectric has been observed by TEM. A reduced surface roughness of gate dielectric has been achieved.
SiO$_2$ capped annealing is another solution for gate dielectric modification. A continuous layer of La-silicate has been obtain by SiO$_2$ capped annealing in O$_2$ ambient at 1000$^\circ$C. However, some La-silicate protrusion appear at the interface, which is considered to be attributed to the facet oxidation from SiC substrate. For SiC substrate after thermal treatment by SiO$_2$ capped annealing at 1050$^\circ$C. A uniform La-silicate layer has been obtained, which shows a huge suppression of oxidation variation. Lanthanum element existence at thermal growth layer at SiC/La-silicate interface has been detected by EELS analysis. A modification of gate dielectric interface layer may achieved from relaxations of silicon tetrahedron networks by Lanthanum atom.

In conclusion, an enhancement in oxidation rate of SiC substrates with La$_2$O$_3$ capping layer has been obtained, however rough interface and surface with La-silicate grains have been observed. SiN interface layer has been adopted for suppress of the oxidation variation. A reduction of surface roughness of formed gate dielectric has been found with initial SiN interface layer. Gate dielectric with uniform La-silicate layer has been obtained by SiO$_2$ capped annealing in O$_2$ ambient at 1050$^\circ$C, showing a huge suppression of oxidation variation. Lanthanum element has been detected from the thermal growth layer near SiC/La-silicate interface, which may help modifying the gate dielectric interface layer.
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Chapter 1
Introduction

1.1 Introduction of SiC semiconductor and its application

1.2 Low electron mobility issue for SiC power devices and relations with interface state density

1.3 Alternative techniques to reduce interface traps in 4H-SiC MOS capacitors and an approach of using La-silicate dielectric

1.4 Purpose and outline of this thesis
1.1 Introduction of SiC semiconductor and its application

Silicon Carbide (SiC) is one of the IV-IV group element semiconductor, which was first artificially synthesized by Acheson in 1882. Silicon carbide powder has been mass-produced since 1893 for use as an abrasive. Electronic applications of SiC as light-emitting diodes (LEDs) and detectors in early radios were first demonstrated around 1907. In 1940, a publication by Seitz “Theory of solids” introduced the notion of semiconductor, which has also state the possibility of SiC as a semiconductor.

In 1950s, driving by the huge demand of developing semiconductor device capable of high temperature operation. The research of SiC semiconductor devices started. However, due to lacking of high quality wafer and a series of problem, the research of SiC semiconductor device get stuck. At the same time, the technology of Si semiconductor devices developed rapidly, the research of SiC devices was set aside for a long time. However, benefit from the technology of bulk crystal growth and step controlled epitaxy in 1980s, the study of SiC revitalized. In 1990s, crystal growth structure, elucidation of step control epitaxy, precise control of impurity doping, all the basic technology has been settled. The research of SiC semiconductor device have had a big break through.
Table 1.1.1 Comparison of basic parameter of silicon and 4H-SiC

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$(ev) bandgap</td>
<td>1.1</td>
<td>3</td>
</tr>
<tr>
<td>$E_{BD}$(10^6V/cm) Breakdown field</td>
<td>0.3</td>
<td>2.8</td>
</tr>
<tr>
<td>$\mu$(cm²/Vs) mobility</td>
<td>1450</td>
<td>900</td>
</tr>
<tr>
<td>$V_{sat}$(10⁶cm/s) Saturated velocity</td>
<td>10</td>
<td>22</td>
</tr>
<tr>
<td>$\kappa$(W/cmK) Thermal conductivity</td>
<td>1.5</td>
<td>5</td>
</tr>
</tbody>
</table>

SiC is a compound semiconductor with stoichiometric ratio of Si: 50%, C: 50%. The interatomic distance of Si and C is as short as 0.189 nm, which has a high bonding energy of 4.5 eV. Due to this high bonding energy, SiC has extreme high hardness only less than diamond. From semiconductor physics side of view, the high bonding energy give SiC the nature of wide bangap and high electrical breakdown field. Table 1.1.1 shows the comparison of basic physics parameter of silicon and 4H-SiC. From which we could see, SiC has a wide bangap of 3 eV and a high break down filed of 2.8 eV which is 10 times larger than Silicon. The saturated velocity of SiC is also two times of Silicon. A wide bangap and well thermal stability shows SiC is suitable for making devices for high temperature operation. High break down filed means SiC is has overwhelming characteristic for power device application over traditional silicon
semiconductor. High saturated velocity also show the possibility for improving the performance of high frequency operation devices.

**Fig 1.1.2 Relation of doping density in PN junction in consideration of theoretical dielectric breakdown field**

Fig 1.1.2 shows the relation of doping density in PN junction in consideration of theoretical dielectric breakdown field of 4H-SiC. Fig 1.1.2 (a) shows the relation of blocking voltage and Fig 1.1.2 (b) shows the relation of maximum depletion width with doping density respectively. To contrast, the characteristic of silicon has also been shown at the same time. For having blocking voltage of 1000V, the necessary doping density of SiC is about $2 \times 10^{16}$ cm$^{-3}$ and $2 \times 10^{14}$ cm$^{-3}$ for Si [1]. Necessary depletion width for SiC and Si is 8 μm and 80 μm, respectively. From the comparison we could know that SiC significantly has better characteristic over traditional silicon semiconductor.
Fig 1.1.3 Relation of ON resistance of 4H-SiC and Si power device (unipolar device) per unit area with blocking voltage

In application field of power devices, the on resistance is a critical parameter to evaluate the electrical characteristic of the device. Fig 1.1.3 shows the relation of ON resistance of 4H-SiC and Si power device (unipolar device) per unit area with blocking voltage. In comparison of same blocking voltage, a dramatically reduction of drift resistance to 1/300 ~1/500 can be achieved by replacing Si power device to SiC power device (for unipolar device), which demonstrate SiC should be a promising material for power device.

As the classification of traditional silicon power devices, for silicon diode, Schottky Barrier Diode (SBD) was used under 200V blocking voltage, beyond this voltage, PiN diode was utilized. For switching devices, 300 V and 600 V is the border for application of unipolar Si device to biopolar Si device. On the other hand, blocking voltage of unipolar SiC power devices over 5KV is applicable. For SiC PiN diode and Insulated
Gate Bipolar Transistor (IGBT), ultra-high voltage application over 5KV-10KV is predicted. Fig 1.1.4 shows the application field and trend of power density for different kind of semiconductor power devices [2]. The combination of Si-switching devices and SiC freewheeling diodes is applicable for higher blocking voltage and higher power density. For application over 10KV field, whole power devices using SiC IGBT/PiN is potential to be used, which can be applied at higher power density at the same time.

![Diagram of power devices](image)

**Fig 1.1.4 Application field and trend of semiconductor power devices**

Now the performance of Silicon power devices are reaching limitation of the material of silicon. An innovation in material or new technology is highly demanded for power devices application. Due to the excellent physics nature of SiC, such as wide bandgap, high breakdown field, high saturated velocity and thermal conductivity, SiC power device are able to operate on high temperature, high frequency, high voltage in smaller size and with far fewer energy losses. A huge energy saving effect can be achieved by shifting from Silicon power devices to SiC based power devices, which could be a significant improvement for the construction of environmentally friendly society.
1.2 Low electron mobility issue for SiC power devices and relations with interface state density

A unique advantage of SiC over other wide bandgap semiconductor is the ability of SiC to grow SiO$_2$ by thermal oxidation, which is advantageous for device fabrication using traditional silicon process. However, thermal grown SiO$_2$ dielectric on SiC substrate suffers from low quality problem. Most of reported the channel electron mobility of SiC transistor using thermal grown SiO$_2$ still at low level of $10\text{cm}^2/\text{Vs}\sim 40\text{cm}^2/\text{V}$ [3,4]. This low inversion channel mobility inevitably lead to much higher on resistance of SiC power devices [5,6].

Lots of evidence shows that this poor electron mobility should be attribute to high interface state density (Dit) nearing the interface of SiO$_2$ and SiC [7]. Many hypothesis has been proposed to explain the defect mechanism at SiC/SiO$_2$ interface. Carbon defect has been suspected as one of the reason for interface state density. During thermal oxidation of silicon carbide, most of the excess carbon is believed to be transferred to CO molecules leaving the interface by diffusion. However, some of the carbon can remain at interface and form carbon clusters or graphitic regions [8]. Oxide defect also considered to attribute to Dit in ther upper bandgap of SiC. Afanas’ev et al. found that the high Dit occurring near the SiC conduction band edge originates from oxide defects located close to the interface and suggested that these defects are responsible for the observed mobility degradation [9,10]. This kind of defect may result from the oxidation vacancy, or from the dangling bond originates from the lattice mismatch of SiO$_2$ with SiC. Fig 1.2.1 show the relation of electron mobility with interface state density for SiC devices [11]. An inverse proportional relationship of Dit and electron mobility can be easily summarized by this bar diagram. It is clear that to achieve electron mobility over
100 cm$^2$/Vs, Dit down $10^{10}$ magnitude is necessary, which means reduction of interface state density are critical for high performance SiC power devices.

![Graph showing Hall-effect mobility and interface state density](image)

**Fig 1.2.1** A strong reduction of the interface trapped charge density at the onset of inversion and a correspondent increase of the peak Hall-effect mobility

### 1.3 Alternative techniques to reduce interface traps in 4H-SiC MOS capacitors and an approach of using La-silicate dielectric

Numerous interface treatment has been applied to reduce the interface traps at SiO$_2$/SiC interface. Annealing in ozone ambient has been found effective for reducing interface state density for SiC MOS capacitor. During annealing process ozone molecules thermally dislocated into radical oxygen, leading a passivation effect on SiO$_2$/SiC interface. R. Kosugi et al [12]. Introduced a mix oxygen/ozone gas annealing into oxidation furnace, where the atomic oxygen was formed by thermal decomposition of the O$_3$ molecules at elevated sample temperatures. The oxidation at 1200°C results in
the significant reduction of the Dit. Consequently, the Dit near conduction band edge was reduced in the oxidation of atomic oxygen with compared to that of O$_2$.

Besides ozone, hydrogen thermal treatment has also shown a Dit reduction effect of SiC devices. Annealing in H$_2$. In Si MOS technology, it is well known that H$_2$ annealing terminates dangling bonds of Si at the SiO$_2$/Si interface and reduces Dit of MOS structures. Tsuchida et al. reported that the clear absorption bands of the Si-H stretching vibrations were observed from the 6H-SiC (0001) surface after H$_2$ annealing at temperatures between 1073 K to 1273 K [13]. This suggests that hydrogen effectively terminates the dangling bonds of Si or C atoms at SiO$_2$/SiC interface after annealing at high-temperature. Dit reduced to one-fifth has been achieved by annealing in H$_2$ at 1000°C compared with sample without H$_2$ treatment [14].

NO, N$_2$O gas annealing is one of the most famous method for SiC surface passivation. Nitridation of SiC surface has been attributed as the most considerable reason for Dit reduction by NO, N$_2$O gas annealing [15, 16, 17]. By introducing N doping in SiC MOS interface, termination of dangling bond of Si or C atoms and removal of carbon residues can be promoted, which lead to reduction of Dit and negative fix charge and improved effective electron mobility[18]. However, surplus N doping enlarge the flatband voltage, which was attributed to the influence of fix charge in gate dielectric induced by SiON, SiN compound near gate oxide/SiC interface [19].

Recently, one research by X. Yang, et al [20] shows that by using Lanthanum silicate (La-silicate) as interface layer between SiO$_2$ and SiC substrate, a significantly reduced Dit has been achieved. Fig 1.5.1 shows the interface state density with and without La-silicate interface layer. One magnitude reduction of Dit is presented in comparison of that without La-silicate IL, due to the modifying effect of La-silicate dielectric.
1.4 Purpose and outline of this thesis

To achieve large scale industrialization of SiC power devices, modification of gate oxides on SiC is critical important for high performance SiC power devices. La-silicate is a promising candidate to reduce Dit and improve effective electron mobility of SiC power MOS, however, the reaction mechanism of La-silicate are still unknown on SiC substrate. In this study, reaction and formation of La-silicate dielectric on SiC substrate using different condition has been conducted, suppression of oxidation fluctuation and fine La-silicate layer forming method on SiC has also been discussed in this paper.

This thesis contain 6 chapters. In chapter 1, SiC semiconductor and its issue of application has been introduced. La-silicate is one promising candidate among the approach of improving gate-dielectric/SiC interface quality. In chapter 2, the common experiment process used in this study is described.

In chapter 3, the reaction of La$_2$O$_3$ on SiC substrate was investigated. An enhanced oxidation effect has been found by La$_2$O$_3$ capped annealing. Analysis by TEM,XPS was followed for further investigation of interface properties.
Chapter 4 describes the La-silicate gate dielectric formation with initial SiN interface layer. Reaction of La$_2$O$_3$ with SiN upon annealing has been analyzed by ATR-FTIR. A reduction of surface roughness of formed SiO$_2$ has been found by AFM.

In chapter 5, the La-silicate gate dielectric formation by cap-oxidation has been evaluated. The interface conformation of SiC with gate dielectric after different thermal treatment has been shown by TEM images. A TEOS/La-silicate dielectric structure has been present after SiO$_2$ capping oxidation at 1050°C.

Finally, in chapter 5, conclusions and prospects for future work are described.

Chapter structure in this thesis is summarized in the following chart.
Reference:


http://www.iisb.fraunhofer.de/de/mobisic.html


Chapter 2
Fabrication and characterization

2.1 experiment procedure

2.2 Experiment process

2.2.1 SPM cleaning and HF treatment
2.2.2 RE-oxides deposition by EB
2.2.3 PDA in 5%O2/95%N2 ambient
2.2.4 RF magnetron sputtering

2.3 Physical characterization method

2.3.1 ATR-FTIR
2.3.2 Electron microscopy
2.3.3 X-ray based method
2.3.4 Atomic force microscopy

2.4 reference
2.1 Experiment procedure

Fig. 2.1(a) shows the fabrication flow of FTIR samples. n-SiC (0001) substrates are first cleaned by SPM and HF treatment. For sample with SiN interface layer, thin film of SiN with a thickness of 1.5 nm and 2 nm was first deposited by PECVD. After that, one layer of La$_2$O$_3$ with thickness ranging from 2 nm to 10 nm was deposited by electron beam evaporation. A FTIR measurement followed after deposition. Then, sample was annealed in 5%O$_2$/95%N$_2$ ambient from 500 to 1000 for 30 min. FTIR measurement was followed after every annealing for examining the reaction on SiC. Further analysis has also been conducted to show more properties of formed La-silicate on SiC substrates. For comparison, sample without La$_2$O$_3$ has also been fabricated and measured. Fig. 2.2(a) shows the sample structure fabricated by this process. Fig. 2.1(b) shows the experiment procedure for SiO$_2$ capping thermal treatment. A thin film of La$_2$O$_3$ with a thickness ranging from 4 to 10 nm was deposited by electron beam evaporation on a HF-last n–SiC (0001) substrates. After that, A SiO$_2$ layer with thickness of 40 nm was deposited by PECVD. Then, sample will be annealed in 5%O$_2$/95%N$_2$ ambient in 1000$^\circ$C or thermal oxidized in O$_2$ at 1050$^\circ$C for 30 min, respectively. For reference of MOS capacitor, 50 nm Tungsten (W) was deposited using magnetron sputtering, followed with post-metallization annealed (PMA) using a rapid thermal annealing (RTA) in a forming gas (F.G.) (N2:H2 = 97%:3%) ambient at 420$^\circ$C for 30 min. After that, samples were analyzed by transmission electron microscopy (TEM). Sample fabricated by this process are shown in Fig 2.2 (b).
Fig 2.1 Fabrication procedure (a) FTIR measurement (b) SiO$_2$ capping thermal treatment

Fig 2.2 sample structure (a) FTIR measurement (b) SiO$_2$ capping thermal treatment
2.2 Experiment process

2.2.1 SPM cleaning and HF treatment

Since the working space for device fabrication is not perfectly clean, pretreatment for wafer sample is very necessary. Substrate before pretreatment basically have pollution of inorganic pollution such as metal and nature oxide film, organic pollution from human body or other object. SPM treatment, using piranha solution which is a mixture of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂), is effectively for removing organic residue on substrate surface. It will also hydroxylate the substrate surface, making the substrate highly hydrophilic.

Hydrofluoric acid (HF) treatment is another pretreatment process for removing inorganic pollutions on substrate. Due to the highly acid property, hydrofluoric acid is able to remove most metal residues and oxides on substrate. HF treatment are often followed after SPM treatment.

In this study, the solution radio of H₂SO₄ and H₂O₂ is set to 3:1, fresh solution heat up to 180°C was used, sample was treated in H₂SO₄/H₂O₂ solution for 4 minutes for removing organic pollutions. After SPM treatment, samples was set into 20% HF for 5 minutes to removing residue particle and metal pollutions.

2.2.2 RE-oxides deposition by EB

Electron beam deposition (EB) is a way for deposit La₂O₃ on SiC substrate. The illustration of deposition by EB has been shown in Figure 2.3. The source of La₂O₃ was set on water cooled holder, Electron beam generated by heated-filament was accelerated by high electron filed. After circular motion in magnetic field, electron beam hit on
source ingot. Target were then transform into gaseous phase and coating on sample surface (To be exactly, most area inside deposition chamber).

In this study, the deposition of La$_2$O$_3$ was conducted in high vacuum under 10$^{-6}$ Pa. Sample holder was slowly rotated to ensure the deposited La$_2$O$_3$ was uniform. Shutter was used for start and stop the deposition.

![Diagram of La$_2$O$_3$ deposition by electron beam](image)

*Fig 2.3 illustration of La$_2$O$_3$ deposition by electron beam*

2.2.3 PDA in 5%O$_2$/95%N$_2$ ambient

Post deposition annealing is a thermal treatment used for formation of La-silicate. After deposition of La-silicate by electron beam. Sample will send into Rapid Thermal Annealing (RTA) chamber for annealing. The temperature curve in annealing process is shown in Fig 2.4. To ensure the oxidation begins at specified temperature. A rapid
heating rates was obtained by high density lamps. In this study, annealing temperature from 500°C to 1000°C are used for the post deposition annealing.

2.2.4 RF magnetron sputtering

In this study, Deposition of gate electrode are conducted by Radio Frequency (RF) magnetron sputtering. The illustration figure of RF magnetron sputtering is shown in Fig 2.5. A high electron field is applied between substrate and target. A magnet is set under target to prevent plasma damage. Argon (Ar) gas flow into the chamber in the process of sputtering, and ionized by high electron field. Argon atom then hit on the target and the atom of target was emitted by impact. Ejected target atom then fly through the vacuum chamber and deposit on the substrate. In this experiment process, high vacuum over 1x10⁻⁶Pa are used. The flow rate of argon are controlled to 0.7 sccm. The sputter power is set to 200W.
2.3 Physical characterization method

2.3.1 ATR-FTIR

Fourier transform infrared spectroscopy (FTIR) is a vibrational spectroscopy measurement method used to obtain an infrared spectrum of absorption, emission, photoconductivity or Raman scattering of a solid, liquid or gas. Basically, Fourier transform infrared spectroscopy is the general for infrared spectroscopy using two interference light. The Schematic diagram of Michelson interferometer, which is used to generate interference light for FTIR analysis, are shown in Fig 2.6 [1]. One beam splitter is set in the middle, a stationary mirror and a moving mirror are set at two places. An infrared light source are generated from coherent light source, when the infrared
light reach the beam splitter. Ideally 50% of the light is refracted towards the fixed mirror and left 50% light is transmitted to the moving mirror. Light are then reflected from the two mirror back to beam splitter. As a result encountered two light beam interfered and pass into the sample compartment. There, the light is focused on the sample. On leaving the sample compartment the light is refocused on to the detector. By moving the right-side mirror, the optical path difference of two separated beam changes and different interference light can be generated. By calculate the received intensity of infrared light through Fourier transform, the absorption infrared spectrum can finally gain.

![Fig 2.6 Schematic diagram of Michelson interferometer](image)

IR spectroscopy is useful for identification, structure determination the compounds by identify the various vibrational modes of a molecule. When the frequency of the infrared
radiation matches the transition energy of the bond or group that vibrates. The radiation will be absorbed and the bond or group will be excited to a high energy level. For absorption of electromagnetic radiation, Molecules with a dipolar moment allow infrared photons to interact with the molecule causing excitation to higher vibrational states. The homo-polar diatomic molecules do not have a dipolar moment since the electronic fields of its atoms are equal. Also, monatomic molecules do not able to interact with IR radiation because they consist only single atom. For same dipole molecules, different vibration mode such as Symmetrical stretching, Antisymmetrical stretching, Twisting mode response to radiation of frequency, which can be observed on the FTIR spectrum.

In this study, Attenuated total reflection Fourier transform infrared spectroscopy (ATR-FTIR) is used for identification of the bond structure of gate dielectric on SiC substrate. ATR-FTIR enables samples to be examined directly in the solid or liquid state without other sample preparation [2]. Fig 2.7 shows the schematic illustration of reflection in ATR-FTIR measurement. The measure face of Sample was fit-closely to a Ge prism by mechanical holder. During measurement, infrared radiation enter the Ge-prism and occurs total reflection at sample/prism interface, because the incident angle \( \theta \) is larger than the critical angle. Infrared absorption happens at the reflection interface by the vibration of molecular at substrate surface. In Fig.2.12, \( D_p \) is the depth from interface and given by

\[
D_p = \frac{\lambda}{2 \pi n_1 \sqrt{\sin^2 \theta - \left( \frac{n_2}{n_1} \right)^2}}
\]

(2.1)

Where \( \lambda \) is wave number, \( \theta \) is incident angle, \( n_1 \) is Ge prism reflective index, \( n_2 \) is sample reflective index. \((n_1 > n_2 \text{ where } n_1 \text{ and } n_2 \text{ are higher and lower refractive index})}
[3]. The whole measurement are conducted in N\textsubscript{2} ambient to eliminate the disturbance IR absorption from CO\textsubscript{2}.

\begin{center}
\includegraphics[width=0.5\textwidth]{schematic.png}
\end{center}

*Fig 2.7 Schematic illustration of reflection in ATR-FTIR measurement*

2.3.2 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a famous method for obtain high resolution image by transmit electron beam through ultra-thin specimen. TEM is competent for ultra-high resolution imaging, owing to the small de Broglie wavelength of electrons. It is capable for analysis small specimen such as atomic arrangement and virus configuration of nanometer scale. TEMs find application in cancer research, virology, materials science as well as pollution, nanotechnology, and semiconductor research.

For tradition light microscopy, the resolution is determined by the wavelength of the photons that are being used to probe the sample, \( \lambda \) and the numerical aperture of the system, NA. [4]

\[
d = \frac{\lambda}{2n \sin \alpha} \approx \frac{\lambda}{2NA}
\] (2.2)
For TEM, electron beam was used for achieving high resolution imaging, by the wave-like properties of electron, electron beam can also behave like a beam of electromagnetic radiation. The wavelength of is related to their kinetic energy via the de Broglie equation. An additional correction must be made to account for relativistic effects, as in a TEM an electron's velocity approaches the speed of light, c. [5]

$$\lambda_e \approx \frac{h}{\sqrt{2m_0E(1+\frac{E}{2m_0c^2})}}$$  \hspace{1cm} (2.3)

Where, $h$ is Planck's constant, $m_0$ is the rest mass of an electron and $E$ is the energy of the accelerated electron.

Fig 2.8 shows the schematic illustration of Transmission Electron Microscopy. On the top side is a filament that used as electron emission source, which may be a tungsten filament, or a lanthanum hexaboride (LaB$_6$) source. Contrast with tungsten filament, LaB$_6$ source could generate electron beam with small energy dispersion. The extraction of electron beam is by the use of Wehnelt cylinder. The extracted electrons are then accelerated by high electron field (typically 100~300 kV), and emitted into the vacuum. The electron beam is then focused and manipulated by condenser lens, which allows the formation of electron beam to desired size and location for later interaction with sample. The lens used in TEM are magnetic field based that manipulate electron beam by adjust the magnetic flow. The lens consist a series of coil that vertical to the direction of electron beam. The convergence of electron beam are enabled by modifying the amount of current to change the magnetic flow in the coil. After transmitted through the sample, the image is magnified and focused by objective lens and imaging lens, and finally project onto an imaging device, such as a fluorescent screen.
2.2.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is a useful tool for analysis of surface element composition for semiconductor devices. It’s a surface-sensitive quantitative spectroscopic technique that that element composition at the parts per thousand range, empirical formula, chemical state and electronic state of the elements that exist within the material can be detected.
Fig 2.9 shows the schematic illustration of XPS measurement. A focused x-ray beam has been radiated on the sample surface. The inner electrons or valance electrons in atoms interacted with x-ray and being stimulated, escape from sample surface. The escaped electron were collected by electron energy analyzer to analysis the kinetic energy of the electron escaped. The signal then be collected by electron detector to get the XPS spectra of sample surface.

![Schematic illustration of XPS measurement](image)

For a certain XPS measurement, particular x-ray beam is used so the energy is known. And because the emitted electrons' kinetic energies can be measured, the electron binding energy of each of the emitted electrons can be determined by using an equation that is based on the work of Ernest Rutherford (1914):

$$E_{\text{binding}} = E_{\text{photon}} - (E_{\text{kinetic}} + \phi)$$  \hspace{1cm} (2.4)

Where $E_{\text{binding}}$ is the binding energy (BE) of the electron, $E_{\text{photon}}$ is the energy of the X-ray photons being used, $E_{\text{kinetic}}$ is the kinetic energy of the electron as measured by the instrument and $\phi$ is the work function dependent on both the spectrometer and the material.

XPS depth profiling is a derive method that using ion beam etching or chemical etching to exposure the deep layer in the sample. By continuous measurement, element
composition distribution in depth orientation can be obtained through etching.

2.3.4 Atomic force microscopy

Atomic force microscope (AFM) is scan probe microscope at nanometer range. Fig 2.10 shows the schematic illustration of AFM measurement. The key part of AFM is a cantilever spring that with a tip to detect the micro structure. This cantilever spring are at range of micro, usually be made by silicon or silicon nitride. The radius of curvature of tip is nano range, when tip reaching sample at very close distance, it will bend to the sample surface according to Hooke's law. Depending on the situation, forces that are measured in AFM include mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces (see magnetic force microscope, MFM), Casimir forces, solvation forces, etc. A laser beam was focus on the top surface of cantilever spring and be reflected to a Position sensitive photon detector, so the micro motion of tip can be detected by the movement of reflected laser on photon detector.

If tip was scanned at a constant height, there is a risk that tip may collides with the surface, which may damage the micro-tip. In practical application, a feedback mechanism is employed to keep the tip maintain a distance with sample.

AFM can be operated in a number of modes, depending on the application. In general, possible imaging modes are divided into static (also called contact) modes and a variety of dynamic (non-contact or "tapping") modes where the cantilever is vibrated. In this study, non-contact modes has been selected as the measurement for surface roughness of SiO₂ layer on SiC substrates.
Fig 2.10 schematic illustration of AFM measurement
2.4 Reference


Chapter 3

Reaction of La$_2$O$_3$ on SiC substrates

3.1 Introduction

3.2 An enhanced oxidation effect by La$_2$O$_3$ capped annealing

3.3 XPS analysis of interface above SiC substrate

3.4 Sectional image of interface above SiC substrate after annealing by TEM

3.5 conclusion

3.6 reference
3.1 Introduction

As a wide band-gap semiconductor, Silicon Carbide (SiC) is a promising candidate for next generation power devices, the ability to grow silicon dioxide (SiO$_2$) by thermal oxidation is a unique advantage over other advantage over other wide band-gap semiconductor material. However, the properties of thermal oxidation grown SiO$_2$ on SiC still suffer from a lot problems. The one issue is that, high temperature dry oxidation causes large thickness variation in SiO$_2$ and also rougher SiO$_2$/SiC interface by enhanced oxidation at step bunches due to large facet dependent oxidation rate, which leads to local electric field crowding to degrade the reliability [1-2]. The issue can be solved by replacing dry oxidation by oxygen radical oxidation, which could reduce the oxidation reaction activation energy difference at step and terrace. Meanwhile, oxidation at lower temperature can also be achievable by the catalyst effect of radical oxygen. Here, La$_2$O$_3$ is known to create radical oxygen atoms from oxygen molecules, so that one can expect an enhanced oxidation even at low temperature [3]. To elucidate the modifying mechanism of La-silicate on SiC substrate, the understanding of reaction and formation of La-silicate on SiC is necessary.

3.2 An enhanced oxidation effect by La$_2$O$_3$ capped annealing.

Fig 3.1.1 shows the infrared spectra of SiC substrate without and with 2nm La$_2$O$_3$ after annealing at different temperature. Both are normalized by signal from SiC substrate. Fig. 3.1 (a) shows the ATR spectra of same SiC substrate annealed at different temperature. The absorption peak at around 1250 cm$^{-1}$ with limited intensity was observed, which are attributed to the LO modes of the asymmetric stretching vibration of Si-O-Si bond absorption. The peak of Si-O-Si bond absorption appeared at 600 °C.
and increase with raising of temperature. Fig. 3.1.1(b) shows the ATR spectra of same SiC substrate with 2nm La$_2$O$_3$ deposited at different annealing temperature. The large absorption peak at around 1250 cm$^{-1}$ and 1065 cm$^{-1}$ are attributed to the LO modes of the asymmetric stretching vibration of Si-O-Si and La-O-Si-O bond. Both of the peaks appeared at 900 °C and increase significantly with the temperature raises. Since Si-O-Si bond are originate from formed SiO$_2$, La-O-Si-O bond related to La-silicate. The huge increase of Si-O-Si bond absorption peak means that more SiO$_2$ has been formed on SiC substrate with La$_2$O$_3$. So it is reasonable that the oxidation of SiC substrate was enhanced by La$_2$O$_3$ capped annealing.

![Fig. 3.1 infrared absorption spectra](image)

**Fig. 3.1** infrared absorption spectra (a) without La2O3/SiC  (b) La2O3 2nm/SiC

### 3.2 XPS analysis of interface above SiC substrate

To re-check the chemical composition on reacted La$_2$O$_3$ capped SiC substrate, XPS measurement has also been conducted. Fig 3.1.2 shows the deconvoluted binding energy of O(1s) and Si(2p) peak of SiC with 2nm deposited La$_2$O$_3$. Fig 3.2 a shows the
deconvoluted binding energy of O(1s). The biggest peak with binding energy of 533 ev should is originate from O-Si bond, a small peak around 531.5 eV is from the bond of La-O-Si. Fig 3.2 b shows the deconvoluted XPS spectra of Si(2p). Si 2p was decomposed into Si-O, Si-O-La, Si-C bond, with bonding energy of 155.5 eV, 153.5 eV, 152 eV, respectively. The biggest peak is Si-O, which should be attribute to composition of SiO₂. A small peak of Si-O-La shows the ratio of La-silicate in oxides grown on SiC is fairly small compared to SiO₂. A weaker peak Si-C should be originate from the SiC substrate. Compare the intensity of O-Si, La-O-Si bond in O1s spectra and Si-O, Si-O-La bond in Si2s spectra, it is clear that the XPS signal from SiO₂ is much higher than La-silicate, which means that SiO₂ is the dominate gate oxide in formed gate dielectric.

![O1s (90˚) XPS spectra](image1)

![Si2s (90˚) XPS spectra](image2)

Fig 3.2 the the deconvoluted binding energy of (a) O 1s and (b) Si 2p XPS spectra

3.3 Sectional image of interface above SiC substrate after annealing by TEM

Since the formed La-silicate is far more thinner than SiO₂. It is necessary to know the morphology of formed gate dielectric on SiC by annealing in 5%O₂. Fig 3.3 shows the
sectional image of interface above SiC substrate after annealing. The black region in SiO$_2$ film is La-silicate and the white region on SiC substrate are SiO$_2$. From the TEM image we could see that the La-silicate grain agglomerated in SiO$_2$ film. The SiO$_2$ that formed on by oxidation however, is much thicker than the origin deposited La$_2$O$_3$ on SiC. SiO$_2$ remains in amorphous and has a thickness about 10nm. A large oxidation fluctuation has been shown by the surface roughness of formed SiO$_2$. The agglomerated La-silicate grain seems tend to gathering on the top of SiC epitaxial step.

![Sectional image of interface above SiC substrate after annealing](image)

**Fig 3.3** sectional image of interface above SiC substrate after annealing

The oxidation fluctuation could be attribute to the facet oxidation of SiC. Compared with thermal oxidation of Si, the unique properties of SiC is to generate CO molecules during oxidation process, the following reaction governs the oxidation of SiC:

$$SiC + 1.5O_2 \leftrightarrow SiO_2 + CO$$  \[[1]\]

Fig 3.4 shows the facet oxidation rate of SiC [4], from which we could see that for SiC, C-face (0001) has the highest oxidation rate, since out-diffusion of CO gas is more easily on C-face. Oxidation rate on $\alpha$–face(1120) follows the C-face. Compared with C-face,
the oxidation rate of Si-face (0001) is one-tenth of C-face, lowest in all SiC face because the unfeasible for out-diffusion of CO gases. For SiC, step controlled epitaxy is a basic process to improve the crystal quality used for device fabrication. By step controlled epitaxy, SiC substrate surface is jagged and form structure so called terrace and step. The terrace is the original Si-face and the crystal face of step is considered to be \( \alpha \)-face(0\overline{1}20). The simulation image for oxidation of SiC substrate with epitaxy layer is shown in Fig 3.5. Since the oxidation rate on different crystal face is different, a thicker layer of SiO\(_2\) will firstly grow on top of the step position. With the oxidation process, the step will gradually consumed and finally form a SiO\(_2\) layer with uneven surface. For La\(_2\)O\(_3\) capped annealing, the same facet oxidation can happen and also cause the oxidation variation of SiO\(_2\).

**Fig 3.4 Oxide thickness as a function of time for dry thermal oxidation of the (0001) C-, (0\overline{1}20) a-, and (0001) Si-terminated faces of 4H-SiC at 1150 °C**

![Diagram of reaction speed difference of step and terrace](image1)

**Fig 3.5 the simulation of oxidation of SiC epitaxy surface layer**
3.4 Enhanced oxidation effect by La$_2$O$_3$ capped annealing

Although La-silicate grain agglomerated in grown SiO$_2$ layer, a thickness of approximately 10 nm has been achieved by annealing in 5%O$_2$ at 1000°C for 30 min. Fig 3.6 shows the enhanced oxidation effect of La$_2$O$_3$ capped annealing compared with traditional dry thermal oxidation. The dash line is SiO$_2$ growth rate of thermal oxidation [5]. The red mark is the oxidation rate by this study. Compared with traditional thermal oxidation, the oxidation rate La$_2$O$_3$ capped annealing is two order of magnitude larger at oxidation temperature at 1000°C, which should be attributed to the catalytic effect of La$_2$O$_3$.

![Graph showing SiO$_2$ growth rate vs. temperature]

Fig 3.6 Enhanced oxidation of La$_2$O$_3$ capped annealing compared with dry thermal oxidation
3.5 Conclusion

An enhanced oxidation of SiC substrates has been achieved by La2O3 capped annealing. XPS analysis shows that La-silicate and SiO2 both formed after annealing, and SiO2 is the dominate product of the reaction on SiC substrates. TEM analysis was followed to show the sectional image of interface layer on SiC substrates. A thick SiO2 layer of over 10nm has been grown on the SiC surface. La-silicate agglomerated at SiO2/SiC interface and grain of La-silicate positioned at bunches of SiC substrate. Thickness variation of SiO2 may due to the facet oxidation of SiC substrate. However, regardless of the oxidation variation, two magnitude higher oxidation rate has been achieved by La2O3 capped annealing, which should be attribute to catalytic effect of La2O3 to generate radical oxygen.
3.6 reference


Chapter 4
La-silicate gate dielectric formation with initial SiN interface layer

4.1 Introduction

4.2 Reaction of La$_2$O$_3$ with SiN upon annealing

4.3 Sectional image of interface on SiC substrate after reaction of La$_2$O$_3$ with SiN

4.4 An interface roughness reduction effect by SiN reaction with La$_2$O$_3$

4.5 Conclusion
4.1 Introduction

In chapter 3, we introduced the reaction of La$_2$O$_3$ on SiC substrates. An enhanced oxidation has been achieved by La$_2$O$_3$ capped annealing. However, the formed La-silicate agglomerated at SiO$_2$/SiC interface and SiO$_2$ is uneven. This oxidation variation is suspected to be related with the facet oxidation of SiC. To avoid oxidation variation, it is critical to suppress the oxidation of SiC substrate.

Silicon Nitride (SiN) is an excellent insulator for semiconductor manufacture. It is well known for use in LOCOS (LOCal Oxidation of Silicon) process. Due to the dense nature of SiN, it can be used as buffer layer between SiC and La$_2$O$_3$ for suppressing facet oxidation of SiC substrates. Fig 4.1 shows the illustration of mechanism for suppression of oxidation variation. In the situation of La$_2$O$_3$ directly deposited on SiC substrate, oxygen molecules diffuse through La$_2$O$_3$ layer and oxidize the SiC surface, which trigger the facet oxidation of SiC substrate and result in uneven insulator film. For sample with SiN buffer layer, SiN layer prohibit the diffusion of oxygen to SiC surface, at the same time, La$_2$O$_3$ react with SiN and form La-silicate. Due to the amorphous nature of deposit SiN and La$_2$O$_3$, the formed La-silicate are without oxidation variation. And finally insulation layer with fine La-silicate dielectric can be achieved with SiN buffer layer.
4.2 Reaction of La$_2$O$_3$ with SiN upon annealing

Reaction of La$_2$O$_3$ with SiN is a key process for SiC substrate with SiN buffer layer. Fig 4.2 shows the infrared spectra of sample with and without SiN after annealed at different temperature. From left to right shows the result of sample with 0 nm, 1.5 nm, 2nm SiN, respectively. From this all three picture we could see that, two infrared absorption peak arise from 900°C and 950°C, the absorption peak with wavenumbers around 1250 cm$^{-1}$ should from Si-O-Si, which from the generation of SiO$_2$. The peak arise from 900°C and arise with the temperature raises. Another peak with wavenumbers around 1070 cm$^{-1}$ is from La-O-Si-O, which is considered from the formation of La-silicate, appear from 950°C and increase with temperature raises. The appearance of La-silicate bond signal from 950°C confirms the reaction of La$_2$O$_3$ with SiN above 900°C. Also, a slightly decrease of absorption intensity of SiO$_2$ shows the weak suppression of SiO$_2$ growth with thicker SiN.
4.3 Sectional image of interface on SiC substrate after reaction of La2O3 with SiN

Fig 4.3 shows the TEM sectional image of sample with 2nm SiN buffer layer after annealing in 1000°C for 30 minutes. Same as TEM image of SiC substrate with La2O3, the white region on SiC substrate are SiO2 and the black region is the grain of La-silicate. A SiO2 layer of about 10 nm thick has been grown on the top of SiC substrate. The La-silicate, however, still has not form a uniform layer and agglomerated in SiO2 layer. If we enlarge the middle region of image A we could see that, although the surface of grown SiO2 layer are still uneven. A moderation of surface roughness been shown by insertion of SiN buffer layer.
4.4 An interface roughness reduction effect by SiN reaction with La$_2$O$_3$

To confirm the roughness reduction by SiN buffer layer, AFM measurement has been conducted for further investigation. Fig 4.4 shows the AFM measurement result of sample with and without SiN buffer layer. Fig 4.4 (a) shows the AFM image of sample with 2nm SiN and Fig 4.4 (b) shows the AFM image for sample only with La$_2$O$_3$ deposition. Both are observed after annealing in O$_2$ ambient for 30 min in 1000°C. For substrate with SiN deposition, a more flat surface has been observed. The Root Mean Square Roughness (RMS) of substrate with and without SiN insertion are 1.80nm and 2.35nm, respectively. This fact strongly indicated a more flat surface has been achieved by SiN buffer layer. With the reaction by SiN and La$_2$O$_3$, facet dependent oxidation should be moderated and a more flat surface has been obtained.
4.5 Conclusion

It has been confirmed that directly reaction of La$_2$O$_3$ with SiC substrate cause oxidation variation and may degrade the reliability of gate dielectric. By using a buffer layer of SiN between La$_2$O$_3$ and SiC, the moderation of facet oxidation has been achieved. SiN was firstly predicted to buffer the oxygen diffusion to SiC substrate and react separately with the La$_2$O$_3$, the fact is that oxidation of SiC still happens and cause the oxidation variation. However, a suppression of oxidation has still been achieved, and a oxidation surface with less roughness has been observed by using SiN buffer layer.
Chapter 5

La-silicate gate dielectric formation by SiO$_2$ capping oxidation

5.1 Introduction

5.2 Sectional image of interface above SiC substrate after SiO$_2$ capping annealing at 1000°C

5.3 Electrical characteristic comparison for SiC capacitor after gate dielectrics annealing in 5% O$_2$ and O$_2$.

5.4 Sectional image of interface above SiC substrate after SiO2 capping oxidation at 1050°C

5.5 Composition analysis of interface region above SiC substrate after SiO2 capping oxidation at 1050°C

5.5 Conclusion
5.1 Introduction

Oxidation variation by reaction of La$_2$O$_3$ with SiC substrate has been an issue for degrade the reliability and quality of gate dielectric. SiN buffer layer between La$_2$O$_3$ and SiC shows a moderation effect of facet oxidation on SiC substrate. For further improvement of gate dielectric formation process on SiC, the elimination of oxidation variation on SiC substrate should be achieved. Here, we change the annealing process by deposit thick SiO$_2$ layer on La$_2$O$_3$ before the annealing. During the annealing process, a thick SiO$_2$ layer can vastly reduce the oxygen diffusion on SiC substrate surface, as shown in Fig 5.1. A reduction of oxygen concentration by several magnitude can be achieved by 50 nm SiO$_2$ capping layer. With enormous reduction of oxygen molecule at SiC surface, a huge suppression of oxidation of SiC substrate can be achieved. Meanwhile, reduction of partial pressure of oxygen at reaction interface may change the oxidation mode of SiC. Fig 5.2 shows the relationship of P(O$_2$) and temperature with oxidation reaction of SiC [1]. For oxidation at 1000$^\circ$C, The reaction that generate carbon residues happens when oxygen is at atmospheric pressure. When the partial pressure of oxygen down to sufficiently low such us 10Pa, the reaction product besides SiO$_2$ will change into CO gas, which can escape from the oxide interface. By SiO$_2$ capped annealing, the partial pressure of oxygen reduces vastly and thus change the reaction product from carbon to CO, which improved the interface quality by leaving less carbon residues at the interface.
5.2 Sectional image of interface above SiC substrate after SiO$_2$ capping annealing at 1000$^\circ$C

Fig 5.3 shows the TEM sectional image of interface above SiC substrate after SiO$_2$ capping annealing at 1000$^\circ$C. The black region above SiC substrate should be La-silicate and the white region is considered to be SiO$_2$ layer. The SiO$_2$ surface remains flat after annealing, which shows an improvement contrast with sample without SiO$_2$ capped.
annealing. A continuous layer of La-silicate has been formed between SiO$_2$ and SiC, indicating the suppression of agglomeration by SiO$_2$ capping layer. However, some protrusion present at the oxidation interface. The formed La-silicate diffused into deposited SiO$_2$ layer. From the magnified TEM image we could see a thin white region at the La-silicate/SiC sub interface, which should be SiO$_2$ formed by oxidation of SiC. This indicate that the facet oxidation of SiC still happens at the interface and may result in the formation of La-silicate protrusion at the interface.

![TEM image of interface above SiC substrate after SiO$_2$ capping annealing at 1000 ºC](image)

**Fig 5.3** Sectional image of interface above SiC substrate after SiO$_2$ capping annealing at 1000 ºC

### 5.3 Electrical characteristic comparison for SiC capacitor after gate dielectrics annealing in 5%O$_2$ and O$_2$.

For searching the best condition of gate dielectric process annealing, SiC capacitor was fabricated by annealing with different oxygen partial pressure. Fig 5.4 shows the C-V characteristic of SiC capacitor annealed in different oxygen partial pressure during the gate dielectric formation process. Oxygen ratio in the O$_2$/N$_2$ hybrid gas is set from 5% to 100% respectively. From the image we could see that with the increasing of oxygen partial pressure. A negative shift of flatband voltage has been observed with higher
oxygen partial pressure. The negative shift of flatband voltage is considered to be induced by elimination of negative charges in oxides. Fig 5.5 shows the relation of hysteresis voltage range with annealing ambient. Large hysteresis reduction by one-third with higher oxidation ratio in annealing ambient has been achieved. The above result indicate that a higher oxygen partial pressure in annealing ambient can improve the interface properties of gate dielectric. For this research, better electrical characteristic can be achieved by changing the annealing ambient from 5%O2 to pure oxygen.

**Fig 5.4** C-V characteristic of SiC capacitor annealed in different oxygen partial pressure

**Fig 5.5** relation of hysteresis voltage range with annealing ambient
5.4 Sectional image of interface above SiC substrate after SiO$_2$ capping oxidation at 1050°C

For further improvement of gate dielectric quality, oxidation in higher temperature and using of thicker La$_2$O$_3$ has been applied to SiC substrates. From Fig 5.2 the P(O$_2$)-T phase diagram we could know that raising the oxidation temperature can help the reaction of SiC shift from region 4 to region 3, which can suppress generation of carbon residues at gate dielectric interface. A thicker La$_2$O$_3$ has also been deposited on SiC substrates. Fig 5.4 shows the illustration of dielectric improve mechanism by thicker La$_2$O$_3$. As we have talked about in chapter 3. La$_2$O$_3$ has catalytic ability to transform oxygen molecule into radical oxygen. When oxygen molecule diffuse into La$_2$O$_3$ layer, due to the catalytic effect, the oxygen molecule will gradually transform into radical oxygen atom. With thicker La$_2$O$_3$ the diffusion length of oxygen molecule in La$_2$O$_3$ layer will be longer and amount of oxygen molecule and radical oxygen will decrease and increase, respectively. Since the facet oxidation are related oxidation by oxygen molecule. A suppression of O$_2$ diffusion at SiC surface can further reduce the oxidation variation of SiC substrates.

Fig 5.4 Illustration of dielectric improve mechanism by thicker La$_2$O$_3$
Fig 5.5 shows the Sectional image of interface above SiC substrate after SiO2 capping oxidation at 1050°C. For contrast with MOS capacitor using same process, a tungsten layer has been deposited after the PDA of gate dielectric. The layer above SiC substrate is La-silicate, SiO2 and W, as shown in the image. A uniform layer of La-silicate has been confirmed, which shows a tremendous suppression of facet oxidation of SiC substrate.

Although a uniform layer of La-silicate and a flat SiO2 surface has been confirmed by SiO2 capped thermal oxidation at 1050°C, another TEM sectional image of the same sample shows different morphology of La-silicate layer. Fig 5.6 shows the sectional image of interface on SiC substrate after SiO2 capped oxidation. It is clear that there is a light shade region in the La-silicate layer. Between La-silicate and SiC substrate there is a thin layer with light color, which is consider to be formed by thermal growth during oxidation.
The thickness of each layer has been measured and shown in Fig 5.7. The layer between SiC substrate and La-silicate which are formed by thermal growth is about 2.4 nm thick. The La-silicate layer has a thickness about 7.4 nm, which is a little bit thinner than deposited La$_2$O$_3$. After annealing, the deposited SiO$_2$ layer is about 23.1 nm thick, however, before annealing, the thickness of deposited SiO$_2$ is 34 nm, which are measured by Spectroscopic Ellipsometry. This thickness reduction shows that deposited SiO$_2$ has been reacted with La$_2$O$_3$ during annealing.

*Fig 5.6 sectional image of interface on SiC substrate with light shade region in La-silicate region*
5.5 composition analysis of interface region above SiC substrate after SiO$_2$ capping oxidation at 1050°C

For further investigation of the light color region and the layer formed by thermal growth, which are mentioned in chapter 5.4, EELS analysis and nano beam electron diffraction has been conducted to identify the composition of each region. Specific spots in each region has been selected and numbered respectively, as shown in Fig 5.8. For investigation, nano beam electron diffraction has been conducted for spot 1 and spot 2. All the spot from 1 to 4 has been analyzed by EELS analysis for identification of the component composition in each region.
Fig 5.8 Specific spots in each region numbered for measurement on TEM cross section image

Fig 5.9 shows the electron diffraction pattern of spot 1 and spot 2. Fig 5.9 (a) shows the electron diffraction pattern of spot 1 and Fig 5.9 (b) shows the electron diffraction pattern of spot 2, respectively. Both of the electron diffraction pattern from spot 1 and 2 well matched with the crystal structure of La-silicate, which indicate that both region are La-silicate that formed after annealing.

Fig 5.9 Electron diffraction pattern of specific spots (a) Spot 1 (b) Spot 2
For further confirmation of the element composition of each spot, EELS analysis has been conducted to show further information. Fig 5.10 shows the EEL spectra of Spot 1 to Spot 4. The peak of Carbon shown on this figure is considered from the contamination of organic pollution. Element Si, O, La has been detected from Spot 1, 2, 4 and only Si and O has been detected from spot 3. The existence of element of Si, O, La at spot 1 and spot 2 indicate that a layer of La-silicate should have formed at the interface. For spot 4, a weak peak of La has been detected, shows that a small ratio of La-silicate also exist at the near SiC surface layer.

![EEL spectra of Spot 1 to Spot 4](image)

*Fig 5.10 Electron energy loss spectra of Spot 1 to Spot 4*

For comparison of the density of La-silicate in each region at the interface, an extraction of O and La peak in EEL spectra has been shown in Fig 5.11. Figure 5.11 (a) to Figure (d) shows the EEL spectra of Spot 1 to 4, respectively. It is clearly that the intensity of La peak of spot 1 is about 4 times that of spot 2. For spot 4, the intensity of La signal is about eighth of intensity of La that in Spot 1, indicating a small proportion of La atom exist in thermal growth layer.
Although selected area electron diffraction analysis support the point of view that region 1 and region 2 are both La-silicate region. The electron energy loss spectra shows that the intensity of La peak at spot 1 and spot 2 is about 4 times different, which means that spot 2 has much small La atom density than that of spot 1. However, the difference result by this two analysis method may simply induced by the existence of hidden SiO$_2$ at region 2. Figure 5.12 shows the illustration of this hypothesis. Interface layer at the right side TEM sectional image has been separated in vertical direction to show the planar structure of each layer. Region 1 and Region 2 are both located at La-silicate layer. Although oxidation variation of SiC substrate has been largely suppressed, facet
oxidation still happened partially at SiC surface and result in formation of SiO$_2$ “island” at La-silicate layer. So at region 2, both La-silicate and SiO$_2$ exist partially. That means, from selected area electron diffraction analysis (SAED), the La-silicate can be detected, but for EELS analysis, due to the partial existence of SiO$_2$, the La-silicate is looks like to be diluted and the intensity of lanthanum signal was reduced.

For the interface layer between La-silicate and SiC substrate surface, which is thermal growth by annealing, the little existence of La atom may have an effect to moderate the SiO$_2$ network. Figure 5.13 shows $t$ bonding structure and illustration of moderation effect of La atom in SiO$_2$ network. For SiO$_2$ network, the oxygen atom are fixed by the bridging bond between silicon atom and oxygen atom, after annealing, thermal stress may remain in the SiO$_2$ network and to cause defect. However, the bond of La and oxygen are flexible the oxygen are non-bridging. In SiO$_2$ network, with the non-bridging bond introduced
by La atom. The stress left by thermal treatment can be absorbed and the SiO₂ network can be modified.

![bonding structure and illustration of moderation effect of La atom in SiO2 network](image)

**Fig 5.12 bonding structure and illustration of moderation effect of La atom in SiO2 network**

(a) Si-O-Si bonding (b) La-O-Si bonding (c) La atom in SiO₂ network

### 5.6 Conclusion

In this chapter, SiO₂ capped annealing on SiC substrate has been studied. For SiO₂ capped annealing at 1000°C, a continuous layer of La-silicate has been formed between SiO₂ and SiC, indicating the suppression of agglomeration by SiO₂ capping layer. However, some protrusion present at the oxidation interface, which should be result from the facet oxidation of SiC substrate. SiO₂ capped annealing at 1050°C with thicker La₂O₃ deposition layer has also been conducted. A uniform La-silicate layer has been confirmed by sectional TEM image of interface layer after annealing at 1050°C. However, some light color region appears at part of La-silicate layer. SAED analysis shows that the existence of La-silicate crystal structure. EELS analysis indicating that the intensity of signal from Lanthanum is much weaker in this region. This may attribute to the oxidation variation of SiC substrate. Although facet oxidation has been largely suppressed by SiO₂ capped annealing. Oxidation variation still happened and SiO₂ island has been formed in La-silicate layer.
5.7 Reference

Chapter 6

Conclusions
In this thesis, the formation of La-silicate dielectric on SiC substrate has been studied. In each chapter, the studies are summarized below:

In chapter 1, SiC semiconductor has been introduced. As a wide band-gap semiconductor, SiC is a promising candidate for power device application. Although silicon dioxide can be grown on SiC substrate by thermal oxidation. The SiC MOSFET using silicon dioxide as gate dielectric is suffered from low mobility and reliability issues. Recent research shows that by using La-silicate as interface gate dielectric, an improved mobility has been achieved. For further improvement, the investigation of La-silicate formation reaction on SiC substrates is highly required.

In chapter 3, Reaction of La$_2$O$_3$ with SiC substrate has been introduced. The formation of La-silicate above 900°C has been confirmed that by ATR-FTIR. Also, compared with sample without La$_2$O$_3$ deposition, the oxidation of SiC substrate has been largely enhanced, which should be attribute to the catalytic effect of La$_2$O$_3$. However, a large oxidation variation has been observed by TEM sectional image. The thickness of formed SiO$_2$ varying by the step of SiC surface, and La-silicate grain agglomerated at the interface layer between La-silicate and SiC substrate.

In chapter 4, SiN barrier layer has been proposed as one solution of the oxidation variation of La$_2$O$_3$ capped annealing. The reaction of SiN and La$_2$O$_3$ has been confirmed above 950°C by ATR-FTIR. The observation result of TEM image shows that oxidation variation still happens despite the existence of SiN barrier layer. A reduction of surface roughness of formed SiO$_2$ indicate that the oxidation variation has been moderated.

In chapter 5, another gate dielectric formation method using SiO$_2$ capped annealing has been investigated. TEM observation result shows that a continuous layer of La-silicate has been formed after SiO$_2$ capped annealing at 1000°C for 30 minutes. However,
some big protrusion appear at the La-silicate layer, showing the oxidation variation existence at the interface. TEM sectional image of interface after SiO₂ capped annealing at 1050°C show improved properties. A uniform layer of La-silicate has been observed, indicating a huge suppression of oxidation variation. Some light color region present at La-silicate region is considered cause by the existence of SiO₂ at the same layer. The Lanthanum element existence has been confirmed at thermal growth layer, the non-bridging bond introduced by Lanthanum atoms are able to moderate the SiO₂ network, which is promising for improving the properties of gate dielectric on SiC substrates.
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