Reaction and formation of La-silicate gate dielectrics on SiC substrates

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Comparison of basic parameter of silicon and 4H-SiC

<table>
<thead>
<tr>
<th>Material</th>
<th>Si</th>
<th>SiC</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$(ev)</td>
<td>1.1</td>
<td>3.2</td>
</tr>
<tr>
<td>Bandgap</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E_{BD}(10^6 V/cm)$</td>
<td>0.3</td>
<td>3</td>
</tr>
<tr>
<td>Breakdown field</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\mu$(cm$^2$/Vs)</td>
<td>1450</td>
<td>900</td>
</tr>
<tr>
<td>mobility</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{sat}(10^6 cm/s)$</td>
<td>10</td>
<td>22</td>
</tr>
<tr>
<td>Saturated velocity</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\kappa$(W/cm$^2$K)</td>
<td>1.5</td>
<td>5</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The advantage of SiC devices over silicon:
- High operation voltage ($\times 10$ times)
- High operation frequency
- Better endurance of High temperature
- Low energy loss (1/100)

SiC is promising material for high efficiency power device
Issue of SiC power devices

SiC has the ability of forming SiO₂ by thermal oxidation.

Most report

Improvement of channel mobility is necessary

Relationship of mobility and Dit

Inverse proportional relationship of mobility with interface state density

Reduction of Dit is critical to make high-speed-SiC power device
Approach of Interface Improvement

- **NO,N$_2$O gas annealing**
  - Effective passivation of interface trap by annealing the gate oxide in NO,N$_2$O gas.

- **SiO$_2$/LaSiO$_x$ gate oxides on SiC**
  - Recently a passivation of interface trap on SiC has been found by forming LaSiO$_x$ interface layer on SiC substrate.

Purpose and outline of this presentation

Investigate the interface reaction of La$_2$O$_3$ on 4H-nSiC substrates to find the best process for gate dielectric application

1. Introduction
2. Interface reaction of La$_2$O$_3$ on 4H-nSiC substrates
3. SiN barrier layer for La-silicate dielectrics
4. Formation of La-silicate dielectrics by SiO$_2$ capped annealing.
5. Conclusion
1. Introduction

2. Interface reaction of La$_2$O$_3$ on 4H-nSiC substrates

3. SiN barrier layer for La-silicate dielectrics

4. Formation of La-silicate dielectrics by SiO2 capped annealing.

5. Conclusion
Sample preparation La$_2$O$_3$/SiC

$n$-SiC(0001)substrate

- Substrate cleaning (SPM, HF)
- La$_2$O$_3$ Deposition (EB)
- FTIR measurement
- Oxidation (5% O$_2$/95% N$_2$)
- FTIR measurement
- TEM analysis

$n$-SiC substrate

Sample 1

La$_2$O$_3$ (2nm)

Sample 2
Oxidation on SiC substrate was enhanced by La$_2$O$_3$ film
Accompanied by La-silicate formation
TEM image of \( \text{La}_2\text{O}_3/\text{SiC} \) oxidized at 1000\(^\circ\)C

sample: \( \text{La}_2\text{O}_3 \) (2nm)/SiC

- Agglomeration of La-silicates above \( \text{SiO}_2/\text{SiC} \) interface
- La-silicate grains positioned at bunches of SiC substrate (4\(^\circ\))
- Thick \( \text{SiO}_2 \) of 11nm is formed (enhanced oxidation rate)
Enhanced growth rate over thermal oxidation

sample: La$_2$O$_3$ (2nm)/SiC
after oxidation in 1000 ℃ 5%O$_2$ 30min

11.8nm

[Image of SiC(0001) sample]

Higher oxidation rate of 1.5 order of magnitude can be achieved by La$_2$O$_3$ capped oxidation
However, rough interface/surface may degrade reliability

Oxidation rate comparison


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SiN barrier layer against agglomeration

La-silicate formation by reaction of La$_2$O$_3$ and SiN layer (SiN: oxygen barrier to suppress oxidation of SiC)
Sample preparation with SiN barrier

- $n$-SiC(0001)substrate
  - SPM, HF cleaning
  - PECVD-SiN deposition
  - EB-La$_2$O$_3$ deposition
  - FTIR measurement
  - Annealing ($5\%$ O$_2$/95$\%$ N$_2$)
  - FTIR measurement
  - AFM, TEM analysis

- $n$-SiC substrate
- Sample
- La$_2$O$_3$ (4nm)
- SiN (2nm, 1.5nm, 0nm)

500°C ~ 1000°C
FTIR spectra of La$_2$O$_3$/SiN/SiC

Without SiN

SiN 1.5nm

SiN 2nm

Formation of La-silicate confirmed above 900°C
Slight suppression of SiO$_2$ with thicker SiN
La$_2$O$_3$/SiN/SiC interface section TEM image

Sample: SiO$_2$/La$_2$O$_3$ 4nm/SiN 2nm/SiC

Annealing temperature: 1000$^\circ$C

- Agglomeration of La-silicates above SiO$_2$/SiC interface
- Thick SiO$_2$ layer is formed (enhanced oxidation rate)
- Little suppression of oxidation variation
Oxides surface roughness reduction with SiN barrier layer has been confirmed by atomic force measurement.
1. Introduction
2. Interface reaction of La$_2$O$_3$ on 4H-nSiC substrates
3. SiN barrier layer for La-silicate dielectrics
4. Formation of La-silicate dielectrics by SiO$_2$ capped annealing.
5. Conclusion
Suppression of oxidation variation by increasing the diffusion length of oxygen to reduce the amount of oxygen reaching oxidating surface.
Sample preparation for SiO$_2$ capped annealing

- **n-SiC(0001) substrate**
- SPM, HF cleaning
- EB-La$_2$O$_3$ deposition
- PECVD-SiO$_2$ deposition
- Annealing (5% O$_2$/95% N$_2$) 1000°C
- Sputter-W(50nm) deposition
- PMA in F.G for 30 min
- Backside Al contact
- TEM analysis

Sample structure:
- Al
- SiO$_2$ (40nm)
- La$_2$O$_3$ (4nm)
- n-SiC substrate
• Suppression of agglomeration by SiO$_2$ capped annealing
• Some protrusion of La-silicates presented at the interface
Modification of SiO₂ capped annealing process

Suppression of carbon generation with higher temperature and low P(O₂)

- Thicker La₂O₃ may suppress the oxidation variation by generating more radical oxygen
- Optimal oxygen pressure may change due to change of annealing temperature.

C-V, Hysteresis on different O$_2$ partial pressure

Electrical properties improved by increasing O$_2$ partial pressure within annealing period
Modification of SiO$_2$ capped annealing process

*Before*

- $n$-SiC substrate
- Al
- W
- SiO$_2$ (40nm)
- La$_2$O$_3$ (4nm)

Annealing in 5% O$_2$, 1000°C

*After*

- $n$-SiC substrate
- Al
- W
- SiO$_2$ (40nm)
- La$_2$O$_3$ (10nm)

Annealing in O$_2$, 1050°C
A uniform La-silicate layer has been achieved by SiO$_2$ capped annealing in O$_2$ ambient, 1050°C
SiO$_2$/La$_2$O$_3$/SiC interface section TEM image

Light color region distributed in La-silicate layer
Both black and light color region in La-silicate layer are indicated to be La-silicate grain region.
EELS analysis result of 4 gate oxide region

- Lower Lanthanum density has been detected in light color region.
- Existence of Lanthanum atom in thermal growth region (4) has been confirmed by EELS.
Hypothesis for light color region in La-silicate

SiO$_2$ protrusion in La-silicate layer by facet dependent oxidation of SiC substrate
Atomic configuration of La-silicate

Si-O-Si bonding
La-O-Si bonding

BO: bridging oxygen atom
NBO: non-bridging oxygen atom

La atoms act as the network modifier to relax the SiO$_4$ network

The interface between La-silicate/SiC may be modified by Lanthanum atom in thin grown SiO$_2$
Conclusion

• Oxidation with La$_2$O$_3$ capped SiC substrate
  • Enhanced oxidation rate with radical oxygen atoms generated by La atoms
  • Grain growth, agglomeration of La-silicates
  • Surface roughness due to step enhanced oxidation

• SiN barrier layer for La$_2$O$_3$/SiC substrates
  • Formation of LaSiON interface layer
  • Reduction of gate oxides surface roughness

• SiO$_2$ capped annealing for La$_2$O$_3$/SiC substrates
  • Formation of uniform La-silicate layer
  • Interface modification with Lanthanum atom relax the SiO4 network of thermal growth layer
Thank you very much
Energy loss (eV)

Counts

Si

C

O

La

Spot 4

Spot 3

Spot 2

Spot 1

4H-SiC (1120)

*1 *2

*4

*3

10nm
FFT測定結果

sample: La$_2$O$_3$ (2nm)/SiC
after oxidation in 1000 ℃ 5%O$_2$ 30min

格子のデータが一致しています
SiO₂膜厚不均一性の説明

ステップ制御エピタキシー

オフ角: 4°

ステップ面とステップ面の反応スピードが違う

SiC酸化スピードの異方性

オフ角
テラス
ステップ
(0001)面

4H-SiC

膜厚不均一

熱処理温度増加によるCV特性の変化

950℃, 1000℃の場合はslow trapが大きい。
・La₂O₃が完全にsilicateに変わっていない
・界面、絶縁膜のバルク欠陥の除去が不十分

1050℃の場合に、その問題は改善
Incomplete oxidation by insufficient oxygen generate fixed negative charges at $\text{La}_2\text{O}_3$/La-silicate interface.
Modification of SiO\textsubscript{2} capped annealing process

- Thicker La\textsubscript{2}O\textsubscript{3} may suppress the oxidation variation by generating more radical oxygen
- Prohibition of carbon generation reaction with higher temperature

Suppression of carbon generation with higher temperature and low P(O\textsubscript{2})

Catalytic effect by La\textsubscript{2}O\textsubscript{3} to generate radical oxygen

Modification of SiO₂ capped annealing process

Suppression of carbon generation with higher temperature and low P(O₂)

- Thicker La₂O₃ may suppress the oxidation variation by generating more radical oxygen
- Optimal oxygen pressure may change due to change of annealing temperature.

SiC (0001) protrusion