Tokyo Institute of Technology Engineering

Bachelor Thesis

Electrical Characteristics of SiC Schottky Diodes with TiC and TiSi$_2$ Electrodes

Supervisor: Professor Hiroshi Iwai
Associate Professor Kuniyuki Kakushima

February, 2015
Presenter

Department of Electrical and Electronic Engineering
Student Number: 11_13380
Name: Tomoyuki Suzuki

<table>
<thead>
<tr>
<th>Supervisor Seal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Department Chairman Seal</td>
</tr>
</tbody>
</table>
SiC power devices have been progressed spectacularly as practical applications in recent years. The reason is that SiC has the superior physical properties for power device uses such as the high breakdown electric field and thermal conductivity. Moreover, the thing that research about SiC was developed more due to the material improvement of SiC substrate has contributed to the progress of SiC power device. Schottky-barrier diode using SiC has been integrated to next generation power device because of its great performance. However, the investigation and control of the interface between metal and SiC are the main subjects for SiC Schottky diodes nowadays. Accordingly, in this study, the metal electrodes TiC and TiSi2 were proposed, and the remarkable differences were found in the electrical characteristics of the fabricated SiC Schottky diodes with each electrode. As a result, the probability of the interface control by TiC and TiSi2 electrodes for the SiC Schottky diodes was certainly suggested.
Contents

Chapter 1 Introduction ............................................................................................................. 1
1.1 Power Electronics .................................................................................................................. 2
  1.1.1 Power Semiconductor Devices ....................................................................................... 3
  1.1.2 Applications of Power Semiconductor Devices ............................................................. 5
1.2 Utility of SiC ........................................................................................................................... 6
  1.2.1 Physical Properties of SiC Semiconductor ................................................................. 6
  1.2.2 Specific On-Resistances and Applicability of SiC Semiconductor Substrate .............. 9
1.3 Schottky-Barrier Diode ....................................................................................................... 11
  1.3.1 Basic Concept of Schottky-Barrier Diode .................................................................. 11
  1.3.2 Applications of Schottky Diode of SiC Substrate ......................................................... 13
  1.3.3 Issues of Metal/SiC Interface for Schottky Diode ......................................................... 14
  1.3.4 Approaches for Solution of Metal/SiC Interface Control for SiC Schottky Diode .... 15

Chapter 2 Experiment ................................................................................................................ 20
2.1 Experiment Outline .............................................................................................................. 21
  2.1.1 Experiment Purpose ..................................................................................................... 21
  2.1.2 Fabrication Procedure .................................................................................................. 22
2.2 Experimental Procedure ..................................................................................................... 24
  2.2.1 SPM Cleaning and HF Treatment .............................................................................. 24
  2.2.2 SiO₂ Deposition by PECVD with TEOS .................................................................. 25
  2.2.3 Patterning and SiO₂ Etching for Metal/SiC Contact Hole by Photolithography ....... 27
  2.2.4 Anode Electrode .......................................................................................................... 31
  2.2.5 Patterning for Residual Metal Etching by Photolithography .................................. 34
  2.2.6 Dry Etching of Residual Metal by RIE with Cl₂ ....................................................... 37
  2.2.7 Cathode Electrode ....................................................................................................... 39
  2.2.8 Annealing in N₂ Atmosphere ...................................................................................... 40
2.3 Current-Voltage Measurement ............................................................................................. 41
  2.3.1 I-V Measurement in Various Annealing Temperatures ............................................ 41
  2.3.2 I-V Measurement in Various Measuring Temperatures ............................................. 41
  2.3.3 C-V Measurement in Various Annealing Temperatures ........................................... 42
Chapter 3  Characterization Method

3.1 Current Density-Voltage Characteristics and Current-Transport Processes of Schottky-Barrier Diode

- 3.1.1 Shockley Diode Equation
- 3.1.2 Thermionic-Emission Theory
- 3.1.3 Image-Force Effect and Schottky-Barrier Lowering
- 3.1.4 Thermionic-Emission-Diffusion Theory

3.2 Capacitance-Voltage Characteristics of Schottky-Barrier Diode

3.3 Circumference Current

3.4 Measurement of Schottky-Diode Characteristics

- 3.3.1 Activation-Energy Characteristics by Arrhenius Plot
- 3.3.2 Current-Voltage Characteristics of Schottky Diode and Theoretical Curves Fitting
- 3.3.3 Capacitance-Voltage Characteristics of Schottky Diode

Chapter 4  Characteristics

4.1 Schottky-Diode Characteristics of TiC Electrode on SiC Substrate in Various Measuring Temperatures

- 4.1.1 J-V Characteristics in Various Measuring Temperatures
- 4.1.2 Evaluations of Effective Richardson Constant and Schottky-Barrier Height from Activation-Energy Characteristics by Arrhenius Plot
- 4.1.3 Evaluation of n-Factors in Various Measuring Temperatures by Fitting J-V Characteristics

4.2 Schottky-Diode Characteristics of Ti, TiC, and TiSi$_2$ Electrodes on SiC Substrates in Various Annealing Temperatures

- 4.2.1 J-V Characteristics in Various Annealing Temperatures
- 4.2.2 Evaluations of Schottky-Barrier Height and n-Factors by Fitting J-V Characteristics in Various Annealing Temperatures
- 4.2.3 Current-Electrode Area Characteristics in Various Annealing Temperatures

4.3 Power Loss of Schottky-Barrier Diodes

- 4.3.1 Specific On-Resistances of Schottky-Barrier Diodes
- 4.3.2 Calculated Power Loss of Schottky-Barrier Diodes

4.4 Capacitance-Voltage Characteristics of SiC Schottky Diode with TiC Electrode in
Chapter 1 Introduction

1.1 Power Electronics
   1.1.1 Power Semiconductor Devices
   1.1.2 Applications of Power Semiconductor Devices

1.2 Utility of SiC
   1.2.1 Physical Properties of SiC Semiconductor
   1.2.2 Specific On-Resistances and Applicability of SiC Semiconductor Substrate

1.3 Schottky-Barrier Diode
   1.3.1 Basic Concept of Schottky-Barrier Diode
   1.3.2 Applications of Schottky Diode of SiC Substrate
   1.3.3 Issues of Metal/SiC interface for Schottky Diode
   1.3.4 Approaches for Solution of Metal/SiC Interface Control for SiC Schottky Diode
1.1 Power Electronics

In the engineering technology, “Power electronics” is defined as the general term of the application of the conversion and control of electric power by using solid-state electronics. Furthermore, it is also a subject of research in electronic and electrical engineering using the circuits for varying the electric characteristics. The conversion of the electric-power systems can be classified below according to a combination of the types, direct current (DC) and alternating current (AC), in the input and output: AC to DC, DC to AC, DC to DC, and AC to AC. The conversion AC – DC is called a rectifier which transports the current to one direction, DC – AC is called an inverter which switches the turn on/off by using Pulse-width modulation (PWM), DC – DC and AC – AC are converters which use the combination of the rectifiers, inverters, and other devices. In this way, an electric characteristic can be converted into various form in the power electronics, so those uses for the electrical applications are very diverse to home use from the industries, for example personal computers or personal digital assistants and electric multiple units or power plants. The conversion of the electric characteristics is achieved and the electric power is controlled by using electronic switches, capacitors, magnetics, and other control systems. In addition, the demands of these electronic and electrical engineering technologies are more increasing for various electric and electronic industry.\(^1\) Moreover, “Power electronics” is one of the most growing fields because the improvement in the technologies and the materialization for more efficient power-electric circuits are required for the global energy-saving orientation at present.
1.1.1 Power Semiconductor Devices

For the efficient conversion of electric power, a power semiconductor device was introduced. The power semiconductor device is also called a power device, and it is used as a rectifier or a switch in the power electronics; it usually works in a state of "commutation mode" which represents turn on or off, which is used in non-linear operation. The power semiconductor device has one or more semiconductors: silicon (Si), gallium nitride (GaN), and silicon carbide (SiC) are the examples for the power device. Furthermore, the device of these semiconductors has a design which is optimized for that usage in the power electronics. The structure of power devices is classified as following categories shown in Figure 1.1 by the differences of the principal power switches:

1) A two-terminal device (diode); it has a path of the current flow but cannot switch the power flow by itself.

2) A three-terminal device (triode); it has a path of the current flow and can switch the power flow by the external switching signal through the terminal.

From the viewpoint of device mechanism of electric current drive, a majority carrier device which uses only one type of electric-charge carriers is faster than a minority carrier device due to the move of both majority and minority carriers. In contrast, while the minority carrier device has a time interval to form a depletion layer and change a switch to off from on, the minority carrier device has a higher performance in on-state. An ideal diode has the following characteristics: the switch of the current drive is the on-state in forward-biased condition, but is off-state in reverse-biased condition; these states are changed without an external control. On the contrary, an ideal triode switch represented as a transistor has the following characteristics: the main path of the current
is usually under a biased condition, and the current can be switched by the external switching signal with the third terminal of the path. The design and structure of the transistor is optimized to the use purpose; it is has very high reverse breakdown voltage, current-carrying capability, switching speed, power efficiency, or other purposes. For example, thyristor or bipolar transistor has high reverse breakdown voltage and current-carrying capability but a problem in the switching speed because of the minority carrier device. On the other hand, a field effect transistor like MOSFET has the opposite properties to those devices due to the majority carrier device. These years, IGBT having a compatibility of these properties had been introduced, and it seems to be researched enthusiastically. However, the power devices of such structures should be used in the suitable condition and application. More detailed classifications of these components and devices are presented in a concise essay (Appendix 1).

![Diagram of power semiconductor devices]

**Figure 1.1** Categories of power semiconductor devices.
1.1.2 Applications of Power Semiconductor Devices

The power device is studied and used in various fields of the industry. As a result, many applications of the power devices have been created for a half century and used for the industrial fields with appropriate devices. In the operation of high power systems, the control of megawatts or gigawatts is required at relatively low frequency. The applications for power devices are sorted as a function of the frequency and a typical trend of the relation, applications and power devices, shown in Figure 1.2. As the frequency of the operation increases, the electric power relatively decrease for the devices. For example, thyristor operates in low frequency and high power application, IGBT for the range of the middle of the frequency and power application, and power MOSFET for high frequency and low power application.

![Figure 1.2 Applications and power devices based on the power capacity and switching frequency.](image)
1.2 Utility of SiC

A semiconductor Si has been adapted to conventional power devices. However, new semiconductor materials, such as SiC or GaN, began to be introduced to the research fields and products of power device in these years. The common background of the superiority and compatibility of SiC for Si is expressed in an essay (Appendix 2) with concision. SiC has industrially been used for the abrasive or the cast iron for about a century. For other example using SiC, vehicle brakes, car clutches, and ceramic structures in applications requiring high endurance have been realized. The turning point into electronic applications had been come by the produce of large single crystals of Silicon carbide, which is concisely expressed in an essay (Appendix 3). Basically, the reasons of using SiC are that the physical properties are especially high performances for featuring uses in comparison with other semiconductors.

1.2.1 Physical Properties of SiC Semiconductor

Table 1.1 shows physical properties and calculated Baliga factors of the semiconductors.\(^4\) Where \(E_g\) is the band gap, \(\mu_n\) and \(\mu_h\) are electron and hole motilities respectively, \(E_c\) is the breakdown-electric field, \(\lambda\) is the thermal conductivity, \(\varepsilon_r\) and \(\varepsilon\) are the relative permittivity and dielectric constant respectively. Moreover, Baliga factor of merits (BM) of each semiconductor were calculated by using these constants.\(^5\) The equation of BM is:

\[
BM = \varepsilon \mu_\text{n} E_c^3
\]  

(1.1)

In Table 1.1, the values of this factor are also shown in addition to the relative values with the standardized Si. In the kinds of SiC, especially 4H-SiC which is a kind of
crystal structure was adopted in this study. The characteristic that is common to SiC is wide-band gap and high thermal conductivity $\lambda$. These are reasons that SiC is used under high voltage and high temperature environment respectively; power device and power electronics are usually employed in such conditions. Moreover, the Baliga factor of 4H-SiC marked about 300 times as much as that of Si. It is suggested that a device made form SiC probably has high performance. In contrast, the Baliga factor of GaN and diamond is higher than that of SiC. GaN represented as a blue LED has also been researched as power device. However, it has problems in the thermal conductivity, and other physical properties. High-electron-mobility transistor (HEMT) for GaN has then been suggested, and it seems to be used in especially high frequency devices. Diamond is one of very exciting semiconductors because it has a very excellent physical characteristic and chemical stability. Nevertheless, because a semiconductor substrate of diamond can hardly be made or molded, it is thought that it is far from practical use as the initial stage of the study. Therefore, SiC is superior as a power device from viewpoints of the performances such as high voltage and heat durability. In addition, production cost and productivity of SiC power devices is about to balance with those performances. Note that Baliga factor indicates vertical electronic devices structure; it means that if device structure is improved, performance of device is also enhanced such as IGBT.
Table 1.1 Physical properties and Baliga factors of semiconductors $^{4,5}$

<table>
<thead>
<tr>
<th></th>
<th>Diamond</th>
<th>GaN</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
<th>3C-SiC</th>
<th>GaAs</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_g$ [eV]</td>
<td>5.47</td>
<td>3.39</td>
<td>3.26</td>
<td>2.93</td>
<td>2.23</td>
<td>1.43</td>
<td>1.12</td>
</tr>
<tr>
<td>$\mu_n$ [cm$^2$/V-s]</td>
<td>2200</td>
<td>900</td>
<td>850</td>
<td>400</td>
<td>800</td>
<td>8500</td>
<td>1400</td>
</tr>
<tr>
<td>$\mu_h$ [cm$^2$/V-s]</td>
<td>1600</td>
<td>150</td>
<td>115</td>
<td>90</td>
<td>40</td>
<td>400</td>
<td>600</td>
</tr>
<tr>
<td>$E_c$ [V/cm]</td>
<td>1.1×10$^7$</td>
<td>3.3×10$^6$</td>
<td>2.5×10$^6$</td>
<td>2.8×10$^6$</td>
<td>1.2×10$^6$</td>
<td>4.0×10$^5$</td>
<td>3.0×10$^5$</td>
</tr>
<tr>
<td>$\lambda$ [W/cm-K]</td>
<td>20</td>
<td>2.0</td>
<td>4.9</td>
<td>4.9</td>
<td>4.9</td>
<td>0.5</td>
<td>1.5</td>
</tr>
<tr>
<td>$\varepsilon_r$</td>
<td>5.5</td>
<td>9.0</td>
<td>9.7</td>
<td>9.7</td>
<td>9.7</td>
<td>12.8</td>
<td>11.7</td>
</tr>
<tr>
<td>$\varepsilon$ [F/cm]</td>
<td>4.9×10$^{-13}$</td>
<td>8.0×10$^{-13}$</td>
<td>8.6×10$^{-13}$</td>
<td>8.6×10$^{-13}$</td>
<td>8.6×10$^{-13}$</td>
<td>1.1×10$^{-12}$</td>
<td>1.0×10$^{-12}$</td>
</tr>
<tr>
<td>BM $[\varepsilon\mu_nE_c^2]$</td>
<td>1.1×10$^{12}$</td>
<td>2.6×10$^{10}$</td>
<td>1.1×10$^{10}$</td>
<td>7.5×10$^9$</td>
<td>1.2×10$^9$</td>
<td>6.2×10$^8$</td>
<td>3.9×10$^7$</td>
</tr>
<tr>
<td>BM (Std. Si)</td>
<td>27359</td>
<td>658</td>
<td>291</td>
<td>193</td>
<td>30</td>
<td>16</td>
<td>1</td>
</tr>
</tbody>
</table>
1.2.2 Specific On-Resistances and Applicability of SiC Semiconductor Substrate

There is specific on-resistance (\(R_{sp,on}\)) of the characteristics calculated from the Baliga factor. This is an ideal resistance of an interface layer of the semiconductor and other materials like metal, and \(R_{sp,on}\) is shown in the following equation: \(^5\)

\[
R_{on,sp} = \frac{4V_B^2}{\varepsilon\mu_c E_c^3} \text{ [\(\Omega\text{cm}^2\)]} \tag{1.2}
\]

Where \(V_B\) [V] is a breakdown voltage of the electronic device; it depends on the device structure. Moreover, a total resistance of the semiconductor \(R_{on}\) [\(\Omega\text{cm}^2\)] also includes a resistance of the substrate \(R_{sub}\) [\(\Omega\text{cm}^2\)], and it shown in the following equation: \(^6\)

\[
R_{on} = R_{on,sp} + R_{sub} = \frac{4V_B^2}{\varepsilon\mu_c E_c^3} + \rho_{sub} w \text{ [\(\Omega\text{cm}^2\)]} \tag{1.3}
\]

Where \(\rho_{sub}\) [\(\Omega\text{cm}\)] is a resistivity of the substrate and \(w\) [cm] is a thickness of the substrate. It is found that, when the Baliga factor is high, the on-resistance is suppressed low even if the device has the structure in which the breakdown voltage is high. Figure 1.3 shows the calculated characteristics of on-resistance versus breakdown voltage of the semiconductors on the assumption of \(R_{sub} = 0.0006\) [\(\Omega\text{cm}^2\)]. Generally, as a resistance decreases, an electrical power loss decreases and a efficiency rises. As a result, 4H-SiC is applicable for many power devices, such as controllers of an electronic motor or power distribution system that need not only the high breakdown voltage but also large current density.
Figure 1.3 Calculated characteristics of on-resistance versus breakdown voltage of the semiconductors \( R_{\text{sub}} = 0.0006 \ \Omega \text{cm}^2 \).

Assumption:
\[ R_{\text{sub}} = 0.0006 \ \Omega \text{cm}^2 \]
1.3 Schottky-Barrier Diode

In this study, Schottky-barrier diodes of SiC substrate were investigated. In this section, a concise basis of a concept and mechanism of Schottky-barrier diode and its applications using SiC substrate are introduced. In addition, some issues of Schottky-barrier diodes about a metal and SiC semiconductor interface are discussed.

1.3.1 Basic Concept of Schottky-Barrier Diode

Schottky-barrier diode is one of the rectifiers to transport current flow in one direction from anode to cathode. The Schottky diode consists of a metal and semiconductor junction called “Schottky junction.” It is also called “Schottky contact.” In band theory, a barrier of the diode is formed by a difference of electric potentials at a metal/semiconductor interface. A schematic example of a band gap of the metal/n-type semiconductor from band structure in thermal equilibrium state is shown in Figure 1.4. Where $\phi_{Bn}$ is a Schottky-barrier height for n-type semiconductor, and $W_D$ is a depletion-layer width. Parameters of the right side of the semiconductor are respectively: a conduction band ($E_c$), a Fermi level ($E_f$), a valence band ($E_v$), and an intrinsic band ($E_i$) in the order from the top side. Electrons on the conduction band or metal are rectified from the semiconductor to metal because there is the Schottky barrier formed by the Schottky junction as a valve. Moreover, the Schottky barrier dam up electrons moving from the metal to the semiconductor; in an ideal diode, it can be said that all electrons are stopped by the barrier and there is no leak current in a reverse direction. As a result, the electric current flows only in a forward direction, so the Schottky diode has rectification characteristics. Note that only the side of the conduction band contributes to the rectification; this diode characteristic is caused by
the Schottky-barrier height on the conduction band in the n-type semiconductor. In addition, in the depletion region, the Fermi level is not replaced with the intrinsic Fermi level; in the band diagram, the Fermi level is not above the intrinsic Fermi level in the semiconductor. Therefore, the rectifier of the Schottky-barrier diode is given by a majority carrier movement, and the switching as a diode is fast in comparison with other diodes which take a long time to form the depletion layer. From such viewpoints, it is suggested that only the electron transportation process of the metal/n-type semiconductor should be discussed. While the depletion layer width relating to the switching speed can be changed and controlled by a donor concentration, the Schottky-barrier height cannot be controlled easily; the reason is expressed in the following. In ideal condition, the Schottky-barrier height (potential energy) can be generally given by the following equation:

\[ q\phi_{bn} = q(\phi_M - \chi) = q\phi_{MS} \]  \hspace{1cm} (1.4)

Where, \( \phi_M \) is a work function of metal, \( \chi \) is an electron affinity for semiconductor, and \( \phi_{MS} \) is a difference between the metal work function and n-type semiconductor. These parameters are determined by the values peculiar to the materials. However, this is hardly realized experimentally. The cause is expected to be that the interface layer of metal and semiconductor may usually be out of the ideal condition, so the Schottky-barrier height measured experimentally can be different value to the theoretical ideal result. Although there are many kinds of methods to investigate the interface in the various report, the control of an interface state formed between metal and semiconductor is the main purpose in the most of them.
Figure 1.4 Schematic band diagram of metal/semiconductor junction (Schottky junction) in thermal equilibrium state.

1.3.2 Applications of Schottky Diode of SiC Substrate

In these years, applications using SiC semiconductor substrate spread to the electric and electronic fields including a power device such as diodes and transistor, for the brilliant physical properties. Especially, a lot of Schottky-barrier diodes of SiC are commercially available at present.\[7\] SiC Schottky-barrier diode (SiC-SBD) has the characteristics of both of SiC and Schottky-barrier diode. As a result, the SiC-SBD has the following characteristics: the switching-power loss is reduced, high switching speed and high voltage are available, and the application is applicable in the severe environment like high temperature.\[8\] For example, a schematic circuit diagram of a power module using SiC-SBD as a component is shown in Figure 1.5. It seems that SiC-SBD is combined with SiC-MOSFET or Si-IGBT for power devices.\[8\], \[9\] In the electric circuit of the power device like Figure 1.5, it is considered that the improvement
of durability and the power-loss reduction of on-resistance are also needed. From the above, it is important to research the reliable metal electrode which is most suitable for SiC-SBD, and investigate the structure for higher performance.

![Figure 1.5 Schematic-circuit-diagram example of a power module using SiC-SBD (half bridge circuit).](image)

1.3.3 Issues of Metal/SiC Interface for Schottky Diode

SiC Schottky diodes of various metals and structures have been investigated since the large wafers with the (homo) epitaxial layer were developed.\cite{10,11} However, there were a lot of reports of a value of the Schottky-barrier height in spite of the same metal electrode because there could be different device structures and different interface conditions of the metal/SiC. Alternatively, it might be caused by the differences: measuring methods, analyzing methods, SiC substrate elements, or other causes. It is considered that there are certainly difficulties to determine the precise Schottky-barrier height at the interface of metal/SiC contact, and to investigate the completed characteristics of SiC-SBD. However, keeping study about SiC-SBD and researching
the characteristics of the metal-SiC interfaces and the diodes are very important, so that technical innovations and scientific discoveries are expected to be achieved by new materials of metal and SiC. Moreover, a major report described this situation as: \[11\]

“Since the performance of Schottky-based devices depends on barrier height, the optimum barrier height leading to high performance should be investigated in detail. In addition, the control of interface properties of Schottky metal/SiC is a very important issue for developing Schottky-based electronic devices.”

Therefore, the main purpose of this study also is an investigation of Schottky-barrier diode characteristics of some metal electrodes on SiC substrates. Especially, in this thesis, the differences of metal/SiC interface reactions by the different annealing temperatures were focused on, and the objectives of this research were the control of the interface reactions, and the progress of the diode characteristics for improving the performances of SiC Schottky-barrier diodes.

1.3.4 Approaches for Solution of Metal/SiC Interface Control for SiC Schottky Diode

The reaction path of metal and SiC interface can be described by a ternary diagram shown schematically in Figure 1.6. There are two way of the phase reaction for metal and SiC because SiC is a compound of Silicon and Carbon in the ration of one to one (i.e. Si:C = 1:1). When the phase reaction of metal and SiC is considered, SiC breaks down and spreads in the metal side. \[12\] The one way is that the metal-carbide is firstly formed on the metal/SiC interface before the metal-silicide is formed. In contrast, the other way is that the metal-silicide is firstly formed on the metal/SiC interface before the metal-carbide is formed. Therefore, it is possible that the reaction states of the
metal/SiC interface are described by the following stacked structures: Metal/Metal-silicide/Metal-carbide/SiC and Metal/Metal-carbide/Metal-silicide/SiC, which are shown in Figure 1.7. The reaction interface can move to SiC side whichever the reaction state is. Although the diffusion speed is determined by the metal, the diffusion speeds of the metal-carbide and metal-silicide are usually different. As a result, in the single metal and SiC interface, the reaction phase is unstably formed and there is a coexistence state of three phase (SiC, metal-carbide, and metal-silicide) on the diffusion path, which is shown in Figure 1.8. \[13\] According to the referenced report, it was confirmed that there are different paths of the reaction phase by metal. For example, the reaction path of the metal Ti (Titanium) and SiC is shown in Figure 1.9. \[14\] When the reaction path of Ti and SiC system are considered, the Ti-silicide can be formed first on the interface via T phase which is a ternary phase (Ti₅Si₃Cₓ). Then, Ti-carbide can be separated out second in the Ti side. This is found in the microphotograph of the reference (Figure 1.10). \[14\] From the above, it is suggested that TiC and TiSi₂ which are out of the reaction path might be hard to react with SiC substrate. As a result, these metal electrodes TiC and TiSi₂ attracted attention as the good electrodes for the SiC Schottky-barrier diodes. Therefore, this study suggested two approaches for the solution of metal/SiC interface control for Schottky diode. One of the approach was that TiC was formed beforehand on SiC substrate as the Schottky diode, and the diode characteristics were evaluated after the annealing at high temperature. The other one was that TiSi₂ was formed beforehand on SiC substrate as the Schottky diode, and the diode characteristics were evaluated after the annealing at high temperature. In order to implement and confirm these approaches, the experiment of the fabrication of the SiC Schottky diode and the measurement of the diode characteristics was conducted.
Figure 1.6 Schematic ternary diagram of metal-Si-C system.

Figure 1.7 Possible reaction states of metal/SiC interface. (a) Metal-silicide forms first and (b) Metal-carbide forms first.
Figure 1.8 Three phase equilibrium state diagram of SiC and metal. \(^{[13]}\) T means a state of ternary compound (Ti\(_5\)Si\(_3\)C\(_x\)).

Figure 1.9 Diffusion path between SiC and Ti on proposed Ti-Si-C three phase diagram. \(^{[14]}\)
Figure 1.10 Microphotograph of SiC/Ti system at 1673 K for (a) 0.3 ks and (b) 0.9 ks. [14]
Chapter 2 Experiment

2.1 Experiment Outline

2.1.1 Experiment Purpose

2.1.2 Fabrication Procedure

2.2 Experimental Procedure

2.2.1 SPM Cleaning and HF Treatment

2.2.2 SiO$_2$ Deposition by PECVD with TEOS

2.2.3 Patterning and SiO$_2$ Etching for Metal/SiC Contact Hole by Photolithography

2.2.4 Anode Electrode

2.2.5 Patterning for Residual Metal Etching by Photolithography

2.2.6 Dry Etching of Residual Metal by RIE with Cl$_2$

2.2.7 Cathode Electrode

2.2.8 Annealing in N$_2$ Atmosphere

2.3 Current-Voltage Measurement

2.3.1 $I$-$V$ Measurement in various Annealing Temperatures

2.3.2 $I$-$V$ Measurement in various Measuring Temperatures

2.3.3 $C$-$V$ Measurement in Various Annealing Temperatures
2.1 Experiment Outline

In this study, an experiment was conducted to fabricate the Schottky diodes and measure the diode characteristics. A main purpose of this research is an investigation that it elucidates the relationship of metals and a new semiconductor material of SiC by a Schottky diode structure. In this section, schematics of the purpose and procedure of the experiment are remarked for a precise-comprehension aid of principle parts of this thesis.

2.1.1 Experiment Purpose

Schottky diodes of Ti, TiC and TiSi₂ electrodes on SiC substrates were examined in this experiment. Especially, 4H-SiC was adapted to the substrate, for the basis electric properties of a vertical device were high in comparison with other crystal structures of SiC, such as 6H-SiC and 3C-SiC. Ti, which was a referenced metal electrode, was researched as a Schottky electrode of the diode on SiC substrate in a lot of monographs. \[10,11\] Moreover, it is known that Ti/SiC interface can be reacted in a high annealing temperature, so unstable phases may be established at the interface and it is suggested that the characteristics of device structures, such as Schottky or ohmic contact, may deteriorate.\[12\] TiC was elected as an electrode including C (carbon) because it was considered that it was hard to react with C of SiC substrate. Furthermore, TiSi₂ also was elected as an electrode including Si (silicon) because it was considered that it was hard to react with Si of SiC substrate. Although Ti electrode might react with SiC substrate by a sintering anneals, TiC and TiSi₂ would possibly be expected to form stable interfaces by such annealing. Therefore, the main purposes of this study were: to improve the characteristics of the Schottky diodes by forming TiC or TiSi₂ electrodes on SiC substrates as referencing one of Ti electrode, to maintain and progress the
rectification characteristics of the Schottky diodes in high annealing temperature, and to suggest that these electrodes can suppress the interface reaction of the metal/SiC-Schottky junction.

### 2.1.2 Fabrication Procedure

A fabrication procedure of Schottky diodes on SiC substrates was performed in this study. The fabrication has a standard semiconductor planar process which also applies other semiconductor devices such as Si, Ge, AlGaN/GaN, and other semiconductors. In addition, it is usually possible for laboratories or factories to conduct this process when they make power devices which have Schottky diodes. Figure 2.1 shows the fabrication process of Schottky diode of Ti, TiC and TiSi$_2$ electrodes on SiC substrates. Schottky diodes were fabricated on 4H-SiC epitaxial layer (12 μm) with SiC substrate. The side of anode electrodes was on the epitaxial layer, another side of cathode electrode was on the back substrate. Silicon dioxide (100 nm) for the oxide isolation of the sample was deposited on the epitaxial layer side by Plasma Enhanced Chemical Vapor Deposition with TEOS. Photolithography was conducted for device patterning, and the contact holes of metal/SiC were formed by removing SiO$_2$ with BHF. Metal layer or stacked layers of Ti, TiC and TiSi$_2$ for anode electrode were deposited by RF magnetron sputtering. Moreover, the cap of TiN was formed for preventing anode electrodes from the oxidation. Second photolithography was conducted for etching residual metal on the sample, and the pattern of the oxide isolation was formed. RIE was used for removing residual metal layer which was on the oxide layer (SiO$_2$) of the anode side mainly. Finally, the cathode electrode Ti, and the anti-oxidation cap TiN was formed by RF magnetron sputtering.
Figure 2.1 Fabrication process of SiC Schottky diodes of Ti, TiC and TiSi$_2$ electrodes.
2.2 Experimental Procedure

Details of each process of the experiment and measuring methods of the diode characteristics are expressed in the following subsections. In addition, experimental principles of the fabrication also are shown.

2.2.1 SPM Cleaning and HF Treatment

It is important to keep the surface of the substrate of SiC, also other semiconductors, clean, because particles and organic substances can become causes of the false operations of the devices. Therefore, keeping the surface of the semiconductor’s substrate clean contributes to improvement of defect rates. In this experiment, SPM cleaning and HF treatment were conducted to removing them on the surface. SPM (Sulfuric acid-Hydrogen Peroxide Mixture) consists of H₂SO₄ and H₂O₂ (H₂SO₄ : H₂O₂ = 4 : 1) and removes organic substances on the surface by oxidation reaction described in a following chemical equation;

\[
H_2SO_4 + H_2O_2 \rightarrow H_2SO_5 + H_2O
\]  

Because of its high oxidation power, particles and organic substances are oxidized and separated from the surface of semiconductor’s substrate. In this experiment, for removing organic substances on the SiC substrate, SPM cleaning was conducted for 10 minutes at 180 degree Celsius for having the chemical reaction activated. In addition, HF treatment, which can remove the oxide films, was used after SPM cleaning. The concentration of HF was below 5% and the HF treatment was conducted for 5 minutes at the room temperature with Teflon containers. The combination of SPM cleaning and HF treatment is one of the effective methods for removing unnecessary substances on the surface of semiconductors.
2.2.2 SiO\textsubscript{2} Deposition by PECVD with TEOS

There are many methods, such as the oxidation method and CVD method, to form SiO\textsubscript{2} on the semiconductors as the insulator materials in semiconductor devices. In this experiment, for making SiO\textsubscript{2} on the SiC substrate, Plasma–Enhanced Chemical Vapor Deposition (PECVD) which is a kind of CVD was used. PECVD has a lot of the merits to form various thin films. For example it forms films rapidly, covers large area and makes flat depositions because PECVD uses plasma which assists the deposition. Especially, for SiO\textsubscript{2} deposition by PECVD, TEOS (tetraethyl orthosilicate) is used. The molecule of TEOS, which is expressed in Figure 2.2, composed of SiO\textsubscript{4}^4- ion with four ethyl groups. In this experiment, the formation process of SiO\textsubscript{2} by PECVD and TEOS (what is called plasma-TEOS) is described below. Oxygen (300 sccm) and TEOS (1 sccm) which were used as material gases were injected into the reactor. These gases were changed into reactive gases by producing plasma using Radio Frequency (RF), and the reactive molecules of the gases were reacted chemically and deposited as SiO\textsubscript{2} (100 nm) on SiC substrates. Furthermore, other gases also, CF\textsubscript{4} and Ar, were used for cleaning the reactor. The deposition temperature of the reactor was kept at 250°C, and the pressure of gases was 30 Pa. Thus, the structure that SiO\textsubscript{2} covered SiC epilayer and substrate (Figure 2.3) was completed for oxide isolation.
Figure 2.2 Skeletal molecular structure of TEOS (Si(OC$_2$H$_5$)$_4$).

Figure 2.3 Schematic cross section Structure of SiC with SiO$_2$ passivation by PECVD (TEOS).
2.2.3 Patterning and SiO$_2$ Etching for Metal/SiC Contact Hole by Photolithography

In this experiment, two times of photolithography were conducted, and this subsection shows the first one. In order to fabricate SiC Schottky-barrier diode, it is necessary for anode electrodes to contact SiC epilayer. Photolithography and SiO$_2$ etching methods were used for forming the pattern and the contact hole of the anode electrodes. Figure 2.4 shows the process chart of positive-type photolithography and etching SiO$_2$, and Figure 2.5 shows cross section structures during patterning metal/SiC contact hole. First of all, the sample was coated with positive-type photoresist (S1805), and rotated by spin-coater for spreading photoresist to the edge of it. Thereafter, the coated sample was pre-baked at 115°C for 5 minutes on the electrical hotplate so as to vaporize the organic solvent and solidify the photoresist. Next, the sample and the patterned mask, shown in Figure 2.6, were aligned by mask aligner. Then, it was exposed to Ultra Violet (UV) light through the patterned mask by the exposure machine, and only the area of the photoresist which was exposed was reacted. The pattern of the mask appeared in the surface of the sample after developing it and removing redundant photoresist by using the developing solution (called NMD-3). NMD-3 consists of Tetra-Methyl-Ammonium-Hydroxide (TMAH) and develops only the reacted photoresist; that is, only the photoresist which was exposed to UV light is developed in positive-type photolithography. When the developing did not go well, exposure time was changed and these processes were repeated again. In the last of photolithography, the sample was post-baked at 130°C for 10 minutes on the electrical hotplate so as to vaporize the developing solution and adhere to the photoresist.

In order to form the pattern of metal/SiC contact holes for Schottky-barrier contacts,
SiO\textsubscript{2} thin film on the pattern of the anode electrodes was etched by the buffered hydrofluoric acid (BHF about 20%), especially this is called wet etching. Here, it is important for the experimenter to measure the etching rate for the best etching. In the last of these process, organic cleaning was conducted to remove the residual photoresist; that is, the substrate having the pattern-formed SiO\textsubscript{2} thin film was cleaned at room temperature by acetone, ethanol, and pure water used in this order, which can remove organic substances. Thereafter, SPM cleaning and HF (1%) treatment were also conducted. A part of the mask of this photolithography is shown by Figure 2.6. The red colored regions surrounded by squares in the mask were exposed to UV light, and the pattern was formed.

\begin{center}
\begin{tikzpicture}
\node (chart) at (0,0) {
\begin{itemize}
\item Coating positive-type photoresist
\item Spinning and Spreading photoresist
\item Prebaking
\item Aligning and Exposure
\item Developing
\item Post-baking
\item BHF etching
\item Organic cleaning
\end{itemize}
\end{tikzpicture}
\end{center}

\textbf{Figure 2.4} Process chart of positive-type photolithography and etching SiO\textsubscript{2}.  

28
Figure 2.5 Cross section structures during patterning of metal/SiC contact hole.
**Figure 2.6** Part of the mask pattern used for contact hole patterning in the photolithography.
2.2.4 Anode Electrode

In this study, three anode electrodes of metals were formed on SiC substrate. (i) Ti (titanium) was used for reference, because it was possible to confirm the characteristic differences between Ti and other metal compounds. (ii) TiC (titanium-carbide) formed by Ti and C was adopted, which was expected to have good property with SiC, especially with carbon. (iii) TiSi$_2$ (titanium-disilicide) formed by Ti and Si was adopted, which was also expected to have good property with SiC, especially with silicon.

This subsection shows the most important experiment process that anode electrodes of Schottky diode are formed on SiC substrate by using stacked structure of the metals.

In this experiment, radio frequency (RF) magnetron sputtering was used for deposition of metals. Figure 2.7 shows the schematic diagram of RF magnetron sputtering. There are three steps to deposit the metal on the substrate by this method. First, RF plasma was generated by applying RF power and supplying Ar (argon) gas which is ionized to Ar$^+$ in RF plasma. Residual gas was evacuated by turbo molecular pump (TMP) and rotary pump (RP). Secondly, the generated ions in plasma collided with the target which is composed of the metal, and atoms of the metal in the target were discharged out. Thirdly, the atoms detached from the metal were moved up, and sputtered on the substrate which was objective. The magnet is used for pulling generated plasma near the target, which can prevent plasma from reacting on the substrate.

The anode electrodes which were deposited by this method were Ti, C, Si and TiN. The experimental details of depositing these materials are shown by following below. In this process, the electrode of only Ti (20 nm) was deposited on SiC substrate with Ar gas (10 sccm, 7.5 mTorr). The TiC anode electrode, which is formed by stacked structures of Ti and C in this experiment, was made by piling up Ti and C layers in turn.
To provide details, a layer of Ti was 0.8 nm and that of C was 0.45 nm, and they were deposited to 18 sets alternately. The TiSi$_2$ anode electrode, which is formed by stacked structures of Ti and Si in this experiment, was also made by piling up Ti and Si layers in turn. To provide details, a layer of Ti was 0.46 nm and that of Si was 1.19 nm, and they were deposited to 16 sets alternately. At the last of this process, an anti-oxidation film of TiN (50 nm) was formed on the electrodes, which could prevent it from oxidation or reacting water in air. TiN was formed by sputtering Ti with N$_2$ gas in addition to Ar (Ar : N$_2$ = 9 : 1 sccm, 7.5 mTorr). Figure 2.8 shows the schematic illustrations of these stacked structures of anode electrodes made by RF magnetron sputtering.

Figure 2.7 Schematic diagram of RF magnetron sputtering.
Figure 2.8 Schematic illustrations of stacked structures for anode electrodes by RF sputtering.
2.2.5 Patterning for Residual Metal Etching by Photolithography

Figure 2.9 (a) shows the cross section structures of the sample after sputtering anode electrodes. In this time, the devices of Schottky-barrier diodes were connected each other via the electrode. In order to separate each device, the residual metal above SiO$_2$ on the substrate had to be eliminated.

In this process, the patterning by photolithography was conducted again like Section 2.2.3. The basic process chart of this photolithography was same as before. However, the photoresist (S1818) whose concentration is higher than previous one (S1805) was used in this process. For that reason, the exposure time of UV light and the developing time were longer than those of the first photolithography. The cross section structures during this photolithography were shown Figure 2.9. The mask used in the exposure is shown by Figure 2.10. Uncolored regions of the mask were exposed to UV light. The sample was aligned with the mask by aligner, and the exposure was conducted after aligning the alignment mark of the mask and the pattern of the sample. When they were aligned, that appearance looked like Figure 2.11 which is a part of the overlay of two masks.
Figure 2.9 Cross section structures of the sample during photolithography.
Figure 2.10 Mask pattern used in this photolithography. A cross of the top right corner in a device element shows an alignment mark.

Figure 2.11 Part of the overlay of two masks.
2.2.6 Dry Etching of Residual Metal by RIE with Cl₂

Reactive ion etching (RIE) is a kind of etching and patterning methods like wet etching by BHF. The operation principles of RIE are similar to those of RF magnetron sputtering, which uses Cl₂ gas and Ar plasma in this experiment. The generated reactive ions (Cl⁺) in Ar plasma collided with the bare electrode of the sample, and atoms of the metal in the electrode were discharged out. On the other hand, the areas of Schottky-barrier diodes covered with the photoresist were not reacted. Here, it is also important to measure the etching rate for the best etching by using extra substrate. Thereafter, the rest of the photoresist was removed by using the remover solution and an ultrasonic cleaning device, and organic cleaning was also conducted. Figure 2.12 shows the cross section structures of the sample during dry etching and removing the photoresist. Especially, Figure 2.12 (c) shows a completed design of Schottky diode devices with oxide isolated structure.
**Figure 2.12** Cross section structures of the sample during dry etching and removing the photoresist.
2.2.7 Cathode Electrode

In this experiment, Ti and TiN were used respectively for cathode electrode of the three SiC Schottky diode devices having anode electrodes of Ti, TiC and TiSi$_2$ covered with TiN which is called cap. RF magnetron sputtering was used for making cathode electrode in the same way as Section 2.2.4. First, Ti (20 nm) was deposited on the whole of the back side of SiC substrate uniformly. Next, TiN (50 nm) was deposited on the metal of Ti on SiC substrate as an anti-oxidation film. The cross section structures of the sample during this process are shown by Figure 2.13.

![Diagram](http://example.com/diagram.png)

**Figure 2.13** Cross section structures of the sample during cathode electrode forming.
2.2.8 Annealing in $N_2$ Atmosphere

Annealing is a kind of heat treatments, which can eliminate distortion and make organization soften. Especially, in order to form the anode electrodes, the rapid thermal annealing (RTA) was used. In this experiment, the purpose of annealing was to form Ti-carbide and Ti-disilicide by sintering of thin layers composed of Ti and C or Ti and Si. The annealing of the sample was conducted in the heat chamber which was filled with $N_2$ gas after evacuating it with a vacuum pump for avoiding the reaction of the electrodes and the atmosphere. The annealing time was always 1 minute, and its temperatures were: 500, 600, 700, 750, 800, 850, 900, 950, 1000, 1050°C. In addition, TiN/Ti electrode and TiN/TiC electrode was exfoliated in the 1050°C annealing.

An as-built drawing of SiC Schottky diode device in this experiment is shown by Figure 2.14.

![Figure 2.14](image_url) As-built drawing of SiC Schottky diode device in this experiment.
2.3 Current-Voltage Measurement

In order to characterize the Schottky diodes, current-voltage measurements were conducted as electric characteristics in this experiment. There were two ways of the measurements: in various annealing temperatures and in various measuring temperatures. These are described in the following sections.

2.3.1 I-V Measurement in Various Annealing Temperatures

In this experiment, current-voltage measurement was conducted after annealing at various temperatures which were shown in Section 2.2.8 so that SiC Schottky diodes of each electrode were characterized. The measured electrode areas were: 206, 100, and 50 μm square. Voltage was applied to Schottky diodes in the range of 5 from -5 V, and current was measured at respective voltages by a measuring instrument. The simple measuring circuit is shown by Figure 2.15.

![Figure 2.15 Schematic measuring circuit of I-V characteristics.](image)

2.3.2 I-V Measurement in Various Measuring Temperatures

Current-voltage measurement was also conducted in various measuring temperatures: 60, 80, 100, and 120°C in order to determine the effective Richardson constant of SiC Schottky diode. The sample of SiC Schottky diode of TiC with 500°C annealing was
used for this measurement, and the measured electrode areas, shown in Section 2.3.1, were same. Because of measuring the very small reverse current, $I-V$ measurement at higher measuring temperatures were needed to increase that current.

2.3.3 C-V Measurement in Various Annealing Temperatures

The capacitance-voltage measurement was additionally conducted for the SiC Schottky-barrier diode with TiC electrode in addition to the current-voltage measurement in various annealing temperatures: 500, 550, 600, 650, 700, 750, 800, 850, 900, 950, 1000, and 1050°C. The schematic measuring circuit is shown in Figure 2.16. A small AC voltage is added on a DC bias in the $C-V$ measurement. Moreover, in the $C-V$ measurement of Schottky diode, charges of one sign are induced on the metal or in semiconductor side and charges having the opposite sign are induced in the other side, which are accumulated as space charges $Q_D$ by the depletion layer. Therefore, a capacitance of the depletion region in the semiconductor is measured by these charges, and a relationship of the capacitance and DC voltage is obtained. The Schottky-barrier height and doping concentration can be calculated by the measurement data.

![Figure 2.16 Schematic measuring circuit of C-V characteristics.](image)
Chapter 3  Characterization Method

3.1 Current Density-Voltage Characteristics and Current-Transport Processes of Schottky-Barrier Diode

3.1.1 Shockley Diode Equation
3.1.2 Thermionic-Emission Theory
3.1.3 Image-Force Effect and Schottky-Barrier Lowering
3.1.4 Thermionic-Emission-Diffusion Theory

3.2 Capacitance-Voltage Characteristics of Schottky-Barrier Diode

3.3 Circumference current

3.3 Measurement of Schottky-Diode Characteristics
3.3.1 Activation-Energy Characteristics by Arrhenius Plot
3.3.2 Current-Voltage Characteristics of Schottky Diode and Theoretical Curves Fitting
3.3.3 Capacitance-Voltage Characteristics of Schottky Diode
3.1 Current Density-Voltage Characteristics and Current-Transport Processes of Schottky-Barrier Diode

In this experiment, $I$-$V$ (current-voltage) characteristics were measured as electrical characteristics. However, it is useful that $J$-$V$ (current density-voltage) characteristics are used for the characterization. Consequently, the measurement current was standardized by the areas of anode electrodes, and the theoretical formulas were applied for analyzing $J$-$V$ data by using theory shown in this section. Basically, because Schottky-barrier diode is unipolar device, in which the majority carriers (electrons) are injected into the conduction band on the semiconductor side, the current-transport processes of free electron are discussed on the conduction band mainly.

3.1.1 Shockley Diode Equation

The ideal current-voltage characteristics of diode, including p-n junction diode, Schottky diode, and other diodes, are given by Shockley diode equation:\[15\]

$$I = I_s \exp \left\{ \left( \frac{qV}{nkT} \right) - 1 \right\} \quad (3.1)$$

Where $I$ is the current of diode, $I_s$ is the reverse bias saturation current which is referred in Section 3.1.2, $q$ is elementary electric charge, $V$ is the bias voltage applied to the diode, $n$ is an ideal factor of diode, $k$ is Boltzmann constant, $T$ is the measuring temperature. The representations of diode’s characteristics by this equation have two states: the current flow grows exponentially in the forward-bias region, and drop in the reverse-bias region. The ideal examples of current-voltage characteristics are shown by Figure 3.1, including the linear and logarithmic scales of the absolute value and the magnitude of current respectively. The characteristic of those is divided into reverse-bias region and forward-bias region by variable voltages.

Equation (3.1) has a diode factor $n$ which expresses a characteristic of a diode, and $n$
usually is in the range of 2 from 1. The $n$-factor of an ideal diode has the value of 1. However, when the ohmic characteristic, in which the current is proportional to the voltage by following Ohm's law, is provided in place of the diode characteristic by current-voltage measurement, the value of the $n$-factor also increases; that is, the $n$-factor shows the ideality as a diode. Moreover, the $n$-factor means that there is the more or less of the quantity of the current-transport by tunneling in a diode, which is shown in the following subsections.

Figure 3.1 Schematic example of current-voltage characteristics of Schottky diode.
### 3.1.2 Thermionic-Emission Theory

Current transport processes of Schottky-barrier diode is described as the following theories. Reverse bias saturation current represented as \( I_s \) by the diode equation (3.1) is not a constant value, but a function which is changed by the structure and materials of diode. The function may be varied by others causes. There are some theories to define reverse-bias-saturation current and current transport process precisely. Figure 3.2 shows the schematic band diagrams of representative current transport processes: Thermionic Emission (TE), for typical Schottky diodes, is a theory considering electrons which passes over the barrier, Thermionic-Field Emission (TFE) is a describing way that electrons can tunnel the conduction band but cannot surmount the potential energy of the barrier, and Field Emission (FE) refers to a phenomenon that the tunneling electrons arise around the conduction-band edge for explaining ohmic contact.\(^{[14]}\) Consequently, TFE and FE are important theories of metal/semiconductor contacts where the semiconductor has a high doping concentration. When Schottky diodes are considered, the TE is the dominant process of current transportation because the semiconductor of such diodes has the low doping concentration and therefore the thick depletion layer.\(^{[17]}\) Especially, two kinds of theories about a current-transport modeling were considered for the characterization in this study.

In the thermionic-emission (TE) theory, the saturation-current density \( J_{TE} \) which is corresponding to \( J_s \) is shown by following:\(^{[16]}\)

\[
J_{TE} = A^* T^2 \exp \left( -\frac{q \phi_{Bn}}{kT} \right) \tag{3.2}
\]

Where \( A^* \) is an effective Richardson constant, \( \phi_{Bn} \) is a Schottky-barrier height for \( n \)-type substrate. Effective Richardson constant, shown by equation (3.2), is a coefficient of the saturation-current density, which does not concern the effects of optical-phonon
scattering and quantum mechanical reflection in the TE theory. \[^{[16],[17]}\]

\[
A^* = \frac{4\pi q m^* k^2}{\hbar^3}
\]  
(3.3)

Where \(h\) is Planck constant, and \(m^*\) is an effective-electron mass. For free electrons, \(m^*\) changes \(m_0\), and the calculated Richardson constant is:

\[
A = \frac{4\pi q m_0 k^2}{\hbar^3} = 120.17 \text{ [A/cm}^2/\text{K}^2]\n\]  
(3.4)

Note that this value can be applied to only free electrons, but not to semiconductors having a crystal structure. Effective Richardson constants of semiconductors has been calculated by the crystal structures, effective electron masses regarded as tensors, and a conduction band minima in various ways based on TE theory. In 4H-SiC, commonly 146 A/cm\(^2\)/K\(^2\) accepted for \(A^*\) was calculated by using following factors: \[^{[18]}\] the effective mass of 0.2\(m_0\) \[^{[19]}\] and the number of conduction band minima of 6 \[^{[20]}\] in 4H-SiC. The value of effective Richardson constant, which was provided in this way, is often used for a qualitative description of a plot of experimentally measured current data by the simple thermionic emission model in a Schottky-barrier diode.\[^{[17]}\] The effective Richardson constant is typically treated as an adjustable parameter for fitting the plot by theoretically calculated curves.\[^{[21]}\] From the TE theory, using the \(A^*\), the current \(J_F\) [A/cm\(^2\)] flowing from the semiconductor to metal under forward-biased condition \(V_F\) [V] is given by the following equation:

\[
J_F = A^* T^2 \exp \left( -\frac{q\phi_{Bn}}{n kT} \right) \exp \left( \frac{qV_F}{kT} \right)
\]  
(3.5)

On the other hand, the current \(J_R\) [A/cm\(^2\)] flowing from the metal to semiconductor under reverse-biased condition \(V_R\) [V] is given by the following equation:

\[
J_R = -A^* T^2 \exp \left( \frac{q\phi_{Bn}}{n kT} \right)
\]  
(3.6)

However, \(V_R\) is not included in this equation in spite of the reverse-biased condition.
The reason is that the Schottky barrier is ideally invariable to the applied voltage. The typical energy-band diagrams of the conduction band in these biased conditions are shown in Figure 3.3. Generally, the ideal Schottky barrier is constant despite a large reverse bias. In addition, the depletion (drift) layer widen by such bias, which also is shown in Figure 3.3. As a result, by the sum of forward current $J_F$ and reverse current $J_R$, the total current density $J_n$ is shown in the following equation: \[ J_n = J_F + J_R = A^*T^2 \exp\left(-\frac{q\phi_{BN}}{nkT}\right) \left\{ \exp\left(\frac{qV_F}{kT}\right) - 1 \right\} \]

However, this equation is improved by taking into account the effects of optical-phonon scattering and quantum mechanical reflection, such as TFE and FE. More precisely, a modified effective Richardson constant $A^{**}$ should be derived from $A^*$ in the Thermionic Emission-Diffusion theory. Note that the TE is usually enough for modeling the current transport process of Schottky diodes because the commonly accepted value of $A^*$ of 4H-SiC (146 A/cm$^2$/V$^2$) was estimated within an error of 30% in $A^*$. The error would affect the value of Schottky-barrier height $\phi_{BN}$ extracted from the saturation current measurements of about 1% in the TE. Therefore, it may adequately be possible to use this $A^*$ as a fitting parameter when the measurements are accurately required in a plotted data.
Figure 3.2 Schematic energy-band diagram of a Schottky-barrier diode illustrating the current transport processes in thermal equilibrium state (TE, TFE, and FE).

Figure 3.3 Schematic conduction-band diagrams of a Schottky diode in different biased condition (a) Thermal equilibrium state, (b) Forward-biased condition, and (c) Reverse-biased condition.
3.1.3 Image-Force Effect and Schottky-Barrier Lowering

The Schottky-barrier lowering is induced by the image-force effect, which is represented for the barrier-energy lowering for carrier emission in an electric field.\textsuperscript{[16]} In a metal-vacuum system shown in Figure 3.4, an electron needs to gain the minimum energy (the work function $q\phi_m$) to move in vacuum level from the Fermi level. When the electron positions at a distance $x$ from the metal, a positive charge can be induced on the surface of the metal. The attractive force between the electron and the induced positive charge equals to the force between the electron at the distance $x$ and an equal positive charge at a distance $-x$. The positive charge represents the image charge, and the attractive force is called the image force $F$. The equation of the force between the electron and the positive charge is given by the Coulomb's law in the electromagnetics:

$$F = -\frac{q^2}{4\pi\varepsilon(2x)^2} = -\frac{q^2}{16\pi\varepsilon x^2}$$

(3.8)

The amount of the energy worked by the electron in the course of its transfer from infinity to $x$ is shown below:

$$q\phi(x) = \int_{\infty}^{x} Fdx = -\frac{q^2}{16\pi\varepsilon x}$$

(3.9)

This energy shows the potential energy of the electron at a distance $x$ from the metal surface. When an external electric field is applied in the $-x$ direction, the total potential energy which is a function of the distance is given by the sum of this energy equation.

$$q\phi_{total}(x) = -\frac{q^2}{16\pi\varepsilon x} - q|E|x$$

(3.10)

The image-force-barrier lowering $\Delta\phi_B$, which is the maximum value of this equation, and the lowering point $x_m$ are calculated by the condition of $\frac{d(q\phi_{total})}{dx} = 0$.

$$x_m = \sqrt{\frac{q}{16\pi\varepsilon |E|}}$$

(3.11)
Because the metal-vacuum system is considered in this subsection, the dielectric constant $\varepsilon$ is equivalent to the permittivity of free space $\varepsilon_0$. Consequently, when a metal-semiconductor or metal-insulator (e.g. silicon dioxide) system is considered, the permittivity should be replaced by a relative permittivity of the material. Especially, in the metal-semiconductor contact (called a Schottky contact), the field exists without bias as result of a built-in potential energy $q\psi_{bi}$.

$$q\psi_{bi} = q\phi_{Bn0} - q\phi_n$$ \hspace{1cm} (3.13)

The electric field of the semiconductor is not constant with the distance due to this potential in a practical Schottky-barrier diode. Therefore, based on the depletion approximation, the maximum value at the interface can be used with a surface potential energy $q\psi_s$ (on n-type substrate):

$$q\psi_s = q\psi_{bi} - qV = q\phi_{Bn0} - q\phi_n - qV$$ \hspace{1cm} (3.14)

The electric field of the semiconductor is

$$E_m = \sqrt{\frac{2qN_D|\psi_s|}{\varepsilon}}$$ \hspace{1cm} (3.15)

This equation gives the Schottky-barrier lowering below:

$$\Delta\phi_B = \sqrt{\frac{qE_m}{4\pi\varepsilon}} = \left[\frac{q^2N_D|\psi_s|}{8\pi^2\varepsilon^3}\right]^{\frac{1}{2}}$$ \hspace{1cm} (3.16)

As a result, the precise Schottky-barrier height (a potential energy) is:
In a reverse bias condition, the Schottky-barrier height is slightly smaller than that in the thermal equilibrium state. Furthermore, the Schottky-barrier height is slightly larger in a forward bias condition.

In this study, the effective Schottky-barrier lowering of metal/SiC Schottky junction was calculated as follows. First of all, the differences of the potential energy between the Fermi level $E_f$ and the intrinsic Fermi level $E_i$ were calculated by using the following values of 4H-SiC: the bandgap energy $E_g = 3.26$ [eV], the dielectric constant $\varepsilon = 8.5\times10^{-13}$ [F/cm] (i.e. $\varepsilon = \varepsilon_0 \varepsilon_r$), and the intrinsic carrier density $n_i = 8.2\times10^9$ [cm$^3$]. \[24\] In addition, the $n$-type carrier density of the 4H-SiC substrates used in this study is $N_D = 1.0\times10^{16}$ [cm$^3$] in the epitaxial layer. Consequently, the differences between the Fermi level and the intrinsic Fermi level are given by the following equation:

$$\frac{E_f - E_i}{q} = \frac{kT}{q} \ln \frac{N_D}{n_i} \quad (3.18)$$

Then, the differences of the potential energy between the conductance band $E_C$ and Fermi level $E_f$ were obtained by the following equation:

$$q\phi_n = E_C - E_f = \frac{E_g}{2} - (E_f - E_i) \quad (3.19)$$

Second, the built-in potential was calculated as:

$$q\psi_{bi} = q\phi_B - q\phi_n \quad (3.20)$$

Therefore, the surface potential energy was given by the following equation:

$$q\psi_s = q\psi_{bi} - qV \quad (3.21)$$

Finally, the electric field and the barrier lowering were described as:

$$q\phi_{Bn} = q\phi_{Bn0} - q\Delta \phi_B \quad (3.17)$$
As a result, the amount of the Schottky-barrier lowering was obtained by the following equation:

\[ E_m = \sqrt{\frac{2qN_D|\psi_s|}{\varepsilon}} \]  

Furthermore, the actual Schottky-barrier height was given by:

\[ \Delta \phi_B = \frac{qE_m}{4\pi\varepsilon} = \left[ \frac{q^3N_D|\psi_s|}{8\pi^2\varepsilon^3} \right]^{\frac{1}{2}} \]  

Therefore, the Schottky-barrier height can be recursively calculated and the barrier-lowering effect also is changeable by the applied voltage. The lowering effect of the Schottky barrier described by these equations was included in the calculation of the theoretical current-voltage characteristics (the diode equation) in the evaluations of the experimental data.

In addition, using the above equations and invariables, the depletion-layer width \( W_D \) of the Schottky junction also can be approximately calculated by the following equation:

\[ W_D = \sqrt{\frac{2\varepsilon(\psi_{bi} - V)}{qN_D}} = \sqrt{\frac{2\varepsilon|\psi_s|}{qN_D}} \]  

Where this equation can be given by the approximation of the depletion-layer width of the p-n junction; in the metal/semiconductor junction, the acceptor donor concentration of is virtually much higher than the donor concentration \( (N_D \ll N_A) \) for the n-type substrate, which is shown in the following equation:
\[ W_D = \sqrt{\frac{2\epsilon(N_D + N_A)}{qN_D N_A}} |\psi_s| = \sqrt{\frac{2\epsilon N_D}{qN_D N_A}} |\psi_s| \rightarrow N_A \rightarrow N_A - \infty \Rightarrow \sqrt{\frac{2\epsilon}{qN_D}} |\psi_s| \]  

(3.26)

Note that the equations argued in this subsection, such as the carrier density and the Schottky-barrier height, can also be applied for a capacitance-voltage measurement and its analysis.

Figure 3.4 Schematic energy-band diagram of a metal-vacuum system with the barrier lowering. The lowering is combined effects of the electric field and the image force.

3.1.4 Thermionic-Emission-Diffusion Theory

Thermionic-Emission-Diffusion theory (TED) is a modified theory of TE model, which includes a part of quantum-mechanical reflection and transmission described in a new effective Richardson constant.\[22\] The first quantum mechanisms of electron transport at a metal/semiconductor structure were introduced by C. R. Crowell and S. M. Sze in 1966.\[25\] A significant modification was that the effective Richardson constant \(A^*\) was replaced by \(A^{**}\) which is a revised factor of the constant. In this subsection, the process of \(A^{**}\) establishment is concisely introduced.
The TED consolidates the thermionic emission and diffusion theory shown following. The diffusion theory, which expresses the current in the depletion region depending on the local field and the concentration gradient, uses the current density equation: \[ J(x,n) = J_x = J_n = q \left( \mu_n E + D_n \frac{dn}{dx} \right) \] (3.27)

Where this \( n \) represents for the concentration of the semiconductor, \( \mu_n \) is the electron mobility, this \( E \) represents for the electric field, \( D_n \) is the diffusion constant, and \( x \) is the distribution in the direction of the semiconductor. Then, the following equation known as the Einstein relation is used:

\[ D_n = \frac{kT}{q} \mu_n \] (3.28)

Moreover, the equation (3.27) changed:

\[ J(x,n) = J_x = J_n = qD_n \left( \frac{n}{kT} \frac{dE_C}{dx} + \frac{dn}{dx} \right) \] (3.29)

In the steady-state condition, equation (3.29) can be integrated by using the following integrated factor.

\[ J_n \int_0^{wp} \exp \left[ \frac{E_C(x)}{kT} \right] dx = q D_n \left\{ n(x) \exp \left[ \frac{E_C(x)}{kT} \right] \right\} \bigg|_0^{wp} \] (3.30)

From the two boundary conditions, \( x=0 \) and \( x=WD \), the following equations are obtained:

\[ E_C(0) = q\phi_{Bn} \] (3.31)

\[ E_C(WD) = q(\phi_n + V) \] (3.32)

\[ n(0) = n(WD) = N_C \exp(-q\phi_{Bn}) \] (3.33)
\[ n(W_D) = N_C \exp(-q\phi_n) \] (3.34)

Where \( N_C \) is effective density of states in conduction band, \( \phi_n \) is Fermi potential from conduction-band edge; \((E_C-E_F)/q\).

Using these equations, the equation (3.30) can be changed:

\[ J_n = qN_CD \left\{ \exp\left(\frac{qV}{kT}\right) - 1 \right\} \int_0^{W_D} \exp\left[ \frac{E_C(x)}{kT} \right] dx \] (3.35)

The conduction-band energy is given by the following equation:

\[ E_C(x) = q\phi_{BN} - \frac{q^2 N_D}{\varepsilon} \left( W_D x - \frac{x^2}{2} \right) \] (3.36)

The equation (3.35) and (3.36) can be integrated bellow:

\[ J_n \approx \frac{q^2 N_C D_n}{kT} \sqrt{2qN_D \left( \phi_{bi} - V \right)} \exp\left( -\frac{q\phi_{BN}}{kT} \right) \left[ \exp\left( \frac{qV}{kT} \right) - 1 \right] \] (3.37)

\[ = J_D \left[ \exp\left( \frac{qV}{kT} \right) - 1 \right] \]

Where \( J_D \) is the saturation-current density of the diffusion theory, \( \psi_{bi} \) represents for the built-in potential:

\[ \psi_{bi} = q\phi_{BN} - E_C = q\phi_{BN} - (q\phi_n + qV) \] (3.38)

Both of the thermionic emission theory and the diffusion theory finally arrive at a similar expression, which may be represented as the Shockley’s diode equation. However, the saturation-current density of the diffusion theory \( J_D \) depends on the applied voltage \( V \), and it is less sensitive to temperature \( T \) in comparison with that of the thermionic emission theory \( J_{TE} \).

A theory on the synthesis of the above theories is the thermionic-emission-diffusion theory.\(^{[25]}\) It takes into account the improved boundary conditions: a thermionic recombination velocity \( v_R \) near the metal/semiconductor interface and an effective diffusion velocity \( v_D \). Since there are diffusion electrons on the conduction band \( E_C \), the
Fermi level is greatly bent in the depletion region through which the diffusion occurs. In the thermionic-emission-diffusion theory, the electron on the conduction band $E_C(x)$ which is a function of the electron potential energy at distance $x$ is considered under the barrier-lowering effect, which is shown in Figure 3.6. Assumptions in this theory are: the Schottky-barrier height is large enough, and a depletion approximation is available between the metal surface and the depletion width $x=W_D$. When there is the applied voltage $V$ between the metal and semiconductor bulk, a flow of electrons toward the metal from the semiconductor is increased. A quasi-Fermi level $E_{Fn}(x)$ which is a pseudo-Fermi level of a band bending for expressing the variable concentration in the semiconductor is also a function of distance $x$. The electron current density between $x_m$ and $W_D$ is given by the following equation:

$$J_{(x,n)} = n\mu_n \frac{dE_{Fn}}{dx}$$  \hspace{1cm} (3.39)

Where the fixed electron density $n$ in Maxwell-Boltzmann distribution is given by the following equation:

$$n = N_C \exp\left(-\frac{E_C - E_{Fn}}{kT}\right)$$  \hspace{1cm} (3.40)

As the quasi-Fermi level is considered, the temperature $T$ is equivalent to the lattice temperature and the region of the Schottky junction is isothermal between $x_m$ and $W_D$. The electron on the barrier between the interface and $x_m$ flows as a sink. The current flow can be described by using the thermionic (effective) recombination velocity $v_R$ at the position $x_m$ of the maximum potential energy:

$$J = q(n_m - n_0)v_R$$  \hspace{1cm} (3.41)

Where $n_m$ is the electron density at $x_m$, and $n_0$ is a quasi-equilibrium electron density at $x_m$. When the current is flowing, the electron density $n_m$ at $x_m$ is given by the following
equation:

\[ n_m = N_C \exp \left( - \frac{E_C(x_m) - E_{Fn}(x_m)}{kT} \right) = N_C \exp \left( - \frac{q\Phi_{Bn} - E_{Fn}(x_m)}{kT} \right) \tag{3.42} \]

When the potential energy of the metal equals to the maximum potential energy under the equilibrium condition, i.e. \( E_{Fm} = E_{Fn}(x_m) \), the quasi-equilibrium electron density is given by the following equation:

\[ n_0 = N_C \exp \left( - \frac{q\Phi_{Bn}}{kT} \right) \tag{3.43} \]

In this equation, it is assumed that the magnitude or the position of the potential energy maximum is not varied. Taking into account a boundary condition, \( E_{Fm} = 0 \) as reference, the quasi-Fermi level equals to the Fermi level of the semiconductor bulk and the potential energy by the applied voltage at a terminal of the depletion region \( W_D \):

\[ E_{Fn}(W_D) = E_F = qV \tag{3.44} \]

From the equations of the electron current density and the fixed electron density, \( n \) can be eliminated, and the result of integrating \( E_{Fn} \) from \( x_m \) to \( W_D \) is given as:

\[ \exp \left( \frac{E_{Fn}(x_m)}{kT} \right) - \exp \left( \frac{qV}{kT} \right) = - \frac{J}{\mu_n N_C kT} \int_{x_m}^{W_D} \exp \left( \frac{E_C}{kT} \right) dx \tag{3.45} \]

From this equation and the current flow equation using the effective recombination velocity \( v_R \), the distribution of \( E_{Fn}(x_m) \) can be solved as:

\[ \exp \left( \frac{E_{Fn}(x_m)}{kT} \right) = \frac{v_D \exp \left( \frac{qV}{kT} \right) + v_R}{v_D + v_R} \tag{3.46} \]

Where \( v_D \) is an effective diffusion velocity related with the diffusion of electrons between \( x_m \) and \( W_D \). The equation of the effective diffusion velocity is given by:

\[ v_D = D_n \exp \left( \frac{q\Phi_{Bn}}{kT} \right) / \int_{x_m}^{W_D} \exp \left( \frac{E_C}{kT} \right) dx \tag{3.47} \]

Where \( D_n \) is a diffusion constant of the semiconductor. By using above equations, the current density equation in the thermionic-emission-diffusion theory is given by the
following equation:

\[ J_{TED} = \frac{qN_c v_R}{1 + \frac{v_R}{v_D}} \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \]  

(3.48)

In this equation, the relative values of \( v_R \) and \( v_D \) contribute to a trend of the current; that is, if \( v_D \) is much larger than \( v_R \) (\( v_R \ll v_D \)), the thermionic emission dominates the current-transport process \( (J_{TED} = J_{TE}) \), and if \( v_R \) is much larger than \( v_D \) (\( v_R \gg v_D \)), the diffusion dominates the process. Moreover, when other disturbances and the quantum-mechanisms are considered, the probability of electron emission crossing the energy potential maximum given by the following equation:

\[ f_p = \exp\left(-\frac{x_m}{\lambda}\right) \]  

(3.49)

Where \( \lambda \) is the wave length of electron optical-phonon scattering. In addition, \( f_Q \) expresses a ratio of the quantum-mechanical tunneling and reflection depending on the electric field and electron energy. The complete equation of the \( J-V \) characteristics accommodating these parameters is expressed by: [16]

\[ J = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \left[\exp\left(\frac{qV}{kT}\right) - 1\right] \]  

(3.50)

Where \( A^{**} \) is the effective Richardson constant, which is completely different from \( A^* \) by the thermionic-emission theory, and the equation is given by:

\[ A^{**} = \frac{f_p f_Q A^*}{1 + \frac{f_p f_Q v_R}{v_D}} \]  

(3.51)

Moreover, when the reverse bias is large enough, the equation of the reverse-saturation current is:

\[ J_s = A^{**}T^2 \exp\left(-\frac{q\phi_{Bn}}{kT}\right) \]  

(3.52)

In the end, it is the most important thing that these effects by TED theory are reflected
in the reduction of the effective Richardson constant (from $A^*$ to $A^{**}$), and the reduction is by as much as 50%. For example, $A^*$ of $n$-type silicon is approximately $240 \text{ A/cm}^2/\text{K}^2$, but $A^{**}$ of that is $110 \text{ A/cm}^2/\text{K}^2$ in the electric field range $10^4$ to $10^5 \text{ V/cm}$. Note that the effective Richardson constant $A^*$ by TE is often available for many investigation of the Schottky diode characteristics as a fitting parameter of $J-V$ characteristics. The effective Richardson constant $A^{**}$ by TED, however, is also important to evaluate the Schottky-barrier height precisely and to study the detailed mechanism of the Schottky-barrier junction.

![Thermionic emission and Diffusion](image)

**Figure 3.5** Schematic energy band diagram of the Schottky-barrier junction in the thermionic-emission and diffusion theory.

![Energy band diagram](image)

**Figure 3.6** Energy band diagram of the Schottky-barrier junction in the thermionic-emission-diffusion theory with the barrier lowering.
3.2 Capacitance-Voltage Characteristics of Schottky-Barrier Diode

In this study, the capacitance-voltage measurement was additionally conducted for the SiC Schottky diode with TiC electrode. From the capacitance-voltage measurement, a \( I/C^2-V \) characteristic is obtained. Moreover, the built-in potential \( \psi_{bi} \) can be obtained by an intercept and the doping concentration (the \( n \)-type carrier density) \( N_D \) can be given by a slope in the \( I/C^2-V \) characteristic. Therefore, the Schottky-barrier height can be directly calculated by the following equations: \(^{[26],[27]}\)

The depletion-layer width \( W_D \) of the Schottky junction at the metal/semiconductor interface is given by:

\[
W_D = \sqrt{\frac{2\varepsilon(\psi_{bi} - V)}{qN_D}} \quad (3.53)
\]

Then, the space charge of the \( n \)-type semiconductor is given by the following equation:

\[
Q_D = qN_D W_D = \sqrt{2q\varepsilon N_D (\psi_{bi} - V)} \quad (3.54)
\]

Because there are not any charges in the depletion region (the depletion layer approximation), the junction capacitance \( C \) formed in the interface by the depletion layer is given by the equation of a capacitor:

\[
C = \frac{\varepsilon}{W_D} = \sqrt{\frac{q\varepsilon N_D}{2(\psi_{bi} - V)}} \quad (3.55)
\]

Then, \( I/C^2-V \) characteristics is calculated by:

\[
\frac{1}{C^2} = \frac{2(\psi_{bi} - V)}{q\varepsilon N_D} \quad (3.56)
\]
As a result, the built-in potential $\psi_{bi}$ can be obtained by an intercept and the doping concentration because $1/C^2$ is a function of the voltage. In addition, the Schottky-barrier height can be calculated by the following equations. The differences between the Fermi level and the intrinsic Fermi level are given by:

$$\frac{E_f - E_i}{q} = \frac{kT}{q} \ln \frac{N_D}{n_i}$$  \hspace{1cm} (3.57)

Then, the differences of the potential energy between the conductance band $E_C$ and Fermi level $E_f$ were obtained by:

$$q\phi_n = E_C - E_f = \frac{E_g}{2} - (E_f - E_i)$$  \hspace{1cm} (3.58)

Furthermore, the built-in potential is:

$$q\psi_{bi} = q\phi_{Bn} - q\phi_n$$  \hspace{1cm} (3.59)

Therefore, the Schottky-barrier height can be calculated by the capacitance-voltage characteristics, and the equation of the Schottky-barrier height is given by:

$$\phi_{Bn} = \psi_{bi} + \phi_n = \psi_{bi} + \frac{E_g}{2q} - \frac{kT}{q} \ln \frac{N_D}{n_i}$$  \hspace{1cm} (3.60)

As the capacitance-voltage measurement can give the Schottky-barrier height by only the calculation, this evaluation method is widely used for the various Schottky diodes.
3.3 Circumference Current

Circumference current is defined as the current of surrounding areas of anode electrodes in this study, and electric current density is defined as below:

\[ I = \int \vec{J} \cdot d\vec{A} \]  \hspace{1cm} (3.61)

Where \( I \) is current, \( \vec{J} \) is the current density, and \( d\vec{A} \) is the differential area of cross-sectional vector. In vertical semiconductor device like Schottky diode, the current density equation is varied:

\[ I = jA + I_c \propto A \]  \hspace{1cm} (3.62)

Where \( A \) is the area of the electrode of Schottky diode and \( I_c \) is the circumference current. Therefore, the current of Schottky diode must be proportional to the electrode area; that is, if the area is zero in the plot of current-area characteristics, it is necessary that the circumference current is zero because the current is also equal to zero in theory. For example, Figure 3.7 shows examples of plots of current \( I \) versus electrode area \( A \) at the same voltage by measuring \( I-V \) characteristics in some areas. Whereas the current of theoretical example is terminated to zero, that of not theoretical example has an intercept by regression analysis. It means that there is the current flowed by reaction or other causes at the circumference of the metal-semiconductor interface, which is irrelevant to the electrode area. Alternatively, the reason may be that the reaction speed is different between the center of the electrode and the edge part which is contacting not only the semiconductor but also the passivation layer of SiO\(_2\), which is described in Figure 3.8.
Figure 3.7 Schematic examples of current-electrode area characteristics.

Figure 3.8 Schematic cross section structure and the surface of the Schottky contact show the electrode circumference with SiO$_2$ device isolation.
3.4 Measurement of Schottky-Diode Characteristics

In this study, Schottky-diode characteristics, such as effective Richardson constant $A^{**}$, $n$-factor, and Schottky-barrier height, were measured by two ways:

1) Activation-energy characteristics are given by Arrhenius plot which is taken by $I$-$V$ measurement in various measuring temperatures.

2) Schottky diode characteristics are given by fitting the theoretical curves on $J$-$V$ characteristics which is taken by $I$-$V$ measurement.

3.3.1 Activation-Energy Characteristics by Arrhenius Plot

The activation-energy method can determine the Schottky-barrier height without assumption of electrically active area.$^{[27]}$ When an unusual metal-semiconductor interface is used for the Schottky junction, this method is important for the investigation of the interface. The reason is that an electrically active area can be restricted to only a fraction of the geometric interface area reacted incompletely. In contrast, a rough nonplanar interface of the metal-semiconductor can be led by a metallurgical reaction with the electrically active area. When the reverse bias is large enough, the equation of the current density $J$ (which was shown in Section 3.1.4) can be approximated as the reverse-saturation-current density $J_s$:

$$J_s = A^{**} T^2 \exp \left( \frac{q(\Phi_{Bn} - \Delta \Phi_B)}{kT} \right) \quad (3.63)$$

Then, this equation can be varied by taking logarithm:

$$\ln \left( \frac{J_s}{T^2} \right) = \ln(A^{**}) - \frac{q(\Phi_{Bn} - \Delta \Phi_B)}{kT} \quad (3.64)$$

Where $q(\Phi_{Bn} - \Delta \Phi_B)$ is regarded as the activation energy. By using this equation and Arrhenius plot, the effective Richardson constant $A^{**}$ can be measured from the slope,
and the Schottky-barrier height $\phi_{Bn} - \Delta\phi_B$ can be obtained from the intercept, which are schematically shown in Figure 3.9. Therefore, the activation-energy characteristics for the Arrhenius plot are given by measuring reverse-bias current at a voltage in various measuring temperatures (i.e. $I$-$V$-$T$ characteristics); when the measuring temperature of the current-voltage characteristics is changed, the reverse-saturation-current will be also changed. It is also possible that the SiC Schottky-barrier diode whose saturation current is too small to be measured can be investigated by increasing the measuring temperature.

![Figure 3.9 Schematic characteristic of Arrhenius plot ($I$-$V$-$T$ characteristics).](image)

Figure 3.9 Schematic characteristic of Arrhenius plot ($I$-$V$-$T$ characteristics).
3.3.2 Current-Voltage Characteristics of Schottky Diode and Theoretical Curves Fitting

In this study, current-voltage characteristics given by the measurements were fitted on the theoretical curves of the Schottky-diode equation shown in Section 3.1.4. By fitting the experimental data, \( n \)-factors which express an indicator of the ideality as the diode and Schottky-barrier height \( \phi_{Bn} \) including the barrier-lowering effect which was also shown in Section 3.1.3 were obtained. The precise theoretical diode curve using those equations is given as the following equation:

\[
J = J_s \left\{ \exp \left( \frac{qV}{nkT} \right) - 1 \right\} = A^{**} T^2 \exp \left\{ \frac{q(\phi_{Bn} - \Delta \phi_B)}{kT} \right\} \left\{ \exp \left( \frac{qV}{nkT} \right) - 1 \right\} \quad (3.65)
\]

Where the experimental data of the current (i.e. Ampere [A]) were standardized at the electrode area [cm\(^2\)]; the theoretical curves used for the fitting always show the current density (i.e. Ampere per square centimeters [A/cm\(^2\)]) versus the voltage [V] characteristics. In addition, the logarithmic scale was always used in the evaluations because the reverse-saturation current could be observable. As shown in the equation, the effective Richardson constant \( A^{**} \) [A/cm\(^2\)/K\(^2\)], elementary charge \( q \) [C], the Boltzmann constant \( k \) [J/K], and the room temperature \( T \) [K] are usually the constant values given by exterior. Furthermore, the Schottky-barrier height \( \phi_{Bn} \) [eV] and the ideally factor \( n \) [a.u.] are the fitting parameters. Moreover, in order to calculate the effective Schottky-barrier lowering \( \Delta \phi_B \) [eV], the calculations shown in Section 3.1.3 were used. The schematic state on the graph, on which the fitting is conducted, is shown in Figure 3.10. In Figure 3.10, the schematic examples of the measurement data and theoretical curve were shown, and an on-resistance of the metal and semiconductor is to be found to exist. However, in the some cases, the reverse-saturation current also was too small to be measured. Therefore, the voltage for the fitting range from
approximately 0 to 1 V was used. The schematic enlarged view of this range in the fitting evaluation is shown in Figure 3.11. In this Figure, the transition of the theoretical curve by changing the fitting parameters ($\phi_{Bn}$ and $n$) was described. When the parameter of the Schottky-barrier height $\phi_{Bn}$ is changed to increasing, the theoretical curve goes down. On the other hand, when the parameter is changed to decreasing, the theoretical curve rises up. Then, in the theoretical curve, when the ideal factor $n$ (beginning at 1.00) increases, the start of the diode characteristic gets bigger incline.

For the measurements of the $J-V$ characteristics in the high measurement temperatures, the reverse-saturation current would be measurable, so the voltage for the fitting range from approximately -1.0 V to 0.2 V was used. The schematic diagram of this fitting measurement is shown in Figure 3.12. When the measuring temperature is high, the reverse-saturation current increases and it is possible to measure the current.

![Schematic graph of $J-V$ characteristics for the fitting evaluation. Example of measurement data with on-resistance and example of theoretical curve are shown.](image)

**Figure 3.10** Schematic graph of $J-V$ characteristics for the fitting evaluation. Example of measurement data with on-resistance and example of theoretical curve are shown.
Figure 3.11 Schematic enlarged view of the fitting-evaluation example.

Figure 3.12 Schematic diagram of the fitting-evaluation example of $J-V$ characteristics in the various measurement temperatures.
3.3.3 Capacitance-Voltage Characteristics of Schottky Diode

In this study, capacitance-voltage measurement was additionally conducted for the SiC Schottky diode with TiC electrode in addition to current-voltage measurements. Furthermore, the Schottky-barrier height could also be obtained from this measurement and its capacitance-voltage characteristics. In capacitance-voltage measurement, the depletion region or the depletion state of the Schottky-barrier diode are usually used for the analysis of the Schottky-barrier height, the doping concentration, and depletion-layer width. \[26\], \[27\]

In the C-V characteristics analysis of the Schottky diode, the depletion region or state in the reverse bias can be used. The reason is that the diffusion capacitance of the neutral region of the substrate rapidly increases larger than the junction capacitance of the depletion region in the forward bias. Therefore, the bias voltage from -1 to 0 V was used for the evaluation of the C-V characteristics in this study, and the frequency of the small AC signal for the analysis was 100 kHz. The schematic C-V characteristic in the rage of this voltage is shown in Figure 3.13. The measured capacitance was standardized in the electrode area. Then, \(1/C^2-V\) characteristics was obtained, which is schematically shown in Figure 3.14. The doping density was obtained by the slope of the characteristics, and the built-in potential was measured by the intercept of the approximation line. \[26\], \[28\] Note that, in this study, the capacitance in the forward bias was omitted on purpose because of including not only the junction capacitance but also the diffusion capacitance.
Figure 3.13 Schematic $C-V$ characteristics of Schottky diode in the range of voltage for depletion state.

Figure 3.14 Schematic $1/C^2-V$ characteristics of Schottky diode in the range of voltage for depletion state. Dotted approximation line connects with the intercept of the built-in potential.
Chapter 4  Characteristics

4.1 Schottky-Diode Characteristics of TiC Electrode on SiC Substrate in Various Measuring Temperatures
   4.1.1 J-V Characteristics in Various Measuring Temperatures
   4.1.2 Evaluations of Effective Richardson Constant and Schottky-Barrier Height from Activation-Energy Characteristics by Arrhenius Plot
   4.1.3 Evaluation of n-Factors in Various Measuring Temperatures by Fitting J-V Characteristics

4.2 Schottky-Diode Characteristics of Ti, TiC, and TiSi₂ Electrodes on SiC Substrates in Various Annealing Temperatures
   4.2.1 J-V Characteristics in Various Annealing Temperatures
   4.2.2 Evaluations of Schottky-Barrier Height and n-Factors by Fitting J-V Characteristics in Various Annealing Temperatures
   4.2.3 Current-Electrode Area Characteristics in Various Annealing Temperatures

4.3 Power Loss of Schottky-Barrier Diodes
   4.3.1 Specific On-Resistances of Schottky-Barrier Diodes
   4.3.2 Calculated Power Loss of Schottky-Barrier Diodes
4.4 Capacitance-Voltage Characteristics of SiC Schottky Diode with TiC Electrode in Various Annealing Temperatures

4.3.1 Reproduced $J-V$ Characteristics of TiC/SiC Schottky Diode in Various Annealing Temperatures

4.3.2 $C-V$ Characteristics of TiC/SiC Schottky Diode in Various Annealing Temperatures
4.1 Schottky-Diode Characteristics of TiC Electrode on SiC Substrate in Various Measuring Temperatures

In order to decide the effective Richardson constant, current-voltage characteristics were measured in various measuring temperatures. The sample of SiC Schottky diode of TiC anode electrode was used for this measurement after the annealing at 500℃. The structure of the device is shown in Figure 4.1, and the Ti-carbide process is also shown in Figure 4.2. The SiC wafers used in this experiment were 4H-SiC (0001) Si-face of n-type with the doping density of $N_D = 1.0 \times 10^{16} \, \text{cm}^{-3}$. The Ti-carbide was formed by annealing of the metal layers of Ti and C.

![Cross section structure of Schottky diode of TiC electrode.](image)

Figure 4.1 Cross section structure of Schottky diode of TiC electrode.
Figure 4.2 Sintering process for forming Ti-carbide by annealing.
4.1.1 J-V Characteristics in Various Measuring Temperatures

J-V characteristics in various measuring temperatures are shown in Figure 4.3 in the range of 0.2 V from -1.0 V, and it is realized that the reverse-bias-saturation current was increased by the temperature increase. The measuring temperatures were: 23 (room temperature), 40, 60, 80, 100, and 120°C. However, the measurements of the room temperature and 40°C were eliminated in Figure 4.3 because the reverse-bias-saturation current could not be measured for too small current. Moreover, these currents were too small to use making the activation-energy characteristics by Arrhenius plot. Figure 4.3 includes the J-V characteristics and the theoretical fitting curves which are overlaying the experimental values respectively.

![Figure 4.3](image)

**Figure 4.3** J-V characteristics in various measuring temperatures (TiC/SiC Schottky diode with 500°C annealing for 1 minute in N₂).
4.1.2 Evaluations of Effective Richardson Constant and Schottky-Barrier Height from Activation-Energy Characteristics by Arrhenius Plot

Effective Richardson constant $A^{**}$ shown in Section 3.1.4 could be extracted from the intercept by Arrhenius plot of activation-energy characteristics shown in Section 3.3.1. Under large reverse biased condition, reverse bias saturation-current density $J_s$ is approximating to current density $J$ which is measured. Therefore, in the range from -20 mV to -1 V, the activation-energy characteristics were obtained by Arrhenius plot, and it is shown in Figure 4.4. As a result, the value of $A^{**}$ of 4H-SiC used in this study was determined from the intercept, and $A^{**}$ was 129 A/cm$^2$/K$^2$ at -1.0 V. It is considered that this value has good agreement with the theoretical (TE model) value of 4H-SiC (146 A/cm$^2$/K$^2$, shown in Section 3.1.2). [2]

In addition, Schottky-barrier height of SiC with TiC electrode was also extracted from the slope, and the value was 0.956 eV at -1.0 V. It is important to pay careful attention that this value includes the barrier lowering effect by image-force lowering; while the net barrier height of $\phi_{Bn} - \Delta \phi_B$ was obtained by this characteristics, it was not the just value of the barrier height of $\phi_{Bn}$.

Thus, it is possible to say that the difference of the effective-Richardson constants $A^*$ and $A^{**}$ of 4H-SiC is not large as that of Si ($A^{**}$ of Si is about a half of its $A^*$). However, using the measured effective-Richardson constant, the $I-V$ characteristics of Schottky diode may be evaluated for measuring Schottky-barrier height and $n$-factor in addition to the activation-energy method. For example, a similar result for the effective-Richardson constant $A^{**}$ of 4H-SiC substrate by the activation-energy characteristics, shown as “the temperature-dependent $I-V$ characteristics”, was also reported in the referenced paper. [29] In the paper, the effective-Richardson constant was
measured as $A^{**} = 129.95 \text{ [A/cm}^2/\text{K}^2\text{]}$.

**Figure 4.4** Activation-energy characteristics of SiC Schottky diode with TiC electrode by Arrhenius plot (TiC/SiC Schottky diode with 500°C annealing for 1 minute in N₂).
4.1.3 Evaluation of $n$-Factors in Various Measuring Temperatures by Fitting $J$-$V$ Characteristics

The $n$-factors of SiC with TiC electrode were extracted in the various measuring temperatures by fitting the theoretical $J$-$V$ characteristics to the experimental values. The detailed way was shown in Section 3.3.2, and the measured value 129 A/cm$^2$/K$^2$ was used for the effective Richardson constant $A^\ast$ of 4H-SiC in this theoretical calculation. Table 4.1 shows the extracted $n$-factors in various measuring temperatures. In most of the measuring temperatures, the values of the $n$-factors were under 1.1 and approached 1.0. Therefore, it is possible that the $J$-$V$ characteristics of these Schottky diodes are expressed with the theoretical models of diode. In addition, the Schottky-barrier height (about 995 eV) of SiC with TiC electrode was also extracted by fitting theoretical curves on the plots, but even if the measuring temperature changes, the value of $\phi_{Bn}$ is still constant approximately. Table 4.1 includes those in 23 (room temperature), 40 degree Celsius, which could be fitted by theoretical curves in the range from 0 to 0.3 V approximately.

<table>
<thead>
<tr>
<th>Measuring temperature ($^\circ$C)</th>
<th>$n$-factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>1.04</td>
</tr>
<tr>
<td>40</td>
<td>1.05</td>
</tr>
<tr>
<td>60</td>
<td>1.09</td>
</tr>
<tr>
<td>80</td>
<td>1.08</td>
</tr>
<tr>
<td>100</td>
<td>1.08</td>
</tr>
<tr>
<td>120</td>
<td>1.13</td>
</tr>
</tbody>
</table>
4.2 Schottky-Diode Characteristics of Ti, TiC, and TiSi₂ Electrodes on SiC Substrates in Various Annealing Temperatures

The SiC Schottky-barrier diodes of Ti, TiC, and TiSi₂ electrodes were fabricated and characterized in various annealing temperatures: 500, 600, 700, 750, 800, 850, 900, 950, 1000, 1050℃ for 1 minute in N₂ atmosphere. In this study, current-voltage characteristics were used for extracting the circumference current, the Schottky-barrier height \( \phi_{Bn} \), and the values of \( n \)-factor at each annealing temperature. Especially, the Schottky-barrier height \( \phi_{Bn} \) and the values of \( n \)-factor that are the most important characteristics of Schottky diode were calculated by the method shown in Section 3.3.2 in this study. As a result, the considerable differences of these characteristics were found in the SiC Schottky diodes of each electrode (Ti, TiC, and TiSi₂).

4.2.1 J-V Characteristics in Various Annealing Temperatures

In this experiment, the current-voltage characteristics as electric characteristics were measured for the characterization of Schottky-barrier diodes in various annealing temperatures. All of the annealing were conducted in N₂ atmosphere for 1 minute. Furthermore, the electric current was divided into the electric current density by the electrode area, for the characteristics of the Schottky diodes were extracted and calculated by the theoretical J-V curves. From the experiment, the J-V characteristics of the SiC Schottky diodes with each anode electrode (Ti, TiC, and TiSi₂) in various annealing temperatures were shown in Figure 4.5 (Ti), 4.6 (TiC), and 4.7 (TiSi₂), in which several annealing temperatures (from 500 to 1000 every 100℃) are expressed for making it easy to compare the transitions of the reverse electric current. In addition, one summary of these Figures is shown in Figure 4.8, for it is comprehensible to compare
the differences of these electrodes. From this result, along with the increase of the annealing temperature, the reverse current of the SiC Schottky diodes of TiC and TiSi$_2$ electrodes had the smaller increasing trend than that of Ti electrode as a reference. Especially, after the annealing of 800°C, the major increase of the reverse current was found in Ti, but was not found in TiC and TiSi$_2$; the diode characteristics of TiC and TiSi$_2$ electrodes with SiC substrates have less deterioration than those of Ti by the increasing of the annealing temperature. From these results, it is suggested that TiC and TiSi$_2$ of the metal compounds are possibly hard to react with SiC substrates under the high annealing temperature. Therefore, the SiC Schottky-barrier diodes of TiC and TiSi$_2$ electrodes had kept the rectifying characteristics in spite of the high annealing temperature. The following is a summary of the above. The SiC Schottky diode with TiC electrode obviously showed very low reverse-saturation current (i.e. low leakage current) in the high annealing temperature. Alternatively, the SiC Schottky diode with TiSi$_2$ electrode showed a restrained increase of the reverse-saturation current in comparison with that of Ti electrode in the high annealing temperature (e.g. 800°C and 900°C annealing). In some case, the reverse-saturation current could not be measured (e.g. the Ti/SiC diode characteristics in 500 and 600°C annealing). This reason was that the instrument used for current-voltage measurements cannot measure the very small current under about $10^{-13}$ A (100 fA). Therefore, the small electric current in the range of $10^{-12}$ ~ $10^{-13}$ A was observed as the noise.

In this study, the diode characteristics of the fabricated Schottky diodes of each metal were evaluated in various annealing temperatures using these $J$-$V$ characteristics in the following subsections.
Figure 4.5 J-V characteristics of SiC Schottky diodes with Ti electrode in various annealing temperatures. The reverse-saturation current was notably increased (RTA for 1 minute in N$_2$, Electrode area: 206×206 $\mu$m$^2$).

Figure 4.6 J-V characteristics of SiC Schottky diodes with TiC electrode in various annealing temperatures. The increase of the reverse-saturation current was notably restrained (RTA for 1 minute in N$_2$, Electrode area: 206×206 $\mu$m$^2$).
Figure 4.7 $J$-$V$ characteristics of SiC Schottky diodes with TiSi$_2$ electrode in various annealing temperatures. The increase of the reverse-saturation current was slightly restrained in comparison with that of Ti (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$).

Figure 4.8 Summarized $J$-$V$ characteristics of SiC Schottky diodes with (a) Ti, (b) TiC, and (c) TiSi$_2$ electrode in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$).
4.2.2 Evaluations of Schottky-Barrier Height and $n$-Factors by Fitting $J$-$V$

Characteristics in Various Annealing Temperatures

In this experiment, three $J$-$V$ characteristics of SiC Schottky diodes of Ti, TiC, and TiSi$_2$ electrodes were obtained in various annealing temperatures, so the Schottky-barrier height $\phi_{Bn}$ and the $n$-factors of each device were extracted to evaluate the diode characteristics, and these values were calculated by fitting theoretical $J$-$V$ curves on the experimental plots. The notice of the calculation is: the value of the effective Richardson constant $A^{**}$ of 4H-SiC was required for the theoretical calculation of $J$-$V$ curves, which was extracted by the activation-energy characteristics in Section 4.1.2. Consequently, the value of 129 A/cm$^2$/K$^2$ for $A^{**}$ was used for this calculation.

Figure 4.9 shows (a) Schottky-barrier height and (b) $n$-factors of SiC Schottky diodes of Ti, TiC, TiSi$_2$ electrodes in various annealing temperatures. In addition, Table 4.2 and Table 4.3 show these values. The anode-electrode area of the respective devices was 206×206 μm$^2$. As a result, the SiC Schottky diodes of TiC and TiSi$_2$ electrodes had the stable values of the Schottky-barrier height $\phi_{Bn}$ and $n$-factors to around 800℃ of the annealing temperature. On the other hand, that of Ti electrode, as a reference, was unstable and had the continuously decreasing trend. In addition, the SiC Schottky diodes of TiC and TiSi$_2$ electrodes kept the value of $n$-factor which was smaller than 1.1 despite the high annealing temperature, but that of the diode with Ti electrode increased as the temperature had been higher. When these characteristics of the SiC Schottky diodes between three electrodes were compared, it was found that the degree of the change of the Schottky-barrier height and the $n$-factor of TiC/SiC or TiSi$_2$/SiC Schottky diode was smaller than that of Ti/SiC Schottky diode. From these results, it is conspicuously suggested that TiC and TiSi$_2$ of the metal compounds are hard to cause
the interface reaction with SiC substrates under the high annealing temperature than the reference-metal Ti. Therefore, TiC and TiSi$_2$ electrodes with SiC probably form the ideal interface of Schottky junction, and the SiC Schottky-barrier diodes of these electrodes have the stable diode characteristics, such as almost constant Schottky-barrier height and small values of $n$-factors, in spite of the high annealing temperature.

Note that the Schottky-barrier height of Ti/4H-SiC has already been reported in the other references: the reported values of the Schottky-barrier height were approximately 1.1–1.2 eV. \cite{10,11}

Figure 4.9 (a) Schottky-barrier height $\phi_{Bn}$ and (b) $n$-factors of SiC Schottky diodes with Ti, TiC, and TiSi$_2$ electrodes in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 $\mu$m$^2$).

85
Table 4.2 Schottky-barrier height $\phi_{bh}$ (eV) of the SiC Schottky diode with each electrode in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$)

<table>
<thead>
<tr>
<th>Annealing Temperatures (℃)</th>
<th>Ti</th>
<th>TiC</th>
<th>TiSi$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposition</td>
<td>0.94</td>
<td>0.84</td>
<td>0.78</td>
</tr>
<tr>
<td>500</td>
<td>1.18</td>
<td>0.98</td>
<td>0.94</td>
</tr>
<tr>
<td>600</td>
<td>1.17</td>
<td>0.97</td>
<td>0.93</td>
</tr>
<tr>
<td>700</td>
<td>0.97</td>
<td>0.92</td>
<td>0.88</td>
</tr>
<tr>
<td>750</td>
<td>0.93</td>
<td>0.92</td>
<td>0.87</td>
</tr>
<tr>
<td>800</td>
<td>0.84</td>
<td>0.89</td>
<td>0.83</td>
</tr>
<tr>
<td>850</td>
<td>0.77</td>
<td>0.92</td>
<td>0.79</td>
</tr>
<tr>
<td>900</td>
<td>0.65</td>
<td>1.07</td>
<td>0.76</td>
</tr>
<tr>
<td>950</td>
<td>0.63</td>
<td>1.16</td>
<td>0.72</td>
</tr>
<tr>
<td>1000</td>
<td>0.76</td>
<td>1.27</td>
<td>0.70</td>
</tr>
<tr>
<td>1050</td>
<td>0.75</td>
<td>1.45</td>
<td>0.88</td>
</tr>
</tbody>
</table>
Table 4.3 Values of $n$-factor (a.u.) of the SiC Schottky diode with each electrode in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$)

<table>
<thead>
<tr>
<th>Annealing Temperatures (℃)</th>
<th>Ti</th>
<th>TiC</th>
<th>TiSi$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposition</td>
<td>1.02</td>
<td>1.00</td>
<td>1.13</td>
</tr>
<tr>
<td>500</td>
<td>1.06</td>
<td>1.01</td>
<td>1.04</td>
</tr>
<tr>
<td>600</td>
<td>1.10</td>
<td>1.01</td>
<td>1.03</td>
</tr>
<tr>
<td>700</td>
<td>1.02</td>
<td>1.02</td>
<td>1.02</td>
</tr>
<tr>
<td>750</td>
<td>1.03</td>
<td>1.02</td>
<td>1.02</td>
</tr>
<tr>
<td>800</td>
<td>1.05</td>
<td>1.01</td>
<td>1.03</td>
</tr>
<tr>
<td>850</td>
<td>1.07</td>
<td>1.02</td>
<td>1.03</td>
</tr>
<tr>
<td>900</td>
<td>1.14</td>
<td>1.02</td>
<td>1.02</td>
</tr>
<tr>
<td>950</td>
<td>1.32</td>
<td>1.02</td>
<td>1.03</td>
</tr>
<tr>
<td>1000</td>
<td>1.26</td>
<td>1.00</td>
<td>1.07</td>
</tr>
<tr>
<td>1050</td>
<td>1.34</td>
<td>1.38</td>
<td>1.13</td>
</tr>
</tbody>
</table>
4.2.3 Current-Electrode Area Characteristics in Various Annealing Temperatures

Circumference current is observable when an intercept of current-electrode areas characteristics is measured from current-voltage characteristics of diodes which have different electrode size, which is also called as an area dependency of the electric current. In this experiment, the areas of the electrodes used for the measurement were: 50×50 μm², 100×100 μm², and 206×206 μm². As a result, the current-electrode area characteristics of the SiC Schottky-barrier diodes of Ti, TiC, and TiSi₂ electrodes in various annealing temperatures were obtained. The reverse-saturation current of the Schottky diodes with these respective electrodes at -1.0 V on each area of the three is shown in Figure 4.10. In addition, Figure 4.11 shows the enlarged figure of Figure 4.10 near the origin point, which shows the increase of the intercept. The annealing temperatures shown in Figure 4.10 and 4.11 are: (a) 700°C, (b) 750°C, and (c) 800°C respectively, and Table 4.4 shows the values of the circumference current at each temperature. In each state, these Figures showed that the following changes were found in each state:

a) The Schottky diodes of each electrode have the very small reverse current in the annealing temperature of 700°C. Moreover, the intercepts of the current-electrode area characteristics was low; the circumference current was extremely small.

b) The reverse current of the reference electrode Ti was increased a little in the annealing temperature of 750°C. However, those of TiC and TiSi₂ electrodes kept the current very small. Furthermore, the intercepts of the current-electrode area characteristics of these electrodes were still low; the circumference currents were small.

c) The reverse current of the reference electrode Ti was increased more in the annealing temperature of 800°C. However, those of TiC and TiSi₂ electrodes kept the current
almost constant. In addition, the intercept of the current-electrode area characteristics of Ti electrode was larger than that of TiC and TiSi$_2$ electrodes; the circumference current of TiC and TiSi$_2$ electrodes was very small for hardly reacting with SiC substrate while that of Ti electrode had the increasing trend for reacting with SiC substrate.

**Figure 4.10** Reverse current versus electrode area characteristics at -1.0 V: (a) 700°C, (b) 750°C, and (c) 800°C (RTA for 1 minute in N$_2$).
Figure 4.11 Enlarged graphs of reverse current versus electrode area characteristics of SiC Schottky diodes at -1 V in the annealing temperatures: (a) 700°C, (b) 750°C, and (c) 800°C (RTA for 1 minute in N₂). The increase of the intercept of Ti could be confirmed.

Table 4.4 Circumference current (A) of diodes in the annealing temperatures (RTA for 1 min in N₂)

<table>
<thead>
<tr>
<th>Annealing Temperatures (°C)</th>
<th>Ti</th>
<th>TiC</th>
<th>TiSi₂</th>
</tr>
</thead>
<tbody>
<tr>
<td>700</td>
<td>2.8×10⁻¹³</td>
<td>4.0×10⁻¹³</td>
<td>1.4×10⁻¹²</td>
</tr>
<tr>
<td>750</td>
<td>5.2×10⁻¹³</td>
<td>3.0×10⁻¹³</td>
<td>7.0×10⁻¹³</td>
</tr>
<tr>
<td>800</td>
<td>6.2×10⁻¹²</td>
<td>5.6×10⁻¹³</td>
<td>2.1×10⁻¹²</td>
</tr>
</tbody>
</table>

90
4.3 Power Loss of Schottky-Barrier Diodes

All of the electric devices have the electrical power loss. Therefore, Schottky-barrier diodes also have the power loss. In this study, the specific on-resistances of the fabricated Schottky diodes were obtained as a simplified. Then, the electric power efficiencies of the diodes were concisely calculated. In the following subsections, the calculated methods of the specific on-resistance and the power loss are introduced, and the result values are shown briefly.

4.3.1 Specific On-Resistances of Schottky-Barrier Diodes

Schottky-barrier diode has a specific on-resistance based on the logic and formulas, which was described in Section 1.2.2. The specific on-resistance \( R_{on,sp} \) [\( \Omega \text{cm}^2 \)] is included in the total on-resistance \( R_{on} \) [\( \Omega \text{cm}^2 \)] which is a ratio of the current density and voltage of on-state; that is, the total on-resistance is given by the following approximate equation:

\[
R_{on} = \frac{\Delta J_F}{\Delta V_F} \approx \frac{J_F}{V_F}
\]  

(4.1)

Where \( J_F \) is a forward current density, and \( V_F \) is a forward voltage. The total on-resistance with the on-resistance, which is called as contact resistance \( R_c \) [\( \Omega \text{cm}^2 \)] in only Ohmic contact, can be describe in the following theoretical equation: \(^{[30]}\)

\[
R_T = R_{sp} + R_c + R_o L^2
\]

(4.2)

Where \( R_{sp} \) is a spreading resistance for a vertical device, \( R_o \) is a residual resistance which includes the metal electrodes resistance of the anode and cathode, and \( L \) is a length of the anode electrode area or contact area. The schematic cross section diagram of these resistances is shown in Figure 4.12. The spreading resistance which is one of
the additional resistances is given by the following equation: \[ R_{sp} = \frac{\rho}{L} \tan^{-1}\frac{2h}{L} \] (4.3)

Where \( \rho \) is a substrate resistivity and \( h \) is a thickness of the substrate. The spreading resistance is schematically shown in Figure 4.13. However, because the SiC substrates used in this study had a relative small thickness (about 300–400 \( \mu \)m) in contrast with the electrode areas, the spreading resistance could be ignored in the calculations of the specific on-resistance.

The total on-resistances \( R_{on} \) of the SiC Schottky diodes with Ti, TiC, and TiSi\(_2\) in various annealing temperature are summarized in Figure 4.14. In Figure 4.14, the length of the one side of the anode electrode area (206, 100, and 50 \( \mu \)m) are schematically shown, and the arrows of the upper direction indicate that the on-resistances are too large to show its value in the range of \( 10^{-3} \) to 1 \( \Omega \)cm\(^2\). These on-resistances were measured values, which were the forward bias (5 V) divided by the current density at the voltage. From Figure 4.14, it is found that the electrode with larger area has the larger on-resistance due to the residual resistances such as the metal or substrate. Therefore, in this study, the specific on-resistance was provided by the following simple equation:

\[ R_{on} = R_o S + R_{on,sp} \] (4.4)

Where \( R_o \) is the residual resistance, and it is assumed that this resistance is proportional to the electrode area. The ideal specific on-resistance is not proportional to the electrode area. Even though the spreading resistance is not considered in this calculation, the specific on-resistance is roughly extracted from the intercept of the equation. Nevertheless, there is also a questionable authenticity of the concept of the specific on-resistance calculation because the specific on-resistance is also given by the
measurement value of the breakdown voltage. Note that: persistently, the specific on-resistances in this study were the expected values. As a result, the values of the specific on-resistances should be read only as a guide, for they might not be extracted well.

The specific on-resistance of SiC Schottky diodes with Ti, TiC, and TiSi2 electrodes in various annealing temperatures is shown in Figure 4.15 and Table 4.5. Some plot data are not displayed or not available because they had the minus values. It is considered that other causes such as the interface reaction might be happened in the metal/semiconductor interface. Especially, the circumference current of the Ti/SiC Schottky diode increased in the high annealing temperatures, which is predominated over 700℃. However, in 500℃ annealing, the specific on-resistances of SiC Schottky diodes with each electrode were about $10^{-3}$~$10^{-4}$ Ωcm$^2$, and the values might be appropriate if they are compared with the theoretical specific on-resistance of 4H-SiC (Section 1.2.2). Moreover, the values of specific on-resistance like these were reported in a referenced paper.\[6\]

![Figure 4.12 Schematic cross section diagram of resistance names in this thesis. Spreading resistance can be applied for vertical devices (e.g. Ohmic device, Schottky diode).](image-url)
Figure 4.13 Schematic diagram of spreading resistance $R_{sp}$.\textsuperscript{[16]}

Figure 4.14 Total on-resistances of the SiC Schottky diodes with Ti, TiC, and TiSi$_2$ in various annealing temperature (RTA for 1 minute in N$_2$).
Figure 4.15 Specific on-resistance of SiC Schottky diodes with Ti, TiC, and TiSi$_2$ electrodes in various annealing temperatures (RTA for 1 minute in N$_2$). Some plot data which are not displayed had the minus values due to other causes such as the interface reaction; N/A.

Table 4.5 Extracted specific on-resistances (Ωcm$^2$) of the SiC Schottky diode with each electrode in various annealing temperatures (RTA for 1 minute in N$_2$)

<table>
<thead>
<tr>
<th>Annealing Temperatures (°C)</th>
<th>Ti</th>
<th>TiC</th>
<th>TiSi$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposition</td>
<td>0.0775</td>
<td>0.0009</td>
<td>27.0082</td>
</tr>
<tr>
<td>500</td>
<td>0.0013</td>
<td>0.0009</td>
<td>0.0003</td>
</tr>
<tr>
<td>600</td>
<td>0.0700</td>
<td>N/A</td>
<td>0.0009</td>
</tr>
<tr>
<td>700</td>
<td>0.0005</td>
<td>0.0008</td>
<td>0.1632</td>
</tr>
<tr>
<td>750</td>
<td>N/A</td>
<td>0.0027</td>
<td>0.0088</td>
</tr>
<tr>
<td>800</td>
<td>N/A</td>
<td>0.0007</td>
<td>0.0121</td>
</tr>
<tr>
<td>850</td>
<td>N/A</td>
<td>0.0011</td>
<td>0.0008</td>
</tr>
<tr>
<td>900</td>
<td>N/A</td>
<td>0.0094</td>
<td>0.0005</td>
</tr>
<tr>
<td>950</td>
<td>N/A</td>
<td>0.0140</td>
<td>0.0018</td>
</tr>
<tr>
<td>1000</td>
<td>N/A</td>
<td>0.0146</td>
<td>0.0022</td>
</tr>
<tr>
<td>1050</td>
<td>N/A</td>
<td>14.9393</td>
<td>27.3108</td>
</tr>
</tbody>
</table>
4.3.2 Calculated Power Loss of Schottky-Barrier Diodes

The electric power loss of the Schottky-barrier diodes was calculated based on the on-resistance in this thesis. The static power loss $P_L$ per unit area is concisely given by the following equation: \[^{[31]}\]

$$P_L = \frac{1}{2}(J_F V_F + J_R V_R) \quad (4.5)$$

Where $J_F$ is the forward current density, $V_F$ is the forward voltage, $J_R$ is a reverse current density, and $V_R$ is a reverse voltage. In this equation, the ratio of the on-state and off-state is one on one; that is, the duty cycle is 50%, and the schematic diagram is shown in Figure 4.16. In this study, the power loss of the Schottky diodes was calculated based on this assumption of the duty cycle. The forward voltage drop $V_F$ and the reverse leakage current density $J_R$ are given by the following equations: \[^{[18]}, [32]\]

$$V_F = \frac{kT}{q} \ln \left( \frac{J_F}{A^{**}T^2} \right) + \phi_{Bn} + R_{on,sp} J_F \quad (4.6)$$

$$J_R = A^{**}T^2 \exp \left\{ -\frac{q(\phi_{Bn} - \Delta\phi)}{kT} \right\} \quad (4.7)$$

Therefore, the synthesized theoretical power loss can be given by the following equation:

$$P_L = \frac{1}{2} \left[ J_F \left( \frac{kT}{q} \ln \left( \frac{J_F}{A^{**}T^2} \right) + \phi_{Bn} + R_{on,sp} J_F \right) \right. \quad (4.8)$$

$$\left. + A^{**}T^2 \exp \left\{ -\frac{q(\phi_{Bn} - \Delta\phi)}{kT} \right\} V_R \right]$$

The theoretical curve of the power loss as a function of the Schottky-barrier height can be calculated by assuming the forward current density $J_F$ and the reverse blocking voltage $V_R$.

Figure 4.17 shows the theoretical curve of the power loss and calculated plot based on
the measured Schottky-barrier height and specific on-resistance in various annealing
.temperatures. In Figure 4.17, the parameters used in the calculation is shown, and the
.measured value in which the specific on-resistance was not available used the expected
.approximate value of 4H-SiC \((10^{-3} \, \Omega \text{cm}^2)\). From the theoretical curve, it is found that
.there is a minimum value for the power loss because the reverse current \(J_R\) will increase
.significantly as the barrier height become low and forward voltage drop \(V_F\) will be
.larger by the barrier height increasing. Moreover, plot data circled by a dotted line
.increased the reverse current as a measured value in the high annealing temperatures.
.Therefore, although the small power loss of these data is observable on the simulation,
.the plot data may substantially have large power loss. It is possible to say that the SiC
.Schottky diode with TiC electrode has relatively high performance in that: the reverse
.leakage current and the power loss are sufficiently small and the switching speed may
.be fast due to the low barrier height in comparison with that of Ti electrode.
.In addition, the power loss in the range of really measured current and voltage is
.shown in Figure 4.18 (in various annealing temperature) and Figure 4.19 (as a function
.of the Schottky-barrier height). For the calculation of the power loss, the power-loss
.equation (4.5) was used. Furthermore, the reverse current \(J_R\) corresponding to \(V_R = 5\)
.[V] and the forward voltage \(V_F\) corresponding to \(J_F = 1 \, \text{[A/cm}^2\text{]}\) were used in the
calculation. As the current-voltage measurement was conducted in the narrow range of
.the voltage, the power loss was very small in comparison with the above simulation.
.However, it is also observable that there is a trend of the power loss decrease with the
.low Schottky-barrier height.
**Figure 4.16** Schematic diagram of 50% duty cycle (50% on-state and 50% off-state).

**Figure 4.17** Power loss of SiC Schottky diodes with each electrode and theoretical curve based on the assumptions of parameters. Plot data circled by a dotted line showed the increase of the reverse current as a measured value in the high annealing temperatures. (Electrode area: 206×206 μm²)
Figure 4.18 Power loss of SiC Schottky diodes with each electrode in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$), which is based on really measured current and voltage.

Figure 4.19 Power loss of SiC Schottky diodes with each electrode as a function of Schottky-barrier height, which is based on really measured current and voltage. (Electrode area: 206×206 μm$^2$)
4.4 Capacitance-Voltage Characteristics of SiC Schottky Diode with TiC Electrode in Various Annealing Temperatures

In this study, additional measurements for TiC/SiC Schottky diode were conducted in order to clarify the interface characteristics of TiC and SiC. On that account, the C-V measurement was added for the evaluation of the diode in the various annealing temperature. In addition, the I-V measurement was performed. The annealing temperatures were: 500, 550, 600, 650, 700, 750, 800, 850, 900, 950, 1000, and 1050°C for 1 minute in N₂ atmosphere. Consequently, in the SiC Schottky diode with TiC electrode, the Schottky-barrier height measured by fitting J-V characteristics and the Schottky-barrier height calculated by the C-V characteristics could be compared.

4.4.1 Reproduced J-V Characteristics of TiC/SiC Schottky Diode in Various Annealing Temperatures

The J-V characteristics of SiC Schottky diode with TiC electrode were measured in the various annealing temperature for the second time in this study. Then, the reproducibility that TiC/SiC Schottky diode had the high stability in the high annealing temperature was confirmed. The reproduced J-V characteristics of the TiC/SiC Schottky diode is shown in Figure 4.20. From this J-V characteristics, it was found that the reverse leakage current of TiC/SiC Schottky diode was very small in the high annealing temperature. The Schottky-barrier height and n-factor will be shown and compared in the following subsection in addition to the C-V characteristics.
Figure 4.20 Reproduced $J$-$V$ characteristics of the TiC/SiC Schottky diode in various annealing temperature (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$).

### 4.4.2 $C$-$V$ Characteristics of TiC/SiC Schottky Diode in Various Annealing Temperatures

The $C$-$V$ characteristics of SiC Schottky diode with TiC electrode was additionally evaluated in this study. The $C$-$V$ characteristics of TiC/SiC Schottky diode in various annealing temperatures (for 1 minute in N$_2$ atmosphere) is shown in Figure 4.21. Moreover, the calculated $I/C^2$-$V$ characteristics is shown in Figure 4.21, which was used for the evaluation of the Schottky diode such as the built-in potential and the $n$-type carrier density (the doping concentration). Note that the range of the voltage used for the analysis was from -1.0 to 0 V because only the depletion state could be available for the Schottky-barrier diode, and the measuring frequency $f$ was 100 kHz.

The $n$-type carrier density and the built-in potential calculated from the $I/C^2$-$V$...
characteristics of the TiC/SiC Schottky diode are shown in Figure 4.23. The value of the doping concentration in the SiC substrate was: \( N_D = 1.0 \times 10^{16} \, \text{[cm}^{-3}\text{]} \). It was found that the carrier density was not changed by the high annealing temperature. This fact probably suggested that the metal TiC had not reacted with SiC substrate on the interface. Moreover, from \( C-V \) characteristics, the Schottky-barrier height shown in Figure 4.24 was calculated by the carrier density and the built-in potential shown in Figure 4.23. Figure 4.24 shows the Schottky-barrier height of the two measurement calculated from the \( C-V \) characteristics and the \( J-V \) characteristics fitting in the various annealing temperatures. Table 4.6 shows the summary of the experiment values measured from the \( C-V \) and \( J-V \) characteristics of the TiC/SiC Schottky diode. In addition, the \( n \)-factor which is an index of ideality of diode is also shown in the same annealing temperatures, which was also given by the fitting of the \( J-V \) characteristics. It was reproducibly confirmed that the TiC/SiC Schottky diode had the high temperature-annealing stability, for the \( n \)-factor kept ideally approximately 1.0 up to the high annealing temperature 900°C. Over 1000°C of the annealing temperature, there was an indication of the deterioration of the Schottky diode because the difference of the two of the Schottky-barrier height was seen in the evaluated values from the \( C-V \) and \( J-V \) characteristics. Furthermore, the Schottky-barrier height of \( C-V \) characteristics measurement accorded well with that of \( J-V \) characteristics measurement up to the high annealing temperature 900°C. From these results, it was revealed that TiC/SiC Schottky diode had the stability to the high temperature annealing. Moreover, it was certainly found that the Schottky barrier which was formed on the interface between TiC and SiC was further from the Schottky-barrier lowering which is discussed in the Ohmic process. The Ohmic characteristics of metal and semiconductor is concisely described as the
following processes: [33], [34], [35]

1. Barrier-Height Lowering

The barrier-height lowering can be made by the choice of the metal electrode which has a small work function. Alternatively, the effective barrier-height lowering on the metal/semiconductor interface can be obtained by the alloying of the semiconductor by high temperature annealing. Therefore, as the barrier height is made small, the reverse bias current increases and the Ohmic characteristics can be obtained.

2. Thin Surface Barrier

The Schottky-barrier potential can be made thinly by changing the effective doping concentration of the semiconductor on the interface of the metal and semiconductor. The change can be also described as a band bending at the metal/semiconductor interface. From this, the tunneling current in the Schottky is increased and the Ohmic characteristics can be obtained.

As other ways of the Schottky-barrier-height lowering for Ohmic process, there are many example reports of the Schottky-barrier-height lowering and controlling by the doping. [36], [37], [38] Then, from the experiment results, the carrier density of the SiC substrate, which is approximately equal with the doping concentration, was constant in the high temperature annealing. Therefore, the thin surface-barrier model could not applied for the TiC/SiC Schottky diode. In addition, it is suggested that the TiC and SiC interface might not be alloyed because the reverse leakage current was kept small in the high temperature annealing. Moreover, it is possible to say that the composition of TiC electrode might be changed because the Schottky-barrier height got high rather than getting low. Note that, on the other hand, it is considered that Ti/SiC Schottky diode was deteriorated due to the alloying in the high temperature annealing (Section 4.2).
As a conclusion, it is considered that the TiC/SiC Schottky diode did not vary the carrier density and was not alloyed on the TiC/SiC interface. Consequently, the TiC/SiC Schottky diode could retain the diode characteristics in the high temperature annealing.

**Figure 4.21** $C$-$V$ characteristics of TiC/SiC Schottky diode in various annealing temperatures (RTA for 1 minute in $N_2$, Electrode area: 206×206 $\mu$m$^2$, $f = 100$ [kHz]).

**Figure 4.22** $I/C^2$-$V$ characteristics of TiC/SiC Schottky diode in various annealing temperatures (RTA for 1 minute in $N_2$, Electrode area: 206×206 $\mu$m$^2$, $f = 100$ [kHz]).
Figure 4.23 Carrier density and built-in potential of TiC/SiC Schottky diode in various annealing temperatures (RTA for 1 minute in N₂, Electrode area: 206×206 μm², f = 100 [kHz]). Each value was calculated from the \( I/C^2-V \) characteristics. (The catalog value of the doping concentration in the SiC substrate: \( N_D = 1.0 \times 10^{16} \) [cm⁻³])
Figure 4.24 (a) Schottky-barrier height $\phi_{Bn}$ and (b) $n$-factor of TiC/SiC Schottky diode in various annealing temperatures (RTA for 1 minute in N$_2$, Electrode area: 206×206 μm$^2$, $f = 100$ [kHz]). Two ways of the Schottky-barrier-height measurement were given by C-V and J-V characteristics.
Table 4.6 Summary of the experiment values measured form the \( C \cdot V \) and \( J \cdot V \) characteristics of TiC/SiC Schottky diode in various annealing temperatures (RTA for 1 minute in \( N_2 \), Electrode area: 206×206 \( \mu m^2 \), \( f = 100 \) [kHz])

<table>
<thead>
<tr>
<th>Annealing Temp. (°C)</th>
<th>( N_D ) [\times 10^{16} \text{ cm}^{-3}]</th>
<th>( \psi_{bi} ) [eV]</th>
<th>( \phi_B ) [eV] ((C-V))</th>
<th>( \phi_B ) [eV] ((I-V))</th>
<th>( n ) [a.u.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-deposition</td>
<td>1.02</td>
<td>0.72</td>
<td>0.92</td>
<td>0.84</td>
<td>1.02</td>
</tr>
<tr>
<td>500</td>
<td>1.00</td>
<td>0.97</td>
<td>1.17</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>550</td>
<td>0.97</td>
<td>0.85</td>
<td>1.05</td>
<td>0.99</td>
<td>1.00</td>
</tr>
<tr>
<td>600</td>
<td>0.99</td>
<td>0.80</td>
<td>1.00</td>
<td>0.99</td>
<td>1.00</td>
</tr>
<tr>
<td>650</td>
<td>1.02</td>
<td>0.78</td>
<td>0.98</td>
<td>0.98</td>
<td>1.00</td>
</tr>
<tr>
<td>700</td>
<td>1.02</td>
<td>0.78</td>
<td>0.97</td>
<td>0.97</td>
<td>1.00</td>
</tr>
<tr>
<td>750</td>
<td>1.02</td>
<td>0.82</td>
<td>1.01</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>800</td>
<td>1.02</td>
<td>0.91</td>
<td>1.11</td>
<td>1.07</td>
<td>1.01</td>
</tr>
<tr>
<td>850</td>
<td>1.02</td>
<td>1.01</td>
<td>1.21</td>
<td>1.17</td>
<td>1.02</td>
</tr>
<tr>
<td>900</td>
<td>0.99</td>
<td>1.12</td>
<td>1.31</td>
<td>1.25</td>
<td>1.02</td>
</tr>
<tr>
<td>950</td>
<td>0.99</td>
<td>1.56</td>
<td>1.76</td>
<td>1.51</td>
<td>1.06</td>
</tr>
<tr>
<td>1000</td>
<td>0.96</td>
<td>1.58</td>
<td>1.78</td>
<td>1.32</td>
<td>1.32</td>
</tr>
<tr>
<td>1050</td>
<td>0.96</td>
<td>1.56</td>
<td>1.76</td>
<td>1.10</td>
<td>1.43</td>
</tr>
</tbody>
</table>
Chapter 5  Conclusion

5.1 Electrical Characteristics of SiC Schottky-Barrier Diodes with Ti, TiC, and TiSi$_2$ Electrodes

5.2 Summary of This Study

5.3 Prospects for Further Study
5.1 Electrical Characteristics of SiC Schottky-Barrier Diodes with Ti, TiC, and TiSi$_2$ Electrodes

In this study, the electrical characteristics of the SiC Schottky-barrier diodes with Ti, TiC, and TiSi$_2$ electrodes were shown in the various annealing temperatures. As a result, the remarkable results were found in the different diode characteristics of Ti, TiC, and TiSi$_2$ electrodes on SiC substrates. The greatest discovery was that the SiC Schottky diodes with TiC and TiSi$_2$ electrodes indicated the stabilities about the Schottky-barrier height and $n$-factor in the high temperature annealing, which were measured from the $J$-$V$ characteristics. Especially, the TiC/SiC Schottky diode designated the best annealing stability in comparison with Ti or TiSi$_2$/SiC Schottky diodes. These results were obviously seen from the increase of the reverse-bias current and the degree of the change of the Schottky-barrier height and $n$-factor. From the diode characteristics, it was certainly confirmed that the formed TiC and TiSi$_2$ electrodes are hard to react with SiC substrate on the interface. This was equal with the expectation that was described in the first experiment purpose. In addition, the Schottky-barrier height of TiC/SiC Schottky diode was increased by the high temperature annealing, which indicated different characteristics from those of the other metal/SiC Schottky diodes and it could not be explained by the usual models of Ohmic process. Accordingly, TiC/SiC Schottky diode was annealed again at high temperatures and $C$-$V$ characteristics was measured in addition to $I$-$V$ characteristics. Consequently, the diode characteristics of TiC/SiC Schottky diode were reproduced and the Schottky-barrier height having the increasing trend at high annealing temperatures was verified by both of the $I$-$V$ and $C$-$V$ characteristics. Moreover, it was certain that TiC electrode was hard to react with SiC substrate, and the high annealing stability of the Schottky diode was demonstrated. The
cause of this particular characteristic has not been revealed yet. However, it is possible to consider that the composition of TiC electrode might be changed by the alloying in the high temperature annealing. Alternatively, a pseudo Schottky-barrier height might possibly be measured as higher by the forming of an interface state at the TiC/SiC junction interface. Thus, the possibilities of the interface control and evaluation were strongly suggested by the electrical characteristics of the SiC Schottky diodes with Ti-carbide and Ti-disilicide metal electrodes.

5.2 Summary of This Study

In this study, the SiC Schottky-barrier diodes were fabricated with Ti, TiC, and TiSi$_2$ electrodes. Then, the $I$-$V$ characteristics of these Schottky diodes were measured and compared in the various annealing temperatures. As a result, there were significant differences in the Schottky diodes. Consequently, it was suggested that the most stable electrode for SiC in the high temperature annealing was TiC. Finally, it was concluded that there were the possibilities of the interface control and evaluation by TiC and TiSi$_2$ electrode for SiC Schottky diode.

In Chapter 1, the backgrounds of power electronics and the applicability of SiC for the field were introduced. In addition, the necessity for research of metal and SiC interface was presented with mixing the introductions of the previous studies reported in the references. Moreover, the expected problems of Schottky-barrier diodes using SiC substrate were mentioned from the perspective of metal/SiC interface reaction in materials technology. Furthermore, the particulars of the metal-electrode selection were concisely outlined.
In Chapter 2, the experiment procedures and details were shown, which was divided into the fabrication process of the SiC Schottky diodes and the measurement method of the diode characteristics.

In Chapter 3, the analysis methods of the Schottky diodes were introduced. First, the theoretical current-transport process was mentioned and the concrete method for evaluating the diode characteristics by the fitting was introduced, which were used in this study. In addition, other analysis procedures of Schottky diodes, such as activation-energy method and C-V characteristics, were concisely mentioned.

In Chapter 4, as the result of the experiments, SiC Schottky-barrier diodes with Ti, TiC, and TiSi$_2$ electrodes were fabricated and the $I$-$V$ characteristics were measured in the various annealing temperatures. In addition, the $I$-$V$ characteristics of TiC/SiC Schottky diode were measured in the various measuring temperature in order to extract the effective Richardson constant. Then, the Schottky-barrier height and $n$-factor of the fabricated devices were extracted and evaluated. Moreover, the specific on-resistances and power loss of the SiC Schottky diodes were additionally discussed in the easy method. Finally, TiC/SiC Schottky diode were fabricated, the reproducible characteristics of the diode from both of the $I$-$V$ and C-V characteristics were precisely confirmed. As a recapitulation, in this study, the electrical characteristics of the SiC Schottky diodes with Ti, TiC, and TiSi$_2$ electrodes were compared, and the possibilities of the interface control were suggested by TiC and TiSi$_2$ electrodes for SiC Schottky diode.
5.3 Prospects for Further Study

The main purpose of this study was to investigate the electrical characteristics of the SiC Schottky diodes with TiC and TiSi$_2$ electrodes which would be suggested as appropriate metals for SiC substrate. Accordingly, it was necessary to compare the differences of the diode characteristics given as a result, and the various electrical methods were conducted to clarify the change by the interface reaction of metal/SiC. However, physical material analysis using X-ray (XRR, XRD, and other material analysis with X-ray) are also probably necessary, which was not mentioned for confirming the forms of TiC and TiSi$_2$ electrodes in this study. In addition, the image observations of the interface between metal and SiC are also certainly needed for the evaluation of the interface reaction, such as TEM. Alternatively, other electrical measurements may be needed such as: DLTS method (Deep Level Transient Spectroscopy conductance) for the investigation of the deep interface state, and Conductance method for the investigation of the bulk interface state.

Henceforth, it is expected that other carbide electrode such as (Mo-C) and tungsten-carbide (W-C) for SiC Schottky diode will show interesting characteristics. SiC Schottky diode with molybdenum-carbide electrode possibly has the particular diode characteristics as same as SiC Schottky diode with the titanium-carbide electrode because Si-C-Mo system has the similar isothermal phase diagram to Si-C-Ti system. [13],[39] SiC Schottky diode with tungsten-carbide electrode may also be stable in high temperature annealing because Si-C-W system does not have the ternary phase and tungsten-carbide is directly on the reaction diffusion path. [40] Finally, it is possible to obviously say that the further study about the investigation and interface control of metal/SiC contact should be needed for the Schottky-barrier diode.
Appendixes

Appendix 1. Classifications of Power Semiconductor Devices

Appendix 2. Differences of Two Semiconductors for Power Devices

Appendix 3. Turning Point of Semiconductor SiC for Power Devices

Appendix 4. Table of Physical Constants

Appendix 5. List of Symbols

Appendix 6. SI Prefixes
Appendix 1. Classifications of Power Semiconductor Devices

A first power semiconductor device which used a power diode of a semiconductor material was proposed by Robert N. Hall in 1952.\textsuperscript{[41]} It was capable of blocking a reverse voltage up by 200 V, and an ampacity (ampere capacity) described as an electric current capacity was 35 A. Afterwards, many kinds of the power semiconductor devices which have a specific structure have come into the research fields and the industry of the electronics for half a century. Common power devices are optimized for the purpose of use: such as high breakdown voltage, low-power loss, high switching frequency, and controllability. As a result, there are classifications of power devices based on the structures and the operating principles.

Power semiconductor devices can be classified as the following categories: diodes and triodes from a viewpoint of the structure. In addition, power devices may be divided into majority carrier devices and minority carrier devices based on that which carrier principally relates to the switching. The diode has two terminals that are called anode and cathode. An electric current flows mainly from the anode to the cathode by a forward-biased voltage. Moreover, a reverse current transported from the cathode to the anode by a reverse-biased condition cannot flow in an ideal diode. The switching operations are caused by only the external applied voltage, so the on/off of the diode switches passively. For example, Schottky diode has a rectification formed by a potential energy difference, called Schottky barrier, which is made from a metal/semiconductor contact. Since the current flow depends on the barrier height controlled by the applied voltage, depletion layer which takes a long time to be formed, especially in case of a turn off, is not related with the switching in this diode. Therefore,
Schottky diode has high speed switching, which is classified as the majority carrier devices. On the other hand, the minority carrier devices like a p-i-n diode have both of n-type and p-type semiconductors. In such devices, because the current flow depends on the depletion-layer width and the height of an energy band by electrons and holes, the switching speed usually low. However, the breakdown voltage can be enhanced by doping concentrations. Note that the majority carrier device is also called a unipolar device and the minority carrier device is also called a bipolar device.

Triodes can control the current flow on a path in the biased voltage by the third terminal. This terminal is known as a base or a gate. The switching of the triode is operated by the control signal that has been sent through the base or the gate. In the power device field, DC-DC, AC-AC, and other converters are realized by PWM which is a control method used in many switches of the triodes. In the VLSI fields, LCD, CPU, and other digital instruments also are realized by transistor which is a representative example of the triode for the integrated circuit. Consequently, there are also classifications in triodes. Thyristor, BJT, and IGBT are main examples of the minority carrier devices for the power devices. Thyristor appeared a first triode for the power device in 1957, and could have very high reverse breakdown voltage and carry high current density. However, Thyristor had a big problem about its controllability because it had some p-n diodes with an equipment-gate electrode in addition to anode and cathode; the turn off of the thyristor is conducted by separating it from the power, other thyristors include a gate turn off thyristor (GTO). Bipolar junction transistor (BJT) is a transistor combining both types of semiconductor such as n-p-n or p-n-p. The switching of BJT is operated by the applied voltage to the base with the electrons and holes. Power MOSFET and JFET are examples of the majority carrier device. Basically,
field-effect transistor (FET) is the unipolar device despite having both regions of n-type and p-type semiconductors, but it is only one carrier (usually electrons) that the switching is carried out for on-state. In these transistors, the path of the current is formed by the field effect which can control the energy barrier blocking the electrons or holes. The characteristic of the power MOSFET is that a metal and an oxidation film are used as the gate and this device is available at high frequency unlike bipolar-type transistor. The first power MOSFET of 25 A, 400V was introduced in 1978. [42] Generally, the breakdown voltage of MOSFET is lower than that of BJT. However, because the structure of metals, oxidation films and semiconductors has been researched in various ways in these days, the performance enhancement of MOSFET is remarkable.

The characteristic of Junction FET (JFET) is that a different type of semiconductor is used as the gate, which is similar to the structure of MOSFET. JFET can control a channel in which carriers are flowing by a semiconductor gate through the depletion region, which can be a relative switch. Commonly, the reverse-leakage current of JFET is a little larger than that MOSFET due to an insulation structure, but much smaller than that of bipolar transistor. Moreover, a transconductance of JFET is lower than MOSFET, so it has low noise and it is used in the application such needs. Furthermore, a new hybrid power device combining structures of MOSFET and BJT is Insulated-gate bipolar transistor (IGBT) which was developed in 1980s. This transistor has both characteristics of the bipolar transistor and the power MOSFET. Although IGBT has a complicated structure, that performance of breakdown voltage is approximately equal to bipolar transistors, and the module is driven at the frequency as high as MOSFET. The schematic structure of IGBT is that a section of the switching controller as gate is adopted for MOSFET. In addition, n-type and p-type regions form a vertical p-n-p BJT;
even though the research of the optimized structures is difficult, it seems that the commercial production was easy because of the combination of two components. As a result, the bipolar transistors in the applications of the power device have been replaced by IGBTs.

In reality, the power device can combine diodes and triodes (switches). Thyristor, BJT, and IGBT use the basic p-n diode structures, which include the structure of FET. Therefore, it is considered that every power semiconductor device have to be researched and improved more. The power device like IGBT is a compilation of the componential electronic devices. As a result, technological developments of the components are important to enhance the performance of all power devices.
Appendix 2. Differences of Two Semiconductors for Power Devices

Both of Si and SiC have been being researched on the cutting edge of the fields of the power semiconductor device or the power electronics for many years. However, many researchers pay great attention to SiC in these years, because a lot of the physical characteristics of SiC are better than those of Si. In this essay, the simple introductions and the characteristic differences of the semiconductors, Si and SiC, are shown.

Si is the most famous and important semiconductor in the electronic engineering in that it has the variable electrical conductivity. Moreover, the most developed semiconductor is also Si in the history of the semiconductor device (including power device) because it can change both of p-type and n-type semiconductor by doping impurities and be made by mass production at low cost. However, recently, the characteristics of Si itself are not able to meet the performances, such as operating speed, power capacity and breakdown voltage, which the newest power devices need. As a result, the new semiconductor SiC appeared and is developed by researchers around the world for complementing them.

It was relatively these days that a single crystal of SiC came to be made by the improvement of chemical vapor deposition (CVD); \([43],[44]\) CVD has been found to be a suitable technique to form homoepitaxial layers on a large-area of SiC \([45]\). As a result, it is seemed that producing the high quality crystal of SiC and researching the characteristics were advanced when researchers came to think that the performance of Si had approached the limit. Because most characteristics of SiC are beyond those of Si, especially breakdown voltage, chemical stability and thermal stability, SiC is suited to power devices using high voltage and high power.\([45]\) Thanks to the technological
innovation of SiC power devices, the importance of Si in the power electronics field may shrink. Moreover, all power devices using Si may be replaced by those using SiC in the future.

There are, of course, many examples of weak points of SiC, particularly the manufacturing costs. A lot of Si is used for other semiconductor device fields such as integrated circuits in which Si is a mainstream semiconductor; that is, the current Si is extremely low cost and has high speed, high efficiency, and easy optimization technology. Moreover, it is not true that every performance of SiC is beyond that of Si. On the contrary, the operating speed of the power devices using Si is basically fast, and the breakdown voltage of them is improved by forming the special structure. Although the operating speed of the power devices using SiC is slow at the present time, it will be improved like Si was so. Fundamentally, Si has the largest share in the semiconductor field, and this trend will be kept for a time. However, SiC should attract attention as a next generation semiconductor, and be researched precisely for the technological innovation. Thus, new semiconductor SiC is expected to improve the technology. On the other hand, it is possible to combine Si and SiC for power devices. The new idea that the power device uses semiconductors complementarily is also needed.
Appendix 3. Turning Point of Semiconductor SiC for Power Devices

East Japan Railway Company gave a press release in July 2014. According to the announcement, the production of a new train (E235 system) for commute was decided, and mass produced foregoing cars of the train have a lot of results of technology developments. A main character of these cars was the improvement of environmental performances, for which a next-generation semiconductor SiC (silicon carbide) was adopted in the main controller. Whereas conventional power devices have been using the semiconductor Si, the electric power loss of the train is certainly decreased by using SiC than Si today. It seems that SiC is one of the semiconductors whose technical applications are about to spread out the electric industrial fields using power devices.

Until 1990s, the research and development of SiC as electronic devices had not been improved since SiC single crystal wafers were not easily available for studies. However, SiC has been industrially produced since late nineteenth century because it has high hardness and heat-resisting property like diamond. Consequently, SiC has been used for: abrasives, refractories, and other industrial products, except for semiconductor devices. From 1950s to 1980s, SiC attracted attention of researchers in the electronic device field since it had potential performances as semiconductor. Although candidates of the blue LED included SiC temporarily, a new compound semiconductor GaN was researched and gave the recipients of the 2014 Nobel Prize in Physics.

From 1990s, however, the epitaxial wafer of SiC was produced, and when single crystal wafers of it came to be available easily, the studies of electronics applications were started. Especially in Japan, SiC has been investigated by various
national projects. Moreover, the research and developments have been conducted by public and private sectors. In 2010s, full-scale practical use of SiC as power devices is going to begin just right. [47]

The usage of semiconductors diverges into many fields, such as industry, electric industry, electronics, information-communication technology, and other fields. That of SiC has been changed into mainly electric and electronic industry as power devices. Furthermore, the ways of thinking and the technology development to expand the usage are very important like this. Especially in the power device field, since the performances of the conventional semiconductors were approaching the limit, the new semiconductor was needed; that is, the semiconductor Si for power devices has been changing to SiC. On the other hand, it is natural that there is a semiconductor, for which diamond is candidate, beyond the next generation semiconductor, but it is not totally at practical use level. In contrast, the example of the practical use of SiC was shown in the new train. In addition, a report showed that: if the developing of SiC power devices progresses like this, a great energy-saving effect about $2 \times 10^{10}$ kWh/year (the quantity of crude oil conversion:4,400,000 kL/year) is expected in 2020.[48] Thus, new semiconductor SiC is expected to improve the electrical and electronic technology.
Appendix 4. Table of Physical Constants

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electronic charge</td>
<td>$q$</td>
<td>$1.60 \times 10^{-19}$ C</td>
</tr>
<tr>
<td>Boltzmann constant</td>
<td>$k$</td>
<td>$1.38 \times 10^{-23}$ J/K</td>
</tr>
<tr>
<td>Thermal voltage ($T=300$ [K])</td>
<td>$kT/q$</td>
<td>0.0259 V</td>
</tr>
<tr>
<td>Free-electron mass</td>
<td>$m_0$</td>
<td>$9.11 \times 10^{-31}$ kg</td>
</tr>
<tr>
<td>Plank constant</td>
<td>$h$</td>
<td>$6.63 \times 10^{-34}$ J-s</td>
</tr>
<tr>
<td>Vacuum permittivity</td>
<td>$\varepsilon_0$</td>
<td>$8.85 \times 10^{-14}$ F/cm</td>
</tr>
<tr>
<td>Richardson constant of free electron</td>
<td>$A$</td>
<td>120 A/cm$^2$/K$^2$</td>
</tr>
<tr>
<td>Speed of light in vacuum</td>
<td>$c$</td>
<td>$3.00 \times 10^8$ m/s</td>
</tr>
</tbody>
</table>
## Appendix 5. List of Symbols

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A)</td>
<td>area</td>
<td>cm²</td>
</tr>
<tr>
<td>(A)</td>
<td>Richardson constant of free electron</td>
<td>A/cm²/K²</td>
</tr>
<tr>
<td>(A^*)</td>
<td>Effective Richardson constant (TE)</td>
<td>A/cm²/K²</td>
</tr>
<tr>
<td>(A^{**})</td>
<td>Effective Richardson constant (TED)</td>
<td>A/cm²/K²</td>
</tr>
<tr>
<td>(D)</td>
<td>Diffusion coefficient</td>
<td>cm²/s</td>
</tr>
<tr>
<td>(D_n)</td>
<td>Diffusion coefficient for electrons</td>
<td>cm²/s</td>
</tr>
<tr>
<td>(E_C)</td>
<td>Breakdown electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>(E_c)</td>
<td>Edge of conduction band</td>
<td>eV</td>
</tr>
<tr>
<td>(E_v)</td>
<td>Edge of valence band</td>
<td>eV</td>
</tr>
<tr>
<td>(E_f)</td>
<td>Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>(E_{F_m})</td>
<td>Metal Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>(E_{F_n})</td>
<td>Quasi-Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>(E_g)</td>
<td>Band gap</td>
<td>eV</td>
</tr>
<tr>
<td>(E_i)</td>
<td>Intrinsic Fermi level</td>
<td>eV</td>
</tr>
<tr>
<td>(E)</td>
<td>Electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>(E_m)</td>
<td>Maximum Electric field</td>
<td>V/cm</td>
</tr>
<tr>
<td>(f)</td>
<td>Frequency</td>
<td>Hz</td>
</tr>
<tr>
<td>(h)</td>
<td>Plank constant</td>
<td>J-s</td>
</tr>
<tr>
<td>(I)</td>
<td>current</td>
<td>A</td>
</tr>
<tr>
<td>(I_s)</td>
<td>Reverse-saturation current</td>
<td>A</td>
</tr>
<tr>
<td>(J)</td>
<td>Current density</td>
<td>A/cm²</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-------------------------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>$J_s$</td>
<td>Reverse-saturation current density</td>
<td>A/cm$^2$</td>
</tr>
<tr>
<td>$J_F$</td>
<td>Forward-bias current density</td>
<td>A/cm$^2$</td>
</tr>
<tr>
<td>$J_R$</td>
<td>Reverse-bias current density</td>
<td>A/cm$^2$</td>
</tr>
<tr>
<td>$k$</td>
<td>Boltzmann constant</td>
<td>J/K</td>
</tr>
<tr>
<td>$m_0$</td>
<td>Free-electron mass</td>
<td>kg</td>
</tr>
<tr>
<td>$m^*$</td>
<td>Effective electron mass</td>
<td>kg</td>
</tr>
<tr>
<td>$n$</td>
<td>Represent for $n$-type semiconductor</td>
<td></td>
</tr>
<tr>
<td>$n$</td>
<td>Ideal factor of diode</td>
<td></td>
</tr>
<tr>
<td>$n$</td>
<td>Concentration of free electrons</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$n_i$</td>
<td>Intrinsic carrier density</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$N$</td>
<td>Carrier density</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$N_A$</td>
<td>Acceptor impurity concentration</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$N_C$</td>
<td>Effective density of states in conduction band</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$N_D$</td>
<td>Donor impurity concentration</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>$P$</td>
<td>Power</td>
<td>W</td>
</tr>
<tr>
<td>$P_L$</td>
<td>Power loss</td>
<td>W</td>
</tr>
<tr>
<td>$q$</td>
<td>Electronic charge</td>
<td>C</td>
</tr>
<tr>
<td>$Q$</td>
<td>Charge density</td>
<td>C/cm$^2$</td>
</tr>
<tr>
<td>$Q_{D}$</td>
<td>Space-charge density of semiconductor</td>
<td>C/cm$^2$</td>
</tr>
<tr>
<td>$R$</td>
<td>Resistance</td>
<td>Ω-cm$^2$</td>
</tr>
<tr>
<td>$R_{on}$</td>
<td>Total on-resistance</td>
<td>Ω-cm$^2$</td>
</tr>
<tr>
<td>$R_{on,sp}$</td>
<td>Specific on-resistance</td>
<td>Ω-cm$^2$</td>
</tr>
<tr>
<td>$R_c$</td>
<td>Specific contact resistance</td>
<td>Ω-cm$^2$</td>
</tr>
<tr>
<td>$T$</td>
<td>Absolute temperature</td>
<td>K</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Unit</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>------</td>
</tr>
<tr>
<td>$V$</td>
<td>Applied voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_B$</td>
<td>Breakdown voltage</td>
<td>V</td>
</tr>
<tr>
<td>$V_F$</td>
<td>Forward bias</td>
<td>V</td>
</tr>
<tr>
<td>$V_R$</td>
<td>Reverse bias</td>
<td>V</td>
</tr>
<tr>
<td>$W_D$</td>
<td>Depletion layer width</td>
<td>cm</td>
</tr>
<tr>
<td>$x$</td>
<td>distance</td>
<td>cm</td>
</tr>
<tr>
<td>$\varepsilon$</td>
<td>Dielectric constant</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_0$</td>
<td>Vacuum permittivity</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\varepsilon_s$</td>
<td>Semiconductor permittivity</td>
<td>F/cm</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Thermal conductivity</td>
<td>W/cm-K</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron mobility</td>
<td>cm²/V-s</td>
</tr>
<tr>
<td>$\mu_h$</td>
<td>Hole mobility</td>
<td>cm²/V-s</td>
</tr>
<tr>
<td>$\phi$</td>
<td>Work function or barrier height</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_B$</td>
<td>Barrier height</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_{Ba}$</td>
<td>Schottky-barrier height on $n$-type semiconductor</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_M$</td>
<td>Metal work function</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_{MS}$</td>
<td>Work-function difference between metal and $n$-type semiconductor</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_n$</td>
<td>Fermi potential from conduction-band edge</td>
<td>V</td>
</tr>
<tr>
<td>$\phi_S$</td>
<td>Semiconductor work function</td>
<td>V</td>
</tr>
<tr>
<td>$\chi$</td>
<td>Electron affinity for semiconductor</td>
<td>V</td>
</tr>
<tr>
<td>$\psi_{bi}$</td>
<td>Built-in potential</td>
<td>V</td>
</tr>
<tr>
<td>$\psi_s$</td>
<td>Surface potential</td>
<td>V</td>
</tr>
</tbody>
</table>
Appendix 6. SI Prefixes

<table>
<thead>
<tr>
<th>Multiple</th>
<th>Prefix</th>
<th>Symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{24}$</td>
<td>yota</td>
<td>Y</td>
</tr>
<tr>
<td>$10^{21}$</td>
<td>zetta</td>
<td>Z</td>
</tr>
<tr>
<td>$10^{18}$</td>
<td>exa</td>
<td>E</td>
</tr>
<tr>
<td>$10^{15}$</td>
<td>peta</td>
<td>P</td>
</tr>
<tr>
<td>$10^{12}$</td>
<td>tera</td>
<td>T</td>
</tr>
<tr>
<td>$10^{9}$</td>
<td>giga</td>
<td>G</td>
</tr>
<tr>
<td>$10^{6}$</td>
<td>mega</td>
<td>M</td>
</tr>
<tr>
<td>$10^{3}$</td>
<td>kilo</td>
<td>k</td>
</tr>
<tr>
<td>$10^{2}$</td>
<td>hecto</td>
<td>h</td>
</tr>
<tr>
<td>$10^{1}$</td>
<td>deca</td>
<td>da</td>
</tr>
<tr>
<td>$10^{0}$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>$10^{-1}$</td>
<td>deci</td>
<td>d</td>
</tr>
<tr>
<td>$10^{-2}$</td>
<td>centi</td>
<td>c</td>
</tr>
<tr>
<td>$10^{-3}$</td>
<td>milli</td>
<td>m</td>
</tr>
<tr>
<td>$10^{-6}$</td>
<td>micro</td>
<td>μ</td>
</tr>
<tr>
<td>$10^{-9}$</td>
<td>nano</td>
<td>n</td>
</tr>
<tr>
<td>$10^{-12}$</td>
<td>pico</td>
<td>p</td>
</tr>
<tr>
<td>$10^{-15}$</td>
<td>femto</td>
<td>f</td>
</tr>
<tr>
<td>$10^{-18}$</td>
<td>atto</td>
<td>a</td>
</tr>
<tr>
<td>$10^{-21}$</td>
<td>zepto</td>
<td>z</td>
</tr>
<tr>
<td>$10^{-24}$</td>
<td>yocto</td>
<td>y</td>
</tr>
</tbody>
</table>
References

   http://www.thompsonrd.com/NOTES%20INTRODUCTION%20TO%20POWER%20ELECTRONICS.pdf


   http://www.rohm.co.jp/web/japan/search/parametric/-/search/SiC%20Schottky%20Barrier%20Diodes

[8] ROHM semiconductor, SiC power modules - application notes.

   http://www.mitsubishielectric.co.jp/corporate/randd/list/device/b145/index.html


Acknowledgments

I would like to express my deep appreciations for my supervisors, Professor Hiroshi Iwai and Associate Professor Kuniyuki Kakushima, because they continuously gave me the thoughtful encouragement and helpful advices for my study. In addition, for their invaluable comments and warm encouragements in the meetings, I am deeply grateful to: Professor Yoshinori Kataoka, Visiting Professor Akira Nishiyama, Visiting Professor Nobuyuki Sugii, Professor Hitoshi Wakabayashi, Professor Kazuo Tsutsui, and Professor Kenji Natori. Moreover, I would like to express my thankfulness for teachers in the department of electrical and electronic engineering because I could improve my academic skills in the instructive lectures. Furthermore, I would like to express my gratitude to Assistant Professor Takamasa Kawanago who gave me the insightful comments and suggestions, particularly for my presentations.

I thank to my good colleagues in Iwai and Kakushima Laboratory, Wakabayashi Laboratory, Tsutsui Laboratory, and other Laboratories for their thoughtful associations and good friendships in addition to a lot of the active discussions of our studies. Especially, in various ways, I am grateful for the support and encouragement given by my seniors: Mr. Tomoya Shouji, Mr. Masaaki Motoki, Mr. Akinori Hasegawa, Mr. Shu Munekiyo, and Mr. Yoshimoto Nakamura. In particular, I would like to express my special thankfulness to my direct senior Ms. Mari Okamoto who taught me almost all experimental procedures. Furthermore, I am thankful to Kazuki Ohga of Iwai and Kakushima Laboratory and Kentaro Matsura of Wakabayashi Laboratory, for many active discussions with our good friendship and cooperation were precious time.
I would like to appreciate gracious support of secretaries: Ms. Nishizawa and Ms. Matsumoto.

Last but not least, I would like to thank my father Katsuhiro, my mother Ikuko, my younger brother Tatsuya, my grandparents, and my uncles/aunts for their everyday support and warm encouragements throughout my study and this thesis.

Without his/her assistance and encouragements, this bachelor thesis would not have been materialized.

Finally, I will never forget their heart-warming support, and I would like to advance continuously comprehensively to my objective in various fields of study.

Thank you.

February, 2015

Tomoyuki Suzuki