Resistive switching of CeO$_x$/SiO$_2$ stacked film based on anodic oxidation and breakdown

K. Kakushima
Tokyo Institute of Technology
Introduction to resistive RAM (RRAM)

Two terminal device

Advantage

• nonvolatile
• fast switching (<100ns)

• large volume
• compatible with BEOL

Fast switching speed to replace DRAM
Basic operation of resistive RAM (RRRAM)

**Forming process:**
Creation of oxygen defect chains for electron conduction

**Set/Reset mechanism:**
Oxygen compensation at the tip of filament to change the electron conductivity

Control of filament is the key for switching
Elimination of forming process
3D stacking of RRAM with cost reduction

RRAM with large volume is possible with the analogy of 3DNAND structure
### Reported materials for RRAM

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Switching type</strong></td>
<td>bipolar</td>
<td>bipolar</td>
<td>bipolar</td>
<td>bipolar</td>
<td>bipolar</td>
<td>bipolar</td>
<td>bipolar</td>
</tr>
<tr>
<td><strong>structure</strong></td>
<td>1T-1R</td>
<td>1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1R</td>
<td>1R</td>
</tr>
<tr>
<td><strong>Cell area (μm²)</strong></td>
<td>~1</td>
<td>~9000</td>
<td>0.0001 (10nm)</td>
<td>0.03</td>
<td>0.01 (100 nm)</td>
<td>~4</td>
<td>0.0004 (20nm)</td>
</tr>
<tr>
<td><strong>Speed</strong></td>
<td>N/A</td>
<td>~10 ns</td>
<td>~10 ns</td>
<td>500ns</td>
<td>N/A</td>
<td>N/A</td>
<td>1 μs</td>
</tr>
<tr>
<td><strong>Peak voltage</strong></td>
<td>&lt;2V</td>
<td>&lt;2.5V</td>
<td>&lt;1.5V</td>
<td>&lt;3V</td>
<td>&lt;3V</td>
<td>3.7 V</td>
<td>&lt;2.2V</td>
</tr>
<tr>
<td><strong>Peak current</strong></td>
<td>~50 nA</td>
<td>~30μA</td>
<td>~50 μA</td>
<td>~60 μA</td>
<td>20nA</td>
<td>150 nA</td>
<td>10μA</td>
</tr>
<tr>
<td><strong>HRS/LRS ratio</strong></td>
<td>&gt;100</td>
<td>&gt;100</td>
<td>&gt;10</td>
<td>&gt;30</td>
<td>&gt;100</td>
<td>&gt;10</td>
<td>100</td>
</tr>
<tr>
<td><strong>endurance</strong></td>
<td>10⁵</td>
<td>10¹²</td>
<td>5x10⁷</td>
<td>10⁶</td>
<td>10²</td>
<td>10²</td>
<td>10⁸</td>
</tr>
</tbody>
</table>

Selection from compatibility with CMOS process
Nice endurance, ON/OFF ratio of <100
RRAM should have large ON/OFF ratio for storage class memory application

Latency gap between DRAM and NAND

Large speed gap between DRAM and flash

Additional memory (storage class memory) is needed to fill this gap

Requirements

- nonvolatile
- switching speed of ~100ns
- large capacity (large ON/OFF ratio)
Issues of RRAM for storage class memory

- ON/OFF ratio comparable to flash with stable and low ON resistance should be achieved
- Forming-free desirable

A. Chen, APL, 2000

$R_{ON}$ depends on current limit

Still, only ratio increase by x10
Selectors for RRAM

1T1R \((6F^2)\)
- Large ON/OFF ratio
- High temp. process for Tr.

1D1R \((4F^2)\)
- Large ON/OFF required
- 3D integration possible

Oxide based, organic based pn junction reported, so far

I. G. Baek, IEDM 2005

More easy to use Si based Zener diode
Our target is based on condition to use Si-based diodes
Outline of the presentation

1. Introduction
2. Proposal of RRAM based on local breakdown and anodic oxidation
3. CeO$_x$/SiO$_2$ stacking on Si bottom electrodes
4. CeO$_x$/SiO$_2$ on NiSi$_2$ bottom electrodes
5. Conclusions
Basic operation of proposed RRAM

Local breakdown for set process
Anodic re-oxidation to recover the spot for reset process
Analytical model for set voltage ($V_{set}$)

$$V = t_{low-k} E_{low-k} + t_{high-k} E_{high-k}$$

$$= t_{low-k} E_{low-k} + t_{high-k} \frac{k_{low-k}}{k_{high-k}} E_{low-k}$$

$$= \left( t_{low-k} + t_{high-k} \frac{k_{low-k}}{k_{high-k}} \right) E_{low-k}$$

Large contrast in k-value is effective in reducing the $V_{set}$
Resistance at LRS ($R_{LRS}$) and HRS ($R_{HRS}$)

\[ R_{LRS} = R_{high-k} + R_{B.D.\ spot} \]

\[ R_{HRS} = R_{high-k} + R_{low-k} \]

Requirements for lower $R_{LRS}$ and higher $R_{HRS}$

- **High-k layer**
  - High electron conductivity
  - Narrow bandgap with low energy band offset in CB at interface

- **Low-k layer**
  - Low k-value
  - Wide bandgap with large CB band offset
Material selection for high-k and low-k

CeO$_x$ as high-k layer
SiO$_2$ as low-k layer

A strong candidate for set process
Material property for reset process

High-k layer should have high oxygen ion conduction at room temperature
Impact of low-k layer thickness for RRAM

Too thick low-k layer needs large forming voltage
High oxygen ionic conductivity for high-k layer can provide forming-free switching
SiO$_2$ layer formation with CeO$_x$

HF treatment

Thin SiO$_2$ layer is automatically formed at CeO$_x$/Si substrate interface even at as-deposited sample
Oxidation of Si with CeO$_x$

\[ Ce^{3+} + mSi + n_1O \rightarrow (Ce^{4+}) \rightarrow xCe_{silicate}^{3+} + (1-x)Ce^{4+} \]
\[ Ce^{4+} + ySi + n_2O \rightarrow yCe^{3+} + (1-y)Ce^{4+} + ySiO_2 \]

- Extract Ce$^{3+}$, Ce$^{4+}$ and silicates from Ce3$d_{5/2}$ spectra
- Silicates and SiO$_2$ from Si1$s$ spectra

\[ x=0.34, y=0.74 \]

-CeO$_x$ forms silicates rather than SiO$_2$
-x and y should be extracted for oxides with valence number fluctuation

-Extract Ce$^{3+}$, Ce$^{4+}$ and silicates from Ce3$d_{5/2}$ spectra
-Silicates and SiO$_2$ from Si1$s$ spectra
Outline of the presentation

1. Introduction
2. Proposal of RRAM based on local breakdown and anodic oxidation
3. $\text{CeO}_x/\text{SiO}_2$ stacking on Si bottom electrodes
4. $\text{CeO}_x/\text{SiO}_2$ on NiSi$_2$ bottom electrodes
5. Conclusions
Sample preparation of $\text{CeO}_x/\text{SiO}_2$ stack

Top electrode (TE): W  
Bottom electrode (BE): $p^+$Si (assuming Zener diode)

- $p^+$-Si substrate ($10^{18}$ cm$^{-3}$)
- SPM&HF cleaning
- CeO$_x$ evaporation at $300^\circ$C
- Top electrode (W) deposition
- Metal etching by RIE
- Backside contact (Al) formation
- Measurement
Polarity for resistive switching

Resistive switching only observed for counter clockwise
Might be the effect of oxygen ions with negative charges
RTO process for SiO$_2$ formation

Top electrode (TE): W
Bottom electrode (BE): p$^+$Si

$p^+$-Si substrate (10$^{18}$ cm$^{-3}$)

- SPM&HF cleaning
- 5%O$_2$, 850$^\circ$C, 5min
- CeO$_x$ evaporation at 300$^\circ$C
- Top electrode (W) deposition
- Metal etching by RIE
- Backside contact (Al) formation

Measurement
Impact of RTO-SiO$_2$ layer on ON/OFF ratio

With RTO-SiO$_2$, lower current limit, larger ON/OFF ratio from $10^3$ to $10^4$, owing to background leakage current suppression.
**p⁺Si and n⁺Si as bottom electrodes**

With n⁺Si BE, shift in $V_{set}$ of 1 V can be observed.
Band diagram with $p^{+}\text{Si}$ and $n^{+}\text{Si}$ BE

Workfunction difference shifts the voltage for switching
One of the supporting evidence for our model
Outline of the presentation

1. Introduction
2. Proposal of RRAM based on local breakdown and anodic oxidation
3. CeO$_x$/SiO$_2$ stacking on Si bottom electrodes
4. CeO$_x$/SiO$_2$ on NiSi$_2$ bottom electrodes
5. Conclusions
Materials for bottom electrodes

The resistance change is due to change of interfacial layer resistance.

Bad insulating property of interface layer for W, and Ti BE -> small ON/OFF ratio

Small Dielectric contrast between CeOx and NiO

$E_{\text{CeOx}}$ $E_{\text{IL}}$

Switching Layer
Due to high k-value of TiO$_2$, CeO$_x$ becomes the switching layer (behavior is similar to conventional RRAM) → Si based metal electrode is preferred.
Stacked sputtering process

Multi layered-deposition of Ni and Si layers

- Atomically flat interface can be achieved
- Interface position can be well-defined
- Applicable for scaled channel

No diffusion of Ni atoms into Si channels

Complete suppression of lateral encroachment

NiSi₂ case

NiSi₂ case

Stacked sputtering process is promising for electrodes for nano-scale devices
Silicide film stability on temperature

(8sets of Si/Ni (total thickness of 10nm))

XPS measurement of silicide film

Sheet resistance and surface roughness

Phase of the silicide is mainly NiSi₂

NiSi₂ films with stacked silicidation process are resistant up to 900 °C annealing

Wide process temperature window (350~900°C)
CeO$_x$/SiO$_2$ stack on NiSi$_2$ BE

SiO$_2$(100nm)/$p^+$-Si substrate

- Metal (NiSi$_2$) deposition & anneal
- Annealing at 500°C for 1min (N$_2$)
- Insulator (CeO$_x$) evaporation at 300°C
- Metal (W) deposition
- Metal etching
- Backside contact formation (Al)

Measurement

20mm

W

CeO$_x$

NiSi$_2$

SiO$_2$

$p^+$-Si

Al
TEM image of CeO$_x$/SiO$_2$ on NiSi$_2$ BE

Smooth NiSi$_2$ BE with uniform 1.5nm-thick SiO$_2$ confirmed
Resistive switching with NiSi$_2$ BE

Forming-free resistive switching can be obtained. ON/OFF ratio over $10^5$ is achieved.
Switching with different CeO$_x$ thickness

Thickness dependency on $V_{set}$ can be modeled with breakdown model
Resistance change with switching cycle

Read @ 0.1V

OFF(HRS) ~10^3X

ON(LRS) ~10^3X

CeO_x 6.5 nm

CeO_x 13 nm

Stable memory operation can be obtained
Effect of additional annealing for NiSi$_2$

ON/OFF ratio over $10^6$ can be obtained with surface oxidation of NiSi$_2$
Conclusions

• Resistive switching device for storage class memory application based on local breakdown and anodic oxidation is proposed and a guideline for material selection has been presented.

• Stacking of CeO$_x$ and SiO$_2$ has shown switching characteristics based on our model.

• Quality of SiO$_2$ layer is the key to increase the ON/OFF ratio.

• With NiSi$_2$ bottom electrode, forming-free switching with a ratio of $10^8$ has been achieved.