Effect of Surface Potential Control and Interface States for Silicon Nanowire Solar Cells

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Abstract

- Experimentally characterized the influence of surface potential and interface state density (Dit) in silicon nanowire (Si NW) photovoltaics (PV).
- Jsc degrades in thinner nanowires due to Dit present at side walls.
- Precise tuning of surface potential and reduction of interface state at passivation interfaces are important for improvements of Si NW solar cells.

Advantages and Issues in Si Nanowire PV

- Bandgap engineering
- Light trapping effect
- Steep degradation in Jsc with w nw > 80 nm
- No change in Voc
- FF decreased, indicating the importance of suppressing the effects of Dit

1. Photovoltaic Characteristics

1-1: Typical PV Properties

<table>
<thead>
<tr>
<th>Width (nm)</th>
<th>Height (nm)</th>
<th>Length (µm)</th>
<th>Voc (V)</th>
<th>Pmax (mW)</th>
<th>FF</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NW1</td>
<td>22</td>
<td>1.5</td>
<td>1.6</td>
<td>0.45</td>
<td>0.71</td>
<td>0.47</td>
</tr>
<tr>
<td>NW2</td>
<td>89</td>
<td>1.5</td>
<td>1.5</td>
<td>0.52</td>
<td>1.10</td>
<td>0.46</td>
</tr>
<tr>
<td>NW3</td>
<td>1.5</td>
<td>22</td>
<td>1.5</td>
<td>1.75</td>
<td>2.40</td>
<td>0.50</td>
</tr>
<tr>
<td>NW4</td>
<td>22</td>
<td>42</td>
<td>1.5</td>
<td>1.96</td>
<td>2.40</td>
<td>1.13</td>
</tr>
</tbody>
</table>

1-2: Nanowire Width Dependence

- Steep degradation in Jsc with w nw > 80 nm
- FF decreased, indicating the importance of suppressing the effects of Dit

2. Surface Potential Control

2-1: Changes in J-V Curves

- Jsc show two peaks around -5 V and 5 V in Si NWs
- Voc strongly modulated by V sub, in Si NWs

2-2: Changes in Nanowire and SOI Solar Cells

- More degradation of Jsc in smaller w nw
- Stronger effect of Voc in smaller w nw
- Highest Voc at V sub ~ -4 V

2-3: Width Dependency of V sub Modulation

- Effect of Dit is more dominant in thinner NWs.
- Improvements can be achieved by shielding the interface states with controlled surface potential.
- Optimized surface potential control is with trade-off in Jsc degradation and Voc enhancement

Device Structure

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- Improvements can be achieved by shielding the interface states with controlled surface potential.
- Optimized surface potential control is with trade-off in Jsc degradation and Voc enhancement

Conclusions

- Precise control of surface potential and Dit with passivation is important