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Electrical characteristics of atomic layer deposited lanthanum oxide (La$_2$O$_3$) films on In$_{0.53}$Ga$_{0.47}$As channel

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Chapter 1
Introduction

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1.1 The importance of semiconductors

There has been an unexampled growth of the semiconductor industry, since the bipolar transistor was invented in 1947. And this growth of semiconductor, has brought enormous impact on the work and life of mankind. There are kinds of electronic equipments serving our daily life around us. The core portion of electronic equipments is composed of semiconductors.

For example, the smart phones, which have brought great convenience to our life and work in recent years. Also today's computers, wireless units, and communication systems which provide superior performance. The electronics industry is a dominant industry in many nations and areas. It is no doubt that the importance of microelectronics in economic, social, and even political will continue to increase. As long as the laws of physics allow, there will be formidable progress in IC integration density and speed. The large worldwide investment in VLSI technology will continue impressive driving force [1.1].

And there is Apple’s all-new 64-bit A7 chip that promises to make apps much faster and games much better looking (Figure 1.1).

Figure 1.1 28-nm A7 chip made by Samsung


1.2 Evolution of LSI technology

Since the first integrated circuit (IC) has been invented over the past five decades, SSI, MSI, LSI, VLSI, With the increasing demand for information, the number of transistors in the integrated circuits is greatly increasing. But considering the cost and practicality, it is necessary to reduce the size of integrated circuits.

There is a very famous principle called Moore’s law (Figure 1.2) to explain transistor scaling. According to the equation (1.1), the number of transistors on the integrated circuit will increase to $P$ times every 18 months (1.5 years) [1.2].

\[
p = 2^{n/1.5}
\]

Therefore, $P$ will be 2.52 times in the 2 years later, will be 10.08 times in the Five years later, and will be 101.6 times in the 10 years later.

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**Figure 1.2** Moore’s law [1.2]
1.3 Scaling limit of CMOS transistors

Moore’s Law scaling has been accepted for more than half a century, it is possible to continue until 2030 year [1.2]. It is found that MOSFET was scale-down about 0.7 times approximately every 2 years (Figure 1.3).

![Miniaturization of MOSFET](image)

**Figure 1.3** Miniaturization of MOSFET

In the past forty years, CMOS technology evolution has followed the pathway of device scaling in order to achieve speed, density, and power improvements. The scaling rule which is called “constant-electric-field scaling” (Dennard et al., 1974) have stated “When device voltages and the device dimensions (both horizontal and vertical) reduced by the same rate, k (k > 1), finally the electric filed keeps the same.” (Figure 1.4). It makes sure that the reliability of the scaled device is not worse than that of the
original device. However, reducing the source-to-drain by MOSFET Scaling, that is the channel length of a MOSFET, led to short channel effects. When it is applied to Digital electronic circuit, the most undesirable short channel effects bring a reduction in the gate threshold voltage at which the device turns on, especially at high drain voltages.

![Diagram of MOSFET devices](image.png)

**Figure 1.4** Principles of MOSFET constant-electric-field scaling [1.1]

Because of the MOSFET constant-electric-field scaling, it shows that both the voltage and the current scaled down by the same factor, k (k > 1). There is a most significant conclusion from constant-electric-field scaling: If the device dimensions and the power supply voltage are scaled down, the circuit will speed up by the same factor, k (k > 1). Furthermore, power dissipation per circuit, which is proportional to VI, is reduced by $k^2$ (Table 1.1).
### Table 1.1 Scaling MOSFET device and circuit parameters [1.1]

<table>
<thead>
<tr>
<th>MOSFET Device and Circuit Parameters</th>
<th>Scaling Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device dimensions ((t_{ox}, L, W))</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Doping concentration ((N_d))</td>
<td>(k)</td>
</tr>
<tr>
<td>Current drift ((I))</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Voltage ((V))</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Capacitance</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Depletion-layer width ((W_d))</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Circuit delay time</td>
<td>(1/k)</td>
</tr>
<tr>
<td>Power dissipation per circuit</td>
<td>(1/k^2)</td>
</tr>
<tr>
<td>Power density</td>
<td>1</td>
</tr>
</tbody>
</table>

This is very high performance of semiconductor technology. But there is technology node (or Feature size) of transistor scaling, which is called “device pitch” or “gate pitch” [1.4]. April 13, 2005, Gordon Moore himself, said in an interview, " Moore's Law will not last long, because the transistor would eventually be reduced to the limit of atomic levels. "[1.2]. Although, Moore’s Law scaling was limited, in order to pursue higher performance, researchers continue to introduce new technology, such as new structures and new materials.

**Figure 1.5** shows the present MOSFETS released by Intel Corporation. In order to improve the mobility, a new technology of silicon germanium(SiGe) Strained silicon which 65nm was introduced in 2005. In order to reduce gate leakage current, another new technology of High-k/Metal gate which is 40nm ~ 28nm were introduced from 2007 to 2009. To realize three dimensional structure (3D) device, Intel introduced Fin-FET which is 20nm in 2011. The technologies of Semiconductor device will continue to develop, but it is difficult to improve the performance of semiconductor device just by miniaturization.
1.4 Advantages of III-V compound semiconductors

It has been showned the basic structure of MOSFET in Figure 1.4. It is a three-terminal device which is designed with three terminals, gate (G), drain (D) and source (S).

The total power dissipation in a CMOS circuit is composed by two parts (Figure 1.6): static electricity (the power of a device is OFF state) and dynamic electricity (the power of a device is ON state).
In order to introduce the relation of power dissipation ($P_d$) and drive current ($I_{on}$), using the device parameters, we can approximately obtain the following equations [1.6].

$$P_d \approx \alpha f C_l \cdot V_{dd}^2 + I_o \cdot 10^\frac{V_t}{S} \cdot V_{dd} + I_l \cdot V_{dd} \quad \text{Eq. (1.2)}$$

$$I_{ON} \approx C_g (V_{dd} - V_t) \cdot v(V_{dd}) \quad \text{Eq. (1.3)}$$

In the two equations, $\alpha$ is a constant, $f$ is the operating frequency, $C_l$ is the load capacitance, $I_o$ is the drain current which is at $V_g$ or $V_t$, $S$ is the subthreshold swing value. $I_l$ is the leakage current, $C_g$ is the gate capacitance, $v$ is the electron speed near the source region.

The first section of Eq. (1.2) is the effective power which is from the power supply voltage when the transistor is operating at a clock frequency of $f$. The second section of
Eq. (1.2) is decided by the instantaneous pass of current which is created as a result of necessary time for one transistor switching off in an inverter circuit. The third section of Eq. (1.2) represents static power dissipation which is decided by leakage current. According to Eq. (1.2), it shows that if the conditions of lower $V_{dd}$, higher $V_{th}$, smaller $S$, and lower $I_l$ are satisfied, the Low Power Consumption of MOSFETs is possible. However, from Eq. (1.3), it show that lower Vdd and higher Vth will lead to dramatic decrease in Ion. Besides, in order to reduce the gate leakage current, the thickness of the gate oxide should be large enough. This is a contradiction with the need of increasing Ion. Therefore, it becomes difficult to satisfy a high performance and low power dissipation just with traditional scaling methods.

In order to obtain both requirements of a high performance and low power dissipation, it is necessary to use high mobility channel materials. Because it is difficult to improve the performance of semiconductor device just by miniaturization, so if use high mobility channel materials to get low supply voltage which can creat high drive current, low power consumption of LSI is likely to be realized. According to Eq. (1.4), it should be explained.

$$P = \alpha NCf V_{dd}^2 + NI_{off} V_{dd}$$  \hspace{1cm} \text{Eq. (1.4)}$$

In this equation, $P$ is the power consumption of LSI (Large scale integrated circuits), $\alpha$ is a constant value, $V_{dd}$ is the Supply voltage, $f$ is the Operating frequency, $I_{off}$ is the leakage current of off-state, $C$ is the Capacity of a transistor, $N$ is the number of transistors. Therefore, in order to obtain low power consumption, it should reduce the Supply voltage ($V_{dd}$). Furthermore, it should use high mobility channel materials.
III-V materials have very high electron mobility. From Table 1.2, It shows that the electron mobility of In$_{0.53}$Ga$_{0.47}$As (one of III-V materials) is about 12 times than Silicon (Si) [1.5]. InGaAs semiconductor is expected to realize the low power consumption, but the high interface state between insulating film and InGaAs remain a challenge.

**Table 1.2** Compare of electron mobility[1.5]

<table>
<thead>
<tr>
<th>Electron mobility (cm$^2$/Vs)</th>
<th>Si</th>
<th>In$<em>{0.53}$Ga$</em>{0.47}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>600</td>
<td>7800</td>
</tr>
</tbody>
</table>

1.5 **High-k material of La$_2$O$_3$ gate stacks on InGaAs**

Now, I want to introduce lanthanum oxide (La$_2$O$_3$) for InGaAs MOS capacitors. High-k material of La$_2$O$_3$ has a high dielectric constant (K = 24), and high quality interface which have been reported [1.7]. Lanthanum could form a complicated network of noncrystalline structure with Si and Ge [1.8], and form an interfacial layer on the oxide/substrate.

In order to compare with La$_2$O$_3$, I use the Hafnium oxide (HfO$_2$) to do an analysis of XPS spectrum (Figure 1.7). After analysis, an interfacial layer which is called lanthanum indium gallium oxide (LaInGaO) is formed on the Interface between La$_2$O$_3$
and the substrate and good interface characteristics have been obtained.

Figure 1.7  XPS spectrum
**Figure 1.8** shows that HfO₂, etc. form the oxide at the interface with In₀.₅₃Ga₀.₄₇As [1.9].

![Interface layer of oxide](image)

**Figure 1.8** Interface layer of oxide

**Figure 1.9** shows that in order to control the supply of oxygen to the insulating film, lanthanum (La) dissolves the oxide of gallium (Ga) and indium (In), and form an interface layer which is called LaInGaO. Interface of InGaAs and LaInGaO is electrically inactive, so that it is stable to reduce interface state density (Dit) [1.10].

![Interface layer of LaInGaO](image)

**Figure 1.9** Interface layer of LaInGaO
1.6 Purpose of this thesis

High-k/ In$_{0.53}$Ga$_{0.47}$As MOS capacitor which is a combination of high-mobility channel material In$_{0.53}$Ga$_{0.47}$As and high-k material is considered as a candidate for the next MOSFET generation. It has been reported that La$_2$O$_3$ which has a high dielectric constant (k ~ 27) has a good interface characteristic by previous studies [1.11]. La$_2$O$_3$ which is in La$_2$O$_3$/InGaAs capacitor can obtain lower interface state than Al2O3, using the ALD method that is suitable for 3D devices, such as Fin-FET [1.12]. However, the reports that is about the dependance of electrical characteristics and interface characteristics by detailed ALD conditions are considerably less.

In this study, I will report on the effects of electrical characteristics and interface characteristics under the conditions of ALD deposition conditions. In order to obtain high quality dielectric films, I will use lanthanum oxide (La$_2$O$_3$) to form a interface layer on In$_{0.53}$Ga$_{0.47}$As by Atomic Layer Deposition (ALD) and then investigate the deposition conditions which are impacted by the electrical characteristics. It is necessary to develop a suitable ALD process.
1.7 References


[1.5] Homepage of Intel.


[1.9] D. Zadeh et al., 2012SSDM.


[1.12] H.Oomine, etc.“ Improvement of La2O3/ In0.53Ga0.47As interface property using atomic-layer-depositon” Japan Society of Applied Physics .Spring, 2013.
Chapter 2
Fabrication and Characterization Method

2.1 Atomic layer deposition (ALD) technology
   2.1.1 Introduction of ALD method
   2.1.2 ALD self-limiting mode

2.2 The detailed processes of fabrication
   2.2.1 InGaAs substrate cleaning
   2.2.2 RF Magnetron Sputtering
   2.2.3 Vacuum evaporation for Aluminium electrode
   2.2.4 Post metallization annealing (PMA)

2.3 References
2.1 Atomic layer deposition (ALD) technology

2.1.1 Introduction of ALD method

Atomic layer deposition (ALD), which was called as atomic layer epitaxy (ALE) in the past, was earliest invented by Dr. T.Suntola in Finland to deposit polycrystalline and amorphous thin films in 1974. ALD is a method that plating the material which is a single atomic film into the surface of the substrate layer by layer (Figure 2.1).

![Figure 2.1](image)

**Figure 2.1** One schematic cycle of Atomic layer deposition [2.1].
Atomic layer deposition (ALD) is similar with regular chemical deposition. However, in the process of the atomic layer deposition, the chemical reaction of new atomic layer is directly associated with the previous atomic layer. This approach allows that only one atomic layer can be deposited each reaction. There are two main chemical reactants which are generally referred to precursors, in the process of the atomic layer deposition. ALD is used to deposit high quality thin films, when one cycle of ALD is completed, it continue to the next cycle. It is possible by controlling the number of reaction cycles, and the material of the correct thickness is deposited. In ALD, the reactants are pushed onto the substrate at one time, excess reactants and reaction by-products are purged out.

Atomic layer deposition (ALD) method is a kind of Chemical Vapor Deposition (CVD) method which is based on binary reactions such as \((a + b) \rightarrow \text{Product}\). Because of CVD using a binary reaction, the reactants \(a\) and \(b\) are appeared at the same time, and then form the film on the substrate continuously [2.2].

2.1.2 ALD self-limiting mode

ALD self-limiting mode is that the constant growth speed is not depended on the supply time. On the other hand, the growth rate increases proportionally with the supply time. Although the supply of \(\text{La(PrCp)}_3\) is varied between 2.5s ~ 10s, the growth rate is fairly constant with the growth temperature is below 175°C. When the growth temperature is 200°C or more, the growth rate is increasing along with the supply time. The water (H₂O) supply time is the same result [2.3-2.4].
2.2 The detailed processes of fabrication

2.2.1 InGaAs substrate cleaning

As cleaning materials, I choose deionized water (DI water), acetone, and alcohol to clean the InGaAs substrates. There are another two materials: hydrofluoric acid (HF, 20%) and (NH₄)₂S (ammonium sulfate). HF is weak poisonous liquid acid, which is formed by solution of hydrogen fluoride in water. (NH₄)₂S is acidic colorless prismatic crystal, and soluble in water.

First, I will get rid of the oil which is covered on the substrate surface with alcohol and acetone in an ultrasonic environment. Second, in order to get rid of native oxides, I will dip the substrate into concentrated hydrofluoric acid (HF, 20%) for 3 minutes. Subsequently, I will rinse the sample with deionized water (DI water) which is water that almost all of mineral ions are removed, highly purified water. Then, in order to form a passivated sulfur surface, I dip the substrate into (NH₄)₂S solution (concentration 8%) rapidly at room temperature (25 °C) for 3 minutes. The final step is transferring the cleaned substrate to the deposition chamber in order to avoid the oxidation again because of prolonged exposure to air.

2.2.2 RF Magnetron Sputtering

Sputtering is a vacuum processes which is frequently used to deposit ultra-thin films that are made up of various materials on the substrates and extensively used in the
semiconductor industry. After ALD-La$_2$O$_3$-10 nm film was deposited, it should form the gate metal electrode tungsten (W-5nm) and titanium nitride (TiN-45nm) by radio frequency (RF) magnetron sputtering with argon (Ar) gas. At the beginning, it is necessary to generate a glow discharge by applying a negative voltage to the target in order to ionize the argon (Ar) gas atoms. On the other hand, strike the argon (Ar) gas ions on the surface of the target violently at a high speed. This will make the particles (atoms and molecules) which make up the film-forming material of the target to flip violently. The particles would deposit on the surface of the substrate forcefully to form the TiN/W gate electrode. In this process, I set a power of 150W RF current to produce a “plasma” which is ionized gas consisted of electrons and gas ions in a high temperature state.

![RF Magnetron Sputtering Diagram](image)

**Figure 2.2** The schematic of RF magnetron sputtering
2.2.3 Vacuum evaporation for Aluminium (Al) electrode

In my study, I deposit the backside contact of Aluminium (Al) by Vacuum evaporator. Setting aluminium (Al) on the boat and heat it up to the boiling point by Joule heating as a means for growing thin aluminum. Keeping the pressure of the chamber to $10^{-3}$Pa, the boat can not became melted, because melting point of the boat is higher than boiling point of Aluminium.
2.2.4 Post metallization annealing (PMA)

Post metallization anneal (PMA) is an annealing method that is very effective to repair the defects on the insulating film that are created during the fabrication process. In this study, post metallization anneal (PMA) is carried out under the conditions of forming gas (FG) (N\textsubscript{2}:H\textsubscript{2} = 97\%:3\%) and annealing temperature 320\degree C.

![Infrared system lamp furnace for PMA in Iwai Laboratory](image)

**Figure 2.4** Infrared system lamp furnace for PMA in Iwai Laboratory
2.3 References


Chapter 3
Process condition for Atomic Layer Deposition (ALD)

3.1 Device Fabrication Process

3.2 Effect of substrate temperature and post metallization annealing (PMA)

3.2.1 Fabrication process for MOS capacitor

3.2.2 Capacitance-voltage (CV) characteristics

3.2.3 Temperature dependence of the interface state density (Dit)

3.2.4 Effect of PMA

3.2.5 Effect of H₂O supply amount

3.3 References
3.1 Device Fabrication Process

Figure 3.1 shows one cycle of ALD reaction for La$_2$O$_3$ film, and Table 3.1 shows the cycle conditions of ALD reaction.

Here, I will introduce the deposition method of Atomic layer deposition (ALD). At the beginning, I would supply the water to the surface of the substrate. Then, flush the surface of the substrate with argon (Ar) to remove any excess water. Subsequently, supplying the raw material of lanthanum (La), and make it oxidization on the surface of the substrate. Then, in the same way, I will remove the excess material of lanthanum (La) with argon (Ar). But, if make use of the inert gas of Nitrogen (N), there maybe is the same effects.
Referring to the bellowing Table 3.1, I set up the supply time of La(PrCp)₃ to 5 seconds, H₂O to 5 seconds, and Ar to 10 seconds. And then it need to exhaust the useless gas, so I set up the exhaust time of La(PrCp)₃ to 20 seconds, H₂O to 50 seconds, and Ar to 30 seconds.

**Table 3.1** Cycle condition for ALD

<table>
<thead>
<tr>
<th></th>
<th>La(PrCp)₃</th>
<th>H₂O</th>
<th>Ar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply time (sec.)</td>
<td>5</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Exhaust time (sec.)</td>
<td>20</td>
<td>50</td>
<td>30</td>
</tr>
</tbody>
</table>
Under the conditions of Table 3.1, we continue to do the loop experiments and watch the rate of ALD. Referring to the bellowing Figure 3.2, the thickness of lanthanum oxide (La$_2$O$_3$) is depended on the cycles of ALD. When the substrate temperature is setted up to 150 °C, as long as one cycle of ALD has been carried out, the thickness of lanthanum oxide (La$_2$O$_3$) will be deposited for 0.14 nm. Moreover the thickness of La$_2$O$_3$ has a liner relation to ALD cycles.

![Figure 3.2](image_url)  
*Figure 3.2*  The relation of La$_2$O$_3$ thickness and ALD cycle.
3.2 Effect of substrate temperature and post metallization annealing (PMA)

3.2.1 Fabrication process for MOS capacitor

According to the steps of Figure 3.3, a MOS capacitor was fabricated. After the substrate cleaning, the substrate would be transferred to ALD chamber for lanthanum oxide (La$_2$O$_3$) film-forming which is followed with metal deposition by RF magnetron sputtering. And in this study, the TiN (45 nm)/W (5 nm) metal gate was fabricated to be used as the gate electrode. And in order to form a back contact, finally deposite Aluminum to the back side of the In$_{0.53}$Ga$_{0.47}$As /InP substrate. (Figure 3.3)
In this fabrication process, the substrate which n-In$_{0.53}$Ga$_{0.47}$As (N$_D$: $2 \times 10^{16}$ cm$^{-3}$) substrates were epitaxially grown on InP substrate was used and in the conditions of growth temperature 150°C and 180°C, deposit the ALD-La$_2$O$_3$ films for 75 cycles. Finally, MOS capacitor was Manufactured. (Figure 3.4)

Figure 3.4  The structure of MOS capacitor.
3.2.2 The CV characteristics

Figure 3.5 shows the CV characteristics of created capacitor. When the substrate temperature is 150°C, I observes that there is less dispersion at each measurement frequency, and all the C-V curve is close to the ideal results.

![Figure 3.5 CV characteristics of ALD-La₂O₃/InGaAs MOS capacitor (CET =2.3 nm).](image)

Figure 3.6 compares the Capacitance-Voltage (CV) characteristics with different frequency dispersion. The samples appear superior CV responses at the growth temperature of 150°C. However, at the growth temperature of 180°C, it appears the
hysteresis on the samples. The reason is considered to the formation of element arsenic (As) on the interface of La$_2$O$_3$/InGaAs. And it is possible that oxide species of arsenic (AsO$_x$) is formed, but in the heat treatment environment, it is not very stable and collapse into highly stable compound GaO$_x$ and element arsenic (As) [3.1-3.2].

**Figure 3.6**  \( C-V \) characteristics of TiN/W/ALD-La$_2$O$_3$/InGaAs capacitors deposited at (a) 150°C and (b) 180°C annealed in FG at 320°C.

### 3.2.3 Temperature dependence of the interface state density (Dit)

Below I will explain the investigation out of the film-forming temperature conditions. With the substrate temperature increasing, there is clearly an increasing trend on the CET. I thought ligand which is the raw material of lanthanum is destroyed, the non-volatile by-products are formed, CET is increasing.
In the range of substrate temperature which is from 150°C to 160 °C, the lowest interface state ($8 \times 10^{11}$ eV$^{-1}$cm$^{-2}$) is clearly examined (Figure 3.7). It could be possibly concluded that the minimum value for lowest annealing temperatures is attributed to the presence of remaining carbon (C) atoms within the synthesized dielectric film that spreads to the interface with the heat treatment temperature increasing. Further physical analysis of the thin film is needed to describe the characteristics of the film quality and its impurity levels. Regulating the exhaust time and purge during the stacking cycles has been reported to be effective in decreasing the proportion of impurities that are contained in the dielectric layer [3.3-3.5]. Although there are good properties by performing the FGA heat treatment when the substrate temperature in the range of 150°C to 230°C. But it still requires more Optimized experimental procedures.

![Figure 3.7 FGA temperature effect on Dit](image)
3.2.4 Effect of PMA

**Figure 3.8** shows the calculated PMA temperature dependence of the interface state density ( Dit ) under the temperature of each deposition using (a) Hysteresis method  (b) Conductance method. From **Figure 3.8** (a), it is clearly that Hysteresis is suppressed at 150°C and when PMA is 370°C it is rotating in the opposite direction at 180°C. In addition, it can be seen that when the PMA temperature is 420°C, the interface state ( Dit = 6.3 × 10^11 eV·cm^−2) of 150°C is lower than that of 180°C from fig. 2 (b). From the above description, it is suggested that the form of arsenic oxides ( As O x ) has been suppressed by La_2 O_3 /InGaAs interface by low-temperature deposition[3.6].

![Figure 3.8](image)

**Figure 3.8**  (a) Hysteresis at V_f and  (b) Dit values at E_i + 0.1 eV as a function of PMA temperature.
ALD-La$_2$O$_3$ layer is a polycrystalline film. Figure 3.9 shows the TEM images, from the experimental results, in the condition of no forming gas annealing (FGA), roughness occurs on the interface of La$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As during the deposition. After FGA 320°C, the interface roughness has decreased and flattening of the La$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface is checked. Moreover, it is considered that the formation of interfacial layer (LaInGaO) is confirmed.

**Figure 3.9** TEM cross-sectional observation
3.2.5 Effect of H$_2$O supply amount

Having a high leakage current is a major obstacle of the ALD-La$_2$O$_3$ film. Perhaps it is because the ALD-La$_2$O$_3$ film has a low density. And because of poly crystalline structure and high impurity levels, ALD-La$_2$O$_3$ film which is formed, using water (H$_2$O) vapor and La(PrCp)$_3$ has high leakage currents.

It is possible that increasing the oxidation time can get a high CET value in the condition of low leakage currents. It means that the high energy oxidation process is necessary, such as H$_2$O or plasma etc. for high quality artificial film. In my study, I optimize the water (H$_2$O) vapor time, in order to obtain more high scalability film deposition. Figure 3.10 shows the functional of interface state density (Dit) and CET. Figure 3.11 shows the functional of gate leakage current (Jg) and CET. According to this two figures, it is possible to reduce the leakage current by increasing the H$_2$O supply amount. When CET is 1.7nm, further scaling can be achieved by increasing the amount of H$_2$O supply amount.
Figure 3.10  Functional of Interface state density (Dit) and CET

Figure 3.11  Functional of Gate leakage current (Jg) and CET

References:
3.3 References


Chapter 4

Conclusions

4.1 Conclusions of this study
4.1 Conclusions of this study

In this study, we evaluate electrical characteristics of atomic layer deposited lanthanum oxide (La$_2$O$_3$) films on In$_{0.53}$Ga$_{0.47}$As channel.

In chapter 1, I have introduced the development situation of semiconductor technology and the superiority of III-V materials. But the high interface state is still a remaining problem.

In chapter 2, I have introduced the Atomic layer deposition (ALD) technology and detailed fabrication processes.

In chapter 3, I have used the gas materials of La($^{i}$PrCp)$_3$ and H$_2$O to deposit ALD- La$_2$O$_3$ films and got some results: ①When the substrate temperature is 150 °C, the thickness of lanthanum oxide (La$_2$O$_3$) has a liner relation to ALD cycles(y ~ 0.14x). ②In the range of substrate temperature which is from 150 °C to 160 °C, the lowest interface state (8 $\times$ 10$^{11}$eV$^{-1}$cm$^{-2}$) is clearly examined. ③After FGA 320 °C, the interface roughness has decreased and flattening of the La$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface is checked. ④It is possible to reduce the leakage current and achieve further scaling by increasing the H$_2$O supply amount. Using La($^{i}$PrCp)$_3$ and H$_2$O is considered as the growth condition of ALD. If the amount of water is not enough, the reaction of La($^{i}$PrCp)$_3$ and H$_2$O can not carry out completely. Increasing the H$_2$O supply amount to get rid of ($^{i}$PrCp)$_3$ can improve the film quality.⑤La$_2$O$_3$ has a strong hygroscopic behavior, with exposure to air, the films will quickly transform into mixtures of LaO(OH) and La(OH)$_3$. But La(OH)$_3$ is more reactive than
La$_2$O$_3$, films as thin as 10 nm, after high-temperature heat treatment in vacuum, LaO(OH) and La(OH)$_3$ can totally converted to hexagonal La$_2$O$_3$. 
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