Electrical characteristics of atomic layer deposited lanthanum oxide (La$_2$O$_3$) films on In$_{0.53}$Ga$_{0.47}$As channel

Department of Electronics and Applied Physics
Iwai/Kakushima Lab
12M53480 Lu Guoqiang

Tokyo Institute of Technology
Outline

1. Background of this study
2. Experimental Procedure
3. Results and Discussion
4. Conclusions
Background I: Scaling limit of CMOS transistors

\[ p = 2^{n/1.5} \quad \text{Eq. (1.1)} \]

The number of transistors on the integrated circuit will increase to \( P \) times every 18 months (1.5 years).

Principles of MOSFET constant-electric-field scaling:

Both the voltage and the current scaled down by the same factor, \( k \) (\( k > 1 \)), finally the electric filed keeps the same.
Background I: low power consumption of LSI

Miniaturization of MOSFET

MOSFET was scaled-down about 0.7 times approximately every 2 years.

Feature size

- 250 → 180 → 130 → 90 → 65 → 45 → 32 → 22 → 16 (nm)

Technology cycle

- High mobility channel materials
- Low supply voltage to create high drive current
- Low power consumption of LSI is likely to be realized

It is difficult to improve the performance just by miniaturization.
Background I: high mobility channel materials and the power consumption of LSI

The electron mobility of In$_{0.53}$Ga$_{0.47}$As (one of III-V materials) is about 12 times than Silicon. InGaAs semiconductor is expected to realize the low power consumption, but the high interface state between insulating film and InGaAs remains a challenge.

**Power consumption of LSI**

$$P = \alpha NCfV_{dd}^2 + NI_{off}V_{dd}$$

- $P$: the power consumption of LSI (Large scale integrated circuits),
- $\alpha$: is a constant value,
- $V_{dd}$: the Supply voltage,
- $f$: the Operating frequency,
- $I_{off}$: the leakage current of off-state,
- $C$: the Capacity of a transistor,
- $N$: the number of transistors.

**Compare of electron mobility**

<table>
<thead>
<tr>
<th>Electron mobility (cm$^2$/Vs)</th>
<th>Si</th>
<th>In$<em>{0.53}$Ga$</em>{0.47}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>600</td>
<td>7800</td>
</tr>
</tbody>
</table>

- High mobility channel material is required.
- Reducing the Supply voltage ($V_{dd}$) is required for low power consumption of LSI.

Ref: intel HP
**Background II: High-k material of La$_2$O$_3$ gate stacks on InGaAs**

<table>
<thead>
<tr>
<th>Interface layer of oxide</th>
<th>Interface layer of LaInGaO</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Metal gate</strong></td>
<td><strong>Metal gate</strong></td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>La$_2$O$_3$</td>
</tr>
<tr>
<td>Oxide spices</td>
<td>LaInGaO</td>
</tr>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As</td>
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</tbody>
</table>

- HfO$_2$, etc. form the oxide at the interface with In$_{0.53}$Ga$_{0.47}$As.

- In order to control the supply of oxygen to the insulating film, lanthanum (La) dissolves the oxide of gallium (Ga) and indium (In), and form an interface layer which is called LaInGaO.

- Interface of InGaAs and LaInGaO is electrically inactive, so that it is stable to reduce interface state density (Dit)

*Ref:*
D. Zadeh et al., 2012 SSDM
D. Zadeh et al., SSE 82(2013) 29
Experimental Procedure

One cycle of ALD reaction for $\text{La}_2\text{O}_3$ film

Fabrication process for MOS capacitor

- Acetone-ethanol degreasing
- Native oxide removal (HF 20%)
- $\text{(NH}_4\text{)}_2\text{S}$ surface treatment
- ALD-$\text{La}_2\text{O}_3$ deposition (10 nm)
- Gate metal (TiN/W) deposition by RF sputtering
- Gate pattern by ICPRIE
- FGA (3% $\text{H}_2$) for 5 min
- Backside $\text{Al}$ contact

The structure of MOS capacitor
Experimental Procedure

Cycle condition for ALD

<table>
<thead>
<tr>
<th></th>
<th>La(PrCp)$_3$</th>
<th>H$_2$O</th>
<th>Ar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply time (sec.)</td>
<td>5</td>
<td>5</td>
<td>10</td>
</tr>
<tr>
<td>Exhaust time (sec.)</td>
<td>20</td>
<td>50</td>
<td>30</td>
</tr>
</tbody>
</table>

As long as one cycle of ALD has been carried out, the thickness of lanthanum oxide (La$_2$O$_3$) will be deposited for 0.14 nm.

The linear relation of La$_2$O$_3$ thickness and ALD cycle

Sub temp. = 150°C

y = 0.14x

Sub: Si

Sub: In$_{0.53}$Ga$_{0.47}$As

ALD Cycles
Results and Discussion

CV characteristics of ALD-La$_2$O$_3$/InGaAs MOS capacitor

There is less dispersion at each measurement frequency, CV characteristics close to the ideal can be obtained by a low-temperature deposition.

FGA temperature effect on $D_{it}$

In the range of substrate temperature which is from 150°C to 160°C, the lowest interface state ($8 \times 10^{11}$eV$^{-1}$cm$^{-2}$) is clearly examined by FGA 320°C.
TEM images

- ALD-La$_2$O$_3$ layer is a polycrystalline film.
- Roughness occurs on the interface of La$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As during the deposition.
- After FGA 320°C, the interface roughness has decreased and flattening of the La$_2$O$_3$/In$_{0.53}$Ga$_{0.47}$As interface is checked.
- Moreover, it is considered that the formation of interfacial layer (LaInGaO) is confirmed.
Effect of H$_2$O supply amount

![Graph showing Interface state density and CET](image1)

![Graph showing Gate leakage current and CET](image2)

- **CET=1.7nm**  \( D_{it}=2.4\times10^{12}\text{eV}^{-1}\text{cm}^{-2} \)
- It is possible to reduce the leakage current and achieve further scaling by increasing the H$_2$O supply amount. (CET=1.7nm)

References:
Conclusions

- Increasing the H₂O supply amount is an effective method to improve the film quality and achieve further scaling.

- ALD-La₂O₃ has formed an interfacial layer LaInGaO by heat treatment, I obtained a low interface state density \( \left( D_{it} = 8 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2} \right) \).

- Low-temperature film-forming can prevent the destruction of the ligand and is possible to realize insulating film growth with few impurities in the film by the formation of volatile by-products.
Thank you for your attention.
PMA at 320°C in FG (N₂:H₂=97%:3%)

(a) Growth temp. = 150°C
Hysteresys at $V_{fb} = 30$ mV
CET = 2.6 nm

(b) Growth temp. = 180°C
Hysteresys at $V_{fb} = 420$ mV
CET = 3.0 nm

- 5 kHz
- 10 kHz
- 100 kHz
- 1 MHz
Background II: High-k material of La$_2$O$_3$ gate stacks on InGaAs

XPS spectrum

![XPS spectrum graph](image)