Influence of Technological and Geometrical Parameters on Low-frequency Noise in SOI Omega-gate Nanowire MOSFETs

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Introduction 1 - Low-frequency noise in MOSFETs

Noise sources in MOSFET:
- Carrier number fluctuations (CNF)
- Mobility fluctuations (MF)

LFN measurement in MOSFETs:
Efficient diagnostic tool of interface properties

Introduction 2 - Silicon nanowire MOSFETs

- **Si nanowire (NW) MOSFETs**
  - High immunity against short channel effect (SCE), drain induced barrier lowering (DIBL)
  - Better electrostatic control

Advantages in further downscaling and power consumption

- **Aggressively scaled FET (channel area size)**
  - Difficulty of detailed measurement/characterization (split C-V, charge pumping…)

LFN measurement is applicable in scaled MOSFETs: Powerful diagnosis tool for ultra-scaled nanowire devices

![Tri-gate nanowire FET](image)
Our study: SOI omega-gate NW MOSFETs

- Contribution of surface orientation
  (NW top vs. side-wall surfaces)
- Technological device parameters
  (additional H$_2$ anneal, stressor impact)
- Detailed properties of LFN

Recent reports of LFN

- Application to scaled multigate devices
  Double-gate, Tri-gate, Gate-all-around…

but… few reports for

- Contribution of multiple surface orientation
- Technological device parameters

Purpose of this work

Tri-gate NWs


GAA-NWs


Outline

✓ Introduction & Motivation

✓ SOI starting omega-gate nanowire devices

✓ Experimental results
  LFN \((S_{ld}/I_d^2)\) behavior in 1-channel omega-gate NWs
  Flat-band voltage noise \(S_{Vfb}\)
  Coulomb scattering parameter \(\alpha_{sc}\mu_{eff}\)
  Gate oxide trap density \(N_t\)
  \(V_d\) influence (linear vs. saturation regions)

- Impacts of technological device parameter and geometrical \((W_{top} & L_g)\) change -

✓ Conclusions
SOI Omega-gate nanowire MOSFETs

Technological splits:

✓ Channel material: Si or sSi
✓ Ch. Orientation: [110] or [100]
✓ w/ or w/o H₂ anneal process

High-k/metal gate stack:
HfSiON/TiN (EOT~1.25nm)

<table>
<thead>
<tr>
<th>Technological splits of Ω-gate NW NMOS FETs</th>
<th>NW height $H_{NW}$</th>
<th>Narrowest NW top width $W_{top}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOI ([110]-oriented)</td>
<td>11nm</td>
<td>13nm</td>
</tr>
<tr>
<td>SOI with H₂ anneal</td>
<td>10nm</td>
<td>11nm</td>
</tr>
<tr>
<td>[100]-oriented SOI</td>
<td>10nm</td>
<td>10nm</td>
</tr>
<tr>
<td>Strained-SOI (sSOI)</td>
<td>11nm</td>
<td>11nm</td>
</tr>
</tbody>
</table>
SOI Omega-gate nanowire MOSFETs

- Ideal properties in all the devices; SS~70mV/dec
- Strained-SOI (sSOI) NW effectively enhances $I_{ON}$

![Diagram of SOI Omega-gate nanowire MOSFETs with labels for gate, source, and drain orientations.](image)

Normalized with $W_{tot} = W_{top} + 2H_{NW}$

$I_{on}$ gain from strain @ $V_g = V_d = 0.9V$ +137%

- $V_d = 0.9V$
- $V_d = 40mV$

$L_g = 22-23nm$
Narrowest NW

Source: [Reference Image]
LFN measurement in SOI \(\Omega\)-gate NW MOSFETs

✓ Drain current noise PSD \(S_{ld}\) measurement

✓ Expected 1/f noise model:

Carrier Number fluctuations with correlated mobility fluctuations (CNF+CMF) model

\[
\frac{S_{ld}}{I_d^2} = \left(1 + \alpha_{SC} \mu_{\text{eff}} C_{ox} \frac{I_d}{g_m} \right)^2 S_{Vfb} \left(\frac{g_m}{I_d}\right)^2
\]


\(S_{ld}/I_d^2\) vs. frequency shows 1/f noise in 1ch-\(\Omega\)-gate NWs
Drain current noise $S_{ld}/I_d^2$ vs. $I_d$

1/f noise model: CNF+CMF model

$$S_{ld} = \left(1 + \alpha_{SC} \mu_{eff} C_{ox} \frac{I_d}{g_m}\right)^2 S_{vfb} \left(\frac{g_m}{I_d}\right)^2$$

Good agreement between $S_{ld}/I_d^2$ plots and the corresponding $(g_m/I_d)^2$ curves.

Our devices down to NW can be interpreted by CNF+CMF model.
Drain current noise $S_{ld}/I_d^2$ vs. $I_d$

1/f noise model:

$$S_{ld}/I_d^2 = \left(1 + \alpha_{SC}\mu_{eff}C_{ox}I_d/g_m\right)^2 S_{vfb}(g_m/I_d)^2$$

- Good agreement of $S_{ld}/I_d^2$ plot vs. $(g_m/I_d)^2$ curve in all technological splits
- Geometrical difference between NW and wide FETs is not clearly visible
Origin of $S_{V_{fb}}$ and $\alpha_{sc}\mu_{eff}$

- $V_{fb}$ fluctuations correspond to charge fluctuations in gate oxide.

- Flat-band voltage: $V_{fb} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}}$

- $\delta V_{fb}$ is equivalent to $\delta Q_{ox}$

- $\delta V_{fb} = -\frac{\delta Q_{ox}}{C_{ox}}$

- $\delta Q_{ox} = -C_{ox}\delta V_{fb}$

- $\alpha_{sc}$: coupling coefficient between mobility and oxide charges

\[
\alpha_{SC} = \frac{\delta (1/\mu_{eff})}{\partial Q_{ox}} = \frac{1}{\mu_{eff}^2} \frac{\delta \mu_{eff}}{\partial Q_{ox}}
\]

\[
\Rightarrow \alpha_{SC} \mu_{eff} = \frac{1}{\mu_{eff}} \frac{\delta \mu_{eff}}{\partial Q_{ox}}
\]

- $\mu_{eff}$: Effective mobility

- $S_{V_{fb}}$ is carrier number fluctuations (CNF) component

- $\alpha_{sc}\mu_{eff}$ is correlated mobility fluctuations (CMF) component
Extracted flat-band voltage noise $S_{Vfb}$

$S_{Vfb}$ is carrier number fluctuations (CNF) component

$S_{Vfb}$ trend is similar in all technological splits
$S_{Vfb}$ simply depends on total area ($\sim 1/W_{tot}$ & $\sim 1/L_g$)
Coulomb scattering parameter $\alpha_{\text{sc}}\mu_{\text{eff}}$

$\alpha_{\text{sc}}\mu_{\text{eff}}$ is correlated mobility fluctuations (CMF) component.

$\mu_{\text{eff}}$ extraction is quite difficult in 1ch-NW devices.

- $\alpha_{\text{sc}}\mu_{\text{eff}}$ is nearly constant with varying $W_{\text{tot}}$ and $L_g$.
- Device-to-device dispersion is only dominant.

Graph showing $\alpha_{\text{sc}}\mu_{\text{eff}}$ vs. $W_{\text{tot}}L_g$ with markers for different conditions: SOI, H$_2$ anneal, [100]-oriented, sSOI.

$V_d=40\text{mV}$, $f=10\text{Hz}$.
Gate oxide trap density $N_t$

✓ Flat-band voltage noise $S_{V_{fb}}$ (McWhorter model)

Physical carrier trapping/de-trapping mechanism between oxide charge traps and channel surface

Tunneling process

$$S_{V_{fb}} = \frac{q^2 kT \lambda N_t}{f W_{tot} L_g C_{ox}^2}$$

$N_t$ (eV$^{-1}$cm$^{-3}$)

$\lambda \approx 0.1$nm: Tunneling attenuation length


Tunneling transitions of electron

(i) Direct tunneling
(ii) Indirect tunneling via interface traps

Extracted gate oxide trap density $N_t$

$$N_t = \frac{f W_{tot} L_g C_{ox}^2 S_{Vfb}}{q^2 kT\lambda}$$

✓ No large alteration by both geometrical (NW vs. wide FET) and technological parameter impacts

✓ Similar values to state-of-the-art Hf-based high-k/metal gate stack reports ($10^{17} \sim 10^{19}$ eV$^{-1}$cm$^{-3}$)
Influence of drain voltage bias $V_d$

✓ $V_d$ dependence in $S_{ld}/I_d^2$ vs. $I_d$ for SOI and sSOI NWs

✓ Noise level in subthreshold (plateauing) region is steady from $V_d$ linear up to saturation regions

✓ $S_{Vfb}$ and $N_t$ are independent of $V_d$ variation
Influence of drain voltage bias $V_d$

- $W_{tot} L_g f S_{Vg}$ characteristics compared to ITRS requirement

- Noise spectra are irrespective of $L_g$ below 120nm

- Strained-NW (sSOI-NW) FETs fulfills the future ITRS requirement on LFN

**Graphs:**

SOI:
- Year: 2015
- $L_g$ values: 17nm, 20nm, 23nm, 28nm, 33nm, 107nm
- $W_{top} = 11nm$, $W_{tot} = 33nm$
- $V_g = 0.55-0.65V (= V_t + 0.2V)$
- $f = 10Hz$

sSOI:
- Year: 2026
- $L_g$ values: 5.9nm, 5.9nm, 22nm, 27nm, 32nm, 57nm, 107nm
- $W_{top} = 13nm$, $W_{tot} = 35nm$
- $V_g = 0.7V (= V_t + 0.2V)$
- $f = 10Hz$

**Equation:**

$$S_{Vg} = \frac{S_{Id}}{g_m}$$
Conclusions

- **CNF+CMF model** can describe 1/f noise behavior in all our devices with various parameters.
- Parameters $S_{Vfb}$ and $\alpha_{sc\mu_{eff}}$ are assessed and discussed.
- Gate oxide trap density $N_t$ is **NOT** altered by both geometrical and technological parameters.
- The $N_t$ values are in the same order as values reported for state-of-the-art **Hf-based high-k/metal gate stack**.
- $V_d$ influence does **NOT** significantly alter LFN properties.
- **sSOI-NWs** satisfy ITRS requirement for LFN by 2026.
Thank you for your attention

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