Reduction of the resistivities of Ni Silicide formed by the reaction of Si nanowire and Ni thin films

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1.1 Background of This Study

Nowadays, Ultra-Large Scale Integrated circuits (ULSIs) constructed from complementally metal-oxide-semiconductor (CMOS) structures, are really indispensable components for our human society. Obviously, almost all the human activities, such as living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS ULSI operation. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software’s required for the integrated circuits. The continuous progress of CMOS technologies in terms of high-performance operation and low power consumption have been and will be very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required. Therefore the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO$_2$ gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the ‘cooling of the earth’ in two ways. One is direct contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by
so called ‘Green IT’ procedure. This can be done by the development of low power and high performance CMOS devices used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point of view, as well as from the global economic point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 16 to 64 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.
1.2 CMOS ultimate scaling

It is well known that the progress of CMOS ULSI has been accomplished by the downsizing of metal-oxide-semiconductor field effect transistors (MOSFETs) [1.1]. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970’s. It was fortunate, however, it has been proven that those forecasts are not true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. There is less than ten years until 2020, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit.

It is expected that about 5 nm is the limit of the downsizing of the gate length, because there are four main reasons: A) Difficulty in off-current suppression, B) Difficulty in the on-current increase, C) Difficulty in the increase of MOSFETs speed, D) Production and development cost increase.

A. Difficulty in off-current suppression

With decrease in gate length, Short channel effect occurs [1.2]. Thus, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.
B. Difficulty in the on-current increase

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

C. Difficulty in the increase of MOSFETs speed

One of the scaling merits is to reduce the gate capacitance, $C_g$, because the switching time of MOSFETs is defined by $C_g V_{dd}/I_d$, where $I_d$ is the drain on-current and $V_{dd}$ is power voltage. However, $C_g$ will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain areas are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.
**E. Possible solution after that**

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called ‘beyond CMOS’ or ‘Post Si’ new devices, which are believed to really replace CMOS transistors used for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with ‘More Moore’ approach with combining that of ‘More than Moore’. Then, what is ‘More Moore’ approach after we reached the downsizing limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the ‘More Moore’ law for certain period by replacing current planar CMOS transistors by three dimensional structure MOSFETs. Furthermore, nanowire and tube MOSFET suppresses off-leakage current and increase of on-current under low voltage could be realized because of having multigate, quasi-one-dimensional conduction and multi-quantum channel per wire/tube. Figure 1.1 shows our roadmap for CMOS transistors after 2020.
Figure 1.1 Roadmap for CMOS transistors.
1.3 Three Dimensional Structure Devices

1.3.1 Multigate Device

Planar transistors have been the core of integrated circuits for several decades, during which the size of the individual transistors has steadily decreased. In MOSFET performance can be basically improved by downsizing. However, "off-state" leakage current increases when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length is reduced, both the operation speed and the number of components per chip increase. It is the phenomenon known as the short-channel effect.

Therefore, it is expected to replace the conventional planar structure by three dimensional structures. The nonplanar devices have multiple channels surrounded by multi gate and effective suppression of "off-state" leakage current. Current in the "on-state" is also enhanced because of multi gate. Moreover, Improvement of on-state current is expected by using nanowire which has ballistic conduction from quasi-one-dimensional structure. Figure 1.2 shows the typical device of the three dimensional structure.

![Figure 1.2 Schematic illustrations of three dimensional structure devices.](image)
### 1.3.2 FinFET

FinFET is a device of the typical three dimensional structures and has the structure which surrounds Si of fin structure – the shape such as extremely narrow fish tail – by a gate. Figure 1.3 shows schematic illustration of the FinFET. It has advantage on suppressing short-channel effect and easiness of fabrication process by using silicon on insulator (SOI) substrates.

As the variants, there is a FinFET owing gate architecture called Tri-gate. It has a lot of gate surface area. Thus, there's a lot more of inversion layer for current to flow through. This makes the difference between the transistor's "on" and "off" states much larger, which means that the transistor can switch between states much faster while still producing a clear string of ons and offs. Tri-gate transistors reduce leakage and consume far less power than current transistors. Currently, Intel has produced a FinFET which has Tri-gate and gate length 22 nm [1.3].

![Diagram of FinFET with Double-Gate and Tri-Gate structures.](image)

**Figure 1.3** Schematic illustrations of FinFET with Double-Gate and Tri-Gate structures.
1.3.3 Si Nanowire FET

Si nanowire FET is considered as one of the promising candidates for further extending the three dimensional device downsizing, owing to its gate-all-around (GAA) of which enables better gate control capability than planar transistors. Figures 1.4 show schematic image of Si NW FET with GAA structure. Moreover, advantage in ballistic conduction from quasi-one-dimensional (Q1D) structure can be achieved [1.4]. Therefore, high $I_{on}/I_{off}$ ratio can be achieved with sufficient low power consumption. Figure 1.5 shows comparison of the requirement to the bulk Si, the ultra-thin body fully depleted (UTB FD) SOI and the double-gate (DG) MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes [1.4-6]. Si NW FETs have already been obtained higher $I_{on}/I_{off}$ ratio than any planer transistors.

Si NW FET has been fabricated by several techniques including, Si Fins are patterned by lithography and etching followed by the oxidation (Figure 1.6 (a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si NW with better controllability of the size of the wire (Figure 1.6 (b) shows Bottom-up method) [1.7].

Figure 1.4 Schematics image of Si Nanowire FETs with gate-all-around structure.
Figure 1.5 Comparison of the requirement to the bulk Si, UTB FD SOI, and DG MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes.

Figure 1.6 Fabrication methods of Si nanowire FET by (a) Top-down and (b) Bottom-up [1.7].
1.4 Nickel Silicidation for Si Nanowire

1.4.1 Nickel Silicide

In CMOS fabrication, Salicide (self-align silicide) often has been used for the contacts of source/drain regions and gate electrodes [1.8]. There are many kinds of metals - Ni, Ti, Co, Mo, W, Pt and so on - for silicides. Especially, Ni-, Co-, and Ti-silicides with low resistivity have been studied for a long time. Though TiSi$_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co - silicides are used in 100 nm - or smaller generations. Although CoSi$_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices [1.9]. In addition to its relatively low resistivity and less contaminated interface can be obtained owing to reactively formed interface enabling to suppress the variability. In particular, Ni is a promised material of metal-silicide, because of its relatively low resistivity, relatively low temperature and relatively small Si consumption during the formation for application to nano-scale structure [1.10-12]. The study on Ni silicide started to become an active research area in the 1970’s and the silicide technology in MOSFET fabrication process since 1980's [1.13]. Figure 1.7 shows the progress of the silicide materials. Table 1.1 is previously reported fundamental data of Ni silicide formation on bulk Si [1.10, 1.14-15]. And, Fig. 1.8 [1.16] and 1.9 [1.17] show the reaction temperature dependent Ni silicide phase which is mainly appeared in bulk Si.
**Figure 1.7** Progress of silicide materials which have been used in CMOS fabrications so far [1.8].

**Table 1.1** Fundamental dates which show phase, resistivity, crystal structure, density and consumption of Ni silicide formed on bulk Si [1.10, 1.14-15].

<table>
<thead>
<tr>
<th>Phase</th>
<th>Resistivity (µΩ·cm)</th>
<th>Crystal structure</th>
<th>Density (g/cm³)</th>
<th>T_{silicide}/T_{Ni}</th>
<th>Si consumption / T_{Ni}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>7-10</td>
<td>Cubic</td>
<td>8.91</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Ni₅Si</td>
<td>80-90</td>
<td>Cubic</td>
<td>7.87</td>
<td>1.31</td>
<td>0.61</td>
</tr>
<tr>
<td>Ni₃Si₁₂</td>
<td>90-150</td>
<td>Hexagonal</td>
<td>7.56</td>
<td>1.4</td>
<td>0.71</td>
</tr>
<tr>
<td>Ni₂Si</td>
<td>24-30</td>
<td>Orthorhombic</td>
<td>7.51</td>
<td>1.47</td>
<td>0.91</td>
</tr>
<tr>
<td>Ni₃Si₂</td>
<td>60-70</td>
<td>Orthorhombic</td>
<td>6.71</td>
<td>1.75</td>
<td>1.22</td>
</tr>
<tr>
<td>NiSi</td>
<td>10.5-18</td>
<td>Orthorhombic</td>
<td>5.97</td>
<td>2.20</td>
<td>1.83</td>
</tr>
<tr>
<td>NiSi₂</td>
<td>34-50</td>
<td>Cubic</td>
<td>4.80</td>
<td>3.61</td>
<td>3.66</td>
</tr>
<tr>
<td>Si</td>
<td>Dopant dependent</td>
<td>Cubic</td>
<td>2.33</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Figure 1.8 Silicidation temperature dependent sheet resistances and the appeared Ni silicide phase on bulk Si. Deposited Ni thickness is 12 nm[1.16].

Figures 1.9 Schematic image of silicidation temperature dependent mainly appeared Ni silicide phase on bulk Si [1.17].
1.4.2 Application to FinFET and Si Nanowire FET

As Nickel silicide formed at relatively low temperature with relatively small Si consumption, Ni salicide (self-aligned silicide) becomes almost an indispensable technique for conventional MOSFET. Moreover, because the resistances of source, drain, and gate electrode increase with more downsizing, it is also expected to apply Ni silicide to the three dimensional device such as FinFET and Si NW FET.

The high performance FinFET with has been reported previously by using Ni silicide formed on source and drain regions [1.18]. Furthermore, Si NW FETs with reduced the parasitic resistance of the source and drain regions by using Ni silicide have also been reported [1.19]. Figure 1.10 shows TEM image of FinFET and Si NW FET which has Ni silicide formed on source and drain regions.

Therefore, considering the more scaling, it is required to form low resistance Ni silicide on Si nanowire.

(a) FinFET (b) Si NW FET

Figure 1.10 TEM image of the reported (a) FinFET [1.18] and (b) Si NW FET fabricated by Ni salicide of source and drain regions [1.19].
1.5 Issues in Nickel Silicidation of Si Nanowire

1.5.1 Reaction between Silicon Nanowire and Nickel

Nowadays, many researches have been performed in Ni silicide formed on bulk Si. Thus, numerous reports also make on the conditions of Ni silicidation such as formed temperature and Ni thickness dependence. Figure 1.11 shows the conditions of Ni silicide phase formed on bulk Si.

However, it is inferred that Ni silicidation for Si nanowire is different from the case of conventional Ni silicidation for bulk Si, considering the amount of Si reacting with Ni is limited in Si nanowire. Furthermore, Ni-rich silicide has also been reported in Ni silicide formed on Si nanowire [1.20-21].

Therefore, there is the issue that low-resistivity silicide such as NiSi may not be formed easily, because Ni silicidation of Si nanowire is not the same as the case of bulk Si.

![Figure 1.11](image-url)

*Figure 1.11* A schematic image of phases of Ni silicides formed on planar silicon. Ni silicidation depends on the initial Ni thickness and annealing temperature.
1.5.2 Resistance Increase of Ni Silicide Nanowire

Unlike Ni silicide resistivity of bulk Si, resistivity of Ni silicide nanowire shows a tendency to increase with down sizing. Figure 1.12 shows the dependence of resistivity on nanowire line width [1.22]. It shows that the constant low resistivity for width larger than 35 nm. However, drastic increases in the resistivity were observed for nanowire line width smaller than 35 nm.

There are possible causes for the resistivity increase. They were line width roughness, surface scattering, grain boundary scattering and difference of the Ni silicide phase.

![Figure 1.12 Dependence of resistivity on nanowire line width. Silicidation annealing was performed at 500 °C for 5 min [1.22].](image-url)
1.5.2.1 Line Width Roughness

One of causes for drastic increases in the resistivity of nanowires at around the width of 35 nm may be the roughness in line width as illustrated in Figure 1.13 [1.22]. The increase in resistance may be caused by the confinement of current in narrow portions of nanowires. However, Figure 1.14 shows that the resistivity of roughness approximation model is much smaller than the resistivity measured [1.22].

Therefore, roughness in line width cannot be the major reason for the drastic increase in resistivity.

![Nanowire roughness](image)

Figure 1.13 Schematic structure of narrow Ni silicide line and the approximation of its roughness [1.22].
Figure 1.14 Comparison of the resistivity calculated using the roughness approximation model with $r = 0.2$ and $r = 0.7$ to measured resistivity shown in Fig. 1.12. [1.22].

1.5.2.2 Surface Scattering

The electrons in the metal are scattered by phonons and impurities. In the case where the current flows in narrow regions as nano-size, the scattering of electrons on surface occurs. This scattering is called surface scattering. Figure 1.15 shows the schematic illustration of surface scattering.

The Surface scattering is caused by the width or thickness of the wire or film close to the mean free path of electrons. As the result, the resistivity increase.

However, the mean free path of resistivity model shown in Figure 1.12 was calculated as 2 nm [1.22]. Also, it was investigated that the 2 nm of mean free path can not affect resistivity increase.
1.5.2.3 Grain Boundary Scattering

This scattering is the electrons scattering on grain boundary. Figure 1.16 shows the schematic illustration of grain boundary scattering. This phenomenon may be leading cause for resistivity increase. However, it is uncertain because 2 nm is a very short distance as mean free path.
1.5.2.4 Ni Silicide Phase

From Table 1.1, each of the Ni silicide phases has a different resistivity. In other words, a phase of high resistivity may have been formed in nanowire of narrow line width. The phases of narrow and wide line may be different because its amount ratio of Ni and reacting Si is different also. This means Ni film thickness could be key to controlling resistivity of Ni silicide nanowire. Figure 1.17 shows the Ni silicide phases of nanowires [1.20].

(a) Ni$_2$Si  
(b) Ni$_{31}$Si$_{12}$

*Figure 1.17* Cross-sectional TEM pictures of Ni$_2$Si and Ni$_{31}$Si$_{12}$ nanowire [1.20].
1.6 Purpose of This Thesis

As discussed in previous chapter, Fabrication of the high performance device with three dimensional structures is expected by the application of silicide used as contact of the conventional planar MOSFET to the multi-gate device such as FinFET and Si NW FET. However, Ni silicides formed on these narrow lines of silicon is considered to be different from the conventional silicidation for bulk Si. Moreover, the increase in resistance of Ni silicide nanowire by any reason is a concern.

In this thesis, in order to apply Ni silicide nanowire as the contact with low resistivity, reduction method of the resistivity increase in Ni silicide nanowire was investigated. For this purpose, 2-step annealing process was performed as thermal annealing process to form Ni silicide in Si nanowire. Also, Ni film thickness sputtering on Si nanowire was controlled for forming low resistivity phase in narrow line width. In order to investigate formed phase, temperature coefficient of resistance and atomic ratio of Ni/Si were calculated. These mathematic datas were compared to TEM and EDS analysis results to demonstrate whether theoretical values accord with real data or not.
References


Chapter 2

Fabrication and Characterization Method

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2.3 Measurement and observation methods

2.3.1 Four-point Probe Method
2.3.2 Scanning Electron Microscope (SEM)
2.1 Experimental Procedure

Figure 2.1 shows the flow of fabrication process. Silicon nanowire patterns were fabricated on a 30-nm-thick silicon-on-insulator (SOI) wafer. After cleaning in SPM (H₂SO₄ and H₂O₂) solution followed by the treatment in HF, Ni films were deposited by RF magnetron sputtering. Next, Rapid thermal annealing (RTA) at from 270 to 500 °C was performed in nitrogen ambient for from 1 to 2 min. Unreacted Ni was removed by SPM. In order to form electrodes on the nanowire, Metal films were deposited. For the patterning of the electrodes, lift-off technique was used. Finally, Ni silicide nanowire was observed and measurement resistance was performed.

- Si nanowire patterning
  - SOI height: 30 nm
  - Nanowire width ranging from 20 to 90 nm

- SPM and HF cleaning

- Ni deposition
  - Ni film thickness: 7, 10, 80 and 120 nm
  - RF sputtering in Ar ambient

- 1st Rapid thermal annealing (RTA)
  - 270°C, 2 min (N₂ ambient)

- Unreacted Ni removal by SPM

- 2nd RTA
  - 500°C, 1 min (N₂ ambient)

- TiN/Ti deposition by RF sputtering
  - Thickness 50 nm/50 nm
  - RF sputtering in Ar and N₂ ambient

- TiN/Ti electrodes patterning by Lift-off technique

- Observation and Measurement

Figure 2.1 Process flow into measurement and observation.
2.2 Experimental Details and Principle

2.2.1 Fabrication of Substrate with Si Nanowires

Si nanowires ranging from 20 to 90 nm in width were fabricated on a (100)-oriented SOI wafer with an SOI layer of 30 nm thick by photolithography and dry-etching process. The direction of the line was aligned to <110>.

2.2.2 Substrate Cleaning Process

At first, the experiments using high quality thin films require ultra clean surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩ·cm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩ·cm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) (H₂SO₄:H₂O₂=4:1), was performed to remove any organic material and metallic impurities. After dipping in the chemicals to clean the substrate, the clean wafer was dipped in DI water to rinse away the chemicals. The process dipping the wafer in DI water after dipping the wafer in chemicals with each cycle is important. Then, the native or chemical oxide was removed by 1% diluted hydrofluoric acid (HF). Finally, the cleaned substrate was loaded to the oxidation chamber to deposit immediately after it was dried by air gun.
2.2.3 Photolithography Process

Photolithography (or "optical lithography") is a process used in microfabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photoresist (Figure 2.2). It is used because it can create extremely small patterns (down to a few tens of nanometers in size), it affords exact control over the shape and size of the objects it creates. In case of this study, photolithography was used for the method to etch only parts of unwanted pattern, form electrodes patterning.

The process flow and a photo of the photolithography apparatus used throughout this study are shown in Fig. 2.3. The apparatus is MJB4 of Karl Süss contact-type mask aligner. At first, the substrates were coated with positive type photoresists by spin-coating method. The thicker photoresist called S1818 and thinner one called S1805 were used. Secondly, the coated photoresists were baked at 115 °C for over 5 min by using electrical hotplate. Then, spin-coated photoresist layers were exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. The exposure duration was set to 2 sec and 4 sec for thinner photoresist and thicker one, respectively. Finally, exposed wafers were developed using the specified tetra-methyl-ammonium-hydroxide (TMAH) developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 1~2 minute.
Figure 2.2 Schematic image of photo lithography by development for photo resist after exposure.

Figure 2.3 The process flow and the photo of photolithography apparatus.
2.2.3 Dry Etching by RIE

Reactive Ion Etching (RIE) was performed to eliminate only parts of required Si nanowire. RIE is one of the dry etching methods. The gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important.

Si combined with F- and forms Si-F. Si-F is evaporated and eliminated from the sample. Therefore, in this experiment, SF$_6$ is used as etching gas for Si etching. On the other hand, photoresist, which is attached to the sample by the photolithography, reacts with not SF$_6$ but O$_2$ to be eliminated. This phenomenon is called ashing. O$_2$ is used as the etching gas of the resist. Fig.2.4 shows the schematic illustration of the RIE process.

![Fig.2.4 Schematic illustrations of the Reactive Ion Etching process.](image-url)
2.2.4 RF Magnetron-Sputtering Process

After eliminating only parts of required Si nanowire by RIE, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive layer) and Ni/Si were formed by an ultra-high-vacuum (UHV) sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra-thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the “target,” composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

In this study, Ni films with thickness of 7, 10, 80 and 120 nm were deposited on the substrate with Si nanowire by RF magnetron-sputtering in argon ambient. As RF magnetron-sputtering system, UHV Multi Target Sputtering System ES-350SU shown in Fig. 2.5 was used and its schematic structure is shown in Fig. 2.6. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2.1 is attached for reference.
Figure 2.5 Photo of UHV Multi Target Sputtering System ES-350SU.

Figure 2.6 Schematic internal structure of UHV sputtering system.
Table 2.1 Specifications for UHV Multi Target Sputtering System ES-350S.

<table>
<thead>
<tr>
<th>Growth chamber</th>
<th>1. Ultimate pressure</th>
<th>$1.5 \times 10^6$Pa</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2. Substrate size</td>
<td>2 inch in diameter</td>
</tr>
<tr>
<td></td>
<td>3. Heating temperature</td>
<td>$600^\circ$C</td>
</tr>
<tr>
<td></td>
<td>4. Heater type</td>
<td>Lamp type heater</td>
</tr>
<tr>
<td></td>
<td>5. Target</td>
<td>3 inch x 5 pieces (motor-driven)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Load lock chamber</th>
<th>6. Vacuum pumps</th>
<th>TMP 500L/sec and RP 250L/min</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>7. Ultimate pressure</td>
<td>$6.6 \times 10^5$Pa</td>
</tr>
<tr>
<td></td>
<td>8. Vacuum pumps</td>
<td>TMP 60L/sec and RP 90L/min</td>
</tr>
</tbody>
</table>

9. Substrate holder with cooling function / Substrate holder with heating function / Cleaning function / Radical beam source
2.2.5 Thermal Rapid Annealing Process

After formation of thin films of Ni/Si, Ni/M/Si, or M/Ni/Si by UHV sputtering system, these structures were transferred to annealing furnace to perform thermal process. The thermal process leads to the reaction between Ni and Si, or among Ni, M, and Si.

In this study, the thermal rapid annealing (RTA) process was performed for Ni films /Si nanowire and led to Ni silicidation for Si nanowire. The silicidation was performed by using infrared image furnace in nitrogen ambient. The 1\textsuperscript{st} annealing temperature and time were 270 °C and 2 min. The 2\textsuperscript{nd} annealing temperature was varied from 400 °C to 600 °C and time was 1 min.

The equipment for annealing used in this study is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 2.7 is the photo of the infrared image furnace, whose schematic illustration was shown in Fig. 2.8. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon coated by SiC. The heating temperature was controlled by thermocouple feedback.

In this study, after the silicidation, the unreacted Ni was removed by dipping the substrate in a heated mixed solution of H\textsubscript{2}SO\textsubscript{4} and H\textsubscript{2}O\textsubscript{2} at 150 °C for over 10 min.
Figure 2.7 Photo of infrared image furnace.

Figure 2.8 Schematic internal configuration of infrared image furnace.
2.2.7 Lift-off technique for electrode formation

Lift-off technique is a method of patterning which is different from wet etching and dry etching. Wet and dry etching is dependent on the material of interest and it is necessary to change the etching conditions. In lift-off technique, it is not necessary.

At first, patterning of the resist on the substrate is performed by lithography. Therefrom, the deposition is carried out leaving the photoresist on the substrate. As a note, deposition condition that does not break the photoresist is required. Finally, ultrasonic cleaning is performed and deposited film on the photoresist peeling. As a result, the desired pattern is formed. Figure 2.9 shows the schematic illustration of the Lift-off technique.

In this study, this process is used after TiN/Ti of the electrode was deposited by RF magnetron sputtering. The electrode is formed without the problem as excessive wet etching.

![Figure 2.9 Schematic illustration of the Lift-off technique.](image-url)
2.3 Measurement and observation methods

2.3.1 Four-point Probe Method

In the resistance measurement, four-point method is one of the most basic methods. The resistance including a contact resistance between the probe and the sample would be obtained in the two probe resistance measurement. In order to measure resistance of the material with low resistance such as metal, the measurement of resistance that doesn’t include the contact resistance is required. The measurement of resistance without including the contact resistance becomes possible by using four-point probe method.

In this study, four-point probe method is used to measure the resistance of the Ni silicide nanowire. Figure 2.10 shows the schematic illustrations of the electrode structure to use this method.

![Figure 2.10 Schematic illustration of the electrodes structure.](image-url)
2.3.2 Scanning Electron Microscope (SEM) for Observation

The formed Ni silicides in Si nanowire were observed by scanning electron microscope (SEM). The observation was mainly performed by overhead viewing.

Figure 2.11 shows Scanning Electron Microscope (SEM) system which is S-4800 (HITACHI High-Technologies Corporation) and its schematic internal configuration is shown in Fig. 2.12. The “Virtual Source” at the top represents the electron gun, producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin, tight, coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion and make the beam dwell on points for a period of time determined by the scan speed. The final lens, the Objective, focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample, interactions occur inside the sample and are detected with various instruments interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a display whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated, the entire pattern can be scanned 30 times per second.
Figure 2.11 Photograph of SEM equipment.

Figure 2.12 Schematic view of internal configuration of SEM equipment.
Chapter 3
Electrical Analysis of Nickel Silicide Nanowire

3.1 Introduction

3.2 Electrical Characteristics of Ni Silicide Nanowire
   3.2.1 I-V Characterization
   3.2.2 The Effect of 2-Step Annealing Process on Resistivity
   3.2.3 Dependence of Resistivity on Line Width
   3.2.4 Temperature Dependence of Resistance
   3.2.5 The Effect of Ultrathin Ni film on Resistivity
   3.2.6 Resistivity Dependence on Ni film Thickness

3.3 Conclusion

References
3.1 Introduction

As described in the chapter 1, it is presumed that Ni silicidation of Si nanowire differs from silicidation of the bulk Si. Moreover, increase of the resistance in narrow line is a concern because of the phase difference. From Table 1.1, NiSi is the most suitable among the various Ni silicide phases because of its low resistivity. However, the 1-step annealing process shows that various phases of Ni silicide can coexist, which makes single phase NiSi formation problematic [3.1-4]. Furthermore, the 1-step salicide process contains problems of excess silicidation which usually causes off state current of MOSFET abnormality [3.5-6]. These problems can be overcome by the 2-step annealing process [3.7].

Therefore, 2-step annealing process was applied to Si nanowire in this chapter. Resistivities were calculated by using measured resistances and size datas of Ni silicide nanowires. Also these electrical characteristics are discussed with temperature coefficient of resistance.
3.2 Electrical Characteristics of Ni Silicide Nanowire

3.2.1 I-V Characterization

At first, I-V characteristics were measured by four-point probe method in order to evaluate the resistance of Ni silicide nanowires. Figure 3.1 shows I-V characteristics of Ni silicide nanowire with the width of 54 nm and the Ni film thickness is 10 nm. The distance between the TiN electrodes was 4 µm. As expected from the electrical properties of metal, the current-voltage relation follows Ohm’s law. This relation expressed as follows:

\[ V = IR \]  

(3.1)

where \( V \) is the voltage, \( I \) is current and \( R \) is the resistance of Ni silicide nanowire.

Therefore, The resistance of the nanowire with the width of 54 nm is 1070 Ω from Ohm’s law.

![Figure 3.1](image.png)

**Figure 3.1** Current-voltage characteristic for Ni silicide nanowire with the width of 54 nm. Deposited Ni film thickness is the 10 nm and the distance between TiN/Ti electrodes is 4 µm. The resistance of 1070 Ω is obtained from Ohm’s law.
3.2.2 The Effect of 2-Step Annealing Process on Resistivity

According to the introduction, 2-step annealing process is effective for stable Ni silicide formation in bulk Si. However, it is not known what occurs in Si nanowire by 2-step silicidation. In order to investigate this problem, resistivities of Ni silicide nanowires formed by 1-step and 2-step annealing were measured.

Figure 3.2 shows the resistivities of Ni silicide nanowires formed by 10 nm thickness Ni film. Forming process of each Figure is (a) The 1-step annealing at 500 °C for 5 min, (b) The 2-step annealing with short time (The 1st annealing: at 270 °C for 40 sec, The 2nd annealing time: at 500 °C for 30 sec) and (c) The 2-step annealing with long time (The 1st annealing: at 270 °C for 2 min, The 2nd annealing: at 500 °C for 1 min) process. These datas shows clearly that 2-step annealing process formed the low resistivities. In the case of (a), a lot of resistivity dispersions in narrow nanowire were detected. its resistivities were high also. However, in the case of (c), the low resistivities were obtained at all over the line width and dispersions were a few also. From these results, the effect of 2-step annealing process for low resistivity was demonstrated. However, resistivities of (b) have no less dispersions than (a). The reason is presumed that Ni silicidation is not enough because of its short annealing time.

Therefore, the 2-step annealing process with long time was selected for the experiment of this study.
Figure 3.2 The resistivities of Ni silicide nanowires formed by (a) the 1-step annealing: 500 °C for 5 min (b) the 2-step annealing: 270 °C for 40 sec, 500 °C for 30 sec (c) the 2-step annealing: 270 °C for 2 min, 500 °C for 1 min.
3.2.3 Dependence of Resistivity on Line Width

Figure 3.3 shows dependence of resistivity on nanowire line width. The resistivity calculated from the resistance obtained by $I-V$ characteristic. Relationship between resistance and resistivity is expressed by the following equation,

$$ R = \rho \frac{l}{hw} $$

(3.2),

where $\rho$ denotes resistivity, and $h$, $w$, and $l$ denote height, width, and length of nanowires. The height of nanowires is 30 nm. Length of nanowire and line width is obtained by SEM observation. Figure 3.4 shows SEM image of formed Ni silicide for Si nanowire. In the chapter 3.2.2, the resistivities were calculated with only their own size datas. However, the resistivities of Figure 3.3 were calculated from dependence of resistance on nanowire length for more exact measurement.

From Figure 3.3, Ni silicide resistivity increased for NW width less than 40 nm for Ni thickness more than 10 nm. This trend was similar to the previous result Figure 1.12. However, the increase was suppressed to a little more than 50 $\mu\Omega$cm when thin Ni (10 nm) was used for the silicidation. Stable and low resistivities were also obtained for 10nm Ni for NW width more than 40nm (about 20 $\mu\Omega$cm). Appropriate Ni/Si amount ratio may lead to the formation of low resistivity silicide phase.
Figure 3.3 Dependence of resistivity on nanowire line width. Deposited Ni films thickness are 10, 80 and 120 nm.

Figure 3.4 SEM image of formed Ni silicide for Si nanowire and TiN/Ti electrodes aligned on it.
3.2.4 Temperature Dependence of Resistance

One of the causes for change of the resistivity may be the phase transition of Ni silicide. In order to investigate the phase of Ni silicide with temperature, the resistance was measured at the temperature in the range from 25 °C to 75 °C. The temperature dependence of the resistance can be expressed by the following equation,

\[
\frac{R}{R_{rt}} = \alpha(T - T_{rt}) + 1
\]  

where \( R \) and \( R_{rt} \) are the resistance at temperature \( T \) and that at room temperature (25 °C), respectively, and \( \alpha \) is temperature coefficient of resistance (TCR).

Figure 3.5 shows the TCR of the Ni silicide nanowires. Table 3.1 shows the TCR of the Ni silicide phases [3.8]. In the area of resistivity for about 50 µΩcm, TCR value was measured from 0.0012 to 0.0016 (A). It shows a value between NiSi and Ni$_2$Si from the TCR value of table 1. Also TCR of 0.0030~38 was measured in the area of the lowest resistivity (B). Considering that Si ratio increase results in the increase of TCR, it is assumed that Si-richer phase was formed with this condition. However, the TCR value of 0.0010 K$^{-1}$ was obtained with the high resistivity (C). It can not conclude that its phase is different because it is close to 0.0012 K$^{-1}$. Figure 3.6 shows dependence of TCR on resistivity of Ni silicide nanowire.
Figure 3.5 The TCR (K$^{-1}$) of the Ni silicide nanowires.

Table 3.1 The TCR of the Ni silicide phases [3.8].

<table>
<thead>
<tr>
<th>Phase</th>
<th>TCR (K$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NiSi</td>
<td>0.0022</td>
</tr>
<tr>
<td>Ni$_2$Si</td>
<td>0.00096</td>
</tr>
<tr>
<td>Ni$<em>{31}$Si$</em>{12}$</td>
<td>0.00048</td>
</tr>
</tbody>
</table>
Figure 3.6 Dependence of TCR on resistivity of Ni silicide nanowire.
3.2.5 The Effect of Ultrathin Ni film on Resistivity

The low resistivities were measured in the Si-rich area of Ni silicide nanowire. From this result, reduction of Ni film thickness for Si-rich phase may form lower resistivity than it.

Figure 3.7 shows dependence of resistivity on nanowire line width with addition of 7 nm-thickness Ni film. Overall, the resistivities increased drastic than the resistivities of Ni silicide nanowires formed by 10 nm-thickness Ni film. This may be due to the Ni silicide agglomeration because the formed Ni silicide was extremely thin [3.9].

![Figure 3.7 Dependence of resistivity on nanowire line width with addition of 7 nm-thickness Ni film.](image)

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3.2.6 Resistivity Dependence on Ni film Thickness

Figure 3.8 shows the resistivity as a function of the Ni thickness. The nanowire width was taken as a parameter. This figure clearly indicates that the thickness around 10nm is an optimum for this Si fin height and the silicidation condition. Figure also shows its dependence of nanowire width. The optimum Ni film thickness barely changed in case of 25 nm and 55 nm. Further investigation such as optimum Ni thickness dependence on nanowire height may reveal more comprehensive view of the Ni reaction with Si nanowires.

![Figure 3.8 Dependence of Ni silicide nanowire resistivity on Ni film thickness.](image)
3.3 Conclusion

Ni silicide was formed on scaled silicon nanowires by 2-step annealing process. The resistances of Ni silicide nanowires were derived from $I-V$ properties obtained by four-point probe method. The Ni silicide line width in the range from 20 nm to 90 nm was obtained by observation of SEM. Furthermore, the resistivity of silicided nanowires was calculated.

Resistivity increased dramatically for the narrow nanowires with the width less than around 40 nm. By controlling the thickness of Ni film, drastic increase of the resistivity at narrow wire was suppressed.

As the cause of resistivity change of Ni silicide nanowires with line width around 40 nm, it was considered that phase of nickel silicide transited. Therefore, in order to determine the transition of the phase, the dependence of resistance of nanowires on the temperatures were evaluated and temperature coefficient of resistance estimated. As the result, the low resistivities were obtained from the Si-rich area with high TCR values. However, when Ni silicide nanowires became Si-richer phase with ultrathin Ni film, all resistivities drastic increased. About this result, Ni silicide agglomeration by extremely thin Ni film was considered.

Therefore, controlling the Ni/Si amount ratio is important for obtaining the low resistivity Ni silicide nanowires. However, it demands that control Ni thickness in order not to be extremely thin.
References


Chapter 4
Discussion in Resistivity of Ni Silicide Nanowire

4.1 Introduction

4.2 Analysis of Ni Silicide Phase
  4.2.1 Atomic Ratio of Ni/Si
  4.2.2 TEM Observation and EDS Analysis

4.3 Conclusion

References
4.1 Introduction

In the chapter 3, the resistivity increase of Ni silicide nanowires with the width smaller than 40 nm was founded. This increase was suppressed with decrease of Ni film thickness. However, extremely thin Ni film caused drastic increase of resistivity.

Although TCR values of Ni silicide nanowires were investigated for Ni silicide phase, concrete phase could not be confirmed. For more detail discussion about experimental datas, it should be investigated.

In this chapter, atomic ratio of Ni/Si was calculated with model equation to enhance reliability of the investigation of Ni silicide phase. Lastly, Ni silicide nanowires were observed by TEM and its components were appeared as peak by EDS analysis. In order to confirm the accordance, the datas of atomic ratio of Ni/Si and physical analysis were compared each other.
4.2 Analysis of Ni Silicide Phase

4.2.1 Atomic Ratio of Ni/Si

In the case of Ni silidation in bulk Si, Si amount is considered to infinite compared to Ni amount. However, it may be possible that atomic ratio of Ni/Si is calculated in Si nanowire. Because Si amount is limited in Si nanowire.

In order to investigate phases of Ni silicide nanowires more detail, atomic ratio of Ni/Si was calculated. Its model equation is expressed as

\[
\text{atomic ratio of Ni/Si} = \frac{(FWHM_{Si} + h_{Si} \cot 54.7^\circ) \times h_{Ni} \times \frac{d_{Ni}}{M_{Ni}}}{FWHM_{Si} \times h_{Si} \times \frac{d_{Si}}{M_{Si}}}
\]

(4.1),

where \(h_{Si}\) is the height of Si nanowires (30 nm); \(h_{Ni}\) is the thickness of Ni films; \(d_{Ni}\) is the density of Ni (8.91 g/cm\(^3\)); \(M_{Ni}\) is the atomic weight of Ni (58.69 g/mole), \(d_{Si}\) is the density of Si (2.33 g/cm3), and \(M_{Si}\) is the atomic weight of Si (28.09 g/mole) [4.1]. Also Figure 4.1 shows schematic diagram of the cross-section of Ni-coated Si nanowire for this equation [4.1]. However, \(\cot 90^\circ = 0\) was used instead of \(\cot 54.7^\circ\) in this study because the cross-section of used nanowire is a rectangular shape. Additionally, the nanowire line width of this study is used instead of FWHM of Si. Figure 4.2 shows schematic diagram of the nanowire used in this study. Ni films react to Si nanowire from three direction against Figure 4.1. Therefore, the atomic ratio of Ni/Si in this case should be considered for the three direction.
Figure 4.1 Schematic diagram of the cross-section of Ni-coated Si nanowire. The white area is the cross-sectional area of Si nanowire. The gray area is the cross-sectional area of the Ni film that is on top of Si surface [4.1].

Figure 4.2 Schematic diagram of the rectangular shape cross-section of Ni-coated Si nanowire.
Figure 4.3 shows the Ni/Si atomic ratio of Ni silicide nanowires. The Ni/Si atomic ratios of Ni silicide nanowires formed by 10 nm-thickness Ni film is distributed from 1.12 to 1.83. According to Table 1.1, these ratios are suitable because the resistivities exist in the range of NiSi, Ni$_3$Si$_2$ and Ni$_2$Si phases. However, in the case of Ni silicide nanowires formed by 7 nm-thickness Ni film, the Ni/Si atomic ratios did not accord with any Ni silicide phase for its resistivity. As assumed in the chapter 3, Ni silicide agglomeration may affect the resistivities.

![Figure 4.3](image)

**Figure 4.3** The Ni/Si atomic ratios of Ni silicide nanowires. They were calculated for the ones formed by 7 and 10 nm-thickness Ni films.
4.2.2 TEM Observation and EDS Analysis

Although Ni silicide phase was investigated by TCR measurement and calculation of Ni/Si atomic ratio, it did not know the concrete phase.

For this reason, TEM observation and EDS analysis were performed in Ni silicide nanowires. Figure 4.4 shows TEM images of Ni silicide nanowires. 27 nm line width with 10 nm-thickness Ni film and 45 nm line width with 7 nm-thickness Ni film were observed. In the case of Ni silicide formed by 10 nm-thickness Ni film, Ni silicide is uniform and grain boundary is monotonous also. In contrast, Ni silicide formed by 7 nm-thickness Ni film is ununiform. Furthermore a lot of contrast and complicated grain boundary were observed. From this result, it is assumed that resistivity increase was affected by not only Ni silicide agglomeration [4.1] but also complicated grain boundary [4.2] and excessive Si.

Figure 4.5 shows result of EDS analysis for Ni silicide nanowire. Condition of nanowire is same with (a) of Figure 4.4. Atomic and mass ratio of Ni/Si indicates a phase of Ni$_3$Si$_2$. It may not exact because semiquantitative method was used. However, as shown in Figure 4.6, crystal structure of Ni$_3$Si$_2$ phase was observed by electron diffraction also. This Ni silicide nanowire has the resistivity of 64 µΩcm and the Ni/Si atomic ratio was calculated to be 1.96. In other words, the phase of Ni$_3$Si$_2$ is reasonable.

Figure 4.7 shows Ni/Si counts for EDS analysis. (a) and (b) correspond with (a) and (b) of Figure 4.4. These Ni/Si ratios are not exact because there is a no standard sample. However, it was investigated already that phase of (a) is Ni$_3$Si$_2$. The peaks of (a) shows Ni-richer ratio than true ratio. Therefore, (b) is considered also that true ratio is more Si-richer than Ni/Si peak ratio. In other word, NiSi$_{(c>2)}$ phase of is derived. However, Si-richer phase than NiSi$_2$ is not exist. It is assumed that extra Si with NiSi$_2$ affect
Figure 4.4 TEM images of (a) 27 nm line width of Ni silicide nanowire formed by 10 nm-thickness Ni film and (b) 45 nm line width of Ni silicide nanowire formed by 7 nm-thickness Ni film.
Figure 4.5 Results of EDS analysis for Ni silicide nanowire formed by 10 nm-thickness Ni film with 27 nm line width. (a) Ni/Si mass ratio and (b) Ni/Si atomic ratio were measured.
Figure 4.6 Crystal pattern of Ni silicide nanowire with 27 nm line width appeared by electron diffraction. Ni silicide nanowire was formed by 10 nm-thickness Ni film. It was investigated that phase of this crystal structure is Ni$_3$Si$_2$. 
Figure 4.7 Results of EDS analysis for (a) 27 nm line width of Ni silicide nanowire formed by 10 nm-thickness Ni film and (b) 45 nm line width of Ni silicide nanowire formed by 7 nm-thickness Ni film. Counts of Ni/Si were measured.
4.3 Conclusion

In order to investigate Ni silicide phase more detail, atomic ratio of Ni/Si was calculated with model equation. In the case of Ni silicide nanowires formed by 10 nm-thickness Ni film, calculated Ni/Si atomic ratios were suitable for its resistivity. However, Ni silicide nanowires formed by 7 nm-thickness Ni film showed the discordance between Ni/Si atomic ratio and resistivity.

For measurement of true ratio, Ni silicide nanowires were observed by TEM and measured EDS. Ni silicide of nanowire with 27 nm line width formed by 10 nm-thickness Ni film was generally good and its phase was Ni$_3$Si$_2$. In contrast, Ni silicide of nanowire with 45 nm line width formed by 7 nm-thickness Ni film was not good condition. Also, its phase was assumed to be NiSi$_2$ with extra Si. It is considered that there are various causes for resistivity increase such as Ni silicide agglomeration, complicated grain boundary and excessive Si.
References


Chapter 5
Conclusion of This Study
5.1 Conclusion

Ni silicidation has been widely used to reduce the parasitic resistance at source and drain regions of MOSFETs. It is because Ni silicide is formed at relatively low temperature, with small Si consumption and has relatively low resistivity. This technology will continue to be used for highly scaled devices such as Si nanowire field effect transistors (Si NW FETs) and FinFETs of 10-20 nm generations. However one of the concerns of Ni silicides is their resistivity increase with the scaling, when applied to Si NW FETs. Also, as source and drain regions become extremely narrow and the amount of Si reacting with Ni is limited in these structures, this may lead to the silicide different from the case of the silicidation of the bulk silicon. In this study, in order to apply Ni silicide to high scale device, method of resistivity reduction was investigated. For this purpose, 2-step annealing process was performed as thermal annealing process to form Ni silicide in Si nanowire. Also, Ni film thickness sputtering on Si NW was controlled for forming low resistivity phase in narrow line width. Slicidation was performed by using 10, 80 and 120 nm-thickness Ni films. The Ni silicide NW line width is in the range from 20 nm to 90 nm. At first, the dependence of resistivity on the line width was obtained. Although drastic increases of the resistivity were observed for line width smaller than 40nm, they were suppressed with decrease of Ni film thickness. In order to investigate formed phase, temperature coefficients of resistance (TCRs) were measured. As a result, the TCRs with Si-rich phase were measured in the lowest resistivity. Therefore, Ni silicide NWs were formed by 7 nm-thickness Ni film to obtain smaller resistivities. However, overall increase of the resistivities were observed. N/Si atomic ratios calculated from the model equation did not accord with their resistivities which formed by 7 nm-thickness Ni film also. For more detail investigation about the
phase, TEM observation and EDS analysis were performed. In the case of 7 nm-thickness Ni film, ununiform silicide and complicated grain boundary were observed. Also, $\text{Ni}_3\text{Si}_2$ phase was measured in narrow line width with 10 nm-thickness Ni film. On the other hand, it was assumed that NiSi$_2$ and extra Si exist in NW formed by 7 nm-thickness Ni film. Increase of the resistivities may be occurred by these causes. Therefore, Ni film thickness should be optimized for NW width.
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Jinhan Song
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