A study on interface properties of La-silicate gate dielectrics with W carbide gate electrode

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Abstract of Master Thesis

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Lanthanum silicate thin films have been expected as candidates for direct contact of high-k to silicon structures in complementary metal-oxide semiconductor circuits for next generations. However, the interface properties are still not sufficient for device applications and a degradation trend with thickness scaling has been one of the issues.

The purpose of the thesis is to investigate the interface of lanthanum silicate and silicon by elucidating the effect of metal gate material. Therefore, new materials and new structures in MOSFET have been introduced to solve these issues. The interface properties have been characterized through fabrication and measurements of lanthanum silicate capacitors with either pure tungsten or nano-grained tungsten carbide gates.

Electrical properties of La-silicate MOS capacitors with nano-sized tungsten carbide (W\textsubscript{2}C) gate electrode has been experimentally investigated. Interface state density (D\text{it}) was suppressed by nano-sized W\textsubscript{2}C gate electrodes. Atomically flat metal/high-k and high-k/Si interfaces can be achieved, where the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. The improvement of interface properties could be attributed to stress-release by slips at grain boundary of columnar-shape nano-sized grains for W\textsubscript{2}C gate electrode.

Reliability of La-silicate with different gate electrodes, such as tungsten carbide and tungsten, was evaluated by degradation with stress time evolution and PBTI. Better reliability was obtained by nano-sized W\textsubscript{2}C gate electrode, presumably duo to nice interface properties.

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Chapter 1. Introduction

1.1 Introduction of high-k materials as gate dielectrics

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1.1 Introduction of high-k materials as gate dielectrics

Metal-oxide-semiconductor field effect transistors (MOSFET) have already been indispensable for very large scale integration (VLSI) technology, which is commonly used in modern electronic products, such as PC, smart phone, and digital cameras and so on. The key to the advancement of VLSI technology is the device scaling which means scaling down the size of MOSFETs. Until recently, SiO$_2$ as insulators has commonly used by doping poly-silicon on SiO$_2$ due to nice interface properties and good thermal stability [1.1]. However, with down-scaling, this system has faced the scaling limit due to the excess leakage current caused by short channel effects [1.2]. As a result, power consumption increases unacceptable level [1.3]. One of the solutions is to introduce high-k (dielectric constants) dielectrics which enables the devices to suppress leakage currents with the same capacitance, compared to SiO$_2$ gate dielectrics as illustrated in Figure 1.1.

![Diagram showing high-k dielectrics](image)

Figure 1.1 High-k dielectrics make it possible to get larger physical thickness than SiO$_2$ with same gate capacitance
High-k materials make it possible to thicken physical thickness with same equivalent oxide thickness (EOT). According to International Technology Roadmap for Semiconductor (ITRS), shown in Figure 1.2, EOT below 0.5 nm for planar bulk MOSFET is in required in near future. The EOT can be written as

$$EOT = \frac{K_{SiO_2}}{K_{high-k}} t_{OX}$$

(1.1)

where $\varepsilon_{SiO_2}$ are the permittivity of SiO2 and that of high-k materials, respectively.

Therefore, it is very important to select high-k materials. It is known that high dielectrics have high dielectric constant. Figure 1.3 shows the relationship of static dielectric constant and band gap for candidate gate oxide [1.4]. There are many materials for gate insulator, such as Al2O3, ZrO3, HfO2 and rare earth oxides. Among them, especially, Hf-based and La-based high-k materials are being utilized to replace SiO2 gate dielectrics for advanced CMOS application [1.5, 1.6].

Figure 1.2 Scaling roadmap of planar bulk MOSFET
1.2 Reported Hf-based oxides with direct contact structure

Here are the example of direct contact of HfO$_2$/Si structure, as shown in Figure1.4. In the figure on the left hand side, SiO$_2$-based IL was completely removed by controlling and reducing oxygen-related vacancy [1.7]. In the figures on the right hand side, direct contact was achieved by scavenging oxygen from a part of formed interfacial layer [1.8]. In both cases, direct contact of high-k/Si has been achieved by selection of gate material to control the oxygen atoms.
Figure 1.4 Examples of the direct contact of HfO₂/Si. In the case of Hf-based oxide, the direct contact of high-k/Si has been achieved by controlling the oxygen atoms [1.7, 1.8].
1.3 La-silicate as high-k gate dielectrics

La-silicate has attracted much attention. First advantage is high dielectric constant (k~20) and wide band gap [1.9]. Second advantage for La-silicate is that direct contact of high-k/Si structure can be easily achieved by simply depositing the La$_2$O$_3$ on the Si substrate to reactively form La-silicate after thermal annealing [1.10], as shown in Figure 1.5. Dielectric constant of La-silicate is dependent on supply of oxygen atoms, but excess supply of oxygen atoms decrease dielectric constant due to formation of Si-rich La-silicate [1.10]. Thus, control of oxygen partial pressure is the key for processing.

Third is that La-silicate is amorphous structure [1.10]. Using amorphous gate oxide has many advantage than a poly-crystalline oxide. For instance, crystallization of the dielectric after annealing treatment could result in grain boundaries serving as a path for dopant diffusion [1.11].

![Figure 1.5 Direct contact of La-based oxide and Si](image)
Another advantage of La-silicate is fairly nice interface properties. It has been reported that the interface state density ($D_{it}$) at the La-silicate/Si interface is reduced by increasing annealing temperature [1.13, 1.14], as shown in Figure 1.5.

Figure 1.5 Interface state density and annealing temperature relationship [1.10]

La-silicate gate dielectrics have advantage for 3D channel device application due to no orientation dependent EOT change [1.15]. Figure 1.6 shows that due to reactively-formed La-silicate gate dielectrics, no significant difference relating to the EOT between (100) and (110) orientation.

Figure 1.6 comparison of gate channel capacitance for (100) and (110) oriented nMOSFETs with deposited Si layer [1.13]
1.4 Scaling issues for La-silicate gate dielectrics

La-silicate gate dielectrics are regarded as promising candidates for gate dielectric materials for further EOT scaling. However, there are still serious issues to solve. One of the serious issues in high-k/metal gate stacks is degradation of effective mobility trend with EOT scaling, as shown in Figure 1.7. For both Hf-based and La-based high-k dielectric devices, the thinner the oxide thickness becomes, the worse effective mobility is [1.10, 1.14].

![Graph showing electron mobility vs. EOT]

Figure 1.7 A benchmark of high-field electron mobility at 1MV/cm [1.14]
It is thought that three factor dependent on electric field causes mobility reduction. One is Columbic scattering by trapped charges in the oxide or channel at low field. Second is phonon scattering at moderate field. Third is roughness scattering at high field [1.4].

Figure 1.8 Schematic of carrier mobility and effective gate field [1.4]
Figure 1.9 shows scaling issues for La-silicate. The interface of metal/high-k and high-k/Si plays an important role in MOS devices. At large EOT, the interface state density is almost determined by La-silicate/Si roughness, resulting in degradation of effective mobility. At scaled EOT, EOT<1nm, interface mixing at metal/high-k interface influences the interface state density, thus it is necessary to minimize the both interfaces for EOT scaling.
For further downsizing, suppression of threshold voltage variability (\(\sigma_{Vth}\)) becomes one of the most difficult challenges below gate length of 20 nm, as it affects yields and reliability of static random access memory and logic circuits [1.15]. The main causes of \(\sigma_{Vth}\) are thought to be random discrete dopants fluctuation (RDF) in channels, other process related origins such as line-edge roughness and working function variation, as shown in Figure 1.10. Moreover, polycrystalline granular structure of metal electrodes has been found to be dominant in \(\sigma_{Vth}\), when the gate dimensions become comparable to the grain size of metal electrodes, due to work function variability of different crystallographic orientation in the metal grains [1.16]. Thus, selection of proper metal gate materials is important to improve device performance.

Another most serious issue in high-k/metal gate stacks is reliability. Aggressive scaling of gate oxide thickness in CMOS transistors has caused the reliability of ultrathin dielectrics. It is therefore important to investigate the reliability of La-silicate gate dielectrics.

Figure 1.10 The cause of \(\sigma_{Vth}\) for EOT scaling
1.5 Introduction of metal gate

Doped poly-Silicon has been used as a gate electrode for CMOS devices for past few decades. However, with continued down-scaling of MOSFET, this system started to exhibit some serious problems, such as the poly-depletion effect at the poly-Si/Silicon oxide interface, the boron penetration, especially for ultra thin SiO$_2$, the boron would diffuse from the gate and into the channel region causing unwanted doping, resulting in the degradation of mobility and reliability, the high gate resistance, and poor compatibility with high-k gate dielectrics [1.17-1.19, 1.21], therefore, the research focus is shifted to metal gate electrodes. It is realized that high-k gate dielectrics must be implemented in conjunction with metal gate electrodes to get sufficient potential for CMOS continuous scaling. In order to improve transistor performance, the gate electrode material must have some good properties, such as thermal stability, high conductivity, CMOS process compatibility, and proper work function. But it is difficult to find metals satisfying these requirements.

![Figure 1.11 Polycrystalline metal [1.20]](image)
Metal gates has not problems of their own. The one of serious problem is threshold
toltage variability. This is due to the polycrystalline nature of the current metal gates, as
Figure 1.11. Polycrystalline metals are problematic as metal gate materials because the
gate dimensions for the metal grain size and orientation distribution exist, hence work
function distribution no longer averages out. This causes the threshold voltage to vary
from device to device since the threshold voltage is directly related to the gate work
function. Thus, metal gates with grain size less than 5 nm or amorphous are preferable,
as in Figure 1.12 [1.22, 1.23].

![Figure 1.12 Relationship of $V_{th}$ and grain size](image)
1.6 Purpose of this study

The purpose of the thesis is to investigate the La-silicate gate dielectrics for improvement.

1. A process for metal gate formation with nano-sized grains
2. Interface property improvement
3. Reliability of gate dielectrics improvement

In chapter 3, a novel process, multi-stacking of carbon and metal films with subsequent annealing process to reactively form metal carbides has been investigated. Nano-sized W₂C has been introduced for gate electrode application.

In chapter 4, electrical characteristic of La-silicate MOS capacitors with nano-sized W₂C gate electrode has been experimentally investigated. Interface state density can be largely reduced. Also, atomically flat metal/high-k and high-k/Si interface can be achieved.

In chapter 5, reliability of La-silicate gate dielectrics have been investigated with degradation with stress time evolution and Positive Bias Temperature Instability (PBTI).

Finally, chapter 6 summarizes of this study.
1.7 References


[1.17] P. Habas, and J. V. Faricelli, Investigation of the physical modeling of the gate


Chapter 2. Experiment and measurement procedures

2.1 Fabrication procedures

2.2 Experimental principle

2.2.1 Wafer cleaning

2.2.2 Deposition of La$_2$O$_3$ dielectrics by MBE

2.2.3 RF magnetron sputtering

2.2.4 Patterning of resist by photo lithography

2.2.5 Dry etching by RIE

2.2.6 PMA in FG ambient

2.3 Characterization method

2.3.1 Estimation of interface state density by conductance method

2.4 References
2.1 Fabrication procedure

Figure 2.1 shows the fabrication flow of capacitors. MOS capacitors were fabricated on $n$-Si (100) substrates with doping of $3 \times 10^{15} \text{ cm}^{-3}$. After performing SPM and HF chemical cleanings with $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$ mixture at 130 °C for 5 minutes, we conducted deposition of thin $\text{La}_2\text{O}_3$ gate dielectric films by e-beam evaporation at a substrate temperature of 300°C. Tungsten and carbon multi-stacking layers with total thickness of 10 nm were deposited by Radio Frequency (RF) magnetron sputtering without breaking the ultra-high vacuum. Then, TiN (10 nm) and Si (100 nm) capping layers were deposited on W/C metal also by RF sputtering to control the silicate reaction [2.1, 2.2]. The samples were annealed at 800°C in forming gas (N$_2$:H$_2$=97:3) ambient. Backside contacts were formed by Al deposition. Finally, the sample was annealed in forming gas ambient at 420 °C for 30 minutes.

![Figure 2.1 Experimental procedure of capacitor](image.png)
2.2 Experimental principle

2.2.1 SPM cleaning and HF treatment

Particles and organic substance at the surface of Si substrate become a cause of false operation. Therefore, it is important to clean the surface of Si substrate. SPM cleaning is one of the effective cleaning methods. The cleaning liquid is made from H$_2$O$_2$ and H$_2$SO$_4$ (H$_2$O$_2$:H$_2$SO$_4$=1:4). Because of its oxidizability, particles and organic substance are oxidized and separated from the surface of Si substrate. However, the surface of Si is oxidized and SiO$_2$ is formed during SPM cleaning. 1% HF is used to eliminate the SiO$_2$.

2.2.2 La$_2$O$_3$ deposition by MBE

Molecular beam epitaxy (MBE) is one of the deposition methods for crystalline growth, which is classified into vacuum evaporation. Figure 2.3 shows schematic illustration of MBE. A source material of La2O3 is heated by electron beam (E-beam) and emits the molecules. The deposition is done in ultra high vacuum (~10$^{-6}$Pa), so that the molecule of La$_2$O$_3$ doesn’t absorb the scattering of other molecules and be deposited on substrates. The physical thickness of deposited film is measured by crystal oscillator.

![Figure 2.3 Schematic illustration of MBE](image_url)
2.2.3 RF magnetron sputtering

Tungsten and carbon which are used as gate electrode in this study are deposited by radio frequency (RF) magnetron sputtering with Ar gas. In the chamber filled with the Ar gas, the high voltage is applied in high frequency between substrate side and target side. A magnet is set underneath the target to prevent plasma damage. Then, Ar molecules are divided into Ar ions and electrons because of the difference of mass. Ar ions hit the target atoms to be deposited on the substrate. By the crush, the particles of the target are emitted and deposited on the wafer.

Figure 2.4 Schematic illustration of RF magnetron sputtering.
2.2.4 Patterning of resist by photo lithography

Resist-patterning is the method to eliminate needless parts of metal to obtain the gate electrode. First, the gate electrode is covered with positive resist, a part exposed to light is removed by the solvent. In order to make thickness of the resist uniform, Si-substrate covered with resist are revolved using spinner. After the resist on the substrates are heated (“Pre-bake”), the position of substrates are adjusted with respect to photo mask for patterning of resist. Then, they are soaked into the developer, and the resist covered with the mask is remained. Finally, they are heated to fix the resist (“Post-bake”).

2.2.5 Dry etching by RIE

Reactive ion etching (RIE) is one of the method to etch for patterning. Etching gases used for etching metal electrodes of W TiN and Si capping layer are Cl₂ and O₂, respectively. The gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important.

2.2.6 PMA in F.G ambient

Post metallization annealing (PMA) is very important process to fabricate high performance devices. The structure and properties of silicon that has periodicity terminate at the surface between Si and gate dielectrics. So many dangling bonds that cause interface state are generated there. PMA is used in order to terminate them. After it is formed a vacuum, forming gas (F.G) (N₂:H₂ = 97:3) is flown and the substrate are heated at 420 or 800°C for 30 min. Thus, forming gas annealing is effective to decrease Dᵢᵣ.
2.2.7 Vacuum evaporation for Al deposition

Al for wiring and backside contact is deposited by vacuum evaporation. Al source is set on W boat and heated up to boiling point of Al by joule heating. However, melting point of W is higher than boiling point of Al, W boat doesn’t melt. The base pressure in the chamber is maintained to be $10^{-3}$ Pa, as shown in.

Figure 2.6 Vacuum evaporation for Al deposition
2.3 Estimation of interface state density by conductance method

In this study, conductance method, proposed by Nicoliian and Goetzberger in 1967 [2.3], is used to estimate interface state density \( D_{it} \). Conductance method is replace to the equivalent circuit of MOS capacitor. AC voltage is applied to the device, and the frequency of that changes, and \( D_{it} \) can be measured. Figure 2.6 shows an equivalent circuit model of MOS capacitor [2.3], where \( C_{ox} \) is the oxide capacitance per unit area, \( C_s \) is the silicon capacitance per unit area, \( R_{it} \) and \( C_{it} \) are the resistance and capacitance components per unit area related to interface trap, and \( G_t \) is tunnel conductance per unit area related to leakage current. On the other hand, the equivalent circuit converts to the equivalent parallel circuit. Figure 2.7 shows the equivalent parallel circuit, where \( C_p \) and \( G_p \) are the equivalent parallel capacitance and conductance per unit area, respectively.

\[
\begin{align*}
&\text{(a)} & \quad \text{(b)} & \quad \text{(c)} \\
&C_{ox} & \quad C_{it} & \quad G_t \\
&C_s & \quad R_{it} & \quad C_m \\
&C_{it} & \quad G_m & \quad C_{ox} \\
&C_p & \quad G_p & \quad \text{MOS capacitor} \\
&\text{MOS capacitor} & \quad \text{measured circuit} & \quad \text{simplified circuit of (a)}
\end{align*}
\]

Figure 2.7 Equivalent circuits of MOS capacitor; (a) an equivalent circuit model of the MOS capacitor, (b) the measured circuit, (c) the simplified circuit of (a)
$C_p$ and $G_p$ are given by

$$C_p = C_s + \frac{qD_{it}}{1 + (\omega \tau_{it})^2}$$  \hspace{1cm} (2.1)$$

$$G_p = \frac{q\omega \tau_{it} D_{it}}{\omega} \frac{1 + (\omega \tau_{it})^2}{1 + (\omega \tau_{it})^2}$$  \hspace{1cm} (2.2)$$

Where $C_{it}=qD_{it}$, and $\tau_{it}=C_{it}R_{it}$. $D_{it}$ is interface state density and $\tau_{it}$ is interface trap time constant here. These equations estimate that interface trap is single energy level in the band gap. Actually, interface traps are continuously distributed. Therefore, these two equations are rewritten as [2.3]

$$C_p = C_s + \frac{qD_{it}}{\omega \tau_{it}} \tan^{-1}(\omega \tau_{it})$$  \hspace{1cm} (2.3)$$

$$G_p = \frac{qD_{it}}{\omega} \frac{\ln[1 + (\omega \tau_{it})^2]}{2\omega \tau_{it}}$$  \hspace{1cm} (2.4)$$

In these two equations, the continuum level for interface traps is considered.

But, there is serious error between continuum level and measurement data. This is generated by inhomogeneities in oxide charge and interface charge. Therefore, we have to consider the effect of surface fluctuations following normal distribution, and then Eq. (2.4) becomes
\[ \frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{ii}}{\omega \tau_{ii}} \ln \left[ 1 + (\omega \tau_{ii})^2 \right] P(\psi_s) d\psi_s \quad (2.5) \]

\[ P(\psi_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp \left[ -\frac{(\psi_s - \overline{\psi}_s)^2}{2\sigma^2} \right] \quad (2.6) \]

Where \( \psi_s \) is surface potential, \( \overline{\psi}_s \) and \( \sigma \) are mean and standard variation of the surface potential, respectively. So the larger \( \sigma \) is, the lower values of the peak and broader width of the curves are. Then, we consider the measurement equation. Figure 2.7(b) changes the figure 2.7(c). Compared with the Eq. (2.5), \( \frac{G_p}{\omega} \) of Figure 2.7(c) is given by

\[ \frac{G_p}{\omega} = \frac{\omega (G_m - G_t) C_{OX}^2}{(G_m - G_t)^2 + \omega^2 (C_{OX} - C_m)^2} \quad (2.7) \]

The measurement data can be obtained from Eq. (2.7), where the capacitance and conductance are \( C_m \) and \( G_m \), respectively.

**2.4 Conclusion**

In this chapter, we explained the experimental procedure, and the principle of measurement. The sample was produced at this laboratory.
2.5 References


Chapter 3. Experiment and measurement procedures

3.1 Tungsten Carbide formation

3.2 Process for W₂C gate electrode

3.3 Characteristic of W₂C electrode

3.4 Conclusion

3.5 References
3.1 Tungsten carbide formation

Tungsten carbide takes several stable composition such as WC or W\textsubscript{2}C in W-C phase diagram, as shown in Figure 3.1. The hardness of tungsten (W) carbide (C) is sufficiently stable and decreases reliability little compared to other carbides [3.1].

![Tungsten carbide phase diagram](image-url)
3.2 Process for W$_2$C gate electrode

It is not easy to obtain W$_2$C because of high temperature process, more than 1523 K. We realized the W$_2$C gate electrode to use multi-stacking of tungsten and carbon layer. A set of carbon and W layer which corresponds to atomic ratio, was cyclically stacked for 18 times, as shown in Figure 3.2. The thickness of each C layers in the stacked sputtering were varied from 0.22 to 0.45 nm, while the thickness of the W layer is kept constant as 0.7 nm. The varied thickness corresponds to an atomic concentration from 1:0.5 to 1:1. Metal gate electrode result in a total thickness of 20 nm before annealing process. Advantage of this kind process, first is that excess growth of grain size is suppressed by layered reaction. Second, carbon content can be controlled. Third, metal carbide can be formed at low temperature. Here, the density and number of carbon atoms in sputter deposited carbon film was evaluated to be 2.05 g/cm$^3$ and $7.8 \times 10^{17}$ /cm$^3$, respectively, by x-ray reflectivity.
3.3 Characteristic of W₂C electrode

Figure 3.3 shows the $\rho_{sh}$ change on annealing temperature for four kinds of C concentrations. First decrease in $\rho_{sh}$ was observed at 700 °C, and second one at 825 °C, indicating drastic phase change in the films.

Figure 3.3 Sheet resistance of multi-stacked W/C layers

Figure 3.4 shows the in-plane XRD spectra of W/C with 1:0.5 and 1:1, annealed at 750 °C, compared to pure W. With W/C of 1:0.5, weak diffraction peaks suggest the mixture of hexagonal W₂C and hexagonal WC phases in the film with grain size of 18 and 19 nm, respectively. On the other hand, for the film with W/C of 1:1, only hexagonal W₂C with grain size of 1.9 nm was detected. The cross-sectional transmission electron microscope
(TEM) image revealed a column-shaped metal layer with grain size of 2 nm, which is in good agreement with the value extracted by XRD peaks, as shown in Figure 3.5. For W/C of 1:1 annealed at 900 °C, TEM image shows the same grain size (width : 20 nm, height : 12 nm) as pure W, corresponding the size of 20 nm extracted by XRD pattern based on strong signals related to cubic W.

Figure 3.4 XRD measurement of multi-stacked W/C layers and pure W
As the interface between W and SiO$_2$ becomes rough with the presence of a weak contrast at the interface, we can consider that interface reaction took place on annealing. At an annealing temperature above 850 $^\circ$C, pure W was formed due to reaction of C and SiO$_2$ as SiO$_2$(s)+3C(s) $\rightarrow$ SiC(s) + CO (g) [3.2].

Therefore, W$_2$C was confirmed at an annealing temperature from 725 to 825 $^\circ$C. The $\rho_{\text{sh}}$ of 94 $\Omega$/sq., 188 $\mu$Ωcm in resistivity, is only a double compared to that of bulk W$_2$C [3.3]. As the electron mean free path of W$_2$C is 1.8 nm, the main scattering mechanism can be attribute to grain boundary and not by the thickness of the film.

To confirm the oriented growth, normalized intensities of each diffraction plane of carbides are summarized in table 3.1. W$_2$C layer showed strong preferred orientation with (002) plane, which indicates that c-axis of W$_2$C crystals is in parallel to the surface of SiO$_2$. 

Figure 3.5 TEM of multi-stacked W/C layers
Table 3.1 Normalized intensities of in-plane XRD measurement and powder diffraction patterns of W$_2$C. (JC-PDS 00-035-0776)

<table>
<thead>
<tr>
<th>(hkl) of hexagonal W$_2$C</th>
<th>(100)</th>
<th>(002)</th>
<th>(101)</th>
<th>(102)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/C stacked film annealed at 750 °C</td>
<td>23</td>
<td>355</td>
<td>100</td>
<td>1</td>
</tr>
<tr>
<td>Powder diffraction pattern of hexagonal W$_2$C$^c$</td>
<td>23</td>
<td>24</td>
<td>100</td>
<td>14</td>
</tr>
</tbody>
</table>

3.4 Conclusion

A set of C/W (0.45/0.70 nm), was cyclically stacked on Si (100) substrates by sputtering, resulting in a total of 20-nm-thick C/W multi-layered film. Sheet resistance ($\rho_{sh}$) showed stable values from 725 to 825 °C, where formation of W$_2$C was confirmed by in-plane XRD with grain size of 1.9 nm. TEM image showed columnar-oriented growth of W$_2$C film, aligned to <100> direction parallel to the surface. W$_2$C has large advantages in terms of grain size and oriented growth for scaled devices.

3.5 References


Chapter 4. Electrical characteristics of La-silicate gate dielectrics

4.1 Electrical characteristic of La-silicate

4.2 Conclusion

4.3 References
4.1 Electrical characteristics of La-silicate capacitors

Figure 4.1 shows the capacitance-voltage (CV) characteristics of La-silicate MOS capacitors with pure W or W\textsubscript{2}C metal gate. We obtained both samples with similar EOT of 0.75 nm, suggesting there is no difference in interface reaction rate between the metal gate electrode materials. Also similar flatband voltage ($V_{fb}$) was measured, indicating that there is little change in the influence of metal gate electrodes to interface charges. Humps in depletion region, which is typically observed for high-k/Si direct contact capacitors, were sufficiently suppressed for both samples, indicating fairly nice interface properties.

![Figure 4.1 Capacitance-voltage curve of La-silicate gate dielectrics on Si (100) substrates with W and W\textsubscript{2}C metal gate electrodes.](image)

We measured the interface state density ($D_{it}$) of both samples with conductance method, taking the surface potential fluctuation of 80 meV into account [4.1]. $D_{it}$ of $9.5 \times 10^{11}$ and...
2.5×10^{11} \text{ cm}^2/\text{eV} \text{ for W and W}_2\text{C metal gate electrodes, respectively, were obtained. A low interface state density was achieved with W}_2\text{C gate electrodes, which is one third of that with W gate electrodes. From the trap time constant dependency on surface potential, identical capture cross sections of 3×10^{-15} \text{ cm}^2 \text{ were extracted among the samples, which is comparable to those reported on thermal SiO}_2 \text{ on Si}(100) \text{ surface [4.2]. Therefore, the physical nature of the } D_{it} \text{ can be thought to be the same, and only the amounts of the trap states are different. Figure. 4.2 shows } D_{it} \text{ dependency on EOT. It reveals that } D_{it} \text{ can be reduced in all the studied EOT range with W}_2\text{C gate electrode. We can see a slight degradation in } D_{it} \text{ with smaller EOT, which is in a good agreement with previous reports [4.3].}

![Figure 4.2 D_{it} dependency on EOT for W and W}_2\text{C metal gate electrodes.}](image-url)

Cross-sectional transmission electron microscope (TEM) images of the electrically measured capacitors with W and W$_2$C gate electrodes are shown in Figure 4.3 (a) and (b), respectively. One can find rough metal/high-k and high-k/Si interfaces with W gated capacitor. Interface height position analysis showed root-mean-square (RMS) roughness of metal/high-k ($R_{a, MG/HK}$) and high-k/Si ($R_{a, HK/Si}$) interfaces to be 0.61 nm and 0.33 nm, respectively. On the other hand, the TEM image of the capacitor with W$_2$C gate electrode showed an atomically flat metal/high-k and high-k/Si interface; $R_{a, MG/HK}$ of 0.26 nm and $R_{a, HK/Si}$ of 0.12 nm. An RMS roughness of 0.12 nm is comparable to those of thermal SiO$_2$ on Si (100) substrates formed at high temperature with enough thickness [4.4].

Figure 4.3 Cross sectional TEM images of La-silicate capacitor with (a) W gate electrode and (b) those of W$_2$C gate electrode.
An intuitive explanation of the reduction in \( D_{it} \) with \( W_2C \) gate electrode can be drawn from the improvement in flatness at La-silicate/Si interface. Generally, edge sites in the step atoms at SiO\(_2\)/Si (100) interface responsible for \( D_{it} \), so that higher atom steps at the interface which constitute a stronger distortion at the step edge increase \( D_{it} \) [4.5]. The appearance of edge steps at the interface is commonly observed when Si (100) substrates are oxidized below a temperature where the viscous flow is hardly presented.

The interface roughness is reported to arise due to inhomogeneous local stress effect, and to be more prominent when surface irregularities increases [4.6]. In addition to the interface roughness difference between the samples, a dark contrast in the Si substrate can be observed in the TEM image of the capacitor with W gate electrode, which is not presented in that with \( W_2C \) gate electrode. Dark contrasts in TEM image in single crystalline silicon can result from poor crystallinity or by strain due to change in the lattice constant [4.6]. Here, both TEM specimens were prepared through identical focus-ion beam (FIB) sampling technology, so that preparation-induced damage to worsen the crystallinity can be eliminated. Thus, one can consider that a strong inhomogeneous residual stress exists in the Si substrate near the surface, which extends down to several hundreds of nanometers deep in Si substrate. Fast Fourier transform (FFT) analysis of the roughness taken from TEM images are shown in Figure. 4.4. By comparing the power spectral density of both interfaces, higher values from 0.04 to 0.06 nm\(^{-1}\) in spatial frequency, which corresponds to interface roughness period of 17 to 25 nm, can be confirmed with W gate electrode. These values are comparable to the average grain size of 20 nm in W gate electrode which is obtained from x-ray diffraction measurements [4.8].
Therefore, a strong correlation exists between the grain size of the metal gate electrode and the interface roughness. The starting materials were both the same for W and W$_2$C gate electrodes, the appearance of interface roughness should arise during the reaction to form La-silicate layers between La$_2$O$_3$ and Si substrate. Generally, surface reaction rate can be anisotropic depending on crystal planes due to difference in surface energy and elastic constants [4.9]. Moreover, the reaction can be inhomogeneous due to defects or impurities at the surface [4.10]. In this study, however, the starting materials are the same and are processed through identical wet cleaning, deposition and annealing processes so that the effects contaminants on the formation of interface roughness can be negligible. As the only difference is the metal gate material, the effect of stress induced from the metal layer can be the origin to change the interface roughness.
According to the reports on amorphous-to-crystalline transformation in silicon, the crystallization rate is affected by the stress applied in the plane of interface; higher rate with tensile stress and lower rate with compressive stress, where the effect of stress is interpreted as the change in the activation energy of reaction, as shown in Figure 4.5 [4.11]. For our case, crystal grains accompanied by grain boundaries in W gate electrode may induce non-uniform stress to the Si surface to change the rate of silicate reaction, which results in roughening the interface. As a result of small average grain size of 1.9 nm with W$_2$C gate electrode, the stress accompanied during reaction can be evened out, so that the initial surface flatness can be hardly infected. The increase in $D_h$ with smaller EOT might be understood from increase in stress due to thinner La-silicate film thickness.
In the meantime, the origin of the intensity observed around a spatial frequency of 0.2 nm\(^{-1}\), which corresponds to spacing of 5 nm, for both W and W\(_2\)C samples, is still not clear. For thermal SiO\(_2\) on Si (100) case, it is reported that high-frequency roughness is increased by longer oxidation, and roughness spacing of 5 nm is typically observed [4.12]. The roughness spacing can be eliminated by specific post-oxidation anneal treatments to smoothen the interface by thermodynamic smoothing effect. Therefore, one can expect further roughness improvement at higher frequency for La-silicate/Si interfaces with post-thermal treatments.
Height-to-height correlations of both La-silicate/Si interfaces are shown in Figure 4.7. Both interfaces did not show any scaling dependency, which suggests that presented interfaces are not self-affine structures, and follows random Gaussian distribution from atomic scale [4.13]. This is not the case for thermal SiO_{2}/Si interface case where a balance between local stress to roughen and viscous flow to smoothen the interface is presented within a specific scale length [4.14]. Therefore, one can conclude that metal gate electrodes with nano-sized grains or even amorphous structures are effective for obtaining atomically flat La-silicate/Si interfaces by removing inhomogeneous local stress. Also, a flat metal/La-silicate interface can be obtained with nano-sized grain metal, which is effective in suppressing gate oxide thickness variability. Incidentally, we would like to note that metal gates with nano-sized grains are mandatory in terms of threshold voltage variability suppression, which holds the right direction for metal gate material selection for scaled devices.
4.2 Conclusion

The interface properties of reactively formed La-silicate gate dielectrics on Si substrates with W or nano-sized grain W$_2$C gate electrodes have been investigated. An interface with periodic roughness comparable to the average grain size of W gate electrode has been observed, where an atomically flat La-silicate/Si interface has been obtained with nano-sized grain W$_2$C gate electrode. The origin of smooth interface roughness may be attributed to the elimination of inhomogeneous stress induced by metal grains during the formation of silicate at the interface.
4.3 References


Chapter 5. Reliability of La-silicate high-k with tungsten carbide gate electrode

5.1 Interface state density degradation for La-silicate dielectrics with W_{2}C gate electrode

5.2 Positive Bias Temperature Instability

5.3 Conclusion

5.4 References
5.1 Interface state density degradation for La-silicate dielectrics with W$_2$C gate electrode

Figure 5.1 shows $D_{it}$ versus stress time plot on different stress bias ($V_{st} = 2.0$ V, 3.0V). Interface state density increase with increasing of stress voltage for both case, indicating the generation of electron trapped state in random positions inside La-silicate dielectrics, but W$_2$C gate electrode effectively suppress the $D_{it}$.

Figure 5.1 Relationship between stress time and interface state density
5.2 Positive Bias Temperature Instability (PBTI)

Bias Temperature Instability (BTI) is typically observed as a flatband ($V_{fb}$) or threshold ($V_{th}$) shift after a bias voltage has been applied to a MOS gate electrode at elevated temperature [5.2]. Figure 5.2 shows dependence of $V_{fb}$ on total at various stress voltage, EOT = 0.75 nm. The both samples were measured at room temperature.

Figure 5. Dependence of flat band voltage shift ($V_{th}$) on total stress time
Symbols denote data from Constant-Voltage Stressing (CVS) measurement and solid lines are model calculations. A model for charge trapping in high-k gate dielectric stack is proposed. The model calculates $\Delta V_{fb}$ function of stressing time and injected charge density using three fitting parameters. The model equation is given by \[5.2\]

$$\Delta V_{fb} = \Delta V_{max} \left( 1 - \exp\left[ -\left( \frac{\tau}{\tau_0} \right)^\beta \right] \right) \quad (5.1)$$

Where, $\Delta V_{max}$, $\tau_0$ and $\beta$ is fitting parameter. As in table 5.1, for SiO2 gate dielectric $\beta$ is 1. Compared to reported results on Hf-based dielectrics, $\Delta V_{fb}$ for La-silicate with W$_2$C gate electrode was suppressed, indicating the capacitor with W$_2$C has better reliability than that with W gate electrode.

<table>
<thead>
<tr>
<th>Structure</th>
<th>$\beta$</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$/Si</td>
<td>1</td>
<td>[5.3]</td>
</tr>
<tr>
<td>$n^+$polysilicon/HfO$_2$/SiON/n-Si</td>
<td>0.33</td>
<td>[5.3]</td>
</tr>
<tr>
<td>polysilicon/TiN/HfO$_2$/n-Si</td>
<td>0.16~0.19</td>
<td>[5.4]</td>
</tr>
<tr>
<td>W/La-silicate/n-Si</td>
<td>0.27</td>
<td>This work</td>
</tr>
<tr>
<td>W$_2$C/La-silicate/n-Si</td>
<td>0.39</td>
<td>This work</td>
</tr>
</tbody>
</table>
5.3 Conclusion

Reliability of La-silicate gate dielectrics with W\textsubscript{2}C and W gate electrode have been investigated by time dependent degradation and PBTI with constant voltage stressing. La-silicate MOS capacitors with W\textsubscript{2}C gate electrodes show better reliability due to nice interface properties.

5.4 References


Chapter 6. Conclusion

6.1 Conclusion of this study

6.2 Prospects for further study
6.1 Purpose of this study

In this thesis, nano-sized $W_2C$ metal gate electrodes were introduced La-silicate capacitor. As a result, improvement of interface properties for La-silicate gate dielectrics was achieved with $W_2C$ gate electrodes.

In chapter 3, a sputtering process using multi-stacking of carbon and metal thin films with subsequent annealing process to reactively form $W_2C$ has been introduced. $W_2C$ layer formed by the process gives high potential to form carbides with highly-oriented and nano-sized grains.

In chapter 4, electrical properties of La-silicate MOS capacitors with nano-sized $W_2C$ gate electrode has been experimentally investigated. Interface state density ($D_{it}$) was largely reduced by one-third for the capacitor with $W_2C$ gate electrode. Atomically flat metal/high-k and high-k/Si interfaces can be achieved, where the interface roughness extracted from TEM is 0.26 and 0.12nm, respectively. The improvement of interface properties could be attributed to stress-release by slips at grain boundary of columnar-shape nano-sized grains for $W_2C$ gate electrode. In chapter 5, Reliability of La-silicate with different gate electrodes, such as tungsten carbide and tungsten, was measured first time by degradation with stress time evolution and PBTI. Better reliability was obtained by nano sized $W_2C$ gate electrode, presumably duo to nice interface properties.

6.2 Prospects for further study

1. More statically study reliability of La-silicate
2. Further EOT scaling of La-silicate gate dielectrics with $W_2C$ gate electrodes.
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