A Study on Process and Device Structure for Schottky and Heterojunction Tunnel FETs using Silicide-Silicon interface

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Introduction

Increase in subthreshold leakage current is a major issue at scaled devices.
Scaling in conventional FET

G. Bidal et al., Silicon Nanoelectronics Workshop (SNW), 2009.

Mobility enhancement

3D:

planar:

Gate

Si

Gate

Si

Less interface roughness scattering in 3D

Potential 1D ballistic transportation


Higher $I_{ON}/I_{OFF}$ ratio

Injection velocity is the dominant limiting factor for drain current at scaled devices.
Scaling Today

Nanowire, multi-gate MOSFET
  • reduce the short channel effect
  • improve gate field effect


Supply voltage scaling can be expected by using III-V compound semiconductors (higher electron injection velocity) at n-MOSFET channels.

Cost and process are main issues.

✓ $I_{on}/I_{off} < 10^7$, $S \sim 62–75$ mV/dec and low DIBL (20mV/V)
✓ $I_{off}$ savings compared to bulk CMOS
✓ Current per NW: $\sim 1 \mu A$ -> need arrays

S value reaches the limit value of 60eV/dec.
Motivation for this Research

**Low subthreshold voltage is desirable for the ease of switching the transistor off.**

Subthreshold factor has a lower bound of 60mV/decade in conventional MOSFETs

\[
S = \ln(10) \frac{dV_G}{d(\ln I_d)} = 2.3 \frac{kT}{q} \frac{C_{ox} + C_d}{C_{ox}} > 60mV / \text{decade}
\]

It is important to increase ON/OFF ratio to reduce device power consumption use new injection mechanism
FETs with new mechanism and principle


G. A. Salvatore, et al., IEDM.2008.4796642

IMOS

FETs with new mechanism and principle


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Negative capacitance

Reliability issues due to using avalanche effect at dielectric vicinity

Crystallization of ferroelectric material, causes, strain on bottom dielectric layer and increase Leakage current.

Advantages of Tunnel FET for steep S-factor

Tunnel FET

Tunneling injection

P-source  N-channel

Carrier injection occurs only when source and channel have equal potential → Steep ON/OFF ratio is possible

Main Challenge of TFET

p⁺in⁺ Si-TFET has high tunnel resistivity → ON current is degraded due to high resistance
Recent examples of Tunnel FET

S-factor below the 60mV/dec. was achieved however, ON current is small.

The highest experimental ON current value of $10^{-4}$A/µm is achieved by using III-V compound semiconductor. (complicated process)
Silicide Schottky source/drain (S/D) FETs

MOSFET scaling

Issue of Short channel effect

Controllability of impurity distribution in S/D region

Silicide S/D

NiSi (metal), Mg2Si (semiconductor)

W. Mizubayashi et al., VLSI symp., 88 (2011).
N. Mise et al., T-ED, 55, 1244 (2008).

Advantage of Silicide S/D

- abrupt and shallow junction
- robust against short-channel effect
- low resistance
- low temperature process


Silicide Schottky S/D is a candidate for scaled FETs
Concept of Schottky junction device

Thermionic tunneling

Band to band tunneling

By using silicide material for MOSFET source region

- abrupt + low defect junction
- lower tunnel resistivity + contact optimization
1. Introduction

2. Detail of Simulation and device process

3. Evaluation of Schottky contact MOSFET with considering structure parameter

4. Schottky contact and barrier height alignment

5. Band Discontinuities at Source-Channel Contact in Tunnel FET Performance

6. Heterojunction Tunnel-FET using Semiconducting silicide-Silicon contact and its scalability

X. Semiconducting silicide/ Si hetero junction

Schottky contact tunnel FET

Heterojunction tunnel FET

7. conclusion
Purpose of this Research

✓ Propose source contact guidelines and process for Tunnel FETs using low defect Schottky contact technology.

✓ Investigating structure parameters of band-to-band Tunnel FET with discontinuous junction.
Thermionic emission and tunneling emission were used to calculate injection current at the Schottky junction.

Device structure was based on FDSOI platform to minimize short channel effects.
Matsuzawa, et al., IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 47, NO. 1, 2000

✓ Martsuzawa model

\[
J_{TE} = \begin{cases} 
\frac{AT}{k_B} \int_{\xi - q \Delta \phi_B}^{\infty} (f_S(\xi) - f_M(\xi)) \, d\xi, \\
\frac{AT}{k_B} \int_{\xi - q \Delta \phi_B}^{\infty} \ln \left( \frac{1 + f_S(\xi)}{1 + f_M(\xi)} \right) \, d\xi, 
\end{cases}
\]

\[
\Delta \phi_B = \sqrt{q |E_d| / 4 \pi e}
\]

✓ Lombardi CVT Model: Matthiessen’s rule

\[
\mu T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1}
\]

\(\mu_{AC}\) scattering with acoustic phonons

\(\mu_{sr}\) The second component, \(\mu_{sr}\), is the surface roughness

\(\mu_b\) scattering with optical intervalley phonons


✓ Shockley-Read-Hall (SRH) Recombination

✓ SRH Concentration-Dependent Lifetime Model

✓ Trap Assisted Auger Recombination

✓ semiconductor bandgap narrowing

✓ Includes the effects of Fermi statistic into the calculation of the intrinsic concentration in expressions for SRH recombination.
2D simulation (Channel concentration)

Higher channel doping concentration leads to
Steep potential barrier $\rightarrow$ increase tunneling probability
Lower $\phi_B$, leads to higher volume Injection $\rightarrow$ lower S-factor can be achieved
Degradation of $S$-factor and $V_{\text{th}}$ roll-off can be suppressed at smaller channel lengths for SBHT-FET compared to conventional FET.
Higher $\phi_B$ results in improved S-factor for short channel.

Increasing channel doping concentration leads to smaller S-factor (same as long channel trend).
At Lg\textasciitilde{}15\,nm $\phi_B$ and S-factor relation is reversed.

It is important to modulate $\phi_B$ according to channel length.
Higher channel doping concentration results in shallow Schottky depletion layer. This leads to higher tunneling probability and improved S-factor.

For short channel devices, SBHT-FET can suppress electric field penetration and prevent S-factor degradation.

S-factor and Ion/Ioff ratio optimization

Barrier heights need low Long Channel high Short Channel (10nm)
Control of silicide phase and interface reaction with wide process window is required for silicide Schottky S/D FETs.
Schottky diode fabrication process

**Ni/Si stacked structure**

Si(1.9nm)/Ni(0.5nm) x 8 layers

**Impurity incorporating**

Si/Ni x 7 layers + Ni₃P:0.68nm/Si:1.9nm

Spreading resistance measurement

(n-Si(100) Sub with 400 nm SiO₂ (3x10¹⁵ cm⁻³))

- SPM and HF cleaning
- Diode patterning
- BHF etching of SiO₂
- Deposition by RF sputtering
  - (Ni:0.5nm/Si:1.9nm) x 8
  - (Ni:0.5nm/Si:1.9nm) x 7 + (Ni₃P:0.68nm/Si:1.9nm)
  - (Ni:0.5nm/Si:1.9nm) x 8 + B:0.13nm
- Backside Al contact
- RTA: 1min in N₂ (silicidation)
Interface reaction of stacked silicidation process

Cross sectional TEM

- atomically flat interface and smooth surface
- no thickness change before and after annealing
- interface position can be well-defined

Silicidation with narrow Fins

Stacked silicidation process is candidate for silicide Schottky S/D.
Schottky barrier height ($\phi_{Bn}$) modulation

Dopant segregation with silicidation

Dopant segregation by activation anneal

Control of dopants and junction position are the key.


W. Mizubayashi et al., VLSI symp. (2011).
$\phi_{Bn}$ modulation by P or B incorporation

**Diode characteristics**

RTA: 500°C, 1min in N$_2$

P: Ohmic

Control: 0.63 eV

B: 0.68 eV

$\phi_{Bn}$ modulation is confirmed.

**Dependence of annealing temperature**

RTA: 500°C, 1min in N$_2$

P: Ohmic

Control

B

$\phi_{Bn}$ modulation is achieved by impurity incorporation at interface with stacked silicidation process.

Stable property with wide process window
SOI-silicide Schottky S/D FET

Fabrication process
- SOI patterning
- Gate oxide (1000 °C)
- Stacked silicide for S/D (with B or P)
- TEOS (200 °C)
- Gate metal depo./etch.
- Contact
- FG anneal (500 °C)

SOI patterning
Gate oxide (1000 °C)
Stacked silicide for S/D (with B or P)
TEOS (200 °C)
Gate metal depo./etch.
Contact
FG anneal (500 °C)

Ambipolar characteristics is suppressed by P incorporating.

\[ \phi_{Bn} \] modulation was also confirmed with FET operation.
Conclusions chapter 4

**Ni/Si stacked silicidation process**

- atomically flat silicide/Si interface
- junction position is well-defined
- stable property up to 850 °C annealing

**Schottky barrier height ($\phi_{Bn}$) modulation**

- $\phi_{Bn}$ modulation is achieved by P or B incorporation at interface (ohmic ~ 0.68 eV)
- suppression of ambipolar characteristics with silicide Schottky S/D FET
✓ Schottky barrier built in potential can suppress electric field penetration.
✓ This prevents degradation of S-factor and ON/OFF ratio at short channel device.
✓ Stack layer spattering could form atomic flat silicide with barrier height moderate

Moderate the barrier height process and the SHBT-FET device design had proposed

The majority injection of SBHT-FET is due to thermionic emission, Therefore the S-factor has a lower limit of 60mV/dec.

To achieve lower S-factor with high ON/OFF ratio, the majority injection Must be due to tunneling emission.
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Drive current imaging in Tunnel FET

Energy barrier ($\Delta E$): material of source and channel
Tunnel width ($z$): electric field apply and

- Lower $\Delta E$ improve ON current
- Interface need more abruptness
Applying Band Discontinuity Concept in a FET

Source- Channel $p^+-n$ junction

Tunnel height is determined by material, Tunnel width is determined by band discontinuity

Band offset effect is investigated by same band gap material.
Band to band Tunneling FET – Calculation model

- Nonlocal band to band tunneling:

\[
T(E) = \exp \left( -2 \int_{x_{\text{start}}}^{x_{\text{end}}} k(x) \, dx \right)
\]

\[
k(x) = \frac{k_e k_h}{\sqrt{k_e^2 + k_h^2}} \quad k_h(x) = \frac{1}{i\hbar} \sqrt{2m_{o} m_{h}(x)(E_v(x) - E)}
\]

\[
k_e(x) = \frac{1}{i\hbar} \sqrt{2m_{o} m_{e}(x)(E - E_E(x))}
\]

\[
J(E) = \frac{q}{\pi \hbar} \int J(E)[f(E + E_\tau) - f_r(E + E_\tau)] \rho(E_\tau) \, dE \, dE_\tau
\]

- Lombardi CVT Model: Matthiessen’s rule

\[
\mu T^{-1} = \mu_{AC}^{-1} + \mu_b^{-1} + \mu_{sr}^{-1}
\]

- \( \mu_{AC} \) scattering with acoustic phonons

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- \( \mu_b \) scattering with optical intervalley phonons


- Shockley-Read-Hall (SRH) Recombination

- SRH Concentration-Dependent Lifetime Model

- Trap Assisted Auger Recombination

- Semiconductor bandgap narrowing

- Includes the effects of Fermi statistic into the calculation of the intrinsic concentration in expressions for SRH recombination.
Effect of Band Discontinuity

Increased band discontinuity can improve S-factor and ON current.

Tunnel width dependence on band discontinuity is a key factor for improving TFET performance.
Band Discontinuity using Silicide/Si

Improving ON current by using III-V hetero-junction is possible

Choosing appropriate $E_g$, $\varepsilon$ is necessary for improving ON current in TFET

Silicide semiconductor has small band gap ($E_g$) and large $\Delta E_v$ is used for source region.
Silicide/Si Tunnel FET Design

- **Source concentration**: $1 \times 10^{20} \text{cm}^{-3}$
- **Channel concentration**: $10^{15}\text{~}10^{18} \text{cm}^{-3}$
- **Oxide thickness**: $t_{\text{ox}}$ 0.3 nm
- **SOI thickness**: 40 nm
- **Gate length**: $L_g$ 20,100 nm

As semiconductor with similar characteristics to Mg$_2$Si ($E_G$, dielectric constant, electron density), was used in a FSOI structure to evaluate TFET electrical properties.
Silicide/Si Tunnel FET Design

Lowest S-factor and highest ON current can be achieved by Mg$_2$Si/Si Tunnel FET
A sharp decrease in tunneling width is observed for MgSi2/Si junction. S-factor and ON current are simultaneously improved.
S-factor is degraded for short channel devices due to electric field penetration.
Tunneling width change due to gate voltage is smaller for channels with high doping concentration.
Drain electric field penetration to channel is reduced for lower drain voltages. 
Same drain current can be achieved regardless of channel length.
Silicide/semiconductor Tunnel-FET Design

Degradation of On current and S-factor has limited in 1 degrade and 10%

It can optimize the apply voltage at 0.3 V

\[ V_g = V_{th} + 0.5V \]

\[ L_g = 100, 20\text{nm} \]
Delay time Compare to TFET and Conv.

TFET’s delay time is lower than conventional below $V_g=0.8V$, due to TFET has high ON/OFF ratio.
The simulation belong in the Two popular published experiment device
Germanium Silicon

IV-semiconductor and III-V compound semiconductor has different wave vector and band gap.

Next step: The tunnel injection needs to consider phonon scattering and various energy potentials.
Mg$_2$Si formation and oxidation

MBE, sputtering deposition has been reported, MgO has formed in Mg$_2$Si/Si interface.

Xiao Qingquan et al., J. Semicond. 2011, 32(8)

Mg$_2$Si 380nm, Annealing with Ar gas, 5h

MgO had formed in MgSi substrate above 400$^\circ$C
Mg$_2$Si p-type formation

M. Akasaka, et al., JOURNAL OF APPLIED PHYSICS 104, 013703 2008

P-type can be achieved by doping Na, Ag during Mg$_2$Si deposition

<table>
<thead>
<tr>
<th>Samples</th>
<th>Carrier type</th>
<th>Hall carrier concentration (cm$^{-3}$)</th>
<th>Hall mobility (cm$^2$ V$^{-1}$ s$^{-1}$)</th>
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<td>Bi-I</td>
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<td>Bi-II</td>
<td>$n$</td>
<td>$1.38 \times 10^{20}$</td>
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<td>Ag-I</td>
<td>$p$</td>
<td>$7.42 \times 10^{18}$</td>
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</table>
Chapter 6, 7 • Comparison to Literature

Si, Ge
Steep Subthreshold response, poor ON current

III-V
Poor S factor, High ON current

ON current is increased due to low electron effective mass in III-V material

It is necessary to achieve high ON current with steep S-factor, for Tunnel FET in Si (large effective density of states)

☑ First demonstration of Si-based Hetero-junction Tunnel FET feasibility
Chapter 6, 7 Conclusions

Tunneling FET with band discontinuity and lower bandgap

Large Band discontinuity lead shorter tunneling width, that improve high ON current, lower S-factor

Semiconducting silicide has lower bandgap, Mg$_2$Si/Si achieved higher ON current and lower S-factor than Ge/Si, Due to larger band offsets.

At short channel, TFET has degradation of S-factor due to drain electric field penetration. $\rightarrow$ optimization at $V_d=0.3$ V, $L_g=20$ nm
Thermionic tunneling

\[ V B_{s, \text{max}} < E_{F,n} \cdot \frac{V B_{s, \text{max}} - C B_{ch, \text{min}}}{q} \]
\[ \text{SS} \approx \ln(10) \cdot \left( E_{F,s} - C B_{ch, \text{min}} \right) \]
\[ V B_{s, \text{max}} > E_{Fp,s} + 3k_B T \]
\[ \text{SS} \propto \ln(10) \cdot \left( \frac{E_{F,s} - C B_{ch, \text{min}}}{q} \right) \]

\[ \text{SS} \approx \frac{k_B T}{q} \cdot \ln(10) = 60 \text{ mV/dec at } T = 300 \text{ K.} \]

Proposed a model for achieving low power consumption Tunnel FET.
### Summary

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<th>$L_{\text{gate}}$</th>
<th>$\text{Ion ((\mu\text{V}/\mu\text{m}))}$</th>
<th>$\text{Ion/loff}$</th>
<th>$\text{SS}$</th>
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<td><strong>pn conventional</strong></td>
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<td>$5.0 \times 10^6$</td>
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</table>
Target and benchmarking

ON current and minimum S-factor are Key factor of benchmarking

Trendy line is lower S-factor has smaller ON current

Ohta et al., AIST Japan GNC symposium 2013
The performance is considered to be comparable of highly-scaled III-V hetero-junction TFETs
Paper publish list of this thesis

Journals

Yan. Wu et al.,
“Influence of Structural Parameters on Electrical Characteristics of Schottky Tunneling Field-Effect Transistor and Its Scalability”
Japanese Journal of Applied Physics, Volume 52, Number 4, 04CC28

Yan. Wu et al.,
“A novel hetero-junction Tunnel-FET using Semiconducting silicide-Silicon contact and its scalability”
Submitted to Microelectronics reliability
International Conference (peer review)

“Influence of Structural Parameters on Electrical Characteristics of Schottky Tunneling Field-Effect Transistor and Its Scalability”
International Conference on Solid State Devices and Materials (SSDM 2012)

“Influence of Band Discontinuities at Source-Channel Contact in Tunnel FET Performance”
2013 International Workshop on DIELECTRIC THIN FILMS FOR FUTURE ELECTRON DEVICES (IWDTF2013)
Other conference

“Observation of tunneling FET operation in MOSFET with NiSi/Si Schottky source/channel interface”
218th Electrochemical Society (ECS) Meeting

“Observation of NiSi/Si Schottky source/channel interface electrical characteristic”
Taiwan-Japan Workshop "Nano Devices"

“An analytical model of a tunnel FET with Schottky junction”
G-COE PICE International Symposium and IEEE EDS Minicolloquium on Advanced Hybrid Nano Devices (IS-AHND)

“The tunnel FET with schottky contact simulation”
Tsukuba Nanotechnology Symposium 2011

“Size dependent resistivity change of Ni-silicides in nano-region”
Workshop and IEEE EDS Mini-colloquium on Nanometer CMOS Technology

“A Study on Fabrication and Analytic Modeling of novel Schottky contact tunneling Transistors”
IEEE EDS MQ WIMNACT 32

“Influence of Structural Parameters on Schottky Tunneling Field-Effect Transistor”
Tsukuba Nanotechnology Symposium 2012

“Electrical Analyses of Nickel Silicide Formed on Si Nanowires with 10-nm-width”
International Symposium on Next-Generation Electronics (ISNE 2013)

“A study of Band offset in Source-Channel Contact improve Tunnel FET Performance”
Tsukuba Nanotechnology Symposium 2013
Thank you very much