

# Silicon Nanowire Solar Cells: Surface Passivation and Interface Analysis

Tomoya Shoji<sup>1</sup>, K. Kakushima<sup>2</sup>, Y. Kataoka<sup>2</sup>, A. Nishiyama<sup>2</sup>, N. Sugii<sup>2</sup>,

H. Wakabayashi<sup>2</sup>, K. Tsutsui<sup>2</sup>, K. Natori<sup>1</sup>, H. Iwai<sup>1</sup>

<sup>1</sup> Tokyo Tech. FRC, <sup>2</sup> Tokyo Tech. IGSSE

e-mail: shoji.t.ab@m.titech.ac.jp

## Introduction

Silicon nanowire (SiNW) solar cells provide potential advantages over planar wafer-based or thin-film cells such as high light absorption and enlarged forbidden energy gap [1][2]. However, due to a large surface-to-volume ratio, nanowires typically suffer from a high surface recombination rate. This work focuses on reducing surface states and developing passivation technique for SiNWs.

## Experimental Procedures

Charge pumping (CP) method is adopted to horizontally synthesized SiNW with varying nanowire size in order to measure interface state density  $D_{it}$ . We prepared p-i-n SiNW diode to measure the recombination current along the nanowires which is schematically illustrated in **Fig. 1**.

## Results and Discussion

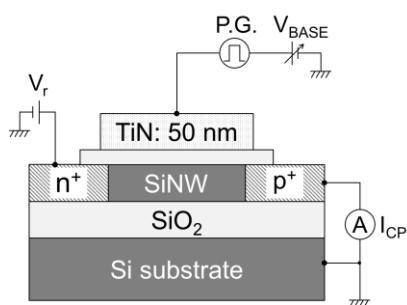
Measured  $D_{it}$  for various nanowire sizes are shown in **Fig. 2**.  $D_{it}$  increases with narrower width, meaning that the effect of localized high  $D_{it}$  is becoming more apparent. Assuming discrete  $D_{it}$  for each surface, top, side, and corner surface, localized  $D_{it}$  are extracted as shown in **Fig. 3**.

## Conclusions

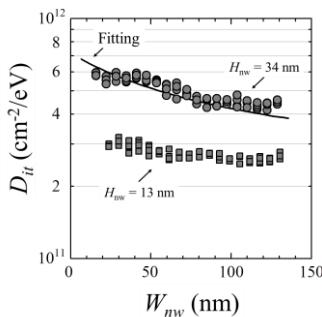
CP measurement is performed to p-i-n SiNW diode.  $D_{it}$  at the corner is one order higher than other surfaces and that effect is more apparent in narrower width. This result implies that adopting rectangular cross-sectional shape provide advantage for reducing surface recombination, and precise surface passivation technique is indispensable for achieving high efficiency.

## Acknowledgement

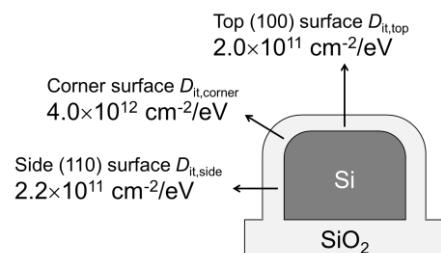
This work was supported by MEXT in Japan, FUTURE-PV Innovation project.



**Fig. 1** Schematic illustration of device structure.



**Fig. 2**  $D_{it}$  for various nanowire sizes.



**Fig. 3**  $D_{it}$  extraction for top, side, and corner surface

## References

- [1] E. Garnett and P. Yang, *Nano Letters* **10**, 1082-1087(2010)
- [2] D. D. D. Ma, C. S. Lee, F. C. K. Au, S. Y. Tong and S. T. Lee, *Science* **299**, 1874-1877(2003)