Future of Nano CMOS Technology

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Although silicon-based CMOS devices have dominated the integrated circuit applications over the past few decades, it is expected that the development of CMOS would reach MOSTET downsizing limits after the next decade. However, there are no promising candidates which can replace CMOS with better performance with high-density integration for the moment. Thus, we have to stick to the CMOS devices until its end. In order to pursue the downsizing of CMOS for another decade, the development of new technologies is becoming extremely important. Not all the companies can necessarily develop the most advanced technology timely and the competition between the leading semiconductor manufacturing companies becomes very severe for their survive. The current status of the frontend of the technology is as follows: Because of the difficulty in the lithography and also in the Ion/Ioff ratio control, the rate of the shrinkage for the line pitch and gate length becomes significantly less aggressive so that we will face the downsizing limit much later than expected before. New device structures (FinFET, Tri-gate, and Si-nanowire MOSFETs) are replacing conventional planar MOSFETs. Continuous innovation of High-k/metal gate technologies has enabled EOT scaling down to 0.9 – 0.7 nm in production, however, new materials are necessary for further EOT scaling. Recent advances in new channel material such as III-V/Ge shows promising device performances, however, it is still behind of the state of the art Si-CMOS technologies. comparable to state of the art Si-based MOSFETs. Device demonstration on emerging technologies (such as Tunnel FET, Junctionless FET, Carbon-based FET..) is increasing. But we cannot draw a successful story to replace the Si-CMOS and much longer time is needed for implementation of these technologies in future generation devices.