Atomically flat interface of La-silicate/Si with W2C gate electrodes

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Introduction

To achieve an EOT 0.5 nm, high-k gate dielectrics should be directly in contact with Si substrate.

- La-silicate is one of the potential candidates for next generation gate electrodes.

Advantages of La-silicate:
- High dielectric constant (ε=23.4)
- Wide band-gap (Eg=5.6 eV)
- Amorphous structure
- Direct contact with Si by forming La-silicate

Concerns for EOT scaling:
- Interface state density (Dit) increase.
- Stress applied below high-k layer.
- Threshold voltage variation due to work function variation.

Selection of metal gate electrode:
- Less orientation dependent work function.
- Small grain size less than 4 nm.
- Thermal stability against agglomeration.

We confirmed formation of oriented growth of hexagonal W2C layer with columnar shaped nano-sized grains.

Purpose of this study:
Investigate the interface property of La-silicate MOS capacitor with W2C gate electrodes.

Result and discussion

- No difference in interface silicate reaction rate between the gate electrode materials.
- Little change in the interface of metal gate electrodes to interface charges.
- Reduction of Interface state density (Dit<3 X 10^{11} cm^{-2}eV^{-1})

TiN/W/La-silicate/n-Si
TiN/W2C/La-silicate/n-Si

- Atomically flat interface metal/high-k and high-k/Si interfaces by W2C gate electrodes.
- No apparent stress with W2C gate electrodes.

- Spatial frequency corresponding to period of 20 nm, comparable to the grain size of W gate electrode is suppressed with nano-sized grain W2C gate electrode.

- Elimination of inhomogeneous stress with nano-sized W2C gate electrodes.

Conclusions

- Atomically flat interface of metal/high-k and high-k/Si was achieved with nano-sized and columnar shaped W2C gate electrodes due to smaller mechanical strain.
- Interface state density was suppressed with W2C gate electrodes.

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