Influence of Band Discontinuities at Source-Channel contact in Tunnel FET Performance

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Introduction

Upon further device size scaling, transistors with steep subthreshold slope have been focused as low standby power devices for next generation [1]. Among variety of steep subthreshold devices, including feedback FET [2], impact-ionization FET [3] and nano-electro mechanical FET [4], tunnel FETs (TFET) have been considered to have high potentials to achieve a large I_{ON}-I_{OFF} ratio over a small gate voltage swing, owing to the elimination of high-energy tail presented in the Fermi-Dirac distribution of the valence band electrons in the source region [5]. As an operation TFET is based on band to band tunneling from valence band of the source region ($E_{V,source}$) to conduction band of the channel ($E_{C,channel}$), the tunneling probability can be determined by a potential barrier with triangular shape as shown in Fig. 1 [6]; a tunneling barrier of ($E_{C,channel} - E_{V,source}$) and tunneling distance which is determined by gate bias and channel concentration(N_d). Therefore, band discontinuities at source and channel interface are the key to improve the performance of TFET. In this study, we investigate the influence of valence band discontinuity (ΔE_V) at source and channel interface on device performance of TFET by numerical simulations.

Simulated model

SILVACO TCAT tool ATLAS with non-local tunneling model was used for the simulation. An *n*-type SOI layer (E_g=1.12eV, N_d=1×10^{17} cm^{-3}) with a thickness of 10 nm and a channel length of 100 nm were used. Gate oxide with an equivalent oxide thickness of 0.3 nm was adopted. ΔE_V between the p^+-source and channel was varied from 0 (homojunction) to 0.6 eV. The carrier distribution of source material property sited Si carrier. The band diagrams are shown in Fig.1.

Influence of valence band discontinuity

Figure 2 shows I_d-V_g and subthreshold swing (SS) characteristics of TFET with different values of ΔE_V. One can observe higher I_{ON} as well as smaller SS with larger ΔE_V. The minimum SS of 14 mV/dec. was obtained with ΔE_V of 0.6 eV. Transconductance (g_m) also increased with larger ΔE_V as shown in Fig. 2(c). Threshold voltage, V_{th}, defined as Vg at I_d=10^{-8}A/μm, decreased gradually with larger ΔE_V, due to reduced tunneling distance, as shown in Fig. 3(a). Large increase in I_{ON}, defined as V_g=V_{th}+0.7V, is due to lower energy barrier, as shown in Fig. 3(b). On the other hand, I_{OFF}, defined as V_g=V_{th}-0.3V, showed no dependency on ΔE_V, as shown in Fig. 3(c), which lead to the large I_{ON}/I_{OFF} ratio.

Considering potential semiconductors for source from the viewpoint of ΔE_V, as summarized in Fig. 4, Mg_2Si (E_g=0.75 eV) source can be a candidate for *n*-TFETs with Si channel. In the same way, β-$FeSi_2$ (E_g=0.85eV) can be a candidate for *p*-TFETs.

Conclusions

We have investigated the influence of valence band discontinuity at source and channel interface on device performance of TFET by numerical simulations. A steep slope with high I_{ON} can be both achieved with larger discontinuity, owing to reduced distance and lower energy barrier for tunneling.

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References

[1] A Tura, et al., IEEE Trans. Electron Dev., Vol. 57, pp. 1362 (2010).
[2] A. Paddilla, et al., IEDM Tech. Dig., pp. 1 (2008).
[3] K. Gopalakrishnan, et al., IEEE Trans. Electron Devices, Vol. 52, pp. 69 (2005).
[4] H. Kam, et al., IEDM Tech. Dig., pp. 463 (2005).
[5] S. Mookerjea, et al., IEDM Tech. Dig., pp. 949 (2009).
[6] D. K. Mohata, et al., IEDM Tech. Dig., p. 781 (2011).

[7] Semiconductor - Basic Data 2nd Edition , O.Madelung, Springer

[8] M. Baleva et al., ECSTransaction 8 ,1 (2007) p.151

[9] T. Suemasu, et al., JJAP 45 (2006) L519

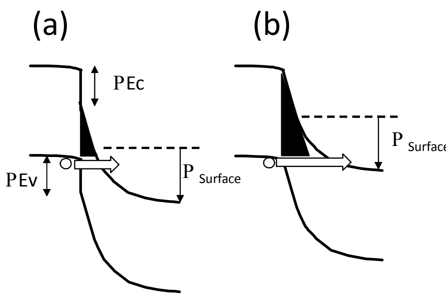

Fig.1 Band diagrams of source-channel junction (a) with band discontinuities and (b) without band discontinuity.

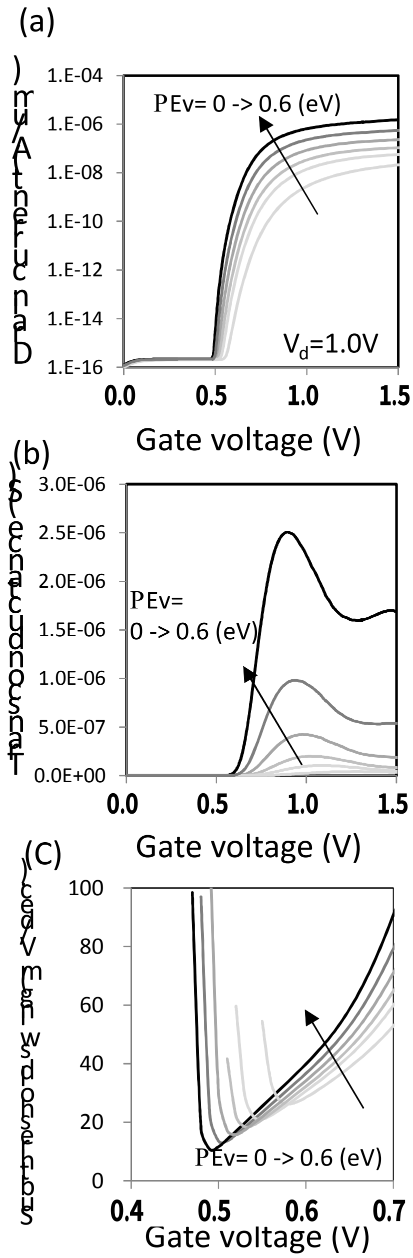

Fig.2 (a) Drain current, (b) trans conductance, and (c) subthreshold swing as a function of gate voltage for each valence band offset in TFET

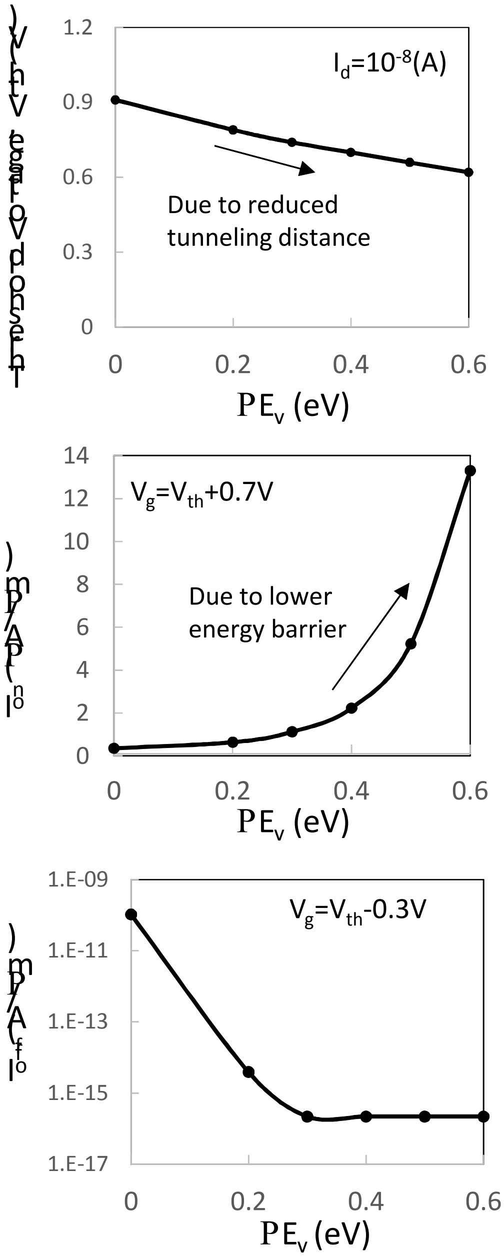

Fig. 3 (a) Threshold voltage, (b) Ion, and (c) Ioff as a function of △Ev.

Fig. 4 Band alignments of various semiconductors and silicides.[7-9]