Scalable La-silicate Gate Dielectric on InGaAs Substrate with High Thermal Stability and Low Interface State Density

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• Introduction
• Fabrication Process
• Electrical characteristics of La-silicate as gate dielectric
• Conclusions
• **Introduction**

• Fabrication Process

• Electrical characteristics of La-silicate as gate dielectric

• Conclusions
The Scaling trend

<table>
<thead>
<tr>
<th>Bulk Planar</th>
<th>3D</th>
<th>III-V, Ge, 2D(MoS$_2$, …)</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm</td>
<td>32nm</td>
<td>22nm</td>
</tr>
<tr>
<td>45nm</td>
<td></td>
<td>15nm, 11nm, 8nm, 5nm, 3nm</td>
</tr>
</tbody>
</table>

$L_g$ 35nm  
$L_g$ 30nm

- Increase in stand-by power at short channel length is becoming a limiting performance factor.
- There is a need to reduce supply voltage with less performance sacrifice.

L. Chang, IEDM Short course, (2012).
There is a trade-off relation between band-gap (BTBT), dielectric constant (SCE), and carrier mobility ($I_{d\text{SAT}}$) of semiconductors.

- In$_{0.53}$Ga$_{0.47}$As offers great trade-off conditions.

- Buried channel is also an option.
InGaAs has a small electron effective mass thus a small conduction band DOS.

Total Gate capacitance ($C_g$) is significantly degraded by the influence of $C_{DOS}$ (low DOS)

It is imperative to increase $C_{ox}$ (Scaling of gate stack) to improve gate controllability
Summary of critical InGaAs gate stack issues

Chemical Point of View

Preserving the stoichiometry of three elements (In, Ga, As) at the interface

Rearrangement of elements at interface, cause dangling bond formation (high $D_{it}$)

Formation of volatile As-O family

As-antisites, dimers can be formed, leading to low mobility in high surface carrier concentration

Electrical Point of View

High density of interface traps (would lead to poor SS and $I_{OFF}$ degradation)

Capacitance Equivalent Thickness (CET) scalability
### High-k selection for InGaAs

<table>
<thead>
<tr>
<th>High-k</th>
<th>k-value scalability</th>
<th>$D_{it}$ (cm$^{-2}$/eV)</th>
<th>High temperature endurance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al$_2$O$_3^*$</td>
<td>$\sim 9 \ (\Delta)$</td>
<td>$\sim 9 \times 10^{11}$</td>
<td>× (\sim 400^\circ C)</td>
</tr>
<tr>
<td>HfO$_2^{**}$</td>
<td>$\sim 16 \ (\bigcirc)$</td>
<td>$&gt; 10^{12}$</td>
<td>$\bigtriangleup$</td>
</tr>
<tr>
<td>HfO$_2$/Al$_2$O$_3$ stack***</td>
<td>$\sim 16/9 \ (\bigcirc)$</td>
<td>$&gt; 10^{12}$</td>
<td>$\bigtriangleup$</td>
</tr>
</tbody>
</table>


Highly scalable high-k with low $D_{it}$ and high temperature tolerance is still missing.
La-silicate has been reported to have excellent dielectric properties on Si.

**Material Properties**
- La-silicate band gap ($E_g$) = 6.2 eV (composition dependent)
- Amorphous structure
- Electric break down field: $\sim 13$ MV/cm

**Controllable composition and excellent dielectric qualities of La-silicate can be applied to InGaAs substrate**
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In$_{0.53}$Ga$_{0.47}$As Substrate

- Oxide removal by HF (20%)
- Surface passivation by (NH$_4$)$_2$S (6%) for 20min in R.T
- Si deposition by sputtering
  - Nitridation at 200 ºC
  - La$_2$O$_3$ deposition by E-beam
- Gate metal (TiN/W) deposition by RF sputtering
- Gate patterning
- Post Metallization Anneal (PMA) in FG (N$_2$:H$_2$ 97%:3%) for 5min
- Backside Al contact

Measurement
• Introduction
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• **Electrical characteristics of La-silicate as gate dielectric**
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La-silicate composition (La-rich or Si-rich) and thickness can be manipulated by changing deposited Si thickness.

Si thickness: 1 nm was the optimum value to achieve small $D_{it}$ and high temperature annealing tolerance.
Impact of nitrogen incorporation in LaSiO-IL

Nitridation of Si layer before La$_2$O$_3$ deposition, improves scalability and thermal stability

$\approx 24$
Similar CET scaling trend with increasing PMA temperature observed for various La$_2$O$_3$ thicknesses.

Higher annealing temperature reduces CET (change in IL structure).
Annealing effect on $D_{it}$ of La-silicate IL

$\Phi_s = -0.1$ eV

La$_2$O$_3$: 5 nm

La$_2$O$_3$: 10 nm

$D_{it}$ near $10^{12}$ cm$^{-2}$ eV$^{-1}$ is achievable

Less degradation with scaling

mid-gap $D_{it}$ can be reduced with high temperature annealing

Deposited Si
Thickness: 1 nm

620 °C

370 °C

100 kHz

Gate Voltage (V)

PMA Temperature (°C)
$D_{it}$ benchmark for high-k/InGaAs interfaces

$D_{it}$ on the order of lower-$10^{12}\text{cm}^{-2}/\text{eV}$ can be achieved even with $570^\circ\text{C}$

$\Phi_s = -0.1 \text{ eV}$

This work (@ 570$^\circ$C)

At smaller CET and at higher annealing temperature gate leakage current is more effectively suppressed for silicate structure than reported HfO₂-based structures.

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• Scaling InGaAs-based gate stacks would benefit device performance in future technology nodes. (<10 nm)

• High temperature endurance with CET<1nm and $D_{it} \sim$ lower $10^{12}$ (cm$^{-2}$eV$^{-1}$) can be obtained with Si(+N) insertion to form LaSiON up to 570 °C, which is enough for S/D activation
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