A Study on Electrical Properties of Rare Earth Oxide High-\(k\) Interfaces with InGaAs MOS Devices

PhD candidate, 公聴発表会

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2013年6月17日
Outline

- Introduction
- Main Accomplishments of this Thesis
- Thesis Structure
- Selected Contents
- Conclusions
- List of Publications
Impact of MOSFETs Scaling on Society

Moore’s law to this date has continued to improve device performance

The demand for Multi-performance, smaller, energy efficient electronic devices will continue to increase.

I. Post, VLSI Short course, (2013).
Scaling Trends

Bulk Planar

<table>
<thead>
<tr>
<th>65nm</th>
<th>45nm</th>
<th>32nm</th>
<th>22nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>NiSi</td>
<td>PolySi</td>
<td>SiGe</td>
<td>SiGe</td>
</tr>
<tr>
<td>SiGe</td>
<td>SiGe</td>
<td>SiGe</td>
<td>SiGe</td>
</tr>
<tr>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
<td>SiO₂</td>
</tr>
<tr>
<td>65nm</td>
<td>45nm</td>
<td>32nm</td>
<td>22nm</td>
</tr>
<tr>
<td>Lg 35nm</td>
<td>Lg 30nm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3D

III-V, Ge, 2D(MoS₂,…)

15nm, 11nm, 8nm, 5nm, 3nm

Lower supply Voltage, and Higher performance

- Increase in stand-by power at short channel length is becoming a limiting performance factor.
- There is a need to reduce supply voltage with less performance sacrifice.

L. Chang, IEDM Short course, (2012).

\[ P_{active} \propto fV_{dd}^2 \]
Enhanced Carrier Transport Effect on MOSFET Performance

Drive current for scaled MOSFET

\[
I_{D,sat} = WC_{ox} v_s(0)(V_g - V_{th})
\]

\[
\frac{1}{v_s(0)} = \frac{1}{v_{inj}} + \frac{1}{\mu_{eff} E(0^+)}
\]

where \( v_{inj} = \sqrt{\frac{2kT}{\pi m_t^*}} \), \( \mu_{eff} = \frac{L_g}{qR_{ch}N_s} (= \mu_{diffusion}) \)

Under \( L_g \ll \lambda \) (limited time to be accelerated)

\[
\frac{1}{\mu_{eff}} = \frac{1}{\mu_{ballistic}} + \frac{1}{\mu_{diffusion}}, \text{ where } \mu_{ballistic} = \frac{2qL_g}{m_t^* \pi v_{th}} \text{ and } v_{th} = \left( \frac{8kT}{m_t^* \pi} \right)^{1/2}
\]

- At short channel length (<10 nm) ballistic transport is the dominant and limiting factor for IDSAT
- Smaller effective mass \( (m_t^*) \) increases ballistic mobility

### Selection of high mobility material

<table>
<thead>
<tr>
<th>Material</th>
<th>Electron Mob. (cm²/Vs)</th>
<th>Electron Effective Mass (/m₀)</th>
<th>Hole Mob. (cm²/Vs)</th>
<th>Hole Effective Mass (/m₀)</th>
<th>Band Gap (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1600</td>
<td>ml:0.19, mₗ:0.916</td>
<td>430</td>
<td>mₗH:0.49, mₗL:0.16</td>
<td>1.12</td>
</tr>
<tr>
<td>Ge</td>
<td>3900</td>
<td>mt:0.082, mt:1.467</td>
<td>1900</td>
<td>mₗH:0.082, mₗL:0.044</td>
<td>0.66</td>
</tr>
<tr>
<td>InP</td>
<td>5400</td>
<td></td>
<td>200</td>
<td>mₗH:0.45, mₗL:0.12</td>
<td>1.34</td>
</tr>
<tr>
<td>GaAs</td>
<td>9200</td>
<td></td>
<td>400</td>
<td>mₗH:0.45, mₗL:0.082</td>
<td>1.42</td>
</tr>
<tr>
<td>In₀.53Ga₀.47As</td>
<td>10000</td>
<td></td>
<td>250</td>
<td>mₗH:0.45, mₗL:0.052</td>
<td>0.74</td>
</tr>
<tr>
<td>InAs</td>
<td>40000</td>
<td></td>
<td>500</td>
<td>mₗH:0.57, mₗL:0.35</td>
<td>0.36</td>
</tr>
</tbody>
</table>

There is a trade-off relation between band-gap (BTBT), dielectric constant (SCE), and carrier mobility (IDSAT) of semiconductors.

- In₀.53Ga₀.47As offers great trade-off conditions.
The improvement in drive current at short $L_{ch}$ is offset by reduction in overdrive (high $V_t$).

High mobility of InGaAs enables lower voltage and higher drive current.
Concerns in InGaAs channel

- Abrupt junctions (heavily doped source merging to channel) of DGFET, degrade InGaAs performance (population of slow satellite valleys)
- Smoother junctions (shallow lightly doped extension) allow population of fast Γ valleys (trade off with series resistance)
- Even with large $v_{th}$ in InGaAs, lack of charge degrades the drivability with scaled MOSFET

$V_{DS} = V_{GS} - V_T = V_{DD}$

$V_{DD} = 1, 0.8, 0.6 V$

**Electronic structures in InGaAs**

\[ m_x = 0.74 \]
\[ m_\Gamma = 0.043 \]
\[ m_L = 0.42 \]

\[ \frac{1}{C_g} = \frac{1}{C_{ox}} + \frac{1}{C_{DOS}} \]

For:
\[ L_g = 45 \text{nm and } t_{ox} = 3.6 \text{ nm at } V_{GS} = 0.5 \text{V and } V_{DS} = 0 \]

Simulation results:
\[ C_G = 1.41 \mu \text{F/cm}^2, \ C_{ox} = 1.12 \mu \text{F/cm}^2 \text{ And } C_{DOS} = 3.05 \mu \text{F/cm}^2 \]

- InGaAs has a small electron effective mass thus a small conduction band DOS.
- Total Gate capacitance \((C_g)\) is significantly degraded by the influence of \(C_{DOS}\) (low DOS)
- It is imperative to increase \(C_{ox}\) (Scaling of gate stack) to improve gate controllability

Nonparabolic
Critical Issues of III-V gate stacks

Chemical Point of View

- Preserving the stoichiometry of three elements (In, Ga, As) at the interface
- Rearrangement of elements at interface, cause dangling bond formation (high D_{it})
- Formation of volatile As-O family
- As-antisites can be formed, leading to Low mobility in high surface carrier concentration

Electrical Point of View

- High density of interface traps (would lead to poor SS and I_{OFF} degradation)
- Capacitance Equivalent Thickness (CET) scalability
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• **Main Accomplishments of this Thesis**
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Main accomplishments in this thesis

- Proposing a high-temperature high-k deposition method to compensate substrate bulk trap formation at HfO$_2$/InGaAs interface  

- Proposing improvement of high-k/InGaAs interface through the formation of reactive interfacial layer by using La$_2$O$_3$ as gate dielectric  

- Proposing a surface passivation method based on mono-layer Si formation, to improve electrical properties of La$_2$O$_3$/InGaAs interface  

- Achieving significant improvement in La$_2$O$_3$/InGaAs electrical properties by controlling interfacial layer thickness and composition  

- Proposing the application of La-silicate as gate material for InGaAs with gate scalability of down to 0.7 nm and temperature tolerance of up to 600 °C  

- Demonstrating InGaAs-MOSFET operation with metal Source.Drain and ALD-La$_2$O$_3$ as gate dielectric
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Chapter 2 Review on III-V issues

Chapter 3 Fabrication and characterization

Chapter 4 Bulk defects at HfO$_2$/InGaAs interface

Chapter 5 Gate Stack Engineering for InGaAs-based MOS capacitors with La$_2$O$_3$ gate dielectric

✔ Chapter 6 Technologies for 3D structure

✔ Chapter 7 InGaAs-based MOSFETs with La$_2$O$_3$ gate dielectric

✔ Chapter 8 Conclusions

InGaAs-based devices
Thesis Structure

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Chapter 3  Fabrication and characterization
Chapter 4  Bulk defects at HfO₂/InGaAs interface
Chapter 5  Gate Stack Engineering for InGaAs-based MOS capacitors with La₂O₃ gate dielectric
Chapter 6  InGaAs-based MOSFETs with La₂O₃ gate dielectric
Chapter 7  Technologies for 3D structure InGaAs-based devices
Chapter 8  Conclusions
Common high-k/InGaAs interface characteristics

H. Zhao et. al, APL. 95, 253501(2009)
E. O’Connor et. al, APL. 92, 022902(2008)

Pinned Fermi level

Interfacial layer formation at Interface during gate first process (PMA > 500 °C)

- Huge frequency dispersion
- Al₂O₃ interface necessary

- Huge frequency dispersion
- High leakage current
- Huge Hysteresis
The formation of unstable oxides at high-k/InGaAs interface must be controlled.


Ref. Han Zhao et. al, Appl. Phys. Lett. 95, 253501(2009)

Oxide specimens lead to inferior C-V characteristics

As dangling bonds, Ga-Ga antibonding
Ga dangling bond, As-As antibonding
Ga$_2$O$_3$, As$_2$O$_3$, As$_3$O$_5$ form Acceptor-like traps which increase interface state density

$D_{it}$

$E_v$

$E_c$

Intensity (Normalized)

Al$_2$O$_3$/InGaAs
As $2p_{3/2}$

Ga $2p_{3/2}$

As$_2$O$_3$
As-As
As-In
Ga$_2$O$_3$
Ga(AsO$_3$)$_3$
Ga-As
Ga-O/S

TMA treated sample
TMA treated +PDA in $H_2$ sample

B.E.(eV)

1120
1124
116

1320
1324
1328

1116

The formation of unstable oxides at high-k/InGaAs interface must be controlled.
Defects formation at InGaAs bulk

- Defects within the bulk of InGaAs at ZrO$_2$/InGaAs Interface have been reported (Their effect not studied)
- Bulk defects at SD cause poor dopant activation and also cause $I_{\text{OFF}}$ increase

High temperature annealing is reported to reconstruct In-rich surface through the compensation of In atoms from substrate bulk

Unary phase separating oxides such as HfO$_2$ and ZrO$_2$, disturb the In, Ga and As elemental balance upon annealing
## Summary of Applied Gate Dielectrics on InGaAs

<table>
<thead>
<tr>
<th></th>
<th>Interface state Density ($D_{it} &lt; 10^{12}$ cm$^{-2}$eV$^{-1}$)</th>
<th>Scalability (EOT&lt; 1 nm)</th>
<th>Thermal Stability (&gt; 500 °C)</th>
<th>Currently used In 3D structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>HfO$_2$</td>
<td>×</td>
<td>●</td>
<td>△</td>
<td>×</td>
</tr>
<tr>
<td>HfAlO$_x$</td>
<td>×</td>
<td>●</td>
<td>△</td>
<td>×</td>
</tr>
<tr>
<td>LaAlO$_x$</td>
<td>×</td>
<td>●</td>
<td>△</td>
<td>×</td>
</tr>
<tr>
<td>TaSiO$_x$</td>
<td>×</td>
<td>●</td>
<td>△</td>
<td>×</td>
</tr>
<tr>
<td>SrTaO$_x$</td>
<td>×</td>
<td>●</td>
<td>△</td>
<td>×</td>
</tr>
<tr>
<td>Al$_2$O$_3$</td>
<td>●</td>
<td>×</td>
<td>×</td>
<td>●</td>
</tr>
<tr>
<td>ZrO$_2$</td>
<td>×</td>
<td>●</td>
<td>×</td>
<td>●</td>
</tr>
<tr>
<td>Al$_2$O$_3$+</td>
<td>×</td>
<td>●</td>
<td>×</td>
<td>●</td>
</tr>
<tr>
<td>HfO$_2$</td>
<td>×</td>
<td>●</td>
<td>×</td>
<td>●</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>?</td>
<td>?</td>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>

- **HfO$_2$** is the currently used material in 3D structures.
- **La$_2$O$_3$** indicates ongoing research but not yet in production.
La$_2$O$_3$ for gate dielectric

There is still a need to find a suitable dielectric for InGaAs to satisfy all gate stack requirements.

Promote the formation of IL with separate phases:
- ZrO$_2$
- HfO$_2$
- BeO

In InGaAs case, this IL is consistent of InO$_x$, GaO$_x$ and AsO$_x$. They all have low K-value and/or are unstable.

Can react with oxide species without phase separation:
- Y$_2$O$_3$
- Gd$_2$O$_3$
- Al$_2$O$_3$
- La$_2$O$_3$

First GaAs MOSFET operation was reported (*Need all in situ process)*

Presently the focus of most gate stack processes (*low-k value, not suitable for scaling)*

Needs more investigation
Purpose of This Study

Investigating La$_2$O$_3$ as a viable gate dielectric for InGaAs

Improving La$_2$O$_3$/InGaAs interface quality
By controlling interface reaction

Reducing CET of La$_2$O$_3$/InGaAs gate stack while preserving the interface integrity

Improving InGaAs-MOSFET operation with La$_2$O$_3$ as gate dielectric
Device Fabrication

<table>
<thead>
<tr>
<th>Oxide removal by HF (20%)</th>
<th>W (50 nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>In$<em>{0.53}$Ga$</em>{0.47}$As Substrate</td>
<td>La$_2$O$_3$</td>
</tr>
<tr>
<td>Surface passivation by (NH$_4$)$_2$S (6%) for 20min</td>
<td>n-InGaAs</td>
</tr>
<tr>
<td>La$_2$O$_3$ deposition at R.T</td>
<td>TiN (45 nm)</td>
</tr>
<tr>
<td>Gate metal deposition</td>
<td>W (5 nm)</td>
</tr>
<tr>
<td>by RF sputtering</td>
<td>La$_2$O$_3$</td>
</tr>
<tr>
<td>W (50 nm) or TiN (45nm)/W (5 nm)</td>
<td>n-InGaAs</td>
</tr>
<tr>
<td>Gate patterning</td>
<td></td>
</tr>
<tr>
<td>Post Metallization Anneal (PMA) in</td>
<td></td>
</tr>
<tr>
<td>FG (N$_2$;H$_2$ 97%;3%) for 5min</td>
<td></td>
</tr>
<tr>
<td>Backside Al contact</td>
<td></td>
</tr>
<tr>
<td>Measurement</td>
<td></td>
</tr>
</tbody>
</table>

Oxygen supply provided through W gate to compensate La$_2$O$_3$ oxygen deficiency created by EB deposition
**HfO$_2$/InGaAs VS La$_2$O$_3$/InGaAs**

- **In-O-La, Ga-O-La bonds are created at La$_2$O$_3$/InGaAs interface**
- **Oxide species from the substrate are spread within**
  - The HfO$_2$ (no IL visible)
**Interface reaction proposal**

- EDX point diameter: ~1.0 nm

- In, Ga and As are detected close to La$_2$O$_3$/InGaAs interface

- La$_a$In$_b$Ga$_c$O$_{12}$ is reported to be a thermally stable, covalent structure (a=3.24, b=1.84, c=2.48)
IL Issues at La$_2$O$_3$/InGaAs

![Graph showing capacitance vs. gate voltage for W (50nm)/La$_2$O$_3$(10 nm)/InGaAs with CET: 2.3 nm.]

- Experimental depletion capacitance fails to reach ideal value (Fermi level pinning).
- Increasing PMA temperature, increases CET and gate leakage.
- Need to control the composition and thickness.
- Improve interface.
- Prevent leakage current increase during CET scaling.

- Scaling

- Experimental
- Ideal
The amount of La$_2$O$_3$ and InGaAs intermixing can be modulated through gate metal choice.
Gate metal Influence on Oxidation States

Gate metal choice greatly impacts interface state after PMA.

Oxidation states reduced by TiN gate.

- As $2p_{3/2}$
- Ga $2p_{3/2}$
- In $3d_{5/2}$

Oxide to substrate peak intensity ratio

Metal gate (13 nm) / La$_2$O$_3$ (10 nm) / InGaAs (TOA = 80$^\circ$) PMA 420 $^\circ$C (FG)
Gate metal Influence on interface thermal stability

Higher PMA temp improves CV, but leakage current increases (max 470 °C)

- Interface integrity is intact for PMA up to 620 °C
- Gate leakage lower than $10^{-2}$ A cm$^{-2}$

TiN (45 nm)/W (50 nm)

**Graphs:**
- Capacitance vs. Gate Voltage for different conditions and materials.

- **Step:** 
  - 370 °C (FG): Ideal behavor
  - 470 °C (FG): Higher PMA temp improves CV, but leakage current increases
  - 620 °C (FG): Interface integrity is intact for PMA up to 620 °C
  - No anneal: Lower gate leakage than $10^{-2}$ A cm$^{-2}$
Comparison between Interface State Density ($D_{it}$)

- $D_{it}$ lower than Al$_2$O$_3$ can be achieved by La$_2$O$_3$ IL control
- $D_{it}$ remain in the order of $10^{11}$ eV$^{-1}$cm$^{-2}$ at 620 °C
Gate metal selection has a great impact on La$_2$O$_3$/InGaAs interface state after PMA.

Replacing W with TiN/W improves the thermal stability, CV characteristics of La$_2$O$_3$/InGaAs by altering LaInGaO composition.

One of the smallest reported $D_{it}$ values ($\sim 6 \times 10^{11} \text{eV}^{-1} \text{cm}^{-2}$), was achieved by IL control.
Si IL has been reported to improve GaAs interface properties by inhibiting the formation of Ga-dangling bonds.

There is an EOT penalty as a result of Interfacial Si.

W. Wang et. al., ME. 88, 1061(2011)
La-silicate has been reported to have excellent dielectric properties on Si.

### Material Properties
- La-silicate band gap ($E_g$) = 6.2 eV (composition dependent)
- Amorphous structure
- Electric break down field: ~13 MV/cm

Controllable composition and excellent dielectric qualities of La-silicate can be applied to InGaAs substrate.
Fabrication Process

1. Acetone and ethanol cleaning + HF 20% treatment
2. (NH₄)₂S treatment
3. Si deposition (0.5 nm~ 2.0 nm) by RF sputtering
   - With Nitridation on Si surface by nitrogen radical beam @200°C
4. La₂O₃ e-beam deposition at R.T
5. Gate metal (W) deposition by sputtering in-situ
6. Gate metal (TiN) deposition by sputtering
7. Gate patterning by RIE
8. F.G anneal for 5 min
9. Backside Al contact
10. Electrical Characterization

Deposition Sequence:
- TiN (45 nm)
- W (5 nm)
- La₂O₃
- n-In₀.₅₃Ga₀.₄₇As
- InP

Epitaxial (from vendor)
Effect of Silicate Structure on CET

Nitridation of Si layer before La$_2$O$_3$ deposition improves scalability and thermal stability.

$k$-value $\approx 25$
La$_2$O$_3$ deposition thickness can be reduced without $CV$ degradation

Lower CET at higher PMA (Change in LaSiON composition)
At smaller CET and at higher annealing temperature, gate leakage current is more effectively suppressed for silicate structure than reported HfO$_2$/Al$_2$O$_3$ structure.
At smaller CET and at higher annealing temperature gate leakage current is more effectively suppressed for silicate structure than reported HfO$_2$-based structures.
Summary on La-Silicate/InGaAs Structure

- Nitridation of Si layer in forming silicate structure is effective for scaling capability of La-silicate stack.

- The balance of Si,N, La₂O₃ determines the composition of LaSiON structure.

- Effective $k$-value of 25 can be achieved for La₂O₃/LaSiON gate stack resulting in CET=0.73 nm.

- Small CET (<1nm), gate leakage current (< $10^{-1}$Acm⁻² at $V_{FB}+1V$), and $D_{it}$ ($\sim 4\times10^{12}$eV⁻¹cm⁻²) can be achieved for PMA up to 600 °C.
Thesis Structure

Chapter 1: Introduction

Chapter 2: Review on III-V issues

Chapter 3: Fabrication and characterization

Chapter 4: Bulk defects at HfO$_2$/InGaAs interface

Chapter 5: Gate Stack Engineering for InGaAs-based MOS capacitors with La$_2$O$_3$ gate dielectric

Chapter 6: Technologies for 3D structure

Chapter 7: InGaAs-based MOSFETs with La$_2$O$_3$ gate dielectric

Chapter 8: Conclusions
Evolution of MOSFETs to FinFETs

- Superior gate electrostatics can be achieved with FinFET structure
- EOT requirements can be relaxed

Gate Oxide Requirements
- Uniformity
- Thickness Control
- Conformity

ALD
La$_2$O$_3$ deposition by ALD

1 Cycle

Supply Gas: H$_2$O

Supply Gas: La($i$PrCp)$_3$

Supply and exhaust times were optimized for better electrical properties
Electrical properties of ALD-La$_2$O$_3$

Growth temp.=150°C
PMA 320°C, 5min
CET = 2.6 nm
75 Cycles

Identical CV characteristics obtained for both depo methods (EB more thermally stable)

Growth temperature affects hysteresis (elemental As formation)

As$_2$O$_3$ + 2Ga $\rightarrow$ Ga$_2$O$_3$ + 2As
XPS analysis of ALD-La$_2$O$_3$/InGaAs interface

- No As and Ga oxidation states were detected prior and post annealing
- In-O, In-OH formation at higher annealing temperature (might contribute to leakage current)
Issues of Metal SD on InGaAs

Metal SD regions might become necessary at small channel lengths and 3D InGaAs devices due to low dopant solubility of InGaAs

- Ni and Co have been investigated as a possibility for metal SD structure
- Ni-InGaAs alloy is formed, thin (<10nm) and uniform layer is difficult to process
- Metal and InGaAs reaction should be suppressed for 3D devices for optimal SD region design
Stacked Ni/Si approach

Ni (0.5 nm)  Si (1.9 nm)  InGaAs

Total of 8 sets

1 set

400 °C in N₂

NiSi₂ formation confirmed

Ni 2p₃/₂

NiSi₂ (400 °C)

Ni (as-depo)

Intensity (a.u.)

Binding energy (eV)

859 857 855 853 851 849

NiSi₂ (10nm) / In₀.₅₃Ga₀.₄₇As

N₂, 1 min

EDX point

Non-alloy structure achieved
NiSi$_2$ surface roughness

Surface roughness of NiSi$_2$ on InGaAs remains almost the same for PMA up to 500 °C.
$10^2$ higher $I_{ON}/I_{OFF}$ ratio can be achieved by NiSi$_2$/InGaAs junction

Temperature based $JV$ measurements for SBH yielded $\sim \phi_{Bp} = 0.62$ eV and $\sim n = 1.1$
ALD deposition method was demonstrated to be very promising to achieve high quality La₂O₃/InGaAs interface.

Excellent CV characteristics (small frequency dispersion and $D_{it} \sim 9 \times 10^{11} \text{eV}^{-1}\text{cm}^{-2}$) were achieved by ALD process.

Formation of unstable oxides can be prevented by choosing right deposition temperature window.

Non-Alloyed, thermally stable up to 600 °C with high quality interface and surface metal/InGaAs contact were demonstrated through the formation of NiSi₂.
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InGaAs-based devices

Chapter 7 InGaAs-based MOSFETs with La$_2$O$_3$ gate dielectric

Chapter 8 Conclusions
Transistor Fabrication Process

- **p-InGaAs substrate cleaning** (Acetone, Ethanol, HF 20%)
- **SiO₂ deposition** (100 nm by TEOS) (Channel region protection)
- **Ni deposition** (10 nm by Sputtering)
- **Low temperate anneal** (250 °C, N₂, 1min)
- **SiO₂ removal** (SD formation)
- **SD field SiO₂ deposition** (400 nm by TEOS) and patterning
- **Channel cleaning** (HCl 10%, (NH₄)₂S)
- **ALD-La₂O₃ deposition** (150°C, 75 cycles)
- **Gate electrode deposition TiN/W** (by sputtering)
- **Gate patterning, SD contact, Al pad deposition**
- **FG anneal for 5 min**
- **Back contact Al deposition**

Measurements
MOSFET Operation

- Fairly good MOSFET operation is confirmed.
- Peak mobility of 345 (cm²/Vs) obtained at a surface carrier concentration of 9x10^{12} (cm⁻²).
Summary and Conclusions

- High mobility semiconductors such as InGaAs offer a promising path for lower power, higher performance devices down the scaling road.

- Finding a scalable high-k/InGaAs structure with a high quality interface is a key challenge for realizing InGaAs-based MOSFETs.

- Formation of IL at high-k/InGaAs interface must be controlled. Lack of IL leads to high-k polarization and scattering, low quality IL increases CET, leakage current and $D_{it}$.

- It is possible to achieve scalable and high quality $La_2O_3$/InGaAs gate stack through the formation of $LaInGaO_x$ or La-silicate at the interface.
• Introduction
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• Thesis Structure
• Contents by Chapter
• Conclusions

• List of Publications

発表論文リスト2

論文誌発表論文(第一著者)-続き

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