A novel interface controlled silicidation process for future 3D Schottky devices

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Introduction

1.1 CMOS scaling
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1.1 CMOS scaling

Very Large Scale Integration (VLSI) technology has been considered essential to modern information society. VLSI circuits have been constructed by Complementally Metal-Oxide-Semiconductor (CMOS) Field-Effect-Transistor (FET). It is necessary for development of Information Technology (IT) that CMOSFET with high speed, low power consumption is achieved. The key to the advancement of VLSI technology is the device scaling which means scaling down the size of MOSFETs. Table 1.1 and figure 1.1 show the scaling rules for various device and circuit parameters. Scaling rules show speed up of circuit and reduction of power consumption are obtained with the scaling of the device dimensions [1.1]. Therefore, scaling leads to improvement of convenience for people and saving energy.

Table 1.1 Constant-field scaling of MOSFET device and circuit parameters.

The scaling remains electrical field unchanged.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Multiplicative factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length (L)</td>
<td>1/k</td>
</tr>
<tr>
<td>Channel width (W)</td>
<td>1/k</td>
</tr>
<tr>
<td>Gate oxide thickness (t_{ox})</td>
<td>1/k</td>
</tr>
<tr>
<td>Junction depth (x_j)</td>
<td>1/k</td>
</tr>
<tr>
<td>Doping concentration (N)</td>
<td>k</td>
</tr>
<tr>
<td>Electric field (E)</td>
<td>1</td>
</tr>
<tr>
<td>Depletion layer width (W_d)</td>
<td>1/k</td>
</tr>
<tr>
<td>Device area (A)</td>
<td>1/k^2</td>
</tr>
<tr>
<td>Circuit delay time (t)</td>
<td>1/k</td>
</tr>
<tr>
<td>Power consumption (P)</td>
<td>1/k^2</td>
</tr>
</tbody>
</table>
Chapter 1. Introduction

Figure 1.1 Schematic illustration of scaling MOSFET.

A lot of the performance of MOSFET has been improved by scaling, however, semiconductor industry has entered the era of material- and structure-limited device scaling [1.2]. Thus, the introduction of new materials such as high-κ gate insulators (to replace SiO₂ gate insulators), strained silicon, Ge and III-V substrates (to replace Si substrates) metal gates (to replace polysilicon gates) and metal source/drains (S/Ds) (to replace doped silicon S/Ds), and structures such as silicon on insulator (SOI), Fin and silicon nanowires (SiNWs), have been investigated as shown in table 1.2 and figure 1.2 [1.3]. However, there remain some issues in MOSFET with extremely scaling, such as short channel effect.
Table 1.2 The building-block materials of conventional and new material MOSFETs.

<table>
<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>New material</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate insulator</td>
<td>SiO₂</td>
<td>high-k</td>
</tr>
<tr>
<td>Gate electrode</td>
<td>Polysilicon</td>
<td>Metal</td>
</tr>
<tr>
<td>Substrate</td>
<td>Si</td>
<td>Strained-Si, Ge, III-V</td>
</tr>
<tr>
<td>S/D</td>
<td>Doped</td>
<td>Metal (silicide)</td>
</tr>
</tbody>
</table>

Figure 1.2 Schematic illustration of MOSFET with new structures.
1.2 Introduction of Schottky barrier S/D FET

When device size is scaled down, short channel effects occur. For short channel MOSFETs, there are some issues which are decrease of threshold voltage, drain induced barrier lowering (DIBL) and so on. Thus, it is one of the key for suppression of short channel effects to achieve abrupt and shallow junction at S/D [1.4]. An approach to realize the abrupt and shallow junction is using Schottky barrier S/D, which is typically formed by silicide. Schottky barrier S/D has some advantages which is atomically abrupt and shallow junctions and low parasitic resistance [1.5]. In addition to these advantages, a low temperature process capability is another advantage of Schottky barrier S/D [1.6]. Therefore, Schottky barrier S/D is the key technology to realize suppression of short channel effects (figure 1.3).

![Diagram](image-url)

**Figure 1.3** (a) 3D-FETs with conventional pn junctions suffer from short channel effects with channel length scaling due to the dopant diffusions which lower the abruptness. (b) Metal (silicide) Schottky junction is one of the solutions to suppress short channel effects because of abrupt junctions [1.7, 1.8].
1.3 Issues in Schottky barrier S/D FET

Schottky barrier S/D has been investigated for replacing conventional doping S/D to overcome short channel effects discussed in previous chapter. Especially, Ni silicides are expected as the material of Schottky barrier S/D because of some advantages which are relatively low resistivity, relatively low formation temperature and relatively small Si consumption during the formation for application to nanoscale structure [1.9]. However, there are some challenges in Ni silicidest. One is changing silicide phases depending on initial Ni thickness and annealing temperature as shown in figure 1.4 [1.10, 1.11, 1.12]. Silicide characteristics, such as resistivity, $\phi_B$ and so on, change with changing silicide phases as shown in table 1.3 [1.13, 1.14]. Thereby, it is important to control the silicide phase to obtain stable characteristics at wide process temperature range.

![Figure 1.4](image_url)

**Figure 1.4** A schematic image of crystalline phases of Ni silicides on the initial Ni thickness and annealing temperature [1.10, 1.11, 1.12].
Another is pattern dependent reaction. Figure 1.5 shows excess encroachment of silicide (a) near STI [1.15] or (b) into narrow channel (SOI/Fin/SiNW) due to supplying excess Ni atoms [1.16]. Forming facets or interface roughness degrades diode characteristics such as $\phi_B$ or $n$-factor. On the other hand, encroachment into narrow channel also degrades controllability of junction position [1.17]. Therefore, it is significant to control interface reaction.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Resistivity ((\mu\Omega \cdot \text{cm}))</th>
<th>Crystal structure</th>
<th>$\phi_B$ (eV)</th>
<th>$T_{\text{silicide}} / T_{\text{Ni}}$</th>
<th>Si consumption / $T_{\text{Ni}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>7-10</td>
<td>Cubic</td>
<td></td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Ni$_3$Si</td>
<td>80-90</td>
<td>Cubic</td>
<td></td>
<td>1.31</td>
<td>0.61</td>
</tr>
<tr>
<td>Ni$<em>{3.1}$Si$</em>{12}$</td>
<td>90-150</td>
<td>Hexagonal</td>
<td></td>
<td>1.40</td>
<td>0.71</td>
</tr>
<tr>
<td>Ni$_2$Si</td>
<td>24-30</td>
<td>Orthorhombic</td>
<td>0.7 ~ 0.75</td>
<td>1.47</td>
<td>0.91</td>
</tr>
<tr>
<td>Ni$_3$Si$_2$</td>
<td>60-70</td>
<td>Orthorhombic</td>
<td></td>
<td>1.75</td>
<td>1.22</td>
</tr>
<tr>
<td>NiSi</td>
<td>10.5-18</td>
<td>Orthorhombic</td>
<td>0.7 ~ 0.75</td>
<td>2.20</td>
<td>1.83</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>34-50</td>
<td>Cubic</td>
<td>0.7</td>
<td>3.61</td>
<td>3.66</td>
</tr>
<tr>
<td>Si</td>
<td>Dopant dependent</td>
<td>Cubic</td>
<td></td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Another is pattern dependent reaction. Figure 1.5 shows excess encroachment of silicide (a) near STI [1.15] or (b) into narrow channel (SOI/Fin/SiNW) due to supplying excess Ni atoms [1.16]. Forming facets or interface roughness degrades diode characteristics such as $\phi_B$ or $n$-factor. On the other hand, encroachment into narrow channel also degrades controllability of junction position [1.17]. Therefore, it is significant to control interface reaction.

Figure 1.5 Pattern dependent silicide reactions (a) near STI region and (b) Si Fin structure. Forming facets or encroachment of silicide degrade diode characteristics or controllability of junction position, respectively.
Chapter 1. Introduction

The other is control of $\phi_B$, $\phi_{Bn}$ and $\phi_{Bp}$, which are $\phi_B$ for electron and $\phi_B$ for hole, respectively, should be optimized for $n$-type SB-FET and $p$-type SB-FET, respectively. It is investigated that large $\phi_{Bn}$ and $\phi_{Bp}$ lead to low on-currents, poor subthreshold swing and ambipolar characteristics [1.5]. Thus, it is necessary for achieving high performances of SB-FET to reduce $\phi_{Bn}$ and $\phi_{Bp}$.

As shown in figure 1.6, the exact control of both (a) the junction position and (b) $\phi_B$ improves the device performance [1.6]. Therefore, it is the key for achieving the high performance of Schottky barrier S/D MOSFET (SB-FET) to control of junction position and $\phi_B$.

![Diagram](image)

**Figure 1.6** (a) Dependence of $I_{on}$-$I_{off}$ characteristics on junction position in SB-FETs.

(b) $I_{on}$-$I_{off}$ characteristics for $\phi_{Bn} = 0$–$0.3$ eV. The data in (a) and (b) were estimated by simulation [1.6].
1.4 Reports on Schottky barrier S/D FET

$\phi_B$ is determined by channel Si and silicide materials at S/D. Proper silicide materials at S/D have to be selected to reduce $\phi_B$. Pt/Pd silicides and Er/Yb silicides have been proposed for $p$- and $n$-type SB-FET, respectively [1.18]. However, there has a problem which is control of silicide formation of these silicides [1.19, 1.20]. Furthermore, when CMOSFETs are taken into account, it is necessary to control two different silicidation.

On the other hand, to obtain the proper $\phi_B$, midgap $\phi_B$ silicide (Ni/Co) with dopant segregation has been examined [1.21, 1.22]. There have two ways to achieve dopant segregation as shown in figure 1.7. One is (a) ion implantation before silicidation where dopants pile up at silicide/Si interface with silicidation and the other is (b) ion implantation after silicidation where dopants segregate at silicide/Si interface by activation annealing. The advantage of dopant segregation method is that the control of silicidation is only single silicide material. However, the issues of dopant segregation are (a) junction position control with silicidation and (b) control of the dopant position, especially 3D devices such as Si Fin or SiNW. Therefore, control of junction position and dopants are the key.
Chapter 1. Introduction

Figure 1.7 Methods of dopant segregation to modulate $\phi_B$. (a) ion implantation before silicidation where dopants pile up at silicide/Si interface [1.23], (b) ion implantation after silicidation where dopants segregate at silicide/Si interface by activation annealing [1.6].
1.5 Purpose of this study

As discussed in previous chapters, it is necessary for SB-FET with high performance to control silicide phase, junction position and impurity position and to modulate $\phi_B$. The purpose of this study is to overcome these issues of SB-FET. Thus, a novel stacked silicidation process is proposed. In this process, a set of Ni/Si is cyclically stacked on Si substrates to form NiSi$_2$ at low temperature. The concept of this process is to suppress the interface reaction between Ni and Si substrate by Si deposition in addition to Ni as shown in figure 1.8. Moreover, $\phi_B$ and impurity incorporated position can be controlled by deposition of impurity without ion implantation process. Finally, the device concept with stacked silicidation process for SOI, Fin, SiNW FETs is proposed as shown in figure 1.9. Atomically flat silicide/channel interface with no pattern dependent silicide reaction and no encroachment, also with $\phi_B$ modulation should be realized.

![Schematic illustration of stacked silicidation process. A set of Si/Ni, with an atomic ratio of 2:1, is cyclically stacked on n-Si (100) substrates, followed by annealing in N$_2$ ambient to form NiSi$_2$ film.](image)
Flat silicide/channel interface with $\Phi_{\text{Br}}$ modulation

Figure 1.9 Schematic illustrations of the device concept with stacked silicidation process for SOI, Fin, SiNW FETs. Atomically flat silicide/channel interface with keeping the shape of various Si substrates is achieved by using stacked silicidation process.
Chapter 1. Introduction

1.6 Outline of this thesis

Figure 1.10 shows the contents of this thesis. This thesis is consisted of 8 parts.

In chapter 1, the introduction of this thesis is stated.

In chapter 2, the fabrication process of devices and electrical characterization of Schottky diodes are explained.

In chapter 3, Ni film thickness dependent characteristics are investigated. It becomes obvious that NiSi₂ which is formed by 3.0-nm-thick Ni layer can be formed at low temperature and has stable characteristics at wide temperature range.

In chapter 4, characteristics of Ni silicide which is formed by stacked silicidation process are examined. An atomically flat interface and stable characteristics can be achieved by using stacked silicidation process. Moreover, an extension of stacked silicidation process to Ti is investigated.

In chapter 5, electrical characteristics of Ni silicide Schottky diodes are investigated. Schottky diode using stacked silicidation process has ideal characteristics.

In chapter 6, Schottky barrier height modulation with impurity incorporation is examined. It is realized that Schottky barrier height is modulated by impurity incorporation to the interface. Moreover, Schottky barrier height modulation controllability is investigated.

In chapter 7, SB-FET using stacked silicidation process is demonstrated. It is confirmed that ambipolar characteristics are suppressed by modulating Schottky barrier height.

Finally, chapter 8 summarizes this study.
Chapter 1. Introduction

Chapter 2
Fabrication and characterization

Chapter 3
Thickness dependent characteristics of Ni silicides

Chapter 4
Ni silicides using stacked silicidation process

Chapter 5
Electrical characteristics of Ni silicide Schottky diodes

Chapter 6
Schottky barrier height modulation

Chapter 7
Demonstration of silicide Schottky S/D FET with barrier height modulation

Chapter 8
Conclusion

Figure 1.10 Contents of this thesis
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Chapter 1. Introduction


Chapter 1. Introduction


Chapter 2
Fabrication and characterization

2.1 Fabrication procedure
2.2 Experimental details
2.3 Electrical characterization of Schottky diode

References
Chapter 2. Fabrication and characterization

2.1 Fabrication procedure

Figure 2.1 shows fabrication procedure of Schottky diodes. The diodes were fabricated on $n$-type (100)-oriented Si substrate. The substrate impurity concentration is $3 \times 10^{15}$ cm$^{-3}$. To determine the diode area, 400nm thermal oxide was formed, patterned by photolithography and etched SiO$_2$ by buffered HF (BHF). After SPM cleaning and HF treatment, thermal oxidation was performed because of protecting Si surface from resists and developers. Lift-off patterning and HF treatment due to removing SiO$_2$ formed by thermal oxidation were performed. Metal layer was deposited by RF sputtering. Metal which exists at excess area was removed by lift off process. An Al film was formed as a back contact by thermal evaporation. Rapid thermal annealing (RTA) in N$_2$ ambient was performed due to silicidation.

\[ n$-$Si(100)$ Sub with 400 nm SiO$_2$ (3x10^{15}$ cm$^{-3}$) \]

- Diode patterning
- BHF etching of SiO$_2$
- SPM and HF cleaning
- Deposition by RF sputtering in Ar
- Lift-off
- Backside Al contact
- Silicidation by RTA in N$_2$

Figure 2.1 Fabrication flow of Schottky diode.
Chapter 2. Fabrication and characterization

2.2 Experimental details

2.2.1 SPM cleaning and HF treatment

Particles and organic substance at the surface of Si substrate become a cause of false operation. Therefore, it is important to clean the surface of Si substrate. SPM cleaning is one of the effective cleaning methods. The cleaning liquid is made from \( \text{H}_2\text{O}_2 \) and \( \text{H}_2\text{SO}_4 \) (\( \text{H}_2\text{O}_2:\text{H}_2\text{SO}_4 = 1:4 \)). Because of its oxidizability, particles and organic substance are oxidized and separated from the surface of Si substrate. However, the surface of Si substrate is oxidized and \( \text{SiO}_2 \) is formed during SPM cleaning. 1% HF is used to eliminate the \( \text{SiO}_2 \).

2.2.2 RF magnetron sputtering

Metal is deposited by radio frequency (RF) magnetron sputtering with Ar gas. An RF with 13.56 MHz is applied between substrate side and target side. Because of the difference of mass, Ar ions and electrons are separated. A magnet is set underneath the target, so that the plasma damage is minimized. Electrons run through the circuit from substrate side to target side, because substrate side is subjected to be conductive and target side is subjected to be insulated. Then, target side is negatively biased and Ar ions hit the target.
2.2.3 Lift-off process

Lift-off is the process which selectively removes deposited films. Following photolithography and deposition, resists and deposited films which exist on excess area are left by ultrasonic cleaning with acetone.

2.2.4 Vacuum evaporation for Al deposition

Al for wiring and backside contact is deposited by vacuum evaporation. Al source is set on W boat and heated up to boiling point of Al by joule heating. However, melting point of W is higher than boiling point of Al, W boat doesn’t melt. The base pressure in the chamber is maintained to be $10^{-3}$ Pa (Fig. 2.4).
2.2.5 Rapid thermal annealing (RTA)

Rapid thermal annealing (RTA) is performed for silicidation. Heating chamber is filled with N₂ to interfere with oxidation. In this study, the time of elevated temperature is 30 seconds and the time of annealing is 1 minute.

A schematic illustration of Schottky diode fabrication process is shown in figure 2.4.
Chapter 2. Fabrication and characterization

Figure 2.4 Schematic illustration of Schottky diode process.
2.3 Electrical characterization of Schottky diode

Schottky diode characteristics are evaluated by $J-V$ characteristics, $\phi_B$ and $n$-factor. $\phi_B$ and $n$-factor can be extracted by fitting with ideal $J-V$ curve. In this study, for analyzing Schottky diode characteristics, image force lowering and thermionic emission are considered [2.1]. In this chapter, Schottky diodes of metal (silicide) and $n$-Si contacts are discussed.

2.3.1 Metal-silicon contact

When metal and silicon contact, these must share the same free electron level at the interface [2.2]. Also, at thermal equilibrium or when there is no net electron or hole current through a system, the Fermi level of the system is spatially constant. These two factors lead to the band diagram as shown in figure 2.5 for a metal-$n$-Si contact at thermal equilibrium. Considering free electron energy level, Schottky barrier height for electron ($\phi_{Bn0}$) is given by

$$q \phi_{Bn0} = q(\phi_m - \chi)$$  \hspace{1cm} (2.1)

where $\phi_m$ is the metal work function and $\chi$ is the electron affinity of silicon.
2.3.2 Image-force lowering

Image-force lowering is the image-force-induced lowering of the barrier energy for charge carrier emission [2.2]. Image-force lowering ($\Delta \phi$) for the metal-Si contact is

$$
\Delta \phi = \frac{qE_m}{\sqrt{4\pi\varepsilon_{Si}}} \tag{2.2}
$$

where $E_m$ is maximum value of electric field and $\varepsilon_{Si}$ is the Si permittivity. Therefore, Schottky barrier height ($\phi_{Bn}$), considering image-force lowering, is given by

$$
q\phi_{Bn} = q\phi_{Bn0} - \Delta \phi \tag{2.3}
$$

as shown in figure 2.6.
2.3.3 Thermionic emission

In thermionic emission, the simplest theory is to deal with the electron as an ideal gas that follows Boltzmann statistics in energy distribution [2.1]. The electron emission current from Si into metal ($J_{s\rightarrow m}$) is given by

$$J_{s\rightarrow m} = A^* T^2 \left[ - \exp \left( \frac{q \phi_{Bn0}}{kT} \right) \right] \exp \left( \frac{qV}{nkT} \right)$$  \hspace{1cm} (2.4)

where $A^*$ is effective Richardson’s constant, $n$ is ideality factor ($n$-factor) and $V$ is applied voltage. On the other hand, the electron emission current from metal into Si ($J_{m\rightarrow s}$) is

$$J_{m\rightarrow s} = A^* T^2 \left[ - \exp \left( \frac{q \phi_{Bn0}}{kT} \right) \right]$$  \hspace{1cm} (2.5)

Therefore, the total current $J_{n0}$ is given by
Chapter 2. Fabrication and characterization

\[ J_{n0} = A^* T^2 \left[ -\exp \left( \frac{q(\phi_{Bn})}{kT} \right) \right] \exp \left( \frac{qV}{nkT} \right) - 1 \] (2.6)

In addition to image-force lowering, total current \( J_n \) is

\[ J_n = A^* T^2 \left[ -\exp \left( \frac{q(\phi_{Bn} - \Delta \phi)}{kT} \right) \right] \exp \left( \frac{qV}{nkT} \right) - 1 \]
\[ = A^* T^2 \left[ -\exp \left( \frac{q\phi_{Bn}}{kT} \right) \right] \exp \left( \frac{qV}{nkT} \right) - 1 \] (2.7)

as shown in figure 2.7. \( \phi_{Bn} \) and \( n \)-factor are extracted by fitting measurement data and (2.7).

**Figure 2.7** Band diagram of metal-n-Si contact incorporating image-force lowering to show the thermionic emission current.
Chapter 2. Fabrication and characterization

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Chapter 3

Thickness dependent characteristics of Ni silicides

3.1 Introduction
3.2 Thermal stability of Ni silicide films
3.3 Bonding states of Ni silicide film
3.4 Conclusion

References
3.1 Introduction

Ni silicides have been widely investigated for contact materials in microelectronic devices because of relatively low resistivity, relatively low formation temperature and relatively small Si consumption during the formation in comparison with other silicide materials [3.1]. One of the issues of Ni silicides is that the formed NiSi, a low-resistive phase in Ni silicides, starts to agglomerate at an annealing temperature of 600 °C [3.2]. As the agglomeration is the results of minimizing the gain boundary between NiSi grains and the interface energy of NiSi and Si substrate, the temperature for agglomeration decreases when the thickness of NiSi is reduced [3.3]. Recently, Ni films with thicknesses less than 4 nm were found to be resistant to agglomeration up to an annealing temperature of 850 °C [3.4]. The difference in the silicide films is the formation of NiSi$_2$ phase even at an annealing temperature of 300 °C, which is commonly formed at an annealing temperature of 800 °C [3.5]. Therefore, the suppression of the agglomeration can be understood by the difference in the energy of NiSi$_2$ and NiSi phases. The suppression of agglomeration is also advantageous to obtain a flat interface between silicides and Si substrates. The interface of silicide and Si substrates tends to form pyramid shapes with Si(111) plane [3.6]. Therefore, another advantage of agglomeration-resistant Ni silicides is the suppression of forming interfaces with different crystallographic orientations. This chapter confirms the phase and the surface morphology changes of Ni silicide films on annealing temperature.
Chapter 3. Thickness dependent characteristics of Ni silicides

3.2 Thermal stability of Ni silicide films

Figure 3.1 and figure 3.2 show sheet resistance ($\rho_{sh}$) and surface roughness of the films on annealing temperature, respectively. For the sample with 5.5-nm-thick Ni layer, $\rho_{sh}$ showed a large decrease over 300 °C, which is attributed to the formation of NiSi phase in the silicide. When the annealing temperature is over 500 °C, the $\rho_{sh}$ showed a large increase due to agglomeration of the silicides which is shown in figure 3.2. On the other hand, for the sample with Ni thickness of 3.0 nm, a gradual reduction in the $\rho_{sh}$ was observed over 300 °C, and the value became stable at annealing temperatures from 400 to 800 °C, which is in good agreement with previous reports [3.4, 3.6]. Considering the resistivity of typical bulk NiSi$_2$ (34~50 $\mu\Omega$cm) [3.7], the phase of the silicide film can be considered as NiSi$_2$. Consequently, both of the thickness of these samples is estimated about 10 nm [3.7].

![Figure 3.1 Sheet resistance ($\rho_{sh}$) of silicides with 3.0 and 5.5 nm thick Ni layers on annealing temperature (t$_{Ni}$ is Ni thickness).](image)

RTA : 1min in N$_2$

$\rho_{sh}$: Sheet resistance (\Omega/sq)

Annealing temperature (°C)

Sheet resistance $\rho_{sh}$ (\Omega/sq)

Annealing temperature (°C)

n-Si(100)

Ni:3.0nm

Ni:5.5nm

agglomeration

wide process window
Figure 3.2 Surface roughness of silicide films with 3.0 and 5.5 nm thick Ni layers on annealing temperature.
3.3 Bonding states of Ni silicide film

Ni $2p_{3/2}$ spectra of the samples annealed at various temperatures are shown in figure 3.3. The binding energy at the peak intensity was found to shift to higher energy from pure Ni, which was obtained by as-deposited sample. At an annealing temperature of 250 °C, the spectrum indicates the main composition is Ni-rich phase, which is in good agreement with the $\rho_{sh}$ as high resistivity is reported for Ni-rich phase. The sample with 5.5-nm-thick-Ni showed a single peak at 500 °C annealing, which corresponds to the NiSi phase at 853.72 eV [3.8]. For 3-nm-thick-Ni samples, while increasing the annealing temperature, two peak intensities, one at 854.19 eV with large intensity and the other Ni-rich phase with small intensity, were observed at 500 °C. The intensity at 854.19 eV further increased when the sample was annealed at 800 °C, indicating that the residual Ni-rich phase was converted to NiSi$_2$ phase by annealing [3.9].

![Figure 3.3 Ni $2p_{3/2}$ spectra of the silicide films annealed at various temperature.](image-url)
3.4 Conclusion

Ni silicides, reactively formed by 3.0-nm-thick Ni, have shown a stable sheet resistance, flat morphology against annealing temperature up to 800 °C compared to those formed with thicker Ni film. These properties are owing to the formation of stable NiSi$_2$ phase at a temperature as low as 500 °C. The summary of Ni silicide phase and morphology change is shown in figure 3.4.

Figure 3.4 Ni silicide phase and morphology change dependent on Ni thickness.

![Diagram showing Ni silicide phase and morphology change](image)
Chapter 3. Thickness dependent characteristics of Ni silicides

References


Chapter 3. Thickness dependent characteristics of Ni silicides


Chapter 4
Ni silicides using stacked silicidation process

4.1 Introduction

4.2 Interface reaction

4.3 Composition and morphology

4.4 Stacked silicidation process of other semiconductor substrates

4.5 Extension of stacked silicidation process for Ti

4.6 Conclusion

References
4.1 Introduction

As described in chapter 3, in the case of 3.0-nm-thick Ni layer deposition, the stable composition and morphology can be obtained at wide process temperature range because NiSi₂, which is the most stable phase in Ni silicides, is formed at low temperature. However, there remain some issues which are pattern dependent reaction and limitation of silicide thickness because of limitation of initial Ni thickness within 4.0 nm to form NiSi₂ at low temperature [4.1, 4.2, 4.3]. Thereby, to solve these issues, stacked silicidation process is proposed as shown in figure 4.1. In this process, interface reaction can be suppressed because Si substrate reacts with only first 0.5-nm-thick Ni layer and silicide thickness can be changed easily by changing the number of a set of Ni/Si. In this chapter, therefore, characteristics of Ni silicide using stacked silicidation process are investigated. Furthermore, stacked silicidation process of other semiconductor substrates and extension of stacked silicidation process to Ti are examined.

![Figure 4.1 Schematic illustration of stacked silicidation process. A set of Si/Ni, with an atomic ratio of 2:1, is cyclically stacked on n-Si (100) substrates, followed by annealing in N₂ ambient to form NiSi₂ film.](image-url)
4.2 Interface reaction

As shown in figure 4.2, TEM images of silicide/Si interface formed from Ni/Si stacked silicidation process before (Figure 4.2(a)) and after annealing at 500 °C for 1 min in N₂ ambient to form NiSi₂ (Figure 4.2(b)). TEM images revealed the formation of 10-nm-thick stacked silicide, no change in the thickness and atomically flat interface and surface before and after annealing at 500 °C because consumption of Si from substrate is limited to the first Ni layer.

Owing to little reaction of NiSi₂ formed from stacked silicidation process with Si channel, diffusions of Ni atoms into channels can be well suppressed. Figure 4.3 shows SEM images of Si Fins after annealing with (a) Ni or (b) stacked silicide stripe on the right-hand-side. Due to excess supply of Ni atoms into Si Fins, in the case of Ni deposition, lateral silicidations were observed with scattered encroachment length.

\[\text{Figure 4.2 TEM images of stacked silicidation process at (a) as deposited and (b) after annealing at 500 °C. Atomically flat interface and surface are achieved.}\]
On the other hand, with the use of stacked silicidation process, one can observe a complete inhibition of encroachments into Si Fins, owing to suppression of interface reaction between silicide and Si Fins. In other words, interface position can be well-defined by using stacked silicidation process. Although suppression of lateral encroachments has been reported with 2-step annealing or nitrogen atom incorporation [4.4, 4.5], stacked silicidation process has an advantage for S/D in 3D Si channels as it completely suppresses the encroachments.

Figure 4.3 SEM images of Si Fins after annealing with (a) Ni or (b) stacked silicide. (a) Ni atoms encroach into Si Fin. (b) Complete suppression of encroachment can be achieved using Ni/Si stacked silicidation process.
4.3 Morphology and composition

4.3.1 Thermal stability of stacked silicidation process

Figure 4.4 and figure 4.5 show sheet resistance ($\rho_{sh}$) and surface roughness of the films on annealing temperature, respectively. The silicide thickness of all samples is 10 nm. For the sample with Ni/Si stacked silicidation process showed a decrease over 325 °C and kept the stable value up to 875 °C. Although $\rho_{sh}$ of stacked silicide is slightly larger than 3.0-nm-thick Ni layer, $\rho_{sh}$ of stacked silicide is stable at wide process temperature window. On the other hand, the surface roughness of stacked silicide is slightly larger than those of 3.0-nm-thick Ni sample, however, the value is small enough. The surface morphology of stacked silicide was flat over wide range temperature.

![Figure 4.4 $\rho_{sh}$ of stacked silicide, 3.0-nm- and 5.5-nm- thick Ni layers on annealing temperature. $\rho_{sh}$ of stacked silicide is stable at wide process window.](image-url)
Figure 4.5 Surface roughness of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers on annealing temperature. Surface roughness of stacked silicide is stable at wide process window.
4.3.2 XRD analysis of stacked silicide film

Figure 4.6 shows Out-of-plane XRD (2\(\theta\)/\(\omega\) scan) profile of stacked silicide. NiSi\(_2\)(004) peak can be detected at 2\(\theta\) = 70.56°. Whereat, Rocking curve measurement (\(\omega\) scan) at 2\(\theta\) = 70.56° is shown in figure 4.7. Because rocking curve width is about 0.1° which is narrow value, it is considered that NiSi\(_2\) formed by stacked silicidation process is epitaxially grown.

![Out-of-plane XRD profile](image)

*Figure 4.6 Out-of-plane XRD (2\(\theta\)/\(\omega\) scan) profile of stacked silicide annealed at 500°C. NiSi\(_2\)(004) peak can be detected at 2\(\theta\) = 70.56°.*
Figure 4.7 Rocking curve measurement (ω scan) at 2θ = 70.56°. Because rocking curve width is about 0.1° which is narrow value, it is considered that NiSi₂ formed by stacked silicidation process is epitaxially grown.

Figure 4.8 shows that In-plane XRD (2θχ/ϕ scan) profile of stacked silicide annealed at 500 °C in ω = 0.3°. In-plane XRD has some characteristics which are large irradiated area and small penetration depth due to low incident angle. Red line shows X-ray incident direction can be observed Si(400) peak (ϕ = 0°) and blue line shows ϕ = 15°. In the case of ϕ = 0°, NiSi₂(200) and NiSi₂(220) peaks are detected. When ϕ is displaced to 15°, NiSi₂(200) can not be observed, on the other hand, NiSi₂(220) can be observed. Rocking curve measurement (ϕ scan) at NiSi₂(200) is shown in figure 4.9. Because rocking curve width is about 0.6° which is narrow value, it is considered that NiSi₂ is epitaxially grown. On the other hand, when ϕ is
displaced, NiSi₂(220) can be observed. Thus, it is expected that in-plane orientation is random. Therefore, it is predicted that the element which is cube-on-cube epitaxially grown for Si substrate and the oriented element that (110) axis is distributed at random in in-plane exist. However, NiSi₂(200) peak cannot be observed in \( \phi = 15^\circ \) (figure 4.8 blue line). From this result, it is expected that the oriented element has a texture that (111) axis is oriented to surface normal direction. In the crystal structure of NiSi₂ (Fluorite type structure), (111) plane is dense plane, it is suggested that this orientation texture can be formed in addition to the epitaxial element as shown in figure 4.10.

**Figure 4.8** In-plane XRD (2\( \theta \)/\( \phi \) scan) profile of stacked silicide annealed at 500 °C in \( \omega = 0.3^\circ \). Red line is \( \phi = 0^\circ \) and blue line is \( \phi = 15^\circ \). When \( \phi \) is displaced to 15°, NiSi₂(200) peak cannot be observed, on the other hand, NiSi₂(220) peak can be observed.
Chapter 4. Ni silicides using stacked silicidation process

**Figure 4.9** Rocking curve measurement (φ scan) at NiSi$_2$(200). Because rocking curve width is about 0.6° which is narrow value, NiSi$_2$ is epitaxially grown.

**Figure 4.10** The images of orientation of NiSi$_2$ film. It is suggested that (111)-oriented texture can be formed in addition to the epitaxial element.
4.3.3 XPS analysis of stacked silicide film

Ni 2$p_{3/2}$ spectra of the samples annealed at various temperatures are shown in figure 4.11. Stacked silicide showed similar peaks with 3.0-nm-thick-Ni, thus, the phase of stacked silicide is NiSi$_2$.

Ni 2$p_{3/2}$ spectra of the stacked silicide annealing at 500 °C measured changing photoelectron take-off angles (TOAs) from 30° to 80° are shown in figure 4.12. Inelastic mean free path ($\lambda$) is calculated by TPP-2M. In this case, $\lambda$ is equal to 9.6 nm. All spectra were close to the same each other independent of TOAs. From the results of TEM images, XRD profiles and Ni 2$p_{3/2}$ spectra, it is considered that stacked silicide film is uniform and epitaxially grown NiSi$_2$.

![Graph showing Ni 2$p_{3/2}$ spectra of the silicide films annealed at 500 °C. The phase of stacked silicide is NiSi$_2$.]

**Figure 4.11** Ni 2$p_{3/2}$ spectra of the silicide films annealed at 500 °C. The phase of stacked silicide is NiSi$_2$. 
Chapter 4. Ni silicides using stacked silicidation process

4.3.4 Annealing temperature dependent the phase of stacked silicide

Ni 2p$_{3/2}$ spectra of stacked silicide annealed at various temperatures are shown in figure 4.13. The phase of stacked silicide is Ni-rich silicide from as deposited to 300 °C. At 325 °C, the phase of stacked silicide is Ni-rich silicide and NiSi$_2$. The Ni-rich silicide intensity decreased and NiSi$_2$ intensity increased with increase in annealing temperature, indicating that the residual Ni-rich silicide is converted to NiSi$_2$ by annealing. Therefore, the silicide phase change on annealing temperature corresponds with $\rho_{sh}$ of stacked silicide on annealing temperature. Then, Ar 1s spectra of stacked silicide annealed at various temperatures are shown in figure 4.14. Ar intensity is large from as deposited to 300 °C. Over 325 °C, Ar intensity

Figure 4.12 Ni 2p$_{3/2}$ spectra of stacked silicide annealed at 500 °C measured by Angle Resolved-XPS (AR-XPS) changing TOAs from 30° to 80°. Stacked silicide film is uniform NiSi$_2$. 

![Diagram showing Ni 2p$_{3/2}$ spectra and TOA values](image_url)
Chapter 4. Ni silicides using stacked silicidation process

decrease. This trend corresponds with the trend of $\rho_{sh}$. Therefore, it is speculated that
the decrease of Ar in stacked silicide film causes the decrease of $\rho_{sh}$, which means
formation of NiSi$_2$. In the following chapter, the relation between the amount of Ar
in the stacked silicide film and the annealing temperature is investigated.

![Ni 2p$_{3/2}$ spectra of stacked silicide on annealing temperature. The phase of stacked silicide changes from Ni-rich silicide to NiSi$_2$ with increase in annealing temperature.](image)

**Figure 4.13** Ni 2p$_{3/2}$ spectra of stacked silicide on annealing temperature. The phase of stacked silicide changes from Ni-rich silicide to NiSi$_2$ with increase in annealing temperature.
4.3.5 The effect of sputtering pressure on sheet resistance of stacked silicide

As previously indicated, it is shown that there are Ar atoms into the silicide film and NiSi$_2$ is formed by desorption of Ar atoms from the silicide film with annealing. Thus, in this section, stacked silicide is deposited in various sputtering pressures to change the amount of Ar atoms in the silicide film. Thereby, the effect of Ar atoms which are in the silicide film on the formation of NiSi$_2$ is investigated.

The amount of Ar atoms in sputtering chamber by increasing sputtering pressure, consequently, it is considered that the amount of Ar atoms in silicide film increases. Also, there is a relationship between sputtering pressure and film properties, such as surface morphology, crystallographic orientation and grain size [4.6, 4.7]. Therefore,
it is possible to relate to quality of NiSi₂.

Figure 4.15 shows the $\rho_{sh}$ of stacked silicide on annealing temperature deposited in various sputtering pressures. The temperature of decreasing $\rho_{sh}$ decreased with decrease in sputtering pressure. The sample of 0.55 Pa achieves the lowest $\rho_{sh}$ and the lowest annealing temperature of formation of NiSi₂. Because for the sample of 0.55 Pa, the amount of initial Ar atoms in silicide film is few in comparison to the sample of 2 Pa, it can be formed NiSi₂ at lower annealing temperature. Thus, it is considered that NiSi₂ can be formed at low temperature by decreasing sputtering pressure to decrease the amount of Ar in the stacked silicide film.

The crystallinity of NiSi₂ film dependent on sputtering pressure is discussed below. Figure 4.16 shows XPS profile of stacked silicide which is deposited in 0.55 Pa annealed at 500°C. NiSi₂(004) peak can be detected at $2\theta = 70.50^\circ$. Whereat, Rocking curve measurement ($\omega$ scan) at $2\theta = 70.50^\circ$ is shown in figure 4.17. Because rocking curve width is about 0.2° which is narrow value, it is considered that NiSi₂ formed by stacked silicidation process is epitaxially grown. However, the crystallinity of the sample of 2 Pa is well in comparison to the sample of 0.55 Pa from the result of rocking curve width (figure 4.7). From the results of $\rho_{sh}$, it is considered that NiSi₂ is formed by desorption of Ar atom from stacked silicide film. However, from the XRD profiles, the crystallinity of NiSi₂ is good when the amount of Ar in the film is few. The relationship of these results has not cleared yet. SIMS profile of Ar should be measured.
Figure 4.15 $\rho_{sh}$ of stacked silicide on annealing temperature. $\rho_{sh}$ of stacked silicide is stable at wide process window. When the sputtering pressure is 0.55 Pa, $\rho_{sh}$ decrease occurs at the lowest annealing temperature.
Figure 4.16 Out-of-plane XRD (2θ/ω scan) profile of stacked silicide annealed at 500 °C. NiSi$_2$(004) peak can be detected at 2θ = 70.50°.

Figure 4.17 Rocking curve measurement (ω scan) at 2θ = 70.50°. Because rocking curve width is about 0.2° which is narrow value, it is considered that NiSi$_2$ formed by stacked silicidation process is epitaxially grown.
Chapter 4. Ni silicides using stacked silicidation process

4.4 Stacked silicidation process of other semiconductor substrates

4.4.1 Characteristics of stacked silicide on different Si orientation

Figure 4.18 shows the $\rho_{sh}$ of stacked silicide which is several thicknesses deposited on various oriented Si substrates. Figure 4.11(a), (b) and (c) show Si(100), Si(110) and Si(111), respectively. In these results, morphology of stacked silicide is stable at wide temperature range independent of stacked silicide thickness and Si substrate orientations. Therefore, it is considered that the stacked silicidation process is promising for Si Fin or Si nanowire FETs.
Figure 4.18 $\rho_{sh}$ of different stacked silicide thickness on annealing temperature. Each stacked silicide is deposited on (a) n-Si(100), (b) n-Si(110) and (c) n-Si(111) substrate. $\rho_{sh}$ of stacked silicide is stable at wide process window independent of Si substrate orientation.
4.4.2 Characteristics of stacked silicide on other semiconductor substrates

Germanium has been receiving attention as an alternative channel material [4.8, 4.9] because of its high intrinsic mobility (two times higher for electrons and four times higher for holes as compared to those in silicon). Reduction of parasitic resistance of metallic contact on Ge substrate is one of the issues for Ge FETs, and low contact resistance of NiGe with Ge substrate has been studied as metallic contact on Ge substrate [4.10]. However, agglomeration of NiGe roughens metal/Ge interface thereby increasing the sheet resistance at the interface [4.11]. Therefore, in order to obtain resistant agglomeration compared to NiGe, Ni/Si stacked silicidation process is applied for Ge substrate.

Figure 4.19 shows $\rho_{sh}$ of stacked silicide on Ge substrate on annealing temperature. Although small sheet resistance could be obtained by forming NiGe on Ni films, process temperature were limited (Ni-5.5-nm film was from 250 °C to 375 °C) due to agglomeration of the NiGe surface. On the other hand, once NiSi$_2$ is formed over 350 °C, stable sheet resistances can be obtained up to 700 °C, which gives process compatibility for dopant activation in Ge devices.
Chapter 4. Ni silicides using stacked silicidation process

Figure 4.19 $\rho_{sh}$ of stacked silicide on Ge substrate on annealing temperature. $\rho_{sh}$ of stacked silicide on Ge is more stable than that of 5.5-nm-thick Ni layer on Ge.
GaN based devices have been focused as a semiconductor for power electronics applications [4.12]. One of the issues is that metal contact with GaN based devices is degraded by surface agglomeration. Thus, it is proposed that stacked silicidation process is applied for GaN based devices.

Figure 4.20 shows $\rho_{sh}$ of stacked silicide on GaN and AlGaN substrates on annealing temperature. It is considered that stable $\rho_{sh}$ can be obtained due to suppression of interface reaction and formation NiSi$_2$ at low temperature.

Figure 4.20 $\rho_{sh}$ of stacked silicide on GaN and AlGaN substrates on annealing temperature. $\rho_{sh}$ of stacked silicide on each substrate is stable.
4.5 Extension of stacked silicidation process for Ti

TiSi\textsubscript{2} is the most stable phases in Ti silicides, however, there are two crystal structure in TiSi\textsubscript{2}. One is C49-TiSi\textsubscript{2} and the other is C54-TiSi\textsubscript{2} \[4.13\]. C54-TiSi\textsubscript{2} is the most stable phase in Ti silicides \[4.14\]. C54-TiSi\textsubscript{2} has been used due to low resistivity but there are some issues. One of the issues is that formation temperature is high and the other is degradation of surface morphology by agglomeration \[4.15\]. As previous indicated, stacked silicidation process using Ni has some advantages compared to conventional Ni silicidation process. Thus, it is investigated about extension of stacked silicidation process for Ti as shown in figure 4.21.

Figure 4.22 shows $\rho_{sh}$ of Ti silicide formed by stacked silicidation process and by deposition 20-nm-thick Ti layer on annealing temperature. In 20-nm-thick Ti layer, it is confirmed that $\rho_{sh}$ decreases over 600 °C and further decreases at 800 °C that correspond with formation of C49-TiSi\textsubscript{2} and C54-TiSi\textsubscript{2}, respectively. On the other hand, Ti/Si stacked silicidation process shows different trend to 20-nm-thick Ti layer. Moreover, Ti/Si stacked silicide can not achieve stable $\rho_{sh}$ at wide range temperature range.

![Figure 4.21](image)

**Figure 4.21** Schematic illustration of Ti/Si stacked silicidation process. A set of Si/Ti, with an atomic ratio of 2:1, is cyclically stacked on n-Si (100) substrates.
The reaction of Ti/Si stacked silicide is between thin-Ti-layer and thin-Si-layer, on the other hand, the reaction of 20-nm-thick Ti layer is between thick-Ti-layer and single crystal Si substrate. Therefore, it is considered that the phase or crystallinity of these samples is different. However, the phase and crystallinity of Ti/Si stacked silicide is not still measured. It is considered that to form the most stable silicide phase by stacked silicidation process at wide process temperature range is unique characteristics of Ni silicide.

\[ \rho_{sh} \]

**Figure 4.22** $\rho_{sh}$ of Ti silicide which is formed by Ti/Si stacked silicidation process and 20-nm-thick-Ti layer on annealing temperature.
4.6 Conclusion

In order to achieve the control of interface reaction and stable composition and morphology at wide temperature range, stacked silicidation process has been investigated. It is realized that an atomically flat interface and surface are formed before and after annealing and Ni atoms encroachment into Si Fin is suppressed completely. In fact, it is an advantage for scaled 3D devices that the shape of Si substrate after silicidation does not change due to suppression of interface reaction.

Second, it is achieved that NiSi₂ which is formed by stacked silicidation process is stable composition and morphology at wide temperature range. Moreover, it is suggested that NiSi₂ formation is advanced by desorption of Ar atoms which are in silicide films.

Third, it is accomplished that the $\rho_{sh}$ of stacked silicide on various substrates is stable at wide temperature range. Stacked silicidation process can be applied for 3D Si channel and other semiconductor substrates.

And finally, extension of stacked silicidation process for Ti has been examined. It is considered that to form the most stable silicide phase by stacked silicidation process at wide process temperature range is unique characteristics of Ni silicide.

As discussed above, it is considered that Ni/Si stacked silicidation process is the key for future scaled 3D SB-FET.
Chapter 4. Ni silicides using stacked silidation process

References


Chapter 5
Electrical characteristics of Ni silicide Schottky diodes

5.1 Introduction
5.2 Schottky diode characteristics
5.3 TiN capping on stacked silicides
5.4 Conclusion

References
5.1 Introduction

In chapter 3 and 4, the physical properties of silicide films, which are formed by different methods, such as interface reaction, composition and morphology are examined. In this chapter, the electrical characteristics of Schottky diodes which are formed by those silicides are investigated.

There are some problems in Ni silicide Schottky diodes [5.1]. One is increasing the reverse leakage current because of the leakage current at the electrode periphery where excess silicidation occurs, and the other is the variation of $\phi_{bn}$ and $n$-factor due to existing on roughness and facets at the interface and the electrode periphery. Thus, to obtain the ideal Schottky diode characteristics, it is necessary to achieve an atomically flat interface including the electrode periphery. In this chapter, therefore, Schottky diode characteristics using stacked silicidation process which can be obtained an atomically flat interface are investigated.

![Figure 5.1 The presence of facets and roughness which occur leakage currents at interface and periphery [5.1].](image)

(a) 350 °C  (b) 350 °C  (c) 750 °C
5.2 Schottky diode characteristics

Figure 5.2 shows diode current density-voltage ($J-V$) characteristics of the fabricated Ni silicide Schottky diodes. For 3-nm-thick and 5.5-nm-thick Ni samples, the increase of reverse current from theoretical value was observed. On the other hand, for stacked silicide, the increase of reverse current from theoretical was not observed. Figure 5.3 shows $\phi_{Bn}$ and ideality factor ($n$-factor) extracted by $J-V$ characteristics on annealing temperature. For stacked silicide, it is observed that $\phi_{Bn}$ is stable value 0.61 ~ 0.63 eV and $n$-factor is less than 1.05 up to 700 °C. On the other hand, for 3.0-nm-thick and 5.5-nm-thick Ni samples, $\phi_{Bn}$ was not stable and $n$-factor was worse than that of stacked silicide. From these results, it is considered that these differentials between stacked silicide and conventional silicides depend on a method of silicide formation. For conventional silicide which formed by reacting between Ni film and Si substrate, issues of interface reaction such as excessive growth of silicide at the periphery of the electrodes and formation of plane orientation which is not Si(100) existed [5.1, 5.2]. Thereby, it is considered that increasing reverse current from theoretical value and variation of $\phi_{Bn}$ and $n$-factor occurred. On the other hand, for stacked silicide, issues of interface such as conventional silicide did not occur because stacked silicide was able to form suppressing the reaction with Si substrate as shown in figure 4.1. Using stacked silicide, the issues of conventional silicide are overcome.
Figure 5.2 The Schottky diode J-V characteristics of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers. J-V characteristic of stacked silicide is ideal.

Figure 5.3 $\phi_{Bn}$ and n-factor of stacked silicide, 3.0-nm- and 5.5-nm-thick Ni layers on annealing temperature. $\phi_{Bn}$ and n-factor of stacked silicide are stable value up to 700 °C.
5.3 TiN capping on stacked silicide

Ni silicides should be protected by etchant, which is used in etching process, in fabrication process of transistors because Ni silicides can be etched by HF \[5.3\]. Then, the protection of Ni silicides by TiN capping is proposed. In this section, the effect of TiN capping on electrical characteristics is stated.

Figure 5.4 shows the fabrication procedures of Schottky diodes with or without TiN capping. 50-nm-TiN layer is deposited by sputtering.

Figure 5.5 shows $J-V$ characteristics of diodes with or without TiN capping. It is clear that $J-V$ characteristics remain ideal even with TiN capping. However, $\phi_{bn}$ of with TiN capping is a little bit larger than that of without TiN capping. Figure 5.6 shows $\phi_{bn}$ and ideality factor ($n$-factor) extracted by $J-V$ characteristics on annealing temperature. It is investigated that stable $\phi_{bn}$ and $n$-factor remain even with TiN capping, furthermore, scatter of $\phi_{bn}$ and $n$-factor with TiN capping is suppressed compared with without TiN capping. Therefore, it is considered that TiN capping on stacked silicide does not degrade electrical characteristics of Schottky diode.

\[\text{Figure 5.4 Fabrication processes of Schottky diodes with or without TiN capping.}\]
Figure 5.5 The Schottky diode J-V characteristics of stacked silicide with or without TiN capping. J-V characteristics remain ideal characteristics even with TiN capping.

Figure 5.6 $\Phi_{bn}$ and n-factor of stacked silicide with or without TiN capping on annealing temperature. Scatter of $\Phi_{bn}$ and n-factor with TiN capping is suppressed compared with without TiN capping.
5.4 Conclusion

Electrical characteristics of Schottky diodes using Ni silicides are investigated. Schottky diode characteristics of conventional Ni silicides show the reverse leakage current and the variation of $\phi_{Bn}$ and $n$-factor due to excess silicidation at the electrode periphery. On the other hand, those of stacked silicide are achieved ideal diode characteristics and robust $\phi_{Bn}$ and $n$-factor because of formation of an atomically flat interface including the electrode periphery. Moreover, more robust $\phi_{Bn}$ and $n$-factor even with ideal $J-V$ characteristics are obtained by TiN capping on stacked silicide.

References


Chapter 6

Schottky barrier height modulation

6.1 Introduction

6.2 $\phi_{Bn}$ modulation with stacked silicidation process

6.3 $\phi_{Bn}$ controllability by impurity incorporation

6.4 Conclusion

References
Chapter 6. Schottky barrier height modulation

6.1 Introduction

As described in chapter 1, it is necessary to modulate $\phi_B$ to achieve SB-FET with high performance [6.1]. $\phi_B$ modulation has been achieved by dopant segregation using ion implantation, however, there are some issues [6.2, 6.3]. Thereby, it is proposed that the method of impurity incorporation without ion implantation, and $\phi_B$ modulation by the impurity incorporation is examined.

In this study, P and B are used as impurity. It is reported that $\phi_{Bn}$ becomes small value by P and $\phi_{Bn}$ becomes large value by B [6.4, 6.5]. The method of impurity incorporation with stacked silicidation process is to deposit Ni$_3$P or B by sputtering. For B incorporation, pure B target is used for sputtering, whereas for P case, a 0.68-nm-thick Ni$_3$P layer is deposited instead of the first 0.5-nm-thick Ni layer as shown in figure 6.1. The number of Ni atoms in 0.68-nm-thick-Ni$_3$P layer equals that of 0.5-nm-thick Ni layer. This method can incorporate impurity without ion implantation, moreover, the control of impurity position is expected because stacked silicidation process can suppress interface reaction.

In this chapter, interface reaction with impurity incorporation at the interface, impurity profiles and electrical characteristics with impurity incorporation are investigated. Furthermore, $\phi_{Bn}$ modulation depending on impurity position and amount are examined.
Chapter 6. Schottky barrier height modulation

Figure 6.1 Schematic illustration of stacked silicidation process with impurity incorporation. P is incorporated at the interface by 0.68-nm-thick Ni$_3$P deposition instead of the first Ni layer. B is incorporated at the interface.
Chapter 6. Schottky barrier height modulation

6.2 $\phi_{Bn}$ modulation with stacked silicidation process

6.2.1 Interface reaction of impurity incorporation

As shown in figure 6.2, TEM images of silicide/Si interface formed from Ni/Si stacked silicidation process incorporated P (Figure 6.2(a)) and B (Figure 6.2(b)) at the interface at annealed 500 °C for 1 min in N$_2$ ambient. TEM images revealed no change in the thickness and atomically flat interface and surface. Even with impurity incorporation, the interface reaction with stacked silicidation process is also maintained.

![Figure 6.2 TEM images of stacked silicidation process incorporated (a) P and (b) B at the interface after annealing at 500 °C. Even with impurity incorporation, atomically flat interface and surface are maintained.](image-url)
6.2.2 SIMS impurity profiles

Figure 6.3 shows SIMS profiles of (a) P and (b) B before and after annealing when impurities incorporated at interface. Although some of the impurities diffused into silicide layer, significant amount of them remained at the silicide/Si interface which is initial incorporated position. Therefore, impurity position can be controlled by stacked silicidation process because stacked silicidation process can be suppressed interface reaction.

![SIMS profiles of P and B before and after annealing](image)

*Figure 6.3* SIMS profiles of (a) P and (b) B before and after annealing. Although some of the impurities diffused into silicide layer, significant amount of them remained at silicide/Si interface.
6.2.3 $\phi_{Bn}$ modulation by impurity incorporation

Figure 6.4 shows the $J$-$V$ characteristics of the stacked silicide Schottky diodes with P and B incorporation annealed at 500 °C. $\phi_{Bn}$ can be effectively modulated by placing P or B atoms at the interface, where the initial $\phi_{Bn}$ of 0.63 eV was modulated to ohmic and 0.68 eV, respectively. Furthermore, robust $\phi_{Bn}$ and $n$-factor were obtained at wide process window as shown in figure 6.5.

**Figure 6.4** $J$-$V$ characteristics of stacked silicide with P and B incorporation annealed at 500 °C. Successful effectively $\phi_{Bn}$ shift by P or B incorporation with stacked silicidation process.
Figure 6.5 $\Phi_{Bn}$ and n-factor of the diodes extracted from J-V characteristics depending on annealing temperature. Ohmic characteristic and larger $\Phi_{Bn}$ is realized by incorporating P and B, respectively. $\Phi_{Bn}$ and n-factor were stable up to 700 °C.
6.3 \( \phi_{Bn} \) controllability by impurity incorporation

6.3.1 Annealing conditions dependent \( J-V \) characteristics with impurity at the interface

Figure 6.6 shows \( J-V \) characteristics of stacked silicide incorporated P at the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 min and 30 min. As shown in figure 6.6(a), annealed at 400 °C, large current density can be obtained by annealing for 30 min compared to the sample annealed for 1 min. On the other hand, current density is almost unchanged annealed 500 °C and 600 °C independent of annealing time. Therefore, large current density can be achieved by long time or high temperature annealing.
Figure 6.6 J-V characteristics of stacked silicide incorporated P at the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 and 30 min. Ohmic characteristics can be achieved by long time or high temperature annealing.

6.3.2 Impurity position dependent J-V characteristics

As shown in figure 6.6, when P is incorporated at the interface, ohmic characteristics can be obtained by annealing at 500 °C for 1min. In this chapter, the impurity position dependent J-V characteristics investigated. Figure 6.7 shows J-V characteristics of stacked silicide depending on the position of P incorporation annealed at 500 °C for 1 min. When the position of P incorporation gradually comes
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Figure 6.7 J-V characteristics of stacked silicide dependent the position of P incorporation annealed at 500 °C. When the position of P incorporation gradually comes close to the interface, small $\phi_{Bn}$ and ohmic characteristic are obtained.

Therefore, it is considered that P which exists at interface is the key to modulate $\phi_{Bn}$.

6.3.3 Annealing conditions dependent J-V characteristics with impurity far from the interface

Figure 6.8 shows J-V characteristics of stacked silicide incorporated P far from the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 min and 30 min. As shown in figure 6.8(a), which is annealed at 400 °C, J-V characteristics are Schottky characteristics both of annealing for 1min and 30 min, however, $\phi_{Bn}$ of 30 min is smaller than that of 1 min. On the other hand, Ohmic characteristics are obtained by annealing for 30 min at 500 °C and 600 °C as shown in figure 6.8(b) and...
(c), respectively. Therefore, it is realized that $\phi_{Bn}$ modulation and ohmic characteristics can be achieved even with the position of P incorporation far from the interface because P atoms are diffused by high temperature or long time annealing and arrive at interface as shown figure 6.8(d).

**Figure 6.8** J-V characteristics of stacked silicide incorporated P far from the interface annealed at (a) 400 °C, (b) 500 °C and (c) 600 °C for 1 min and 30 min. (d) the image of P diffusion by annealing. Ohmic characteristics can be achieved by long time or high temperature annealing.
Finally, electrical characteristics of P incorporation depending on incorporated position and annealing temperature and time are summarized as shown in table 6.1, and here the origin of $\phi_{Bn}$ modulation is discussed. One of the origins is the formation of a dipole which is generated from dopant at the silicide/Si interface as shown in figure 6.9 [6.4]. The other of the origins is the change of silicide work function by impurity doping into silicide [6.5]. As the result of table 6.1, it is considered that the origin of $\phi_{Bn}$ modulation is not so much the change of silicide work function as the presence of impurities at the interface in using stacked silicidation process.

**Table 6.1 Electrical characteristics of P incorporation depending on incorporated position and annealing temperature and time**

<table>
<thead>
<tr>
<th>Sample</th>
<th>Annealing temperature (°C)</th>
<th>Annealing time (min)</th>
<th>Ohmic</th>
<th>Schottky</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>300</td>
<td>0 1 20 30</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>400</td>
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<td>600</td>
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<td></td>
</tr>
<tr>
<td>P3</td>
<td>300</td>
<td>0 1 20 30</td>
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</tr>
<tr>
<td></td>
<td>400</td>
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<td>600</td>
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<tr>
<td>P5</td>
<td>300</td>
<td>0 1 20 30</td>
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<td>400</td>
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<tr>
<td>P7</td>
<td>300</td>
<td>0 1 20 30</td>
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<td>600</td>
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</tbody>
</table>
6.3.4 Impurity amount dependent diode characteristics

In the previous chapters, it is investigated that impurities which exist at the interface cause $\phi_{\text{Bn}}$ modulation. In this chapter, it is stated that impurity amount dependent diode characteristics. Figure 6.10 shows $J$-$V$ characteristics of stacked silicide dependent the amount of B incorporation at the interface annealed at 500 °C for 1 min. Reverse currents decrease with increasing the amount of B incorporation at the interface compared to control sample. In addition, figure 6.11 shows $\phi_{\text{Bn}}$ of the diodes extracted from $J$-$V$ characteristics depending on the amount of B incorporation at the interface. Large $\phi_{\text{Bn}}$ modulation can be achieved by increasing the amount of B incorporation at the interface. Therefore, effective $\phi_{\text{Bn}}$ modulation is controlled by controlling the amount of B atoms which exist at interface.
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**Figure 6.10** J-V characteristics of stacked silicide dependent the amount of B incorporation at the interface annealed at 500 °C. \( \Phi_{\text{Bn}} \) can be controlled by the amount of B incorporation.

**Figure 6.11** \( \Phi_{\text{Bn}} \) of the diodes extracted from J-V characteristics depending on the amount of B incorporation at the interface. Large \( \Phi_{\text{Bn}} \) modulation can be achieved by increasing the amount of B incorporation at the interface.
6.4 Conclusion

The effect of impurity incorporation on $\phi_{Bn}$ is investigated. At first, even with impurity incorporation, the interface reaction with stacked silicidation process is also maintained. Second, it is obtained that the significant amount of the impurities remained at the initial incorporated position due to suppression of interface reaction. Further, effective $\phi_{Bn}$ modulation is achieved by impurity incorporation at interface with stacked silicidation process. Moreover, impurity incorporation position and amount dependent $\phi_{Bn}$ modulation is examined. As a result, the main fact of $\phi_{Bn}$ modulation is that impurity exists at the interface. Additionally, it is found that $\phi_{Bn}$ modulation is controlled by controlling the amount of impurity which exists at interface.
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References


Chapter 7 Demonstration of Schottky barrier S/D FET with barrier height modulation

7.1 Introduction
7.2 Fabrication process
7.3 Electrical characteristics for SB-FET
7.4 Conclusion
References
Chapter 7 Demonstration of Schottky barrier S/D FET with barrier height modulation

7.1 Introduction

As described above, it is considered that stacked silicidation process with impurity incorporation is the key to achieve the future scaled 3D SB-FETs. In this chapter, SB-FET using stacked silicidation process with $\phi_{Bn}$ modulation is demonstrated. Then, the effect of $\phi_{Bn}$ modulation on the device characteristics is investigated.

7.2 Fabrication process

SB-FET using the stacked silicide with B or P incorporation at S/D was fabricated on a SOI wafer as shown in figure 7.1. After SOI patterning, gate oxide was formed by thermal oxidation in 1000 °C. To form S/D, stacked silicidation process with impurity incorporation was performed. SiO$_2$ was deposited by plasma CVD (TEOS) owing to passivation. After gate metal deposition and etching, Al was deposited as contact by vacuum evaporation. Finally, annealing was performed at 500 °C in forming gas (F.G.) (N$_2$:H$_2$=97:3), so that the effect of terminating the dangling bonds with H$^+$ at the interface of oxide/Si substrate is obtained. Therefore, this process can achieve a process temperature below 500 °C, except for the gate oxidation.
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Fabrication process

- SOI patterning
- Gate oxide (1000 °C)
- Stacked silicide for S/D (with B or P)
- TEOS (200 °C)
- Gate metal depo./etch.
- Contact
- FG anneal (500 °C)

The process temperature was set below 500 °C except for gate oxide formation.

Figure 7.1 Fabrication process of Schottky S/D FET.

7.3 Electrical characteristics for SB-FET

$I_d-V_g$ characteristics are shown in figure 7.2. B incorporated device showed ambipolar characteristics. On the other hand, P incorporated device can suppress ambipolar characteristics with lower $\phi_{Bn}$, moreover, improvement in the on-current ($V_g=V_d=3V$) also supports the $\phi_{Bn}$ modulating. The schematic illustration of band diagram for operation is shown in figure 7.3 [7.1, 7.2, 7.3].
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Figure 7.2 $I_d$-$V_g$ characteristics of SB-FET with $\phi_{bn}$ modulated stacked silicide. $P$ incorporated device shows larger on-current with suppressed ambipolar characteristics.

Figure 7.3 Band diagram of the SB-FET at (a) on and (b) off-states with different $\phi_{bn}$. Ambipolar characteristics are suppressed and larger on-current is obtained by modulating $\phi_{bn}$ to smaller value.
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7.4 Conclusion

SB-FETs using stacked silicidation process with B or P incorporation at S/D were fabricated below 500 °C except for the gate oxidation. The effect of $\phi_{Bn}$ modulation on the device characteristics is confirmed. It is considered that ambipolar characteristics are suppressed and on-current is improved because $\phi_{Bn}$ is modulated to small value. It is necessary for high performance to modulate $\phi_{Bn}$ to smaller value.

References


Chapter 8
Conclusions
In this thesis, a novel stacked silicidation process is proposed for future scaled 3D devices. In this chapter, the studies are summarized below.

(i) Thickness dependent characteristics of Ni silicides (chapter 3)

Ni silicides, reactively formed by 3.0-nm-thick Ni, have shown a stable sheet resistance, flat morphology against annealing temperature up to 800 °C compared to those formed with thicker Ni film. These properties are owing to the formation of stable NiSi$_2$ phase at a temperature as low as 500 °C.

(ii) Ni silicides using stacked silicidation process (chapter 4)

In order to achieve the control of interface reaction and stable composition and morphology at wide temperature range, stacked silicidation process has been investigated. It is realized that an atomically flat interface and surface are formed before and after annealing and Ni atoms encroachment into Si Fin is suppressed completely. Further, it is achieved that NiSi$_2$ which is formed by staked silicidation process is stable composition and morphology at wide temperature range. Moreover, it is accomplished that the $\rho_{sh}$ of stacked silicide on various substrates is stable at wide temperature range. On the other hand, extension of stacked silicidation process for Ti has been examined. It is considered that the formation of the most stable silicide phase, such as NiSi$_2$, can be formed by stacked silicidation process at low temperature is unique characteristics of Ni silicide.

(iii) Electrical characteristics of Ni silicide Schottky diodes (chapter 5)

Electrical characteristics of Schottky diodes using Ni silicides are investigated. Schottky diode characteristics of conventional Ni silicide show the
reverse leakage current and the variation of $\phi_{Bn}$ and $n$-factor due to excess silicidation at the electrode periphery. On the other hand, those of stacked silicide are achieved ideal diode characteristics and robust $\phi_{Bn}$ and $n$-factor because of formation of an atomically flat interface including the electrode periphery.

(iv) Schottky barrier height modulation (chapter 6)

The effect of impurity incorporation on $\phi_{Bn}$ is investigated. At first, even with impurity incorporation, the interface reaction with stacked silicidation process is also maintained. Second, impurity position can be controlled by stacked silicidation process because significant amount of the impurities remained at the silicide/Si interface. Further, $\phi_{Bn}$ modulation is achieved by impurity incorporation at interface with stacked silicidation process. Moreover, impurity incorporation position and amount dependent $\phi_{Bn}$ modulation is examined. As a result, the main fact of $\phi_{Bn}$ modulation is that impurity exists at the interface. Additionally, it is found that $\phi_{Bn}$ modulation is controlled by controlling the amount of impurity which exists at interface.

(v) Demonstration of Schottky barrier S/D FET with barrier height modulation (chapter 7)

SB-FETs using stacked silicidation process with B or P incorporation at S/D were fabricated below 500 °C except for the gate oxidation. The effect of $\phi_{Bn}$ modulation on device characteristics is confirmed. It is considered that ambipolar characteristics are suppressed and on-current is improved because $\phi_{Bn}$ is modulated to small value.
Chapter 8. Conclusions

Publications and Presentations

Publications


Chapter 8. Conclusions

Invited Talk

International Presentations


Chapter 8. Conclusions


Domestic Presentations


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