Electrical characterization of Ni Silicide formed by Ni reaction with scaled Si nanowires

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Abstract of Master Thesis

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Nickel salicide (self-aligned silicide) have been widely used in ULSIs to reduce the parasitic resistance at source and drain regions of MOSFETs. This technology may be continuously used for highly scaled device such as Si nanowire field effect transistors (Si NW FETs) and FinFETs. As source and drain regions become extremely narrow and the amount of Si reacting with Ni is limited in these structures, this may lead to the silicide different from the case of the silicidation of the bulk silicon. On the other hand, it has been reported that the narrow metal lines, for example copper narrow lines, suffer from the increase in effective resistivity due to higher probability of the surface scattering of the electrons. In this study, in order to apply Ni silicide to high scale
device, the impact of size effect in Ni silicide nanowires is investigated. Silicidation was performed using Ni thin films and Si nanowire with the line width down to 10 nm. The Ni silicide line width is in the range from 80 nm to 15 nm. At first, the dependence of resistivity on the line width was obtained. Low and constant resistivity was obtained for width larger than 35 nm. However, drastic increases in the resistivity were observed for nanowire line width smaller than 35 nm. In order to investigate the phase of Ni silicide with temperature, the resistance was measured at the temperature in the range from 25 °C to 100 °C. Temperature coefficient of resistance was estimated to be 0.0013 K⁻¹. It was found that Ni₂Si was formed for all widths. Another cause for drastic increases in the resistivity of nanowires at around the width of 35 nm may be the roughness in line width. In order to evaluate the influence of the roughness in line width on the resistivity, the simple model of roughness in line width was compared with experimentally obtained resistivity. Roughness in line width cannot be the major reason for the drastic increase in resistivity. Secondly, the increase in resistivity was discussed due to the size effect. From the mean free path of 2 nm in Ni₂Si, surface scattering cannot be the cause of the increase in resistivity. Therefore, the grain boundary scattering was investigated. The grain existed in nanowire with the line width of 62 nm. It is considered that the cause of increase in resistivity of line width smaller than 35 nm can be the impact of grain boundary scattering.
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1.1 Background of This Study

Nowadays, Ultra-Large Scale Integrated circuits (ULSIs) constructed from complementally metal-oxide-semiconductor (CMOS) structures, are really indispensable components for our human society. Obviously, almost all the human activities, such as living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS ULSI operation. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software’s required for the integrated circuits. The continuous progress of CMOS technologies in terms of high-performance operation and low power consumption have been and will be very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required. Therefore the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO₂ gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the ‘cooling of the earth’ in two ways. One is direct contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by
so called ‘Green IT’ procedure. This can be done by the development of low power and high performance CMOS devices used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point of view, as well as from the global economic point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 16 to 64 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.
1.2 CMOS ultimate scaling

It is well known that the progress of CMOS ULSI has been accomplished by the downsizing of metal-oxide-semiconductor field effect transistors (MOSFETs) [1.1]. In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970’s. It was fortunate, however, it has been proven that those forecasts are not true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. There is less than ten years until 2020, but there is no sufficiently clear image for the world after CMOS reaches its scaling limit.

It is expected that about 5 nm is the limit of the downsizing of the gate length, because there are four main reasons; A) Difficulty in off-current suppression, B) Difficulty in the on-current increase, C) Difficulty in the increase of MOSFETs speed, D) Production and development cost increase.

A. Difficulty in off-current suppression

With decrease in gate length, Short channel effect occurs [1.2]. Thus, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.
B. Difficulty in the on-current increase

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

C. Difficulty in the increase of MOSFETs speed

One of the scaling merits is to reduce the gate capacitance, $C_g$, because the switching time of MOSFETs is defined by $C_g V_{dd}/I_d$, where $I_d$ is the drain on-current and $V_{dd}$ is power voltage. However, $C_g$ will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain areas are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.
E. Possible solution after that

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called ‘beyond CMOS’ or ‘Post Si’ new devices, which are believed to really replace CMOS transistors used for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with ‘More Moore’ approach with combining that of ‘More than Moore’. Then, what is ‘More Moore’ approach after we reached the downsizing limit or with no more decrease in gate length? Because the number of the transistors in a chip is limited by the power consumption, we could continue the ‘More Moore’ law for certain period by replacing current planar CMOS transistors by three dimensional structure MOSFETs. Furthermore, nanowire and tube MOSFET suppresses off-leakage current and increase of on-current under low voltage could be realized because of having multigate, quasi-one-dimensional conduction and multi-quantum channel per wire/tube. Figure 1.1 shows our roadmap for CMOS transistors after 2020.
Figure 1.1 Roadmap for CMOS transistors.
1.3 Three Dimensional Structure Devices

1.3.1 Multigate Device

Planar transistors have been the core of integrated circuits for several decades, during which the size of the individual transistors has steadily decreased. In MOSFET performance can be basically improved by downsizing. However, "off-state" leakage current increases when the channel length is the same order of magnitude as the depletion-layer widths of the source and drain junction. As the channel length is reduced, both the operation speed and the number of components per chip increase. It is the phenomenon known as the short-channel effect.

Therefore, it is expected to replace the conventional planar structure by three dimensional structures. The nonplanar devices have multiple channels surrounded by multi gate and effective suppression of "off-state" leakage current. Current in the "on-state" is also enhanced because of multi gate. Moreover, Improvement of on-state current is expected by using nanowire which has ballistic conduction from quasi-one-dimensional structure. Figure 1.2 shows the typical device of the three dimensional structure.

![Figure 1.2 Schematic illustrations of three dimensional structure devices.](image)

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1.3.2 FinFET

FinFET is a device of the typical three dimensional structures and has the structure which surrounds Si of fin structure – the shape such as extremely narrow fish tail – by a gate. Figure 1.3 shows schematic illustration of the FinFET. It has advantage on suppressing short-channel effect and easiness of fabrication process by using silicon on insulator (SOI) substrates.

As the variants, there is a FinFET owing gate architecture called Tri-gate. It has a lot of gate surface area. Thus, there's a lot more of inversion layer for current to flow through. This makes the difference between the transistor's "on" and "off" states much larger, which means that the transistor can switch between states much faster while still producing a clear string of ons and offs. Tri-gate transistors reduce leakage and consume far less power than current transistors. Currently, Intel has produced a FinFET which has Tri-gate and gate length 22 nm [1.3].

Figure 1.3 Schematic illustrations of FinFET with Double-Gate and Tri-Gate structures.
1.3.3 Silicon Nanowire Field Effect Transistor

Si nanowire FET is considered as one of the promising candidates for further extending the three dimensional device downsizing, owing to its gate-all-around (GAA) of which enables better gate control capability than planar transistors. Figures 1.4 show schematic image of Si NW FET with GAA structure. Moreover, advantage in ballistic conduction from quasi-one-dimensional (Q1D) structure can be achieved [1.4]. Therefore, high $I_{on}/I_{off}$ ratio can be achieved with sufficient low power consumption. Figure 1.5 shows comparison of the requirement to the bulk Si, the ultra-thin body fully depleted (UTB FD) SOI and the double-gate (DG) MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes [1.4-6]. Si NW FETs have already been obtained higher $I_{on}/I_{off}$ ratio than any planer transistors.

Si NW FET has been fabricated by several techniques including, Si Fins are patterned by lithography and etching followed by the oxidation (Figure 1.6 (a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si NW with better controllability of the size of the wire (Figure 1.6 (b) shows Bottom-up method) [1.7].

**Figures 1.4** Schematics image of Si Nanowire FETs with gate-all-around structure.
Figure 1.5 Comparison of the requirement to the bulk Si, UTB FD SOI, and DG MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes.

Figure 1.6 Fabrication methods of Si nanowire FET by (a) Top-down and (b) Bottom-up [1.7].
1.4 Nickel Silicidation for Si Nanowire

1.4.1 Nickel Silicide

In CMOS fabrication, Salicide (self-align silicide) often has been used for the contacts of source/drain regions and gate electrodes [1.8]. There are many kinds of metals - Ni, Ti, Co, Mo, W, Pt and so on - for silicides. Especially, Ni-, Co-, and Ti-silicides with low resistivity have been studied for a long time. Though TiSi$_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co - silicides are used in 100 nm - or smaller generations. Although CoSi$_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices [1.9]. In addition to its relatively low resistivity and less contaminated interface can be obtained owing to reactively formed interface enabling to suppress the variability. In particular, Ni is a promised material of metal-silicide, because of its relatively low resistivity, relatively low temperature and relatively small Si consumption during the formation for application to nano-scale structure [1.10-12]. The study on Ni silicide started to become an active research area in the 1970’s and the silicide technology in MOSFET fabrication process since 1980's [1.13]. Figure 1.7 shows the progress of the silicide materials. Table 1.1 is previously reported fundamental data of Ni silicide formation on bulk Si [1.10, 1.14-15]. And, Fig. 1.8 [1.16] and 1.9 [1.17] show the reaction temperature dependent Ni silicide phase which is mainly appeared in bulk Si.
Figures 1.7 Progress of silicide materials which have been used in CMOS fabrications so far [1.8].

Table 1.1 Fundamental dates which show phase, resistivity, crystal structure, density and consumption of Ni silicide formed on bulk Si [1.10, 1.14-15].

<table>
<thead>
<tr>
<th>Phase</th>
<th>Resistivity (µΩ-cm)</th>
<th>Crystal structure</th>
<th>Density (g/cm³)</th>
<th>T_{silicide}/T_{Ni}</th>
<th>Si consumption / T_{Ni}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>7-10</td>
<td>Cubic</td>
<td>8.91</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Ni₃Si</td>
<td>80-90</td>
<td>Cubic</td>
<td>7.87</td>
<td>1.31</td>
<td>0.61</td>
</tr>
<tr>
<td>Ni₃Si₁₂</td>
<td>90-150</td>
<td>Hexagonal</td>
<td>7.56</td>
<td>1.4</td>
<td>0.71</td>
</tr>
<tr>
<td>Ni₂Si</td>
<td>24-30</td>
<td>Orthorhombic</td>
<td>7.51</td>
<td>1.47</td>
<td>0.91</td>
</tr>
<tr>
<td>Ni₃Si₂</td>
<td>60-70</td>
<td>Orthorhombic</td>
<td>6.71</td>
<td>1.75</td>
<td>1.22</td>
</tr>
<tr>
<td>NiSi</td>
<td>10.5-18</td>
<td>Orthorhombic</td>
<td>5.97</td>
<td>2.20</td>
<td>1.83</td>
</tr>
<tr>
<td>NiSi₂</td>
<td>34-50</td>
<td>Cubic</td>
<td>4.80</td>
<td>3.61</td>
<td>3.66</td>
</tr>
<tr>
<td>Si</td>
<td>Dopant dependent</td>
<td>Cubic</td>
<td>2.33</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Figures 1.8 Silicidation temperature dependent sheet resistances and the appeared Ni silicide phase on bulk Si. Deposited Ni thickness is 12 nm [1.16].

Figures 1.9 Schematic image of silicidation temperature dependent mainly appeared Ni silicide phase on bulk Si [1.17].
1.4.2 Application to FinFET and Si Nanowire FET

As Nickel silicide formed at relatively low temperature with relatively small Si consumption, Ni salicide (self-aligned silicide) becomes almost an indispensable technique for conventional MOSFET. Moreover, because the resistances of source, drain, and gate electrode increase with more downsizing, it is also expected to apply Ni silicide to the three dimensional device such as FinFET and Si NW FET.

The high performance FinFET with has been reported previously by using Ni silicide formed on source and drain regions [1.18]. Furthermore, Si NW FETs with reduced the parasitic resistance of the source and drain regions by using Ni silicide have also been reported [1.19]. Figure 1.10 shows TEM image of FinFET and Si NW FET which has Ni silicide formed on source and drain regions.

Therefore, considering the more scaling, it is required to form low resistance Ni silicide on Si nanowire.

(a) FinFET 
(b) Si NW FET

Figures 1.10 TEM image of the reported (a) FinFET [1.18] and (b) Si NW FET fabricated by Ni salicide of source and drain regions [1.19].
1.5 Issues in Nickel Silicidation of Si Nanowire

1.5.1 Reaction between Silicon Nanowire and Nickel

Nowadays, many researches have been performed in Ni silicide formed on bulk Si. Thus, numerous reports also make on the conditions of Ni silicidation such as formed temperature and Ni thickness dependence. Figure 1.11 shows the conditions of Ni silicide phase formed on bulk Si.

However, it is inferred that Ni silicidation for Si nanowire is different from the case of conventional Ni silicidation for bulk Si, considering the amount of Si reacting with Ni is limited in Si nanowire. Furthermore, Ni-rich silicide has also been reported in Ni silicide formed on Si nanowire [1.20-21].

Therefore, there is the issue that low-resistivity silicide such as NiSi may be formed easily, because Ni silicidation of Si nanowire is not the same as the case of bulk Si.

Figures 1.11 A schematic image of phases of Ni silicides formed on planar silicon. Ni silicidation depends on the initial Ni thickness and annealing temperature.
1.5.2 Concern about Resistance Increase of Ni Silicide Nanowire

As Ni silicide is a metal, it has obviously low resistivity. Especially, resistivity of NiSi is 18 µΩ-cm. However, as the size of metal becomes smaller, there is issue that the resistance of metal increases dramatically by the size effect.

There are many studies on the size effect in copper interconnects [1.22]. Causing the increase in resistance is due to surface scattering of electron. This effect is associated with the mean free path of the electrons. Figure 1.12 shows the relationship between the resistivity and the width of nanowire. As the copper becomes narrow, the resistivity increases dramatically. The surface scattering is also reported other metal such as Au, Ni, Al, and Ag.

In addition, resistivity increases by the grain boundary scattering. This effect is caused by the scattering of electrons on the grain boundaries. The resistivity increases with decreasing this grain size.

Therefore, it is a concern that the resistivity of Ni-silicide-nanowire increases by the size effect as surface scattering and grain boundary scattering.

![Figure 1.12](image)

**Figures 1.12** Line width of copper nanowire dependent its resistivity. The increase of resistivity is caused by size effect [1.22].
1.6 Purpose of This Thesis

As discussed in previous chapter, Fabrication of the high performance device with three dimensional structures is expected by the application of silicide used as contact of the conventional planar MOSFET to the multi-gate device such as FinFET and Si NW FET. However, Ni silicides formed on these narrow lines of silicon is considered to be different from the conventional silicidation for bulk Si. Moreover, the increase in resistance of Ni silicide nanowire is a concern by size effect as reported in nanowire of Cu, Au, and other metal.

In this thesis, in order to apply Ni silicide nanowire as the contact with low resistance, the resistance of Ni silicide nanowires is evaluated and the impact of these effects is investigate.

In chapter 3, Ni silicide nanowires are formed on scaled Si nanowires with the width of 10 nm. Furthermore, the electrical characteristic of Ni silicide nanowires is evaluated.

In chapter 4, the size effect of Ni silicide nanowires is investigated from the electrical properties obtained in chapter 3.

Finally, chapter 5 summarizes this study.
References


Chapter 2
Fabrication and Characterization Method

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2.2.8 Lift-off technique for electrode formation

2.3 Measurement and observation methods

2.3.1 Four-point Probe Method
2.3.2 Scanning Electron Microscope (SEM)
2.1 Experimental Procedure

Figure 2.1 shows the flow of fabrication process. Silicon nanowire patterns were fabricated on a 30-nm-thick silicon-on-insulator (SOI) wafer. After cleaning in SPM (H$_2$SO$_4$ and H$_2$O$_2$) solution followed by the treatment in HF, Ni films were deposited by RF magnetron sputtering. Next, Rapid thermal annealing (RTA) at 500 °C was performed in nitrogen ambient for 5 min. Unreacted Ni was removed by SPM. In order to form electrodes on the nanowire, Metal films were deposited. Wet etching was used for the patterning of the electrodes. However, there is the problem in using wet etching. Therefore, Lift-off technique was used for the patterning of the electrodes. Finally, Ni silicide nanowire was observed and measurement resistance was performed.
2.2 Experimental Details and Principle

2.2.1 Fabrication of Substrate with Si Nanowires
Si nanowires ranging from 10 to 80 nm in width were fabricated on a (100)-oriented SOI wafer with an SOI layer of 30 nm thick by photolithography and dry-etching process. The direction of the line was aligned to <110>.

2.2.2 Substrate Cleaning Process
At first, the experiments using high quality thin films require ultra clean surface without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 M$\Omega \cdot$cm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 M$\Omega \cdot$cm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H$_2$SO$_4$) and hydrogen peroxide (H$_2$O$_2$) (H$_2$SO$_4$:H$_2$O$_2$=4:1), was performed to remove any organic material and metallic impurities. After dipping in the chemicals to clean the substrate, the clean wafer was dipped in DI water to rinse away the chemicals. The process dipping the wafer in DI water after dipping the wafer in chemicals with each cycle is important. Then, the native or chemical oxide was removed by 1% diluted hydrofluoric acid (HF). Finally, the cleaned substrate was loaded to the oxidation chamber to deposit immediately after it was dried by air gun.
2.2.3 Photolithography Process

Photolithography (or "optical lithography") is a process used in microfabrication to selectively remove parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photoresist (Figure 2.2). It is used because it can create extremely small patterns (down to a few tens of nanometers in size), it affords exact control over the shape and size of the objects it creates. In case of this study, photolithography was used for the method to etch only parts of unwanted pattern, form electrodes patterning.

The process flow and a photo of the photolithography apparatus used throughout this study are shown in Fig. 2.3. The apparatus is MJB4 of Karl Süss contact-type mask aligner. At first, the substrates were coated with positive type photoresists by spin-coating method. The thicker photoresist called S1818 and thinner one called S1805 were used. Secondly, the coated photoresists were baked at 115 °C for over 5 min by using electrical hotplate. Then, spin-coated photoresist layers were exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. The exposure duration was set to 1.5 sec and 3.8 sec for thinner photoresist and thicker one, respectively. Finally, exposed wafers were developed using the specified tetra-methyl-ammonium-hydroxide (TMAH) developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 1~2 minute.
Figure 2.2 Schematic image of photo lithography by development for photo resist after exposure.

Figure 2.3 The process flow and the photo of photolithography apparatus.
2.2.3 Dry Etching by RIE

Reactive Ion Etching (RIE) was performed to eliminate only parts of required Si nanowire. RIE is one of the dry etching methods. The gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important.

Si combined with F- and forms Si-F. Si-F is evaporated and eliminated from the sample. Therefore, in this experiment, SF₆ is used as etching gas for Si etching. On the other hand, photoresist, which is attached to the sample by the photolithography, reacts with not SF₆ but O₂ to be eliminated. This phenomenon is called ashing. O₂ is used as the etching gas of the resist. Fig.2.4 shows the schematic illustration of the RIE process.

![Schematic illustration of Reactive Ion Etching process](image)

Fig.2.4 Schematic illustrations of the Reactive Ion Etching process.
2.2.4 RF Magnetron-Sputtering Process

After eliminating only parts of required Si nanowire by RIE, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive layer) and Ni/Si were formed by an ultra-high-vacuum (UHV) sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra-thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the “target,” composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

In this study, Ni films with thickness of 50 nm were deposited on the substrate with Si nanowire by RF magnetron-sputtering in argon ambient. As RF magnetron-sputtering system, UHV Multi Target Sputtering System ES-350SU shown in Fig. 2.5 was used and its schematic structure is shown in Fig. 2.6. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2.1 is attached for reference.

In this study, Ni with thickness of 50 nm is deposited on the substrate with Si nanowires.
Figure 2.5 Photo of UHV Multi Target Sputtering System ES-350SU.

Figure 2.6 Schematic internal structure of UHV sputtering system.
<table>
<thead>
<tr>
<th>Growth chamber</th>
<th>1. Ultimate pressure</th>
<th>1.5 x 10^{-6}Pa</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Substrate size</td>
<td>2 inch in diameter</td>
<td></td>
</tr>
<tr>
<td>3. Heating temperature</td>
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<td>4. Heater type</td>
<td>Lamp type heater</td>
<td></td>
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<tr>
<td>5. Target</td>
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<tr>
<td>Load lock chamber</td>
<td>6. Vacuum pumps</td>
<td>TMP 500L/sec and RP 250L/min</td>
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<tr>
<td></td>
<td>7. Ultimate pressure</td>
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<tr>
<td></td>
<td>8. Vacuum pumps</td>
<td>TMP 60L/sec and RP 90L/min</td>
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<tr>
<td></td>
<td>9. Substrate holder with cooling function / Substrate holder with heating function / Cleaning function / Radical beam source</td>
<td></td>
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</tbody>
</table>
2.2.5 Thermal Rapid Annealing Process

After formation of thin films of Ni/Si, Ni/M/Si, or M/Ni/Si by UHV sputtering system, these structures were transferred to annealing furnace to perform thermal process. The thermal process leads to the reaction between Ni and Si, or among Ni, M, and Si.

In this study, the thermal rapid annealing (RTA) process was performed for Ni films /Si nanowire and led to Ni silicidation for Si nanowire. The silicidation was performed by using infrared image furnace in nitrogen ambient. The annealing temperature and time were 500 °C and 5 min.

The equipment for annealing used in this study is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 2.7 is the photo of the infrared image furnace, whose schematic illustration was shown in Fig. 2.8. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon coated by SiC. The heating temperature was controlled by thermocouple feedback.

In this study, after the silicidation, the unreacted Ni was removed by dipping the substrate in a heated mixed solution of H$_2$SO$_4$ and H$_2$O$_2$ at 150 °C for over 10 min.
Figure 2.7 Photo of infrared image furnace.

Figure 2.8 Schematic internal configuration of infrared image furnace.
2.2.6 The Electrode Formation Method with the Problem

2.1.6.1 Vacuum Evaporation for Al Deposition

Before patterning the electrodes by wet etching, Al films are deposited by using bell-jar type thermal evaporation as illustrates in Fig. 2.9.

This system utilized a turbo molecular pump (TMP) to achieve background pressure up to $1.0 \times 10^{-5}$ Pa prior to Al evaporation. Highly pure Al source is set on tungsten (W) boat and heated up to boiling point of Al by joule heating.

However, melting point of W is higher than boiling point of Al, W boat doesn’t melt. Chamber pressure during evaporation is $2 \times 10^{-5} - 5 \times 10^{-5}$ Pa. A DC current about 60A was used to evaporate Al.

Figure 2.9 Schematic illustration of the structure of Bell Jar.
2.2.6.2 Wet Etching for Electrode Formation and the Problem

Wet etching is used widely in semiconductor process. For example, SiO2 is selectively etched by BHF.

In this study, Al is selectively etched by using of phosphoric acid (H_3PO_4), deionized water (DI H_2O), nitric acid (HNO_3) and acetic acid (CH_3COOH) (H_3PO_4:DIH_2O:HNO_3:CH_3COOH = 16:2:1:1) or NMD after depositing Al by thermal evaporation. The electrode is formed by this wet etching.

However, there is arises problem that electrode is etched excessively by observing the region of the electrode and nanowires. Figure 2.10 shows the SEM image of the regions etched excessively. As the cause of this problem, the bad adhesion between the photoresist and the substrate is presumed. Furthermore, it is estimated that etching solution encroaches to a space between the electrode and the nanowire. Figure 2.11 shows the schematic images.

Therefore, the electrode formation is performed by post bake (Baking substrate in 130 °C for 10 min) after the development at Lithography in order to improve adhesion between the photoresist and substrate with silicide nanowires. However, the same results were obtained. Thus, it is inferred that the cause of the problem is the space between the Ni silicide nanowires and the Al electrode deposited by thermal evaporation.

In order to avoid the problem, RF magnetron sputtering is used to eliminate the space between metal electrode and the substrate. Moreover, the electrode is formed by Lift-off technique without wet etching.
Figure 2.10 SEM images of the regions in excess etching between Ni silicide nanowire and Al electrode.

Figure 2.11 Schematic illustration of the cross section before wet etching for electrode formation. There is the space because of bad adhesion between Resist and Al electrode as left image or between Al electrode and Ni silicide nanowire as the right image.
2.2.7 Lift-off technique for electrode formation

Lift-off technique is a method of patterning which is different from wet etching and dry etching. Wet and dry etching is dependent on the material of interest and it is necessary to change the etching conditions. In Lift-off technique, it is not necessary.

At first, patterning of the resist on the substrate is performed by lithography. Therefrom, the deposition is carried out leaving the photoresist on the substrate. As a note, deposition condition that does not break the photoresist is required. Finally, ultrasonic cleaning is performed and deposited film on the photoresist peeling. As a result, the desired pattern is formed. Figure 2.12 shows the schematic illustration of the Lift-off technique.

In this study, this process is used after TiN of the electrode was deposited by RF magnetron sputtering. The electrode is formed without the problem as excessive wet etching.

![Figure 2.12 Schematic illustration of the Lift-off technique.](image-url)
2.3 Measurement and observation methods

2.3.1 Four-point Probe Method

In the resistance measurement, four-point method is one of the most basic methods. The resistance including a contact resistance between the probe and the sample would be obtained in the two probe resistance measurement. In order to measure resistance of the material with low resistance such as metal, the measurement of resistance that doesn’t include the contact resistance is required. The measurement of resistance without including the contact resistance becomes possible by using four-point probe method.

In this study, four-point probe method is used to measure the resistance of the Ni silicide nanowire. Figure 2.13 shows the schematic illustrations of the electrode structure to use this method.

Figure 2.13 Schematic illustration of the electrodes structure.
2.3.2 Scanning Electron Microscope (SEM) for Observation

The formed Ni silicides in Si nanowire were observed by scanning electron microscope (SEM). The observation was mainly performed by overhead viewing.

Figure 2.14 shows Scanning Electron Microscope (SEM) system which is S-4800 (HITACHI High-Technologies Corporation) and its schematic internal configuration is shown in Fig. 2.15. The “Virtual Source” at the top represents the electron gun, producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin, tight, coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion and make the beam dwell on points for a period of time determined by the scan speed. The final lens, the Objective, focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample, interactions occur inside the sample and are detected with various instruments interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a display whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated, the entire pattern can be scanned 30 times per second.
**Figure 2.14** Photograph of SEM equipment.

**Figure 2.15** Schematic view of internal configuration of SEM equipment.
Chapter 3
Electrical Analysis of Nickel Silicide Nanowire

3.1 Introduction

3.2 Electrical Characteristics of Ni Silicide Nanowire

  3.2.1 $I-V$ Characterization
  3.2.2 Wire-Size Dependent the Resistivity
  3.2.3 Temperature Dependence of Resistance
  3.2.4 Influence of Roughness in Line Width

3.3 Conclusion

References
3.1 Introduction

As described in the chapter 1, it is presumed that Ni silicidation of Si nanowire differs from silicidation of the bulk Si. Moreover, increase of the resistance in narrow line is a concern because of the effect by surface scattering. However, NiSi of typical phase has a relatively low resistivity and a small mean free path with 5 nm [3.1]. From this, it has been estimated that the impact of surface scattering doesn’t become major. The resistivity, which does not increase in NiSi single crystal nanowire with the line width of 23 nm, has been reported[3.1]. Figure 3.1 shows parts of the reported result. In another study, it has been reported that resistivity of Ni silicide nanowire with the width larger than 23 nm is nearly equal to the resistivity of bulk Ni silicide. Therefore, the resistivity of scaled Ni silicide nanowire as the width of 10 nm has needs to be investigated.

In this chapter, electrical analysis of Ni silicide nanowire with the width from 80 nm to 10 nm is performed by four-point probe method and observations of SEM.

Figure 3.1 (a) Cross-sectional TEM image of NiSi nanowire with the line width of 23 nm and (b) Current-voltage characteristic[3.1].
3.2 Electrical Characteristics of Ni Silicide Nanowire

3.2.1 I-V Characterization

At first, I-V characteristics were measured by four-point probe method in order to evaluate the resistance of Ni silicide nanowires. Figure 3.1 shows I-V characteristics of Ni silicide nanowire with the width of 37 nm and 21 nm. The distance between the TiN electrodes was 4 µm. As expected from the electrical properties of metal, the current-voltage relation follows Ohm’s law. This relation expressed as follows:

$$V = IR$$

(3.1),

where $V$ is the voltage, $I$ is current and $R$ is the resistance of Ni silicide nanowire.

Therefore, The resistance for the nanowire with the width of 37 nm is 1816 Ω and 8250 Ω obtained for the line width of 21 nm from Ohm’s law.

![Figure 3.2](image)

Figure 3.2 Current-voltage characteristic for Ni silicide nanowire with the width of (a) 37 nm and (b) 21 nm. Distance between TiN electrodes is the 4 µm. The resistance of (a) 1816 Ω and (b) 8250 Ω is obtained from Ohm’s law.
3.2.2 Wire-Size Dependent the Resistivity

Figure 3.2 shows the dependence of resistivity on line width of nanowire. The resistivity calculated from the resistance obtained by $I-V$ characteristic. Relationship between resistance and resistivity is expressed by the following equation,

$$R = \rho \frac{l}{hw}$$

(3.2),

where $\rho$ denotes resistivity, and $h$, $w$, and $l$ denote height, width, and length of nanowires. The height of nanowires is 30 nm. Length of nanowire and line width is obtained by SEM observation. Figure 3.3 shows SEM image of formed Ni silicide for Si nanowire.

Typically, the resistivity can’t depend on line width in the same material. Therefore, Figure 3.2 shows that the constant low resistivity for width larger than 35 nm. However, drastic increases in the resistivity were observed for nanowire line width smaller than 35 nm.

One of the causes for drastic increases in the resistivity of nanowires at around the width of 35 nm may be the phase transition of Ni silicide at around this width.
Figure 3.3 Dependence of resistivity on nanowire line width. Silicidation annealing was performed at 500 °C for 5 min.

Figure 3.4 SEM image of formed Ni silicide for Si nanowire and TiN electrodes aligned on it.
3.2.3 Temperature Dependence of Resistance

The resistance was measured at the temperature in the range from 25 °C to 100 °C. The temperature dependence of the resistance can be expressed by the following equation,

\[ \frac{R}{R_{rt}} = \alpha(T - T_{rt}) + 1 \]  

where \( R \) and \( R_{rt} \) are the resistance at temperature \( T \) and that at room temperature (25 °C), respectively, and \( \alpha \) is temperature coefficient of resistance.

Figure 5 shows the temperature dependence of resistance measured for the nanowire line widths of 18, 30, and 62 nm. It is shown that the temperature coefficient of the resistance is almost the same for three widths.

Therefore, the phase of Ni silicide must be the same for three widths although the resistivity measured for three widths is not the same as can be seen in Fig. 3.3. From this figure, temperature coefficient \( \alpha \) was estimated to be 0.0013 K\(^{-1}\). This value of \( \alpha \) is almost the same with the reported value for Ni\(_2\)Si [3.2]. Moreover, in Fig. 3.3 for the nanowire line width larger than 35 nm, the resistivity is close to 34 \( \mu \Omega\)-cm, which is the same with the reported value for Ni\(_2\)Si [3.2-3]. For this reason, it was concluded that for three nanowire line widths the same phase consisting of Ni\(_2\)Si is formed. Thus, drastic increases in resistivity cannot be caused by the change in the phase of Ni silicide.
Figure 3.5 Dependence of resistance ratio on measurement temperature for nanowire line width of 18, 30, and 62 nm. Temperature coefficient of resistance is 0.0013 K⁻¹.
3.2.4 Influence of Roughness in Line Width

Another cause for drastic increases in the resistivity of nanowires at around the width of 35 nm may be the roughness in line width as illustrated in Fig. 3.6. The increase in resistance may be caused by the confinement of current in narrow portions of nanowires.

In order to evaluate the influence of the roughness in line width on the resistivity, Ni silicide nanowires were observed by SEM. Figure 3.7 shows typical SEM image of Ni silicide nanowire. The resistance $R$ for the structure shown in Fig. 3.6 can be expressed by the following equation,

$$R = \rho_{\text{bulk}} \frac{rL}{HW} + \rho_{\text{bulk}} \frac{L(1-r)}{H(W-D)}$$

$$= \rho_{\text{bulk}} \frac{W - rD}{HW(W-D)}$$

(3.4),

where $\rho_{\text{bulk}}$ denotes resistivity of bulk Ni silicide, and $H$, $W$, and $L$ denote height, width, and length of nanowires, respectively, $r$ denotes a fraction of nanowire with wide width, and $D$ denotes the difference in the line width.

If the resistivity $\rho_{\text{rough}}$, for nanowire with roughness, is defined by $R(HW/L)$ for the structure shown in Fig. 3.6, a following relation is obtained.

$$\rho_{\text{rough}} = \rho_{\text{bulk}} \left(1 + \frac{1-r}{W-D}D\right)$$

(3.5),
Figure 3.8 shows the dependence of $D$ on $W$. According to this figure, $D$ increases with the decrease in $W$ except for $W = 10$-20 nm. $\rho_{\text{rough}}$ calculated from Fig. 3.8 is shown as a function of $W$ in Fig. 3.9 by assuming $r = 0.2$ and 0.7. $\rho_{\text{rough}}$ is much smaller than the resistivity measured. Therefore, roughness in line width cannot be the major reason for the drastic increase in resistivity.

**Figure 3.6** Schematic structure of narrow Ni silicide line and the approximation of its roughness.
Figure 3.7 Line width roughness observed by high resolution SEM.

Figure 3.8 Dependence of roughness in line width $D$ on nanowire line width $W$. 
Figure 3.9 Comparison of the resistivity calculated using the roughness approximation model with $r = 0.2$ and $0.7$ to measured resistivity shown in Fig. 3.4.
3.3 Conclusion

Ni silicide was formed on scaled silicon nanowires by annealing at 500 °C for 5 min. The resistances of Ni silicide nanowires were derived from \( I-V \) properties obtained by four-point probe method. The Ni silicide line width in the range from 80 nm to 15 nm was obtained by observation of SEM. Furthermore, the resistivity of silicided nanowires was calculated.

Wire-size dependence of the obtained resistivity has been evaluated and the resistivity was estimated to be small value with 34 \( \mu \Omega \)-cm in the regions of line width more than 35 nm. However, the significant increase in resistivity of Ni silicide nanowire with line width smaller than 35 nm was confirmed.

As the cause of sudden increase in resistivity of silicided nanowires with line width around 35 nm, it is considered that phase of nickel silicide transited. Therefore, in order to determine the transition of the phase, the dependence of resistance of nanowires on the temperatures were evaluated and temperature coefficient of resistance estimated. By the comparing the temperature coefficient of resistances of line width with 18, 30 and 62 nm, it is suggested that there were the transition of the silicide phase and NiSi\(_2\) was formed in any line width.

Therefore, as a cause of sudden increase in resistivity, the roughness with line width was considered. In order to investigate the effect of line width roughness, the simple roughness model was proposed and the comparisons of resistivity in roughness model with the obtained resistivity have been performed. However, the resistivity of roughness model is much smaller than the evaluated resistivity. Thus, it has been suggested that roughness in line width cannot be the major reason for the drastic increase in resistivity.
References


Chapter 4
Discussion in Increase of Resistivity by Size Effect

4.1 Introduction

4.2 Impact of Size Effect
   4.2.1 The Effect of Surface Scattering
   4.2.2 The Increase of Resistivity by Grain Boundary Scattering

4.3 Conclusion

References
4.1 Introduction

In the chapter 3, the increase in resistivity of Ni silicide nanowires with the width smaller than 35 nm was founded. In order to investigate the cause of resistivity increase, the influence such as the transition of phase and line width with roughness was investigated. However, the major cause of the abrupt increase in the resistivity can’t be explained.

Therefore, as described in chapter 1, it is conceivable that there is the resistivity increase by the size effect such as surface scattering and grain boundary scattering of electrons [4.1]. Figure 4.1 shows the schematic illustrations of surface scattering and grain boundary scattering. Moreover, Table 4.1 shows the increase of the resistivity reported in metal nanowire.

In this chapter, abrupt increase of the resistivity by the size effect which has become a problem in the copper interconnects [4.2] is investigated.

<table>
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<th>H (nm)</th>
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<th>ρ_{bulk} (µΩ·cm)</th>
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<td>12</td>
<td>10</td>
<td>1300</td>
<td>42</td>
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</table>

**Table 4.1** Widths, lengths, height, and resistivity of the reported metal nanowires [4.3].
Figure 4.1 Schematic illustrations of electron flow in (a) bulk metal, (b) surface scattering and (c) grain boundary scattering.
4.2 Impact of Size Effect

4.2.1 The Effect of Surface Scattering

The electrons in the metal are scattered by phonons and impurities. In the case where the current flows in narrow regions as nano-size, the scattering of electrons on surface occurs. This scattering is called surface scattering.

The Surface scattering is caused by the width or thickness of the wire or film close to the mean free path of electrons and the resistivity. As the result, the resistivity increase. This effect also occurs in thin film not only occur to the wire.

Therefore, in order to investigate the impact of the surface scattering that is one of the size effects, Fuchs-Sondheimer model [4.2,4.4] is used. This model equation is expressed as:

\[
\rho = \rho_{bulk} \left\{ 1 + 2C (1 - P) \left( \frac{1}{H} + \frac{1}{W} \right) \times \lambda \right\} \quad (4.1),
\]

where \( \lambda \) denotes the mean free path of electron in bulk, \( C = 1.2 \) is used for a rectangle cross-section. \( P \) denotes the probability of elastic electron reflection on the surface of nanowire.

In addition, One of the important parameters in this equation is \( \lambda \), which is given by the following equation for metal [4.5],

\[
\lambda = \frac{h \left( \frac{3}{8\pi} \right)^{\frac{1}{3}}}{e^2 n^\frac{2}{3} \rho_{bulk}} \quad (4.2),
\]
where $h$ is Planck’s constant, $e$ is the elementary charge, and $n$ denotes the electron density. Using $n = 1.8 \times 10^{23} \text{ cm}^{-3}$ [4.5] for Ni$_2$Si and $\rho_{\text{bulk}} = 34 \, \mu\Omega\cdot\text{cm}$ obtained from Fig.3.3, $\lambda = 2 \text{ nm}$ is obtained. Then, the dependence of resistivity on nanowire line width $W$ calculated using the value of $\lambda$ thus obtained is compared with the experimentally obtained data in Fig.4.2. Because the nanowire size effect cannot explain the increase in resistivity with the decrease in nanowire line width.

![Resistivity vs Nanowire Width](image)

**Figure** 4.2 Comparison of the resistivity calculated by surface scattering model to experimentally obtained resistivity data shown in Fig. 3.3.
4.2.2 The Increase of Resistivity by Grain Boundary Scattering

As it was suggested the surface scattering don’t become a major cause of the resistivity increase from small mean free path with 2 nm, the grain boundary scattering which is one of the size effects is investigated.

This scattering is the electrons scattering on grain boundary. Therefore, it is necessary to investigate the existence of the grain in the formed Ni silicide for Si nanowire. In order to confirm the grain of Ni silicide nanowires, the surface of nanowires was observed by back scattered electron (BSE) of SEM. Figure 4.3 shows the SEM image by BSE.

Because contrast exists in SEM image of Ni silicide nanowire with the width of 62 nm, it is considered to be the grain of nanowire. In line width of 21 nm, contrast can’t be confirmed.

However, it has been reported that poly-Ni silicide was obtained in Ni silicide formed on Si nanowire [4.6]. Moreover, because the effect of surface scattering is not much, it was considered that the cause of the resistivity increase can be the effect of grain boundary scattering.
Figure 4.3 SEM image obtained by back scattered electrons. The width of nanowire is (a) 62 nm and (b) 21 nm.
4.3 Conclusion

As the increase in the resistivity are considered because of size effect, surface scattering that is one of them has been investigated. The equation of the surface scattering model was used by calculating the mean free path of electrons in Ni$_2$Si. This results is compared with the experimentally obtained resistivity. Because the mean free path of electrons in Ni$_2$Si is small (2 nm), it has been suggested that surface scattering cannot be the major reason of resistivity increase.

As another impact, the increase in resistivity was considered by grain boundary scattering. In order to investigate the effect of the grain boundary scattering, Ni silicide nanowire was observed by SEM of back scattered electrons. As the result, it has been suggested that there is the grain in nanowire of the line width with 62 nm. The grain can’t be not observed in the line width of 21 nm which has the higher resistivity. According to the study which already done, it is confirmed that Poly Ni silicide nanowire is obtained by forming Ni silicide on Si nanowire.

Therefore, possibility of grain boundary scattering as the cause of increase in resistivity may be suggested.
References


Chapter 5
Conclusion of This Study
5.1 Conclusion

Nickel salicide (self-aligned silicide) have been widely used in ULSIs to reduce the parasitic resistance at source and drain regions of MOSFETs. This technology may be continuously used for highly scaled device such as Si nanowire field effect transistors (Si NW FETs) and FinFETs of 10-20 nm generations. As source and drain regions become extremely narrow and the amount of Si reacting with Ni is limited in these structures, this may lead to the silicide different from the case of the silicidation of the bulk silicon. On the other hand, it has been reported that the narrow metal lines, for example copper narrow lines, suffer from the increase in effective resistivity due to size effect as surface scattering and grain boundary scattering. In this study, in order to apply Ni silicide to high scale device, the impact of size effect in Ni silicide nanowires is investigated. At first (in chapter 3), Electrical analysis of Ni silicide with the line width from 80 nm to 10 nm was performed. The resistivity of regions smaller than 35 nm increase significantly. Moreover, Ni$_2$Si nanowire was formed for any line width. It is also suggested that the roughness of line width is not major reason in the increase of resistivity. Secondly (in chapter 4), the increase in resistivity was discussed due to the size effect. From the mean free path of 2 nm in Ni$_2$Si, surface scattering cannot be the cause of the increase in resistivity. Therefore, the grain boundary scattering was investigated. The grain existed in nanowire with the line width of 62 nm. It is considered that the cause of increase in resistivity of line width smaller than 35 nm can be the impact of grain boundary scattering.
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