Process dependent Electrical characteristics of High-k gate dielectrics on AlGaN/GaN devices

Department of Electronics and Applied Physics
Iwai/Kakushima Lab.
11M55440 陳 江寧
Power electronics for home appliances

Inverters with Si-based IGBT have been the main power converters for home appliances of several kW.

Converter efficiency of 95% should be further improved for coming energy saving mission in Japan.

GaN is an attractive widegap semiconductor for power electronics around 1 kW.
Advantage of AlGaN/GaN HEMT

- High mobility \( \sim 1000 \text{cm}^2/\text{Vs} \)
  \( \rightarrow \) two dimensional electron gas (2DEG)
- High-power operation at high voltage
  \( \rightarrow \) high breakdown field (x10 that of Si)

Epi-wafer using Si substrates

AlGaN/GaN on Si(111) through buffer layer

A key process for mass production on large wafer size (8”, 12”) for low cost over 4H-SiC or sapphire sub
Insulated gate AlGaN/GaN HEMT

Dielectrics between gate and AlGaN

- Suppression of gate leakage current
  → MIS structure with high $E_g$

- Reliability improvements
  → Suppression of $V_N$ formation

Selection of gate dielectrics

<table>
<thead>
<tr>
<th>Dielectrics</th>
<th>SiO$_2$</th>
<th>Si$_3$N$_4$</th>
<th>Al$_2$O$_3$</th>
<th>HfO$_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant (k-value)</td>
<td>4</td>
<td>7</td>
<td>10</td>
<td>18</td>
</tr>
<tr>
<td>Bandgap (eV)</td>
<td>8</td>
<td>5.3</td>
<td>9</td>
<td>5.5</td>
</tr>
<tr>
<td>Interface with AlGaN</td>
<td>Poor</td>
<td>Nice</td>
<td>Poor</td>
<td>Mid</td>
</tr>
</tbody>
</table>

High dielectric constant (high-k) with wide bandgap and also nice interface property should be achieved at the same time.
Issues on MIS gate dielectrics for AlGaN

Gate controllability

\[
\frac{1}{C_{total}} = \frac{1}{C_{dielectric}} + \frac{1}{C_{AlGaN}}
\]

- Capacitance coupling of gate electrode and channel decreases
- Threshold voltage shift to negative direction
- Reduction in transconductance ($g_m$)
- Concerns for short-channel effect

The thickness of dielectric layer should be minimized and the $k$-value should be as high as possible
La$_2$O$_3$ as a gate dielectrics for AlGaN/GaN

<table>
<thead>
<tr>
<th>Properties of La$_2$O$_3$</th>
<th>La$_2$O$_3$ as gate dielectrics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap: 5.5 eV</td>
<td><strong>Substrate</strong></td>
</tr>
<tr>
<td>k-value: 23.4</td>
<td>Si</td>
</tr>
<tr>
<td>Easy to react with substrate</td>
<td>Ge</td>
</tr>
<tr>
<td></td>
<td>InGaAs</td>
</tr>
</tbody>
</table>

Reactively formed dielectric layer seems to have nice interface properties

Purpose of this work

An attempt to use La$_2$O$_3$ as a gate dielectric for AlGaN/GaN
Process for $\text{La}_2\text{O}_3$-AlGaN/GaN MOSHEMT

- Device isolation by RIE with Cl$_2$
- Contact formation with Ti-base metal (750°C)
- $\text{La}_2\text{O}_3$ deposition (from 3 to 12 nm) by e-beam deposition (RT)
- Tungsten (W) gate metal formation
- Annealing in 3%-H$_2$ (from 300°C to 700°C)

FET characteristics, capacitance measurement
Typical FET characteristics

$L_g=10\mu m$, $W_g=50\mu m$, $t_{La2O3}(6nm)$

- $V_{th}=-3.26$ V
- $SS=61.5$ mV/dec.

Effective mobility ($cm^2/Vs$) Split CV measurement

Charge density ($/cm^2$)

Nice FET operation confirmed
Annealing effect on C-V characteristics

- Capacitance increases along with annealing temperature
- Suggestion of reaction at La$_2$O$_3$/AlGaN to form an interface layer with high k-value
Threshold voltage shift with annealing temperature

- $V_{th}$ shifts to positive direction while increasing the annealing temperature
  → either thinning in AlGaN layer thickness or negative charges in $\text{La}_2\text{O}_3$

- Increase in drain current → either $\mu_{eff}$ improvement or $C_g$ reduction
Thickness dependency on capacitance and threshold voltage

<table>
<thead>
<tr>
<th>La₂O₃</th>
<th>AlGaN</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Thickness of La₂O₃ (nm) 25nm

Capacitance density (F/cm²)

\[ C_g = \left( C_{AlGaN}^{-1} + C_{oxide}^{-1} \right)^{-1} \]

\[ V_{th}^{MOS} = V_{th}^{Schottky} \times \frac{C_{AlGaN}}{\left( C_{AlGaN}^{-1} + C_{oxide}^{-1} \right)^{-1}} \]

Threshold voltage (V)

no anneal

\[ k_{AlGaN} = 9 \]
\[ k_{La₂O₃} = 23 \]
Threshold voltage and reaction at La$_2$O$_3$/AlGaN

- Generally, $V_{th}$ shift to negative direction with gate dielectric thickness
- Formation of LaGaO at interface consumes AlGaN layer
- Thinner AlGaN layer includes $V_{th}$ shift to positive direction

A balance of AlGaN thickness with reactively formed interface layer
Conclusions

La$_2$O$_3$ films have been used as gate dielectrics for AlGaN/GaN MOSHEMT

- Capacitance increase with annealing suggests interface reaction at La$_2$O$_3$/AlGaN
- Threshold voltage shift to positive direction with increasing annealing temperature
- A model to explain the $V_{th}$ shift and capacitance increase was proposed using an interface layer with relatively high k-value