A Study on Formation of High Resistivity Phases of Nickel Silicide at Small Area and its Solution for Scaled CMOS Devices

Doctor Thesis

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Supervisor : Prof. Iwai
Outline

- Background
- Purpose of this work
- Configuration of this thesis
- Chapter 3~6
- Conclusion
MOS Scaling and SALICIDE

Scaling: $\kappa(<1)$

Results by scaling:
- Area: $\text{LW} \Rightarrow \kappa^2 \text{LW}$
- Parasitic Resistance: $R \Rightarrow R/\kappa$
- Gate capacitance: $C \Rightarrow \kappa C$
- Power consumption: $P \Rightarrow \kappa^2 P$
- Delay Time: $T \Rightarrow \kappa T$

SALICIDE is invented for reducing the resistance for both gate and S/D.

Titanium SALICIDE

The first SALICIDE material used in fabrication.

Limitation of TiSi$_2$ as scaling
1. Difficulty in transforming C49 to C54 TiSi$_2$.
2. Low thermal stability as thinning.
3. Si is dominant diffusion specie.

*J.A. Kittl, W.T. Shiau, Q.Z. Hong, D. Miles
Cobalt SALICIDE has better scalability than Titanium SALICIDE.

Limitation of CoSi₂ as scaling
1. Large Si consumption.
2. Rough interface by nucleation control.
3. High formation temperature of CoSi₂.
4. Si is dominant diffusion specie in CoSi.

Nickel SALICIDE: Superiority

Superiority of Nickel SALICIDE
1. low Si consumption
2. low formation temperature
3. Ni diffusion kinetics

<table>
<thead>
<tr>
<th>Dominant moving species</th>
<th>Si consumption ratio</th>
<th>Resistivity [μΩ·cm]</th>
<th>Formation Temperature</th>
<th>Si consumption ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>NiSi2</td>
<td>2.27</td>
<td>C54:13<del>20, C49:80</del>100</td>
<td>600~700°C</td>
<td>2.27</td>
</tr>
<tr>
<td>CoSi2</td>
<td>3.64</td>
<td>14~20</td>
<td>600~700°C</td>
<td>3.64</td>
</tr>
<tr>
<td>NiSi</td>
<td>1.83</td>
<td>10.5~18</td>
<td>300~400°C</td>
<td>1.83</td>
</tr>
</tbody>
</table>

*参考 Silicide Technology for Integrated Circuits L.J. Chen*
Nickel SALICIDE: Issues for practical use

Critical Issues of Nickel SALICIDE
1. Controlling phase formation
2. Controlling and limiting diffusion of Ni in Si
3. Poor thermal stability of NiSi
4. Oxidation of NiSi
5. Reducing the specific contact resistivity

Silicide Phase and Resistivity

<table>
<thead>
<tr>
<th>Phase</th>
<th>Resistivity (μΩ·cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>7-10</td>
</tr>
<tr>
<td>Ni₃Si</td>
<td>80-90</td>
</tr>
<tr>
<td>Ni₃Si₁₂</td>
<td>90-150</td>
</tr>
<tr>
<td>Ni₂Si</td>
<td>24-30</td>
</tr>
<tr>
<td>Ni₃Si₂</td>
<td>60-70</td>
</tr>
<tr>
<td>NiSi</td>
<td>10.5-18</td>
</tr>
<tr>
<td>NiSi₂</td>
<td>34-50</td>
</tr>
</tbody>
</table>

*Silicide Technology for Integrated Circuits, L.J. Chen

Series Resistance v.s. Gate Length

*S-D Kim et al. TED2002
Purpose of this work

Following issues of Nickel silicide are investigated.

1. Phase control of nickel silicide at small areas.
2. Thermal stability of NiSi.
3. Schottky barrier height lowering at NiSi and silicon interface.
Chapter 2 CMOS Silicide Process Flow and Sheet Measurement Pattern

STI, Gate, Junction, Wet Clean

Ni/TiN sputter: Ni → TiN in-situ

1st Anneal: 270°C 150sec heating up by hot plate

Selective Wet Etch: SPM(H₂SO₄ + H₂O₂)

2nd Anneal: 395°C 30sec hold

Contact, Cu Interconnects

STI or Side Wall

Top View of test structure

Silicide

W = 0.10 ~ 1.0μm

L = 0.5 ~ 100μm

Substrate or Poly-Si

Sectional view of test structure
Chapter 3 High Resistivity Phase of Nickel Silicide at Small Area

Purpose of this chapter

Understanding the formation of high resistivity phase of Nickel silicide at small area.

- Identified nickel silicide phase
- Compared to CoSi$_2$
- Reaction Mechanism and Thermodynamics of nucleation
Sheet resistance increase in only narrow line.
High resistance sample has NiSi and Ni$_3$Si$_2$.

Long line has NiSi only. No increase in resistance.
Sheet Resistance on p+ Active Areas

(a) L/W=0.5/0.10μm. 7.2Ω/sq.
Thickness: 19.8nm, Resistivity: 14.3μm·cm

(b) L/W=0.5/0.10μm. 27.0Ω/sq.
Thickness: 19.4～59.9nm

High resistance sample has NiSi and NiSi₂.
Long line has NiSi only. No increase in resistance.
NiSi on poly also has degradation in uniformity.
⇒ Not crystal states of Si but size of area is dominant.
CoSi$_2$ has no degradation in uniformity.

⇒ Complex phase diagram of Ni-Si system is main cause in the formation of high resistivity phase.
### Presumed Ni-Si Reaction Path on n⁺ Area

<table>
<thead>
<tr>
<th>Step</th>
<th>Chemical equation</th>
<th>$\Delta H$ (kJ/mol of Ni atoms)</th>
<th>Total Volume Change [(post-pre)/pre]</th>
<th>Volume Change of Silicide [(post-pre)/pre]</th>
<th>Volume Expansion [(Silicide-Si)/Si]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$2\text{Ni} + \text{Si} \rightarrow \text{Ni}_2\text{Si}$</td>
<td>-66</td>
<td>-23.3%</td>
<td>-</td>
<td>0.0% → 60.5%</td>
</tr>
<tr>
<td>2</td>
<td>$3\text{Ni}_2\text{Si} + \text{Si} \rightarrow 2\text{Ni}_3\text{Si}_2$</td>
<td>-9</td>
<td>-1.3%</td>
<td>+19%</td>
<td>60.5% → 43.5%</td>
</tr>
<tr>
<td>3</td>
<td>$\text{Ni}_3\text{Si}_2 \rightarrow \text{Ni}_2\text{Si} + \text{NiSi}$</td>
<td>+2.7</td>
<td>-2.1%</td>
<td>-2.1%</td>
<td>43.5% → 40.5%</td>
</tr>
<tr>
<td>4</td>
<td>$\text{Ni}_2\text{Si} + \text{Si} \rightarrow 2\text{NiSi}$</td>
<td>-19</td>
<td>-7.5%</td>
<td>+50%</td>
<td>60.5% → 20.5%</td>
</tr>
</tbody>
</table>

### Reaction Step Model

1. Formation of $\text{Ni}_2\text{Si}$. Increasing compressive stress.
2. Formation of $\text{Ni}_3\text{Si}_2$. Relaxing stress. Reaction is noticeable at fine patterns.
3. $\Delta H$ is small. Nucleation reaction like.
4. Formation of $\text{NiSi}$.

- Step3 is limiting step. $\text{Ni}_3\text{Si}_2$ tends to remain.
- 2 reaction paths complicate phase sequence.
  1:$\text{Ni}_2\text{Si} \rightarrow \text{NiSi}$, 2:$\text{Ni}_2\text{Si} \rightarrow \text{Ni}_3\text{Si}_2 \rightarrow \text{NiSi}$.

Large impurities; As, P, and Silicide stress.

⇒ Compressive stress retards the reaction.

⇒ Difficulty in transition from $\text{Ni}_3\text{Si}_2$ to $\text{NiSi}$.

*L. W. Cheng et al. / Materials Science and Engineering A 409 (2005) 217–222*
## Presumed Ni-Si Reaction Path on p+ Area

<table>
<thead>
<tr>
<th>Step</th>
<th>Chemical equation</th>
<th>$\Delta H$ (kJ/mol of Ni atoms)</th>
<th>Total Volume Change [(post-pre)/pre]</th>
<th>Volume Change of Silicide [(post-pre)/pre]</th>
<th>Volume Expansion [(Silicide-Si)/Si]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Ni+2Si→NiSi$_2$</td>
<td>-87</td>
<td>-22.5%</td>
<td>-</td>
<td>0.0%→-1.4%</td>
</tr>
<tr>
<td>2</td>
<td>3Ni+NiSi$_2$→2Ni$_2$Si</td>
<td>-10.5</td>
<td>-11.1%</td>
<td>+62.8%</td>
<td>-1.4%→60.5%</td>
</tr>
<tr>
<td>3</td>
<td>NiSi$_2$+Ni$_2$Si→3NiSi</td>
<td>-12</td>
<td>+1.0%</td>
<td>+1.0%</td>
<td>19.3%→20.5%</td>
</tr>
<tr>
<td>4</td>
<td>NiSi$_2$→NiSi+Si</td>
<td>+2</td>
<td>-11.8%</td>
<td>-38.9%</td>
<td>-1.4%→20.5%</td>
</tr>
</tbody>
</table>

### Reaction Step Model

1. **Formation of NiSi$_2$.** Small stress. Thickness of NiSi$_2$ depends on implanted dose spices and amounts.

2. **Unreacted Ni and NiSi$_2$ form Ni$_2$Si.** Large stress is formed.

3. **NiSi$_2$ and Ni$_2$Si form NiSi.**

4. **Without Ni, NiSi$_2$ hardly transforms to NiSi.**

Large amount B makes thicker NiSi$_2$ layer. Thicker NiSi$_2$ tends to remain because of lack of Ni.

* T. Isshiki et. Al. RTP 2006 14th IEEE International Conf. on RTP
Effect of Tensile Stress on silicidation

Implanted Boron and STI makes tensile stress.

⇒ Tensile stress promotes the reaction.

⇒ NiSi₂ is formed in early stage of silicidation.

Interfacial Energy increase by implanted B (?)

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FIG. 2. BF micrographs of a B sample, o-s, 400 °C, (a) 10 min, (b) 1 h, (c) 5 h.
Thermodynamics of Nucleation

(a) The free energy of a nucleus as a function of its radius

(b) The free energy of a nucleus when a uniform planar film

Boundary surface increases free energy change → nucleation reaction is promoted at small areas.

*F.M. d'Heurele J. Mater. Res. 3(1), 1988, pp. 167-195
### Comparison between TiSi$_2$ and NiSi cases

<table>
<thead>
<tr>
<th>Reaction</th>
<th>C49-TiSi$_2$→C54TiSi$_2$</th>
<th>Ni$_2$Si→Ni$_3$Si$_2$→NiSi</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
</tbody>
</table>

- **Reaction Mechanism**
  - TiSi→C49-TiSi$_2$→C54TiSi$_2$
  - Sequential reaction.
  - 1. Ni$_2$Si→NiSi
  - 2. Ni$_2$Si→Ni$_3$Si$_2$→NiSi
  - 2 paths to form NiSi.

- **Volume Change by reaction**
  - -2% C49-TiSi$_2$→C54TiSi$_2$
  - +50% Ni$_2$Si→Ni$_3$Si$_2$→NiSi

- **Effect of Scaling on Phase Transition**
  - Transition from C49 to C54-TiSi$_2$ is difficult for decreasing nucleation sites.
  - Ni$_2$Si→Ni$_3$Si$_2$ reaction is promoted at small area for stress reduction.

- **Formation of NiSi** is much complex than TiSi$_2$ case in terms of stress formation and reaction mechanism.
Conclusions of Chapter 3

- Firstly, formation of $\text{Ni}_3\text{Si}_2$ on small $n^+$ or $\text{NiSi}_2$ on small $p^+$ active and poly-Si areas is confirmed.

- The formation of high resistivity phases at small areas is characteristic features of nickel silicide which has complex phase diagram and reaction mechanism.

- Tensile or compressive stress affects the formation of $\text{NiSi}_2$ and $\text{Ni}_3\text{Si}_2$ respectively.
Purpose of this chapter

Modify silicidation conditions in order to improve the uniformity of sheet resistance at small area.
Effect of First Anneal

n⁺ active area W/L=0.10/0.5μm

Only p⁺ active area is improved.

p⁺ active area W/L=0.10/0.5μm

*Process condition 2nd Anneal 395°C
Effect of second anneal on n⁺ active area

*Process condition 1st Anneal 270°C

Not Ni₃Si₂ but NiSi₂ is formed.
Effect of second anneal on p$^+$ active area

*Process condition 1$^{st}$ Anneal 270°C

Sheet Resistance[ohm/sq.]
Cumulative probability[%]

<table>
<thead>
<tr>
<th>Temperature</th>
<th>Cumulative Probability [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>395°C</td>
<td>99.9</td>
</tr>
<tr>
<td>500°C</td>
<td>99.99</td>
</tr>
<tr>
<td>550°C</td>
<td>99.99</td>
</tr>
<tr>
<td>575°C</td>
<td>99.99</td>
</tr>
</tbody>
</table>

*Process condition 1$^{st}$ Anneal 270°C

L/W=0.5/0.10μm. 14.8Ω/sq. at 575°C

Epi-NiSi$_2$ is formed.
Effect of Nickel Thickness

*n + active area W/L=0.10/0.5μm*

Sheet Resistance [ Ω/sq ]

*Process condition 1st Anneal 270°C /2nd Anneal 395°C*

- thicker Ni increases volume energy.
Both Ni$_3$Si$_2$ and Ni$_2$Si are identified.

⇒ Process before 1$^{st}$ Anneal should be improved.
High Temp. Ni PVD on n\textsuperscript{+} active area

\begin{itemize}
  \item N\textsuperscript{+}diff. W/L = 0.10/0.5 \mu m
  \item Sheet Resistance [ohm/sq.]
  \item Cumulative probability [%]
  \item 200\degree C SPT
  \item 300\degree C SPT
  \item RT SPT
  \item TEM & NBD
  \item NiSi\textsubscript{2}
  \item NiSi\textsubscript{2}
  \item Si

\*Process condition 1\textsuperscript{st} Anneal 270\degree C / 2\textsuperscript{nd} Anneal 500\degree C

High resistance sample, 18.2\Omega/sq. of Ni PVD at 200\degree C

\begin{itemize}
  \item Not Ni\textsubscript{3}Si\textsubscript{2} but NiSi\textsubscript{2} is formed.
\end{itemize}
High Temp. Ni PVD on p+ active area

*Process condition 1st Anneal 270°C / 2nd Anneal 500°C

High resistance sample, 22.6Ω/sq. of Ni PVD at 200°C

Epi-NiSi₂ is formed.
Effects of Anneal Time

N⁺ Active Area
L/W=0.5/0.10µm

P⁺ Active Area
L/W=0.5/0.10µm

Cumulative probability [%]

Sheet Resistance [Ω/sq]

- 270C REF
- 270C 2 times long

*Process condition 1st Anneal 270°C / 2nd Anneal 500°C

- Longer anneal improves the uniformity.
Effect of Furnace Anneal

n+ active area (L/W=0.5/0.10μm)

p+ active area (L/W=0.5/0.10μm)

*Process condition  1st Anneal 270°C / 2nd Anneal 500°C

Furnace anneal improves the uniformity dramatically.
Width dependence of Sheet Resistance on n+ active area by Furnace Anneal

Hot plate (Reference) (L=100μm)

Furnace Anneal (L=100μm)

- No increase in sheet resistance at narrow line by furnace anneal.

*Process condition
1st Anneal single 270°C
2nd Anneal 395°C

*Process condition
1st Anneal furnace 350°C
2nd Anneal 500°C
Width dependence of Sheet Resistance on p+ active area by Furnace Anneal

- No increase in Sheet resistance at narrow line by furnace anneal.

Hot plate (Reference) (L=100μm)

- Process condition
  1st Anneal single 270°C
  2nd Anneal 395°C

Furnace Anneal (L=100μm)

- Process condition
  1st Anneal furnace 350°C
  2nd Anneal 500°C
# Comparison among Annealing tools

<table>
<thead>
<tr>
<th>Anneal Tool</th>
<th>RTA</th>
<th>Hot Plate</th>
<th>Furnace</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td><img src="image" alt="RTA System Configuration" /></td>
<td><img src="image" alt="Hot Plate" /></td>
<td><img src="image" alt="Furnace" /></td>
</tr>
<tr>
<td><strong>Atmosphere</strong></td>
<td>( \text{N}_2 )</td>
<td>Vacuum or ( \text{N}_2 )</td>
<td>( \text{N}_2 )</td>
</tr>
</tbody>
</table>
| **Advantage** | Excellent temperature control. | • Easy for process below 300 °C.  
• Available for in-situ treatment after PVD. | • Suitable for long-term treatment.  
• Suitable for low temperature treatment. |
| **Drawback** | • Unsuitable for temperature below 300 °C.  
• Unsuitable for long-term treatment. | • Hard to control the temperature profile.  
• Unsuitable for long-term treatment. | • Impossible for short-term treatment. |
| **Silicide application** | Commonly used in silicidation. | • Hardly used in silicidation. | • Hardly used in silicidation. |

- **Furnace suitable for long and low temperature Annealing.**
### Effect of Furnace Anneal on The Formation of High Resistivity Phases

<table>
<thead>
<tr>
<th>High resistivity Phase</th>
<th>Ni$_3$Si$_2$ on n type</th>
<th>NiSi$_2$ on p type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Example</td>
<td><img src="image1.jpg" alt="Image" /></td>
<td><img src="image2.jpg" alt="Image" /></td>
</tr>
<tr>
<td></td>
<td><em>T. Isshiki et. al. 14th IEEE International Conf. on RTP, 2006 [4.4]</em></td>
<td><em>T. Isshiki et. al. 14th IEEE International Conf. on RTP, 2006 [4.4]</em></td>
</tr>
<tr>
<td>Reaction path</td>
<td>2 way paths</td>
<td>2 way paths</td>
</tr>
<tr>
<td>Path1: Ni$_2$Si → NiSi</td>
<td>Path1: Ni$_2$Si → NiSi</td>
<td></td>
</tr>
<tr>
<td>Path2: Ni$_2$Si → Ni$_3$Si$_2$ → NiSi</td>
<td>Path2: NiSi$_2$ → Ni$_2$Si → NiSi</td>
<td></td>
</tr>
<tr>
<td>Effect of furnace anneal</td>
<td>1. Promote Ni$_3$Si$_2$ → NiSi reaction by large heat quantity by long anneal. 2. Grain growth Ni$_2$Si phase.</td>
<td>1. Promote NiSi$_2$ → Ni$_2$Si reaction by large heat quantity by long anneal. 2. Initial NiSi$_2$ layer is not thicken (?)</td>
</tr>
</tbody>
</table>
Conclusions of Chapter 4

- Furnace anneal successfully improves the uniformity of sheet resistance at small areas.

- Increasing temperature of 1\textsuperscript{st} anneal or thickness of Ni improves the uniformity of $R_s$ on $p^+$ active area only.

- Increasing temperature of Ni PVD stage or 2\textsuperscript{nd} anneal promotes the formation of NiSi$_2$ phase.
Chapter 5 Thermal Stability of NiSi

Purpose of this chapter

To Investigate thermal stability of NiSi.

- Clarify thermal stability difference between $n^+$ and $p^+$ active areas.

- Clarify thermal stability difference between NiSi on Si(100) and Si(110).
Crystal Orientation and Thermal stability of NiSi

*C. Lavoie et. al, Microelectronics Engineering 70, 144-153 (2003)

Crystal Orientation of NiSi depends on Si.
⇒Orientation of NiSi or Si changes thermal stability?

*Process condition
P type poly-Si,
Ni=15nm, 3 °C/s N₂ ambient

*C.Detavernier et al. Nature 2003
Thermal Stability of Sheet Resistance

n+ active area (L/W=100/10μm)  

p+ active area (L/W=100/10μm)

\[ \begin{align*}
\text{Sheet Resistance} & [\Omega/\text{sq}] \\
\text{Cumulative probability} & [%] \\
& 500^\circ C \\
& 600^\circ C \\
& 650^\circ C \\
& 700^\circ C
\end{align*} \]

*pProcess condition*  
1st Anneal 270^\circ C / 2nd Anneal 500^\circ C

**p+ active area has better thermal stability than n+ active area.**
Agglomeration of NiSi on n⁺ active area is confirmed.
NiSi (020) // Si (110) is observed on p⁺ implanted Si.
The space of b axis decreases as temperature increases.
⇒ NiSi grains relax by arranging each grains.
Annealed NiSi Images by optical microscope

- NiSi on deep-SD B shows no agglomeration.
  ⇒ Highly implanted B is the cause in high thermal stability.

*Process condition
1st Anneal 270°C
2nd Anneal 500°C
Add. Anneal 650°C
**Effect of B dose on NiSi orientation**


- **Si<100> direction**
  - NiSi (020) // Si (110) is formed at $5 \times 10^{15}$ atoms/cm$^2$ and above of B dose.

- **Si<110> direction**

  - *Process condition*
    - 1$^{st}$ Anneal 270°C
    - 2$^{nd}$ Anneal 500°C

- NiSi (020) // Si (110) is formed at $5 \times 10^{15}$ atoms/cm$^2$ and above of B dose.
Thermal Stability Comparison between NiSi/Si(100) and Si(110)

- **Process Flow**
  - SPM 9:1
  - BOE 20:1
  - Ni-PVD 10nm
  - RTA 225 to 700°C 30sec

- **Graph**
  - Sheet Resistance [Ω/sq.]
  - Anneal Temp. [°C]

- **Note**
  - Thermal stability: NiSi on Si(100) > Si(110).
NiSi on both Si(100) and Si (110) align to Si substrates.
- NiSi on Si(100) is 4 fold symmetry.
- NiSi on Si(110) is 2 fold symmetry.

Strong NiSi(020)//Si(110) relation is observed from both samples.
NiSi on Si(110) cannot relax by contracting b-axis of NiSi because of 2 fold symmetry.
Conclusions of Chapter 5

- Thermal stability of NiSi depend on crystal orientation of NiSi to Si.

- Thermal stability: NiSi on p⁺ > n⁺ active area. Highly implanted B (> 5E15atms/cm²) ⇒ NiSi(020) aligns to Si(110). ⇒ b-axis of NiSi contacts by increasing Temp.

- Thermal stability: NiSi on Si(100) > Si(110) NiSi on Si(110) cannot relax by b-axis of NiSi because of two fold symmetry of Si(110).
Chapter 6 Schottky Barrier Height of NiSi and Si Interface

Purpose of this chapter

- Lowering Schottky barrier height of NiSi on Si by Al.
- Comparing Schottky barrier height of NiSi on Si (100) and (110).
Logic CMOS Series Resistance

Series Resistance

Specific Contact Resistivity

\[ \rho_c = \rho_{co} \exp \left( \frac{2 \phi_B}{q \hbar} \sqrt{\frac{\epsilon_s m^*}{N}} \right) \text{ ohm} - \text{cm}^2 \]

To decrease Specific Contact Resistivity
- Doping Density N ↑
- Barrier Height \( \varphi_B \) ↓

Schottky Barrier Height need to be reduced in order to reduce \( \rho_c \).
Schottky Barrier Height

Interface state and Fermi Level Pining

- Dangling Bond
- Metal Induced Gap State (MIGS)
- Fermi Level of Metal/Si interface
  - $\varphi_{bp} = 1/3E_g$

Modulation of Barrier Height
- PtSi for PFET, ErSi for NFET
- Introducing impurities at the interface.

CMOS on Si(110) and NiSi

- NiSi(112)
- NiSi(202)/(211)

CMOS Performance
- Si(110) > Si(100)

NiSi is affected by Surface Orientation of Si.

Is Schottky Barrier Height on Si(110) different from Si(100)?
Schottky Diode I-V Characteristic w or w/o Al

Process Flow
1. SPM 9:1
2. SPM 4:1, HF50:1, HPM
3. Thermal SiO₂ 1000 Å
4. Photolithography
5. SiO₂ Etch, BOE 20:1
6. Resist Strip
7. Al-Implantation
   1e14 atm/cm² 5keV
8. HF Treatment
9. Ni-PVD 10nm
10. RTA 500°C 30sec
11. Metal strip SPM4:1
12. Al-PVD 1000 Å
   for back side contact

*Si(100): p-type, 10-20Ω·cm, 475-575μm
*Si(110): p-type, 1-10Ω·cm, 500-550μm

Reverse Current increases by Al.
Activation-Energy Measurements
For SBH Determination, without Al

\[ \phi_{Bp} = 0.38 \text{ eV} \]

\[ \phi_{Bp} = 0.34 \text{ eV} \]

\[ \phi_{Bp} \text{ of Si(100)} > \phi_{Bp} \text{ of Si(110)} \]
⇒ Charge neutral level : Si(100) > Si(110)
SIMS Profile after NiSi Formation

Al conc. of Si(110) ≈ Si(100) at NiSi/Si interface.
Activation-Energy Measurements For SBH Determination, with Al

\[ \phi_{\text{Bp}_{\text{Si}(100)}} = 0.17 \text{ eV} \]
\[ \phi_{\text{Bp}_{\text{Si}(110)}} = 0.23 \text{ eV} \]

- \( \phi_{\text{Bp}} \) of Si(100) < \( \phi_{\text{Bp}} \) of Si(110)
- NiSi/Si(100): \( \Delta \phi_{\text{Bp}} = 0.21 \text{ eV} \), NiSi/Si(110): \( \Delta \phi_{\text{Bp}} = 0.11 \text{ eV} \)  
  \( \Rightarrow \) interface states: Si(100) < Si(110)
In-plane XRD

- No orientation change observes by Al implantation.
Analysis on Schottky barrier lowering by Al implant.

Band structure of NiSi₂/Si interface by Y addition.
*Li Geng et. Al. EDL Vol.29 pp.446(2008)

Solid solubility of Al in Si is below $7 \times 10^{18}$ atms/cm³ (600°C)
⇒Accepter like Al in Si is few.

Addition of Se, S, Y, Al to NiSi/Si interface has following effects.
①Charge Neutral Level is changed by interface state change.
②Work function is changed by dipole formation.
Conclusions of Chapter 6

- Schottky Barrier Height is successfully reduced by Al implantation for both Si(100) and Si(110).

- Barrier lowering by Al implantation is significant for Si(100) than Si(110).

- No crystal structure change of NiSi was observed by Al implantation.
Firstly the formation of high resistivity phase at small area has been observed, the issue has successfully been solved by furnace anneal for 1st anneal. This process has successfully been used for a CMOS fabrication condition.
Conclusions of Chapter 7-2

■ Chapter 3
The formation of Ni$_3$Si$_2$ or NiSi$_2$ at small areas is confirmed.
⇒ The formation of Ni$_3$Si$_2$ or NiSi$_2$ is related to complex Ni-Si phase diagram and reaction mechanisms.

■ Chapter 4
Modifying silicide condition for improve the uniformity of sheet resistance at small area.
⇒ Furnace anneal for 1$^{st}$ anneal dramatically improves the uniformity.
Conclusions of Chapter 7-3

Chapter 5

- Thermal stability: NiSi on \( p^+ > n^+ \) active area.
  \( \Rightarrow \) NiSi(020) aligns to Si(110) on \( p^+ \) active area.
  \( \Rightarrow \) b-axis of NiSi contacts by increasing Temp.

- Thermal stability: NiSi on Si(100) > Si(110)
  \( \Rightarrow \) NiSi on Si(110) cannot relax by b-axis of NiSi.
  Because of Two folds symmetry of Si(110).

Chapter 6

- Schottky Barrier Height is successfully reduced by Al implantation for both Si(100) and Si(110)

- Barrier lowering by Al is significant for Si(100) than Si(110).
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