(100)- and (110)-oriented nMOSFETs with highly Scaled EOT in La-silicate/Si Interface for Multi-gate Architecture

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• EOT scaling with direct contact of high-k/Si in multi-gate architecture
• Detailed comparison between (100)- and (110)-oriented nMOSFET
  - Reaction at interface
  - Interfacial property
  - Electrical characteristics
• Conclusions
Scaling limit in EOT

- SiO$_x$ interfacial layer (typ. 0.5~0.7nm)
- High-k based oxide
- Excess gate leakage

SiO$_2$ interfacial layer
- Recovery of degraded mobility
- Interface state, reliability (TDDB, BTI), etc.

SiO$_2$-IL free structure (direct contact of high-k/Si) is required for EOT=0.5nm
Direct contact La-silicate/Si structure

Superior interfacial property and high mobility were demonstrated at EOT of 0.62nm

Multi-gate with high-k/metal

Decreasing body thickness and EOT

Suppression of SCE and $V_{th}$ variability

Lower $V_{DD}$

Lower power
Motivation and objective in this study

Fabrication and characterization of (110)-oriented planar MOSFET with direct contact La-silicate/Si

- Interface reaction and EOT
- Interface state density,
- Quality of La-silicate dielectrics, etc.
Experimental procedure

LOCOS isolated p-Si wafer (S/D pre-formed)

- SPM and HF cleaning
- \( \text{La}_2\text{O}_3 \) deposition (300°C)
- \( \text{La}_2\text{O}_3 \) deposition (300°C)
- \( \text{TiN} \) deposition (10nm)
  - by RF sputtering
- Si deposition (100nm)
  - by RF sputtering
- Gate patterning
- Post metallization annealing (PMA) in FG (H\(_2\):N\(_2\)=3:97% ) at 800°C for 30min
- Si removal by TMAH for electrical measurement
- S/D & Backside Al contact
- FGA (H\(_2\):N\(_2\)=3:97% ) at 420°C for 30min

(100)/<110> Si substrate
(110)/<110> Si substrate
Same impurity concentration
(3 x 10\(^{16}\) cm\(^{-3}\))

Three types of devices were prepared with various EOT
Dependence of EOT

**SiO₂**

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**La-silicate**

- Oxidation of Si is dependent on surface orientation
- In La-silicate, no dependence between (100) and (110)

**H. S. Momose et al., T-ED, vol. 50, no. 4, p. 1001, 2003**
Larger interface state density on (110) orientation

Degradation of SS in (110)-oriented MOSFET
Almost no frequency dispersion in C-V curve

Fairy nice interfacial property was achieved
Comparison of gate leakage current

Carrier separation method

- Gate leakage current is almost identical
- High breakdown voltage is considered to be good interfacial property
Effective electron mobility

Channel direction is parallel to <110>

- Electron mobility is close to SiO₂ at high $N_{inv}$ region
- Mobility is reduced with decreasing EOT in both (100) and (110) orientation
Time evolution of the $V_{th}$ shift


- $V_{th}$ shift is increased with increasing stress time and measured temperature.
- A model for fitting $V_{th}$ shift versus stress time

$$\Delta V_{th}(t) = \Delta V_{max} \cdot \left[1 - \exp\left(-\frac{t}{\tau_0}\right)^\beta\right]$$
Low Ea are thought to be direct tunneling of electron, causing the $V_{th}$ shift similar to Hf-based oxides ($E_a=0.08\text{eV}$).

No degradation of SS indicates electron trapping in La-silicate.
Electrical characteristics of (100)- and (110)-oriented nMOSFETs has been investigated with direct contact La-silicate/Si structure.

- No significant difference in EOT and scaled EOT were obtained irrespective of Si substrate orientation.
- Large interface state density on (110) orientation is one of the challenging issues, while fairly nice interfacial property has been demonstrated.
- Mobility is degraded with decreasing EOT in both (100)- and (110)-oriented nMOSFETs.
- Bulk trapping in La-silicate is found to be main origin responsible for the $V_{th}$ shift even with larger interface state density on (110) orientation.
- For future work, (110)-oriented pMOSFET must be investigated, higher mobility is expected, while NBTI is thought to be one of the crucial issues.
Acknowledgement

This study was supported by New Energy and Industrial Technology Development Organization (NEDO)

Thank you very much for your kind attention!