Metal Inserted Poly-Si with High Temperature Annealing for Achieving EOT of 0.62nm in La-silicate MOSFET

T. Kawanago1, Y. Lee1, K. Kakushima2, P. Ahmet1, K. Tsutsui2, A. Nishiyama2, N. Sugii2, K. Natori1, T. Hattori1 and H. Iwai1
1 Frontier Research Center, Tokyo Institute of Technology, 4259, Nagatsuta, Midori-ku, Yokohama 226-8502, Japan,
2 Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology,
Tel.: +81-45-924-5847, E-mail: kawanago.t.ab@m.titech.ac.jp

Abstract— This paper reports device process approach for further EOT scaling with small interface state density based on controlling La-silicate/Si interface. The interface state density of \(1.6 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1}\) can be achieved by annealing at 800°C for 30 min in forming gas while significant increase in EOT has been also observed. EOT increase caused by high temperature annealing has been drastically inhibited with MIPS stacks accompanied by high quality interface. The effective electron mobility of 155 \(\text{cm}^2/\text{Vsec}\) at 1MV/cm with an EOT of 0.62 nm has been obtained in direct contact La-silicate/Si structure by combination of MIPS stacks with high temperature annealing.

I. INTRODUCTION

The scaling in an equivalent oxide thickness (EOT) with high-k/metal gate stacks has been required to suppress the short-channel effect and threshold voltage variability in state-of-the-art MOSFETs [1, 2]. Since a SiO2 interfacial layer is typically formed to recover the interfacial property or effective mobility degradation [3], EOT below 0.5nm is limited by the presence of SiO2 interfacial layer. Several groups have been reported that an EOT below 0.5 nm can be achieved with Hf-based oxides in directly contact with Si by sophisticated methods to inhibit or scavenge SiO2-based interfacial layer growth [4, 5]. Moreover, it has been reported that a direct contact structure can be also easily achieved using rare earth oxides such as La2O3 for gate dielectrics due to the formation of La-silicate at the La2O3/Si interface and fairly nice nMOSFET operation has been demonstrated with scaled EOT [6]. One of the critical issues is how to control La-silicate/Si interface. There are mainly two problems remained to be solved at La-silicate/Si interface. Improving interface property is principal importance for MOSFET application [7]. Excess silicate reaction between La2O3 and Si should be suppressed for scaled EOT [8]. These requirements should be accomplished simultaneously for further EOT scaling. Thus, device process concept for controlling La-silicate/Si interface must be established. In this study, our concept to control La-silicate/Si interface are described and experimentally demonstrated. A method for improving interfacial property is firstly investigated. Subsequently, our approach for achieving scaled EOT with nice interfacial property is proposed. The impact of device process is also discussed through fabrication and characterization of nMOSFETs.

II. GATE STACK FORMATION AND EXPERIMENT

La2O3 was deposited on HF-last Si (100) substrate by e-beam evaporation in an ultra-high vacuum chamber, followed by in-situ W (tungsten) metal deposition by RF sputtering for MOS capacitors and nMOSFETs. nMOSFETs were fabricated by gate last process using source and drain pre-formed p-Si (100) substrates with a substrate doping concentration of 3 x 10^{16} \text{ cm}^{-3} [9]. Al was deposited on the source/drain region and back side of the substrate as a contact. EOT was estimated by NCSU CVC program [10]. Charge pumping measurement was conducted to evaluate the interface state density [11]. Split-CV method was employed to measure an effective electron mobility of nMOSFET [12].

III. EFFECT OF HIGH TEMPERATURE ANNEALING

First, device process for improving interfacial property was experimentally investigated. Previous study has been reported that the interface state density at La-silicate/Si interface is reduced with increasing the annealing temperature [13]. However, previous study mentioned that the interface state density was still \(10^{12} \text{ cm}^{-2} \text{eV}^{-1}\) order by rapid thermal annealing for 10–20 sec to simulate the source/drain activation [13]. On the basis of this previous report, post-metallization annealing was performed for 30 min in forming gas ambient with various annealing temperatures after gate patterning. By conducting the post-metallization annealing, La-silicate is formed at La2O3/Si interface [8].

Figure 1. Impact of annealing temperature on C-V characteristics of MOS capacitors with La-silicate. The samples were annealed for 30 min in forming gas at (a) 500°C, (b) 700°C, and (c) 800°C, respectively.

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Figure 1 shows the impact of annealing temperature on C-V characteristics of MOS capacitors. Large frequency dispersion of hump in C-V curve can be observed at temperature of 500 °C. It indicates the large interface state density at La-silicate/Si interface [13]. On the other hand, frequency dispersion of hump is reduced with increasing the annealing temperature. At annealing temperature of 800 °C, little frequency dispersion can be confirmed, indicating small interface state density. nMOSFETs were also fabricated with same annealing conditions to quantitatively examine the interface state density. Figure 2 (a) shows the charge pumping current ($I_{cp}$) as a function of annealing temperature. $I_{cp}$ is decreased with increasing the annealing temperature, corresponding to the reduction of interface state density. A mean interface state density can be estimated from the slope of $I_{cp}$-frequency characteristics. The mean interface state density of $1.6 \times 10^{11} \text{cm}^{-2}\text{eV}^{-1}$ can be attained by annealing at 800 °C. This value is one order of magnitude smaller than that of previous study [13]. Figure 2 (b) shows the effective electron mobility as a function of annealing temperature. Improving effective electron mobility can be confirmed with increasing annealing temperature. Especially, peak mobility is improved because of the decrease in Coulomb scattering associated with interface state density. It has been reported that the formation of La-silicate is attributed to Si penetration from substrate to La$_2$O$_3$ dielectrics [14]. At high temperature annealing, hence, high quality interface with Si may be realized because of reaction at the growing interface.

However, EOT increase is also observed with increasing annealing temperature shown in Figure 3. It implies the excess silicate reaction during annealing process [8]. The increase in EOT with increasing annealing temperature has been also reported by previous study [13]. Therefore, it was revealed that small interface state density can be achieved by La-silicate formation using high temperature annealing while EOT is also concurrently increased.

IV. MIPS STACKS WITH HIGH TEMPERATURE ANNEALING

Next, our approach to solve the problem for accomplishing the scaled EOT with nice interfacial property is described in terms of oxygen control and experimentally demonstrated. It has been reported that silicate reaction is basically triggered by the presence of oxygen during annealing process [8]. Since the W metal has material nature of high oxygen diffusivity [15], it is considered that residual oxygen in annealing furnace may be introduced through the W metal during high temperature annealing. It has been reported that poly-Si can prevent the oxygen diffusion from atmosphere [16]. Thus, metal inserted poly-Si (MIPS) stacks is attracted much attention for suppressing excess oxygen incorporation.
Figure 4 shows the concept to accomplish the scaled EOT with nice interfacial property based on oxygen control by MIPS structure and device fabrication process. The Si layer plays a role to inhibit the oxygen diffusion from atmosphere while thin W layer supplies the oxygen into gate dielectrics to cause the silicate reaction at La$_2$O$_3$/Si interface [17]. TiN is as barrier layer for reaction between Si and W. TiN/W stacks and W single layer were also prepared to investigate the impact of MIPS stacks. The thickness of Si, TiN and W are 100nm, 10nm and 5nm, respectively. Post-metallization annealing was performed at 800 °C for 30 min in forming gas ambient with various gate structures. Si layer was removed after post-metallization annealing by wet etching using TMAH for electrical measurement [18].

Figure 5 (a) shows the impact of gate structures on gate-channel (C$_{gc}$-V) capacitances of nMOSFETs. To properly compare the effect of MIPS stacks, La$_2$O$_3$ and W were deposited in one experiment. EOT increase caused by high temperature annealing is drastically suppressed by MIPS stacks. This is the experimental evidence that excess oxygen is incorporated from atmosphere and induces the excess silicate reaction. Moreover, no hump in C$_{gc}$-V curve is also confirmed. Figure 5 (b) shows the I$_d$-V$_g$ characteristics of nMOSFETs normalized by the threshold voltage (V$_{th}$). The sub-threshold slope (SS) is 65~70 mv/dec irrespective of gate structures, indicating the high quality of interface.

Figure 6 shows cross-sectional TEM images. The increase in physical thickness due to interfacial layer growth can be observed from W single layer. On the other hand, no interfacial layer growth can be observed from MIPS and TiN/W devices. Based on the cross-sectional TEM observations, an average k-value (k$_{av}$) in overall gate dielectrics is also shown in Figure 6. A k-value of ~16 can be obtained by combination of MIPS stacks with high temperature annealing. Moreover, the La-silicate by high temperature annealing forms amorphous structure and no crystalline was observed from cross-sectional TEM images. The amorphous form of the La-silicate by high temperature annealing has been also reported [14].

Figure 7. (a) Gate-channel capacitance, and (b) effective electron mobility, respectively. EOT of 0.62 nm with effective electron mobility of 155 cm$^2$/Vsec at 1MV/cm is obtained.
By scaling down the La$_2$O$_3$ thickness, the EOT of 0.62 nm can be attained with MIPS structure in direct contact La-silicate/Si stacks shown in Figure 7 (a). No frequency dispersion can be confirmed, indicating high quality La-silicate/Si interface. The effective electron mobility of 155 cm$^2$/V·sec at 1MV/cm is obtained shown in Figure 7 (b).

Figure 8. (a) Gate leakage current density at $V_g$ of 1 V, and (b) effective electron mobility at 1MV/cm compared with HfO$_2$ dielectrics, respectively.

The gate leakage current density at $V_g$ of 1 V is shown in Figure 8 (a). The gate leakage current density is two orders of magnitude lower than that of ITRS roadmap. Excellent dispersion can be confirmed, indicating high quality La-silicate/Si stacks shown in Figure 8 (b). The effective electron mobility of 155 cm$^2$/V·sec at 1MV/cm is comparable to that of HfO$_2$ gate dielectrics [5]. This is because the effective electron mobility of La-silicate gate dielectrics is dramatically suppressed by introduction of MIPS structure in direct contact La-silicate/Si interface. The effective electron mobility of 155 cm$^2$/V·sec at 1MV/cm with an EOT of 0.62 nm has been obtained owing to the improvement of interfacial property by MIPS structure in conjunction with high temperature annealing.

V. CONCLUSIONS

The problem and concept to control La-silicate/Si interface has been described and experimentally demonstrated for further EOT scaling. Interfacial property can be improved by high temperature annealing with significant increase in EOT. Excess EOT increase caused by high temperature annealing has been dramatically suppressed by introduction of MIPS stacks. The effective electron mobility of 155 cm$^2$/V·sec at 1MV/cm with an EOT of 0.62 nm has been obtained owing to the improvement of interfacial property by MIPS structure in conjunction with high temperature annealing.

REFERENCES