Evaluation of interface state density in three-dimensional SiO₂ gated MOS capacitors

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Outline

1. Background of this study
2. Purpose of this study
3. Experiment process and measurement:
   Quasi-static method and Conductance method
4. Modeling for extraction of interface state density of bulk silicon Fin
5. Summary
Background: CMOS Scaling

- Short-channel effect

Planar downsizing is coming to a limitation

Scaling of successive generations of MOSFETs into the nanoscale regime (from Intel)
(http://www.technologyreview.com/computing/37526/page2/)
Background: Prospect of 3D Channel Structure

32-nm transistor used in Intel’s chips today

New three-dimensional 22-nm transistor will be used in Intel’s chips in the near future

1. Better Control of Channel
2. Lower Power Consumption
3. High Performance Operation

✓ 3D Channel Structure is a promising choice for further downsizing
Background: Interface State Density of 3D Structure

Interface state density is strongly dependent on surface orientation and process.

It is very necessary to know the distribution of \( D_{it} \) in 3D channel.
Purpose of This Work

Evaluation of Interface state density of MOS capacitance with 3D channel

1. Conductance Method and Quasi-static Method are adopted to evaluate the interface state density of bulk silicon Fin MOS device.

2. A modeling of conductance spectra by deconvolution has been proposed in this study. The conductance spectra can be expressed by weighted average of the top and side surfaces of Fin.
Fabrication Process

- **p-Si (100) and (110) planar substrate**
- **Silicon bulk Fin with the height of 50nm substrate**
- SPM+HF cleaning
- Dry oxidation for 30 min, O₂ 1L/min
- Gate metal (W) deposition by RF magnetron sputter
- Electrode patterning process
- Al contact formation on backside
- F.G. annealing at 420°C for 30min

Characteristic Measurement
SEM images of Fin MOS

Bulk Si Fin with the height of 50 nm

Dry oxidation 30min 1L/min

The Fin sample area is 50 µm x 51 µm (Length x Width).

Due to the oxidation retardation in convex and concave, there is no big difference between SiO2 on the top and side surfaces.

From the SEM image, it is roughly evaluated that (100)-oriented and (110)-oriented surface is respectively 80% and 20% of the total area.
A comparison of C-V characteristics of 3D and planar devices

Roughly equal $C_{ox}$ shows the similar $Tox$ in Fin and (100) planar.

The lower capacitance in inversion may be due to the Fully-depletion in Fin.
In the quasi-static method, the low frequency means the interface traps can respond to the measurement ac probe frequency, and at the high frequency, the interface states are assumed not to respond.
Extraction of $D_{it}$ of Planar and Fin by Quasi-static Method

Energy distribution of $D_{it}$ in Planar and Fin is extracted by quasi-static method.
Conductance Method

**Equivalent circuit**

\[ V \boxed{\frac{G}{\omega}} = \frac{qD_{it}}{2\omega\tau_{it}} \ln\left[1 + \left(\omega\tau_{it}\right)^2\right] \]

(Continuous level)

\[ P(\psi_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(\psi_s - \bar{\psi}_s)^2}{2\sigma^2}\right) \]

(Surface potential fluctuation)

**Simplified circuit**

**Measured circuit**

Time constant is dependent on orientation

\[ \frac{G_P}{\omega} = q \int_{-\infty}^{\infty} \frac{D_{it}}{\omega\tau_{it}} \ln\left[1 + \left(\omega\tau_{it}\right)^2\right]P(\psi_s) d\psi_s \]

This equation considers the continuous level of interface trap and the surface potential fluctuation.
Extraction of $D_{it}$ of Planar and Fin by Conductance Method

Energy distribution of $D_{it}$ in Planar and Fin is extracted by conductance method.
A Rough Simulation of Surface Potential of Fin

Simulation results show the same tendency and value approximation of the two surfaces.

It can be approximated that the top and side surfaces are roughly the same as planars.
A Modeling of Conductance Spectra by Deconvolution

So far,

1. Fin used in this study is mainly composed of (100) and (110) oriented surfaces.

2. From the SEM image, (100) and (110) area ratios in the total area are obtained respectively: 80% and 20%.

3. Surface potential fluctuation and time constant of (100) and (110) oriented planar devices are respectively obtained by conductance method.
A Modeling of Conductance Spectra by Deconvolution

20% of (110) component + 80% of (100) component = Fin

Conductance spectra of Fin is roughly fitted by this modeling.
1. Conductance method and Quasi-static method have been adopted in this study to obtain characteristics of interface state density of three-dimensional MOS devices.

2. A modeling of conductance spectra by deconvolution has been proposed in this study. The conductance spectra can be expressed by weighted average of the (100) and (110) oriented surfaces.
Background: CMOS Scaling

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Background: Reliability of 3D Structure

Bad effects of Interface State Density

- Change the silicon charge distribution and the surface potential
- Give rise to an additional capacitance component in parallel with the silicon capacitance
- Contribute to the leakage current

Various surface orientations are used as 3D channels

SiNW FET

Interface state density is strongly dependent on surface orientation and process.


S. Ogata, et al., APL, 98, 092906 (2011)
The energy distribution of interface state density of Fin by this modeling has the same tendency as quasi-static method.
Bad effects:
- Change the silicon charge distribution and the surface potential
- Give rise to an additional capacitance component in parallel with the silicon capacitance
- Contribute to the leakage current
- Mobility of carrier decreases