2012 Master Thesis

Interface Engineering of Extremely Scaled Silicate Gate Dielectrics

-EOT of 0.5 nm and beyond-

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High-k materials have been introduced as gate dielectrics to extend device scaling which is hindered due to excess gate leakage current and short channel effects. Rare-earth (RE) oxides such as La$_2$O$_3$ have an advantage to achieve ultimate requirement for an EOT of 0.5 nm, since they can achieve direct contact on Si substrate by forming RE-silicate at high-k/Si interface easily. One of the issues of La$_2$O$_3$ dielectrics is the excess growth of the silicate layer post annealing, which increases EOT. In addition, degradation in the mobility is a commonly observed issue when the thickness of La$_2$O$_3$ or other high-k materials becomes thinner than a certain value. Therefore, the suppression of EOT increase and mobility degradation is of utmost important to achieve high performance MOSFETs. In this thesis, various approaches are employed for interface engineering to overcome these critical issues.

Silicate layer formation is promoted by the presence of oxygen atoms. Thus, as a novel method to control the silicate reaction, the influence of the thickness of W
which is an oxygen-containing gate metal on the electrical characteristics has been investigated. Almost no change in EOT from the as-deposited condition was observed and an appropriate transistor operation at EOT of 0.5 nm has been confirmed by short time annealing at high temperature. However, small effective mobility indicates the existence of fixed charges induced by oxygen vacancies and metal atoms diffusion from gate electrode. A thin layer of Si was deposited between W and La$_2$O$_3$ to create an amorphous La-silicate layer at gate metal/La$_2$O$_3$ interface, anticipating a reduction of the fixed charges enhanced by the grain boundaries within high-k layer. As a result, net positive fixed charges were reduced and a large improvement in mobility has been confirmed.

Moreover, the effect of annealing ambient gas during silicate formation on device electrical characteristics has been investigated, suspecting the formation of oxygen vacancies induced by annealing in reducing ambient. It has been confirmed that the high-k dielectric oxygen vacancies can be prevented by separating the annealing process for silicate formation and for dangling bond termination. Consequently, La$_2$O$_3$-based MOSFETs with a high temperature annealing in N$_2$ ambient for silicate formation, and a low temperature annealing in FG ambient for dangling bond termination, achieve slightly higher mobility than record data with Hf-based oxide. This is especially apparent at low electric field region. These achievements provide a useful guidance for fabricating MOSFETs with high performance and small EOT.
Contents

Chapter 1. Introduction
1.1 Introduction of high-k materials as gate dielectrics .........................9
1.2 Issues in high-k gate dielectrics ......................................................11
1.3 Reported Hf-based oxides with direct contact structure .............12
1.4 La2O3 as high-k gate dielectrics .....................................................13
1.5 Issues in RE-oxides
   1.5.1 Increase in EOT by high temperature annealing .......................15
   1.5.2 Mobility degradation by EOT scaling........................................18
1.6 Purpose of this study .......................................................................20
References ..............................................................................................22

Chapter 2. Fabrication and Characterization
2.1 Fabrication procedure .....................................................................27
2.2 Experimental principle
   2.2.1 SPM cleaning and HF treatment ...............................................28
   2.2.2 RE-oxides deposition by MBE ...................................................28
   2.2.3 RF magnetron sputtering ..........................................................29
   2.2.4 Dry etching by RIE .................................................................30
   2.2.5 PMA in F.G. ambient .................................................................31
   2.2.6 Wet etching with HCl and BHF ..................................................31
   2.2.7 Vacuum evaporation for Al deposition .......................................31
2.3 Characterization of MOS Device

2.3.1 Threshold voltage extraction..............................................34
2.3.2 Subthreshold slope measurement......................................35
2.3.3 Mobility measurement method based on split $C-V$...............37

References..................................................................................40

Chapter 3. Selection of High-k Dielectrics with Annealing Process

3.1 Introduction...........................................................................42
3.2 Effect of annealing temperature and time..............................44
3.3 CeO$_x$ insertion at Si substrate interface
   3.3.1 Direct contact with Si substrate.................................47
   3.3.2 Comparison of La$_2$O$_3$ and La$_2$O$_3$/CeO$_x$ structure.........51
   3.3.3 Effect of annealing temperature and time with La$_2$O$_3$/CeO$_x$
       stacked gate dielectric......................................................54
3.4 MOSFET characteristics for La$_2$O$_3$/CeO$_x$ dielectric with EOT of
   0.50 nm under different annealing conditions.........................58
3.5 Conclusion...........................................................................62

References..................................................................................63
## Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

4.1 Introduction ................................................................. 66  
4.2 Control of silicate reaction by TiN/W gate electrode .............. 69  
4.3 Effect of W electrode thickness on electrical characteristic ...... 74  
4.4 MOSFET characteristics with thin W film .......................... 81  
4.5 Conclusion ................................................................. 84  
References ........................................................................ 85  

## Chapter 5. Thin Si Insertion at Metal Gate/High-k Interface

5.1 Introduction .................................................................. 89  
5.2 Electrical characteristics for MOS capacitors .................... 94  
5.3 Electrical characteristics for MOS transistors .................... 97  
5.4 Quantitative understanding for mobility improvement ........ 104  
5.5 Conclusion ................................................................. 108  
References ........................................................................ 109  

## Chapter 6. Influence of Annealing Ambient during Silicate Formation on Electrical Characteristics

6.1 Introduction .................................................................. 111  
6.2 Electrical characteristics with capacitors ............................ 115
Chapter 1
Introduction

1.1 Introduction of high-k materials as gate dielectrics
1.2 Issues in high-k gate dielectrics
1.3 Reported Hf-based oxides with direct contact structure
1.4 La$_2$O$_3$ as high-k gate dielectrics
1.5 Issues in RE-oxides
   1.5.1 Increase in EOT by high temperature annealing
   1.5.2 Mobility degradation by EOT scaling
1.6 Purpose of this study
References
1.1 Introduction of high-k materials as gate dielectrics

Metal-oxide-semiconductor field effect transistor (MOSFET) is a requisite element for very large scale integration (VLSI) technology, which is commonly used in modern electronic equipments which are indispensable for our modern life. The progress in VLSI technology thus improves the quality of life. The key to the advancement of VLSI technology is the device scaling which means scaling down the size of MOSFETs. Table 1.1 shows the scaling rules for various device and circuit parameters. Scaling rules show speed up of circuit and reduction of power consumption are obtained with the scaling of the device dimensions [1.1]. Therefore, scaling leads to improvement of convenience for people and saving energy. However, increase in the leakage current due to thinned physical thickness of SiO₂, which have been used as gate dielectrics, has been one of the problems [1.2]. Instead of SiO₂, materials with high dielectric constant (high-k) are required as gate dielectrics of MOSFETs. High-k materials make it possible to thicken physical thickness with the same equivalent oxide thickness (EOT), which means physical thickness can be thickened with the same gate capacitance (Figure 1.1) [1.3]. The EOT can be written as

\[
EOT = \frac{\varepsilon_{SiO_2} t_{ox}}{\varepsilon_{high-k}}, \quad (1.1)
\]

where \(\varepsilon_{SiO_2}\) and \(\varepsilon_{high-k}\) are the permittivity of SiO₂ and that of high-k materials, respectively.

Therefore, study of high-k materials as gate dielectrics is important.
### Table 1.1
Constant-field scaling of MOSFET device and circuit parameters. The scaling remains electrical field unchanged. Speed up of circuit and reduction of power consumption is obtained with the scaling.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Multiplicative factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length (L)</td>
<td>1/s</td>
</tr>
<tr>
<td>Channel width (W)</td>
<td>1/s</td>
</tr>
<tr>
<td>Gate oxide thickness ((t_{ox}))</td>
<td>1/s</td>
</tr>
<tr>
<td>Doping concentration (N)</td>
<td>s</td>
</tr>
<tr>
<td>Device area (A)</td>
<td>1/s²</td>
</tr>
<tr>
<td>Gate capacitance ((C_{ox}))</td>
<td>1/s</td>
</tr>
<tr>
<td>Circuit delay time (t)</td>
<td>1/s</td>
</tr>
<tr>
<td>Power consumption (P)</td>
<td>1/s²</td>
</tr>
</tbody>
</table>

**Figure 1.1** High-k dielectrics make it possible to get larger physical thickness than SiO₂ with same gate capacitance.
1.2 Issues in high-k gate dielectrics

The high-k dielectrics have been studied for advanced MOSFETs mainly with interfacial SiO₂ layer to recover the degraded carrier mobility and enhance reliability [1.4]. However, the thickness of SiO₂ interfacial layer (IL) of small dielectric constant would become a limit of EOT scaling [1.5]. Therefore, direct contact of high-k/Si substrate (without SiO₂-IL structure) is required for further scaling [1.6]. Nowadays, Hf-based oxides have been extensively studied as high-k gate dielectrics and already in practical use. However, Hf-based oxides form SiO₂-IL between high-k dielectrics and Si substrate after annealing (Figure 1.2). In order to achieve a direct contact of high-k/Si, the choice of high-k gate dielectrics is important.

**Fig. 1.2** Cross sectional TEM image of HfO₂ gate dielectrics after annealing. Hf-based oxides form SiO₂-IL easily after annealing.
1.3 Reported Hf-based oxides with direct contact structure

Here are the examples of direct contact of HfO₂/Si structure (Figure 1.3). In the figures on the left hand side, SiO₂-based IL was completely removed when TaN electrode was alloyed with a scavenging element [1.7]. Then, capacitance-voltage (C-V) characteristic shows dramatic EOT scaling with direct contact of high-k/Si. In the figures on the right hand side, there is no SiO₂-IL, where scavenging element is doped in TiN electrode, resulting in achievement of small EOT of 0.54 nm with direct contact structure [1.8]. In both cases, the direct contact of high-k/Si has been achieved by selection of gate material to control the oxygen atoms.


Fig. 1.3 Examples of the direct contact of HfO₂/Si. In the case of Hf-based oxide, the direct contact of high-k/Si has been achieved by controlling the oxygen atoms [1.7, 1.8].
1.4 La$_2$O$_3$ as high-k gate dielectrics

Besides process approaches shown in chapter 1.3, a direct contact of high-k/Si can be achieved using rare-earth oxides (RE-oxides) such as La$_2$O$_3$ as gate dielectrics [1.9-1.10]. A La$_2$O$_3$ can achieve a direct contact of high-k/Si structure by forming a La-silicate layer of fairly high dielectric constant at the high-k/Si substrate interface. Annealing of RE-oxides in oxygen containing atmospheres result in competing reactions of interfacial SiO$_2$ formation by oxygen diffusion through the high-k film.

![Diagram](image)

**Figure 1.4** RE-oxides can achieve direct contact of high-k/Si by forming silicate easily. Cross sectional TEM image of La$_2$O$_3$/Si shows direct contact of high-k/Si by forming La-silicate.
and the RE-oxide to RE-silicate. In contrast to Hf-based oxides, RE-oxides have a much greater driving force to form the silicate [1.11]. The k-value and bandgap of each RE-oxides and its silicate is summarized in table 1.2 [1.12]. Fig. 1.4 shows a cross sectional TEM image of MOS structure with La$_2$O$_3$ dielectric. Direct contact of high-k/Si by forming La-silicate can be seen. In addition, a fairly good interfacial property with a peak effective mobility of over 300 cm$^2$ V$^{-1}$ s$^{-1}$ has been reported for La$_2$O$_3$ gate dielectric [1.13]. Therefore, we select the La$_2$O$_3$ as gate dielectrics.

<table>
<thead>
<tr>
<th>Oxide</th>
<th>Dielectric constant</th>
<th>$E_g$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>La$_2$O$_3$</td>
<td>24</td>
<td>5.5</td>
</tr>
<tr>
<td>CeO$_2$</td>
<td>32</td>
<td>3.2</td>
</tr>
<tr>
<td>Pr$<em>6$O$</em>{11}$</td>
<td>32</td>
<td>5.5</td>
</tr>
<tr>
<td>La-silicate</td>
<td>~9</td>
<td>6.4</td>
</tr>
<tr>
<td>Ce-silicate</td>
<td>~21</td>
<td>6.1</td>
</tr>
<tr>
<td>Pr-silicate</td>
<td>~10</td>
<td>6.5</td>
</tr>
</tbody>
</table>

*Table 1.2* dielectric constant and bandgap of RE-oxides and its silicates [1.12].
1.5 Issues in RE-oxides

1.5.1 Increase in EOT by high temperature annealing

As described in chapter 1.1, EOT scaling is required for performance improvement of MOSFETs. Figure 1.5 shows the EOT requirement as a function of year [1.14]. In the near future, extremely small EOT of 0.5 nm is required for high-k gate dielectrics. RE-oxides have an advantage to achieve EOT requirement, since it can achieve direct contact of high-k/Si easily. However, one of the issues of RE-oxides is increase of EOT by high temperature annealing [1.15]. Annealing temperature dependence of EOT for La$_2$O$_3$ gate dielectric is shown in figure 1.6. The increase of EOT accompanied with increase of annealing temperature can be confirmed.

![Figure 1.5](image_url)

*Figure 1.5* EOT requirements of ITRS 2009. An extremely small EOT of 0.5 nm is required in the near future.
Figure 1.6 Annealing temperature dependence of EOT with La$_2$O$_3$ dielectric. An EOT is increased by high temperature annealing.

Figure 1.7 Si 1s photoelectron spectra arising from La$_2$O$_3$ deposited sample. A positive correlation of the amount of La-silicate layer with annealing temperature is observed.
Figure 1.7 shows Si 1s photoelectron spectra arising from La$_2$O$_3$ deposited sample measured by XPS as a function of annealing temperature. A positive correlation of the amount of La-silicate layer with annealing temperature is observed. Therefore, the increase of EOT accompanied with the increase of annealing temperature is considered to be due to excess growth of silicate layer. To meet the requirement of EOT scaling, excess silicate formation has to be prevented.
1.5.2 Mobility degradation by EOT scaling

Figure 1.8 shows the peak effective electron mobility of La$_2$O$_3$ gated MOSFETs as a function of EOT [1.13]. It is confirmed that the mobility degradation accompanied with the EOT scaling is occurred. This mobility degradation is anticipated to reduce effectiveness of scaling. Interfacial trap density and subthreshold slope of La$_2$O$_3$ gated MOSFETs as a function of EOT is shown in figure 1.9. Characteristics degradation accompanied with the EOT scaling is observed as well as mobility degradation.

![Figure 1.8](image-url)

**Figure 1.8** Peak effective electron mobility of La$_2$O$_3$ gated MOSFETs as a function of EOT. The mobility degradation accompanied with the EOT scaling is observed [1.13].
Chapter 1. Introduction

- 19 -

Figure 1.9 Interfacial trap density and subthreshold slope of La$_2$O$_3$ gated MOSFETs as a function of EOT. Characteristics degradation accompanied with the EOT scaling is observed as well as mobility degradation. [1.16]

It is reported that the metal atoms diffused from gate electrode to gate dielectrics degrade the interfacial properties [1.16]. Moreover, mobility degradation accompanied with EOT scaling by generation of fixed charges induced by oxygen vacancies or metal atoms diffused from the gate electrode [1.17, 1.18]. In any case, the fixed charges play an important role for the mobility degradation.
1.6 Purpose of this study

As discussed in previous chapter, the suppression of the increase in EOT and that of mobility degradation are important to achieve MOSFETs with high performance. In this thesis, novel methods to overcome these issues are investigated by various approaches.

In chapter 3, the effect of short time annealing at high temperature is examined to suppress the EOT increase by high temperature annealing. Moreover, a gate stack structure using CeO$_x$ which can form silicate layer with high permittivity is investigated.

In chapter 4, as a method to control the amount of oxygen atoms supplied, the influence of the thickness of an oxygen-containing gate metal on the electrical characteristics is investigated to control the silicate reaction during high temperature annealing.

In chapter 5, a thin amorphous La-silicate layer formed by Si deposition at the interface of W and La$_2$O$_3$ is examined, anticipating formation of the amorphous La-silicate layer at the metal gate/La$_2$O$_3$ interface eliminate the grain boundaries. As a result, diffusion of metal atoms thorough grain boundaries and oxygen vacancies segregated at grain boundaries might be reduced. Then, its effect on the electrical characteristics at scaled EOT has been observed.

In chapter 6, the effect of annealing ambient during silicate formation on electrical characteristics is examined, being anxious about formation of oxygen vacancies induced by annealing in reducing ambient. The fabricated samples are subjected to annealing in F.G. or N$_2$ ambient.

Finally, chapter 7 summarizes this study.
As described above, chapter 1 summarizes the background and the purpose of this study. Figure 1.10 shows the contents of this thesis. This thesis is consisted of 7 parts.

\[\text{Diagram}\]

Figure 1.10 Contents of this thesis
Chapter 1. Introduction

References


Chapter 2
Fabrication and Characterization

2.1 Fabrication procedure

2.2 Experimental principle
   2.2.1 SPM cleaning and HF treatment
   2.2.2 RE-oxides deposition by MBE
   2.2.3 RF magnetron sputtering
   2.2.4 Dry etching by RIE
   2.2.5 PMA in F.G. ambient
   2.2.6 Wet etching with HCl and BHF
   2.2.7 Vacuum evaporation for Al deposition

2.3 Characterization of MOS Device
   2.3.1 Threshold voltage extraction
   2.3.2 Subthreshold slope measurement
   2.3.3 Mobility measurement method based on split $C-V$

References
2.1 Fabrication procedure

Fig. 2.1 shows the fabrication flow of capacitors and transistors. MOS capacitors and transistors were fabricated on HF-last n-type Si (100) substrates. Thin films of RE-oxides (La$_2$O$_3$, CeO$_x$, and Pr$_6$O$_{11}$) were successively deposited by MBE. A tungsten film was in situ deposited by magnetron sputtering to avoid any moisture or carbon-related contamination. The gate electrodes were patterned by reactive-ion etching (RIE) with SF$_6$. The samples were subjected to RTA at different annealing conditions. In order to contact with source and drain of transistor, RE-oxides and SiO$_2$ were etched by HCl and buffered HF (BHF). Al contact layers on the front and backside of the substrate were deposited by thermal evaporation.

**Figure 2.1 Experimental procedure of capacitor and transistor**
2.2 Experimental principle

2.2.1 SPM cleaning and HF treatment

Particles and organic substance at the surface of Si substrate become a cause of false operation. Therefore, it is important to clean the surface of Si substrate. SPM cleaning is one of the effective cleaning methods. The cleaning liquid is made from H₂O₂ and H₂SO₄ (H₂O₂:H₂SO₄ = 1:4). Because of its oxidizability, particles and organic substance are oxidized and separated from the surface of Si substrate. However, the surface of Si substrate is oxidized and SiO₂ is formed during SPM cleaning. 1% HF is used to eliminate the SiO₂.

2.2.2 RE-oxides deposition by MBE

Molecular beam epitaxy (MBE) is one of the deposition methods for crystalline growth, which is classified into vacuum evaporation. A source material of RE-oxide is heated by electron beam (E-beam) and emits the molecules. The deposition is done in ultra high vacuum (~10⁻⁶ Pa), so that the molecule of RE-oxide doesn’t absorb the scattering of other molecules and be deposited on substrates. The physical thickness of deposited film is measured by crystal oscillator. Fig. 2.2 shows a schematic illustration of MBE.
2.2.3 RF magnetron sputtering

Tungsten which is used as gate electrode in this study is deposited by radio frequency (RF) magnetron sputtering with Ar gas. An RF with 13.56 MHz at a power of 150 W is applied between substrate side and target (W) side. Because of the difference of mass, Ar ions and electrons are separated. A magnet is set underneath the target, so that the plasma damage is minimized. Electrons run through the circuit from substrate side to target side, because substrate side is subjected to be conductive and target side is subjected to be insulated. Then, target side is negatively biased and Ar ions hit the target.
2.2.4 Dry etching by RIE

Reactive ion etching (RIE) is one of the patterning methods. Etching gas becomes the plasma in a similar way in the case of RF sputtering. However, RIE is not only physical but also chemical reaction. For etching of tungsten, SF$_6$ chemistry is used as etching gas in this study. The tungsten which is uncovered with resist reacts with F$^-$ and becomes WF$_6$ which is gas at room temperature. When the resist is eliminated, O$_2$ is used as etching gas and this process is called ashing.

Figure 2.3 Schematic illustration of RF magnetron sputtering.
2.2.5 PMA in F.G. ambient

Post metallization annealing (PMA) is effective to recover the defects in the dielectric film, which is made during fabrication process such as sputtering. In addition, PMA is done in forming gas (F.G.) (N₂:H₂=97:3), so that the effect of terminating the dangling bonds with H⁺ at the interface of high-k/Si substrate is obtained. Dangling bonds are become a causes of interfacial trap. Therefore, PMA is a very important factor to achieve high quality MOS devices. In this study, different annealing conditions such as annealing time and annealing temperature are examined.

2.2.6 Wet etching with HCl and BHF

HCl and buffered HF (BHF) are used for wet etching process. When the RE-oxides uncovered with resist are etched, HCl is used as etching liquid which is called etchant. When the SiO₂ is etched, BHF is used as etchant.

2.2.7 Vacuum evaporation for Al deposition

Al for wiring and backside contact is deposited by vacuum evaporation. Al source is set on W boat and heated up to boiling point of Al by joule heating. However, melting point of W is higher than boiling point of Al, W boat doesn’t melt. The base pressure in the chamber is maintained to be 10⁻³ Pa (Fig. 2.4).
Figure 2.4 Schematic illustration of vacuum evaporation.

~10^{-3} \text{ Pa}

quartz thickness monitor

Al source

W boat
A schematic illustration of MOSFET fabrication process is put together in Fig 2.5.

Figure 2.5 Schematic illustration of MOSFET process.
2.3 Characterization of MOS Device

2.3.1 Threshold voltage extraction

Threshold voltage \( V_{th} \) is an important MOSFET parameter. However, \( V_{th} \) is a voltage that is not uniquely defined [2.1]. The existent of nonlinear curve at subthreshold region on the \( I_d-V_g \) plot make it difficult to have a universal definition. One of the most common threshold voltage measurement techniques is the “linear extrapolation method” with the drain current measured as a function of gate voltage at a low drain voltage of 50-100 mV to ensure operation in the linear MOSFET region [2.1]. The drain current is not zero below threshold and approaches zero only asymptotically. Hence the \( I_d \) versus \( V_g \) curve is extrapolated to \( I_d=0 \), and the threshold voltage is determined from the extrapolation or intercept gate voltage \( V_g \) by

\[
V_{th} = V_{Gt} - \frac{V_d}{2}
\]

(2.1)

where \( V_{Gt} \) is the intercepted \( V_g \) value at \( I_d=0 \) and \( V_d \) is the drain voltage used during the measurement (50 mV in this study).

The \( I_d-V_g \) curve deviates from the straight line at low gate voltage below threshold voltage due to subthreshold currents and above threshold voltage due to series resistance and mobility degradation effects. Thus, in order to determine the threshold voltage accurately, it is a common practice to find the point of maximum slope on the \( I_d-V_g \) curve by maximum in the transconductance \( (g_m) \), fit a straight line to the \( I_d-V_g \) curve at the point and extrapolate to \( I_d=0 \), as illustrated in figure 2.6 [2.1].
2.3.2 Subthreshold slope measurement

Depending on the gate and source-drain voltages, a MOSFET device can be biased in one of the three following regions; subthreshold, linear or saturation. In the subthreshold region where \( V_g < V_{th} \), the drain on the linear scale appears to approach zero immediately below the threshold voltage. However, on a logarithmic scale, the descending drain current remains at nonnegligible levels for several tenths of a volt below threshold voltage [2.2]. This is because the inversion charge density does not drop to zero abruptly. Rather, it follows an exponential dependence on gate voltage. Subthreshold behavior is of particular important in modern ULSI application because it describes how a MOSFET device switches off (or turns on).

Figure 2.6 Threshold voltage determination by the linear extrapolation technique.
The subthreshold current is independent of the drain voltage once drain voltage is larger than a few kT/q, as would be expected for diffusion-dominated current transport. The dependence on gate voltage, on the other hand, is exponential with an inverse subthreshold slope [2.2].

$$S.S. = \left( \frac{d \log_{10} I_{ds}}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{ds}}{C_{ox}} \right)$$

(2.2)

Subthreshold slope, which is that gate voltage necessary to change the drain current by one decade, is typically 70-100 mV/decade in modern MOSFET device [2.2]. Figure 2.7 illustrates the determination technique of subthreshold slope from log $I_d$ versus linear $V_g$ plot.

*Figure 2.7 Determination technique of subthreshold slope.*

If the oxide/Si interface trap density is high, the subthreshold slope will be more graded since the capacitance associated with the interface is in parallel with the
depletion capacitance $C_{dm}$. Hence eq. (2.2) can be rewritten as

$$S.S. = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{dm}}{C_{ox}} \right) = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{dm} + C_{it}}{C_{ox}} \right)$$

(2.3)

where $C_{it}$ is the interface trap capacitance. The direct relationship between S.S. and $C_{it}$, as shown in eq. (2.3) can be used as an index of quality of interfacial property.

2.3.3 Mobility measurement method based on split C-V

The MOSFET drain current is due to drift and diffusion of the mobile carriers in the inverted Si channel. Let consider an n-channel device of gate length $L$ and gate width $W$ for the derivation. The derivation for p-channel device is similar to n-channel device with minor changes. The drain current $I_d$ can be written as

$$I_d = \frac{W\mu_{eff}Q_{inv}V_{ds}}{L} - W\mu_{eff} \frac{kT}{q} \frac{dQ_{inv}}{dx}$$

(2.4)

Where $Q_{inv}$ is the carrier channel charge density and $\mu_{eff}$ is the effective mobility. The effective mobility is measured at low drain voltage under 100 mV. At low $V_{ds}$, one can assume that channel charge to be fairly distribute and uniform from the source to drain, allowing the diffusive second term in eq. (2.4) to be dropped. Solving eq. (2.4) then gives,

$$\mu_{eff} = \frac{g_dL}{WQ_{inv}}$$

(2.5)

where the drain conductance $g_d$ is defined as

$$g_d = \frac{\partial I_d}{\partial V_{ds}} \bigg|_{V_j = constant}$$

(2.6)

To accurately determine the $Q_{inv}$, direct measurement of $Q_{inv}$ from 100 kHz high
frequency capacitance measurement, with mobile channel density or inverted charge
density determined from the gate-to-channel capacitance/unit area ($C_{gc}$) according to
the following equation

$$Q_{\text{inv}} = \int_{V_{fb}}^{V_g} C_{gc} dV_g$$  \hspace{1cm} (2.7)

where $V_{fb}$ and $V_g$ are the flatband voltage and gate voltage, respectively. The $C_{gc}$ is
measured by using the connection of figure 2.8 (a). The capacitance meter is
connected between the gate and the source-drain connected together with substrate
grounded. Setup in figure 2.8 (b) is used to measure the gate-to-substrate
capacitance/unit area ($C_{gb}$). The connected source-drain is grounded during $C_{gb}$
measurement. $C_{gb}$ is used to calculated bulk charge density ($Q_b$) according to the
following equation

$$Q_b = \int_{V_{gs}}^{V_{gs}} C_{gb} dV_g$$  \hspace{1cm} (2.8)

Both $Q_{\text{inv}}$ and $Q_b$ are then used to calculate the effective vertical electric field ($E_{\text{eff}}$)
according to

$$E_{\text{eff}} = \frac{Q_b + \eta Q_{\text{inv}}}{\varepsilon_S}$$  \hspace{1cm} (2.9)

where $\eta$ is the inversion layer charge accounts for averaging of the electric field over
the electron distribution in the inversion layer. The parameter $\eta=1/2$ for the electron
mobility and $\eta=1/3$ for the hole mobility. The $\varepsilon_S$ is the Si permittivity [2.3-2.5]. In
this study, $C_{gc}$ is measured at 100 kHz. The $\mu_{\text{eff}}$ and $g_d$ are extracted from the area of
$C_{gc}$-$V_g$ characteristic and the slope of the $I_{ds}$-$V_{ds}$ characteristic, respectively as shown
in figure 2.9 (a) and (b).
Figure 2.8 Configuration for (a) gate-to-channel, (b) gate-to-substrate capacitance measurement for split C-V measurement. [2.4]

Figure 2.9 (a) $Q_{\text{inv}}$ is obtained from $C_{gc}$-$V_g$ characteristic. (b) $g_d$ is obtained from $I_{ds}$-$V_{ds}$ characteristic.
References


Chapter 3

Selection of High-k Dielectrics with Annealing Process

3.1 Introduction

3.2 Effect of annealing temperature and time

3.3 CeOx insertion at Si substrate interface
   3.3.1 Direct contact with Si substrate
   3.3.2 Comparison of La₂O₃ and La₂O₃/CeOₓ structure
   3.3.3 Effect of annealing temperature and time with La₂O₃/CeOₓ stacked gate dielectric

3.4 MOSFET characteristics for La₂O₃/CeOₓ dielectric with EOT of 0.50 nm under different annealing conditions

3.5 Conclusion

References
3.1 Introduction

Electrical characteristics of MOS devices are strongly affected by annealing conditions such as annealing time and temperature. Figure 3.1 shows charge pumping current as a function of pulse frequency [3.1]. Small charge pumping current corresponds to the small interfacial trap density ($D_{it}$). The smaller $D_{it}$ is observed as an annealing temperature becomes high.

![Figure 3.1](image)

**Figure 3.1** Annealing temperature dependence of charge-pumping current for $La_2O_3$ gated nMOSFET. Smaller $D_{it}$ is obtained with higher temperature annealing. [3.1]

The annealing temperature dependence of the effective electron mobility is shown in figure 3.2 [3.1]. All the nMOSFETs compared in figure 3.2 are same EOT of 1.3 nm. Higher effective electron mobility is obtained with higher temperature annealing. In particular, effective electron mobility is largely improved at low effective electric
field ($E_{\text{eff}}$) region. It can be considered that the improvement of mobility is occurred by suppression of Coulomb scattering induced by interfacial trapped charges and fixed oxide charges [3.2].

![Graph showing electron mobility vs effective electric field for different annealing temperatures.](image)

**Figure 3.2** Annealing temperature dependence of effective electron mobility for La$_2$O$_3$ gated nMOSFET. Mobility improvement is confirmed with high temperature annealing. [3.1]

We can see from the above that high temperature annealing is necessary to fabricate MOS devices with good electrical characteristics. However, as is shown in figure 1.6, high temperature annealing leads to excess silicate formation, which increases the EOT. In this chapter, therefore, the effect of short time annealing at high temperature is examined. Moreover, a gate stack structure using CeO$_x$ which can form silicate layer with high permittivity is investigated.

- 43 -
3.2 Effect of annealing temperature and time

Annealing temperature dependence on EOT for W(60 nm)/La$_2$O$_3$(3 nm)/n-Si capacitors with annealing duration of 30 min or 2 s is shown in figure 3.3. From this result, it is confirmed that the increase in EOT after annealing can be effectively suppressed by shortening the annealing time.

![Image](image_url)

**Figure 3.3** Annealing temperature dependence of EOT with La$_2$O$_3$ gated capacitors with different annealing time. Increase in EOT is suppressed by shortening the annealing time.

To examine the effect of annealing conditions, leakage current analysis of two capacitors for the same EOT of 1 nm, namely one annealed at 850 °C for 2 s and another at 600 °C for 30 min, are compared. Figure 3.4 shows Leakage current density-electric field ($J_{\text{leak}}$-E) plot of two samples which are same EOT of 1 nm.
From Schottky plot, thermionic emission is dominant at the region where electric field is lower than 4 MV/cm. On the other hand, at the region where electric field is higher than 4 MV/cm, Poole-Frenkel (PF) emission is confirmed from PF plot [3.3]. Comparing the $J_{\text{leak}}$ at the electric field where thermionic emission is dominant, smaller leakage current is obtained with capacitor annealed at 850 °C for 2 s. It can be considered that the conduction band offset at the interface facing to Si substrate is higher with annealing at high temperature due to formation of Si-rich silicate at Si substrate interface (Figure 3.5). In addition to leakage current, the effect of annealing temperature and time on the amount of fixed charges and interfacial property are discussed with other gate dielectric material in chapter 3.

Figure 3.4 $J_{\text{leak}}$-E plots of two samples which are same EOT of 1 nm. Smaller thermionic emission is confirmed for a capacitor annealed at 850 °C for 2 s.
Figure 3.5 Band diagram of $\text{La}_2\text{O}_3$ gated capacitors with different annealing conditions. Si-rich silicate whose barrier height is higher than that of La-rich silicate might be formed with high temperature annealing.
3.3 CeO\textsubscript{x} insertion at Si substrate interface

3.3.1 Direct contact with Si substrate

As is shown in table 1.2, Ce-silicate has high dielectric constant and wide bandgap. Therefore, a capacitor using CeO\textsubscript{x} as a gate dielectric is fabricated. Figure 3.6 shows cross sectional TEM image of CeO\textsubscript{x} on Si after annealing at 500 °C for 30 min. A formation of an SiO\textsubscript{2} interfacial layer is confirmed. To achieve an EOT of ~0.5 nm, a formation of gate stack structure with no SiO\textsubscript{2} interfacial layer is required. Then, La\textsubscript{2}O\textsubscript{3} which can easily form silicate layer with Si is deposited on the CeO\textsubscript{x}, and a La\textsubscript{2}O\textsubscript{3}/CeO\textsubscript{x} gated capacitor is fabricated.

![Figure 3.6](image)

**Figure 3.6** Cross sectional TEM image of CeO\textsubscript{x} on Si after annealing. A formation of SiO\textsubscript{2} interfacial layer is confirmed.
Figure 3.7 C-V characteristics of as-deposited La$_2$O$_3$/CeO$_x$ dielectric capacitor and that annealed at 800 °C for 2 s. Smaller EOT is obtained for annealed capacitor.

An EOT of as-deposited La$_2$O$_3$/CeO$_x$ dielectric capacitor, extracted from capacitance-voltage (C-V) characteristics, is 0.90 nm, whereas that of the capacitor annealed at 800 °C for 2 s is 0.73 nm (Figure 3.7). This result indicates that SiO$_2$-IL changes to silicate layer, whose dielectric constant is higher than that of SiO$_2$, by annealing. Figure 3.8 shows cross sectional TEM image of La$_2$O$_3$/CeO$_x$ on Si after annealing. A direct contact of high-k/Si structure without SiO$_2$-IL is confirmed. A uniform contrast indicates a compositional uniformity of amorphous LaCe-silicate. Figure 3.9 shows the observed photoelectron intensity ratio I(Ce)/I(La) as a function
Chapter 3. Selection of High-k Dielectrics with Annealing Process

Figure 3.8 Cross sectional TEM image of La$_2$O$_3$/CeO$_x$ dielectric capacitor after annealing at 800 °C for 2 s. A direct high-k/Si structure is confirmed. A uniform contrast indicates a compositional uniformity.

Figure 3.9 Intensity ratio of Ce 3d$_{5/2}$ to La3d$_{5/2}$ by angle-resolved XPS analysis confirms the silicate layer and intermixing of Ce and La atoms, especially when annealed at high temperature. [3.4]
of photoelectron take-off angle. Here, $I(\text{Ce})$ and $I(\text{La})$ are the intensity of Ce 3d$_{5/2}$ and La 3d$_{5/2}$ spectra arising from W/La$_2$O$_3$/CeOx/Si structure [3.4]. This result indicates that the diffusion of Ce and La atoms occurs at La$_2$O$_3$/CeOx interface, especially when annealed at high temperature. Thus, it is considered that direct contact of LaCe-silicate/Si is achieved by La atoms, which can easily form silicate layer, diffusion to Si substrate interface.
3.3.2 Comparison of La$_2$O$_3$ and La$_2$O$_3$/CeO$_x$ structure

Figure 3.10 shows the Annealing temperature dependence of EOT for W(60 nm)/La$_2$O$_3$(3 nm)/$n$-Si and W(60 nm)/La$_2$O$_3$(2 nm)/CeO$_x$(1 nm)/$n$-Si capacitors with different annealing time. A suppression of EOT increase after annealing at both 800 °C for 2 s and 500 °C for 30 min are confirmed with CeO$_x$ insertion at Si substrate interface. As discussed in chapter 3.3.1, this result is due to formation of silicate layer with high dielectric constant.

\[\text{Figure 3.10} \text{ Annealing temperature dependence of EOT for W(60 nm)/La}_2\text{O}_3(3 \text{ nm})/n-\text{Si and W(60 nm)/La}_2\text{O}_3(2 \text{ nm})/\text{CeO}_x(1 \text{ nm})/n-\text{Si capacitors with different annealing time. Increase in EOT is suppressed by CeO}_x\text{ insertion.}\]
Figure 3.11 C-V characteristics of W(60 nm)/La$_2$O$_3$(3 nm)/n-Si and W(60 nm)/La$_2$O$_3$(2 nm)/CeO$_x$(1 nm)/n-Si capacitors annealed at 500 °C for 30 min. Lower $D_{it}$ and Smaller EOT are obtained with Si insertion.

C-V characteristics of W(60 nm)/La$_2$O$_3$(3 nm)/n-Si and W(60 nm)/La$_2$O$_3$(2 nm)/CeO$_x$(1 nm)/n-Si capacitors annealed at 500 °C for 30 min are shown in figure 3.11. It is observed that the hump shapes of C-V curve, which is due to interfacial traps, is smaller with CeO$_x$ inserted capacitor, as well as an EOT. Figure 3.12 shows X-ray photoelectron spectroscopy (XPS) of each RE-silicate after annealing at 500 °C for 30 min. The Si 1s spectra arising from the La, Ce, and Pr-silicate gated samples reveal compositional differences in the layer. Relatively SiO$_2$-rich silicate is formed with Ce-silicate, resulting in fairy nice interfacial property of CeO$_x$ inserted capacitor. (Fig. 3.12) [3.5].
Figure 3.12 Synchrotron XPS measurement through gate metal reveals difference in composition of RE-silicates. Relatively SiO$_2$-rich silicate is formed with Ce-silicate, resulting in fairy nice interfacial property of CeO$_x$ inserted capacitor.
3.3.3 Effect of annealing temperature and time with La$_2$O$_3$/CeO$_x$ stacked gate dielectric

Figure 3.13 shows the C-V characteristics of W(60 nm)/La$_2$O$_3$(1.5-2.5 nm)/CeO$_x$(1 nm)/$n$-Si capacitors with different annealing conditions. Comparing the capacitors annealed at 800 $^\circ$C for 2 s with those annealed at 500 $^\circ$C for 30 min, smaller EOT is achieved for all samples. Moreover, lower $D_{it}$ are confirmed for capacitors annealed at 800 $^\circ$C for 2 s. It can be considered that the profile of mutual diffusion of atoms such as Ce, La and Si is changed by annealing time and temperature. As shown in

![Figure 3.13 C-V characteristics of W(60 nm)/La$_2$O$_3$(1.5-2.5 nm)/CeO$_x$(1 nm)/$n$-Si capacitors with different annealing conditions. From hump shapes of C-V curves, lower $D_{it}$ are confirmed with capacitors annealed at 800 $^\circ$C for 2 s.](image)
Figure 3.5, Si-richer interface might be formed by higher temperature annealing, resulting in lower interfacial trap density for capacitors annealed at 800 °C for 2 s.

Fig. 3.14 shows a flat-band voltage ($V_{fb}$)-EOT plot of W(60 nm)/La$_2$O$_3$(1.5-2.5 nm)/CeO$_x$(1 nm)/n-Si capacitors with different annealing conditions. The fixed charge density ($N_{fix}$) in gate insulator can be calculated from the slope of $V_{fb}$-EOT plot by using eq. 3.1

$$V_{fb} = -\frac{qN_{fix}}{\varepsilon_{SiO_2}} EOT + \Phi_{ms}.$$  

(3.1)

$N_{fix}$=2.4×10$^{13}$/cm$^2$ with capacitors annealed at 500 °C for 30 min and $N_{fix}$=9.1×10$^{12}$/cm$^2$ with those annealed at 800 °C for 2 s are calculated from figure 3.14 [3.6]. Then, small fixed charge density is achieved with annealing at 800 °C for 2 s. A reduction of the fixed charges by high temperature annealing even for short time is confirmed.

![Figure 3.14 V$_{fb}$-EOT plot of W(60 nm)/La$_2$O$_3$(1.5-2.5 nm)/CeO$_x$(1 nm)/n-Si capacitors with different annealing conditions. A calculated fixed charge density from the slopes of plots is smaller for capacitors annealed at 800 °C for 2 s.](image-url)
Figure 3.15 shows the EOT dependence of leakage current density of W(60 nm)/La₂O₃(1.5-2.5 nm)/CeOₓ(1 nm)/n-Si capacitors annealed under different conditions. The J_{leak} of capacitors annealed at 500 °C for 30 min and those annealed at 800 °C for 2 s are meet the requirements of gate leakage current in a roadmap of ITRS 2009 [3.7]. Comparing the J_{leak} of the capacitors annealed at 800 °C for 2 s with those annealed at 500 °C for 30 min in each EOT, smaller leakage current is obtained with short time annealing at high temperature. As described above, higher temperature annealing forms Si-richer silicate layer with wide bandgap and a gate dielectric with smaller fixed charges even by short time annealing. Thus, thermionic emission current is considered to be small. Moreover, PF emission current which

![Graph showing J_{leak}-EOT relation for W(60 nm)/La₂O₃(1.5-2.5 nm)/CeOₓ(1 nm)/n-Si capacitors with different annealing conditions. All samples meet the requirements in the ITRS roadmap and smaller leakage current is obtained by high temperature annealing.](image)

**Figure 3.15** J_{leak}-EOT relation of W(60 nm)/La₂O₃(1.5-2.5 nm)/CeOₓ(1 nm)/n-Si capacitors with different annealing conditions. All samples meet the requirements in the ITRS roadmap and smaller leakage current is obtained by high temperature annealing.
flows thorough traps in the dielectric is also considered to be small. As a result, observed gate leakage current is suppressed by high temperature annealing for 2 s. Because of the good results on CeO$_x$ inserted capacitors with high temperature annealing for 2 s, the MOSFETs with La$_2$O$_3$/CeO$_x$ gate dielectric annealed at 800 °C for 2 s are fabricated and be compared with that annealed at 500 °C for 30 min in the following chapter.
3.4 MOSFET characteristics for La$_2$O$_3$/CeO$_x$ dielectric with EOT of 0.50 nm under different annealing conditions

Fig. 3.16 shows gate to channel capacitance ($C_{gc}$)-gate voltage ($V_g$) characteristic of the $n$MOSFET with W (60 nm)/La$_2$O$_3$ (1.5 nm)/CeO$_x$ (1 nm) gate stack annealed at 800 °C for 2 s. A hysteresis is observed for $C_{gc}$-$V_g$ curve. A measurement error due to excess gate leakage current increases rapidly at the region of $V_g$ > 0.5 V. It is confirmed that the EOT of W (60 nm)/La$_2$O$_3$ (1.5 nm)/CeO$_x$ (1 nm) gate stacked MOSFET annealed at 800°C for 2s is 0.50 nm from $C_{gc}$-$V_g$ curve.

![Figure 3.16](image.png)

**Figure 3.16** $C_{gc}$-$V_g$ curve of W(60 nm)/La$_2$O$_3$(1.5 nm)/CeO$_x$(1 nm) gate stacked MOSFET with EOT of 0.50 nm. A measurement error due to gate leakage current and hysteresis are observed.
Drain-to-source current ($I_{ds}$)-$V_g$ and $I_{ds}$-drain voltage ($V_d$) characteristics of W(60 nm)/La$_2$O$_3$(1.5 nm)/CeO$_x$(1 nm) gate stacked MOSFET annealed at 800°C for 2s are shown in figure 3.17. Operation of EOT=0.50 nm MOSFET is achieved. A relatively large subthreshold voltage swing (SS) values over 130 mV/dec. indicates the presence of large $D_{it}$ and should be improved by further process optimization including the selection of metal gate materials. The effect of metal gate materials is investigated in chapter 4.

![Figure 3.17](image)

**Figure 3.17** (a) $I_{ds}$-$V_g$ and (b) $I_{ds}$-$V_d$ characteristics of W(60 nm)/La$_2$O$_3$(1.5 nm)/CeO$_x$(1 nm) gate stacked MOSFET with EOT of 0.50 nm. Operation of EOT=0.50 nm MOSFET is achieved.
Chapter 3. Selection of High-k Dielectrics with Annealing Process

Fig. 3.18 shows effective electron mobility of W(60 nm)/La$_2$O$_3$(1.5 nm)/CeO$_x$(1 nm) gate stacked MOSFET annealed at 800°C for 2s. Annealing at 500°C for 30min is shown as a reference. The $\mu_{\text{eff}}$ of the MOSFET annealed at 800°C for 2s revealed a peak value of 120 cm$^2$/Vs and 100 cm$^2$/Vs at an effective field of 1 MV/cm. Relatively-high $\mu_{\text{eff}}$ for 800 °C annealing compared with that for 500 °C annealing is considered to be due to smaller fixed charges and interfacial traps as shown in figure 3.13 and 3.15.

![Figure 3.18](image)

**Figure 3.18** Effective electron mobility of MOSFET annealed at 800 °C for 2 s and that annealed at 500 °C for 30 min. Relatively higher effective mobility is observed with high temperature annealing for 2 s.

Fig. 3.19 shows the $\mu_{\text{eff}}$ obtained with annealing at 800°C for 2s at 1 MV/cm together with reported MOSFETs with Hf-based oxides [3.8-3.10]. Our result with RE-oxides marks slightly smaller value than others, however, further process optimization including shorter time annealing with higher temperature may recover the $\mu_{\text{eff}}$. 
Figure 3.19 Effective electron mobility on EOT trend at 1 MV/cm with reported direct contact structure data.
3.5 Conclusion

In order to achieve a direct contact of high-k/Si substrate, La$_2$O$_3$/CeO$_x$ structure as gate dielectric has been investigated. A formation of SiO$_2$-IL is confirmed with CeO$_x$ dielectric. However, it is revealed that SiO$_2$-IL changes to LaCe-silicate layer, whose dielectric constant is higher than that of SiO$_2$, by depositing La$_2$O$_3$ on CeO$_x$. Suppression of an increase of EOT and fairly nice interfacial property are confirmed with CeO$_x$ insertion.

Second, capacitors annealed at 800 °C for 2 s and those annealed at 500 °C for 30 min are compared. It is confirmed that annealing at 800 °C for 2 s is suitable to obtain better electrical property of MOSFETs in terms of EOT, interfacial trap density, fixed charge, and gate leakage current.

And finally, an operation of the MOSFET with an EOT of 0.50 nm has been successfully demonstrated even if RE-oxide is used as gate dielectric. The relatively large S. S. and slightly degraded $\mu_{\text{eff}}$ compared should be improved by further process optimization including the selection of metal gate materials and annealing method.
Chapter 3. Selection of High-k Dielectrics with Annealing Process

References


Chapter 4

Selection of Metal Electrode for Controlling Silicate Reaction

4.1 Introduction
4.2 Control of silicate reaction by TiN/W gate electrode
4.3 Effect of W electrode thickness on electrical characteristics
4.4 MOSFET characteristics with thin W film
4.5 Conclusion
References
4.1 Introduction

As described in chapter 1, one of the issues of La$_2$O$_3$ dielectrics is the excess growth of the silicate layer after annealing, which increases EOT. In chapter 3, annealing time and gate dielectric material is investigated for highly scaled MOSFETs. Next, the effect of gate metal on electrical characteristics including EOT is examined. Silicate layer formation is promoted by the presence of oxygen atoms as shown in following chemical reaction of

$$\text{La}_2\text{O}_3 + \text{Si} + n\text{O}_2 \rightarrow \text{La}_2\text{SiO}_5, \text{La}_{10}(\text{SiO}_4)_6\text{O}_3, \text{La}_{9.33}\text{Si}_6\text{O}_{26}, \text{La}_2\text{Si}_2\text{O}_7$$

Thus, an excess supply of oxygen atoms results in the excess silicate layer formation. On the other hand, an insufficient oxygen atom supply leads to the formation of oxygen vacancies, which results in mobility degradation [4.1]. Hence, controlling the amount of oxygen atoms is important for achieving MOSFETs with an EOT of 0.5 nm without degrading electrical characteristics. It is known that W, Mo, and column VA metals such as Ta contain oxygen atoms depending on the free energy of oxygen [4.2-4.4]. Secondary ion-microprobe mass spectrometry (SIMS) analysis revealed oxygen concentration of $\sim 10^{22}$ atoms/cm$^3$ for W electrode used in this study (Figure 4.1). In this chapter, as a method to control the amount of oxygen atoms supplied, the influence of the thickness of an oxygen-containing gate metal on the electrical characteristics is investigated. A schematic concept of the oxygen supply control method is illustrated in figure 4.2.
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

Figure 4.1 Oxygen profile of the W electrode layer obtained by SIMS analysis. Oxygen concentration of ~$10^{22}$ atoms/cm$^3$ is revealed.

Figure 4.2 Schematic illustration of oxygen supply control method. Silicate reaction is controlled by the thickness of oxygen-containing metal.
Figure 4.3 shows fabrication process of MOS devices used in this chapter. The oxygen-containing metal s of various thickness such as W, Mo and Ta layers were *in-situ* deposited by RF sputtering. A 40-nm-thick TiN layer was also deposited on some samples. Wafers were subjected to postmetallization annealing (PMA) in FG ambient under different annealing temperatures for 2 s.

*Figure 4.3 Process flow of MOS capacitors and transistors fabricated in this chapter.*
4.2 Control of silicate reaction by TiN/W gate electrode

Figures 4.4 (a)-(c) show the C-V characteristics of Mo, Ta, and W/La$_2$O$_3$(3.5 nm)/n-Si gate stack capacitors annealed at 800 °C for 2 s. From these C-V characteristics, it is confirmed that a smaller EOT is obtained using thinner gate metal capacitors. These results indicate that changing the thickness of an oxygen-containing metal is effective for controlling the amount of oxygen supplied to gate dielectrics. Moreover, the smaller hump shapes of C-V curves are observed for thinner oxygen-containing metal. About a relation of thickness of oxygen-containing meal and hump shapes of C-V curves are discussed later. Having confirmed the oxygen concentration of the W electrode by SIMS (~10$^{22}$ atoms/cm$^3$), W thickness was used as the parameter to control amount of oxygen supplied.

The C-V characteristics of TiN(40 nm)/W(6 nm)/La$_2$O$_3$(3.5 nm)/n-Si gate stack capacitors annealed at 800 oC for 2 s are shown in Fig. 4. Filled circles represent the C-V curve of the capacitor annealed before TiN deposition and open circles represent those annealed after TiN deposition. The reduction of EOT from 0.86 to 0.53 nm is observed with TiN capping. It is reported that oxygen diffusion from the gate dielectric to the TiN electrode is induced by annealing and suppressing EOT increase [4.5]. Then oxygen in the W layer diffuse to TiN electrode, resulting in reduction of amount of oxygen atoms supplied to gate dielectric, which could be the reason for the EOT behavior observed in Fig. 4.4.
Figure 4.4 C-V characteristics of La$_2$O$_3$(3.5 nm)/n-Si gate stack capacitors using (a) Mo, (b) Ta, and (c) W electrodes annealed at 800 °C for 2 s. EOTs positively correlate with the thickness of the metal.
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

Figure 4.5 C-V characteristics of TiN(40 nm)/W(6 nm)La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed at 800 °C for 2 s. Closed dots represent the capacitor annealed before TiN deposition and open dots represent that annealed after TiN deposition.

Figure 4.6 shows EOT dependence on annealing temperature for TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/n-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/n-Si gate stack capacitors annealed for 2 s. The increase in EOT after annealing is well suppressed as the W layer becomes thin and the controllability such as range of EOT from 0.51 to 1.2 nm at 800 °C annealing is confirmed. Moreover, almost no change in EOT from the as-deposited condition occurs with thin W and TiN capping. To ensure the effect of W film thickness on silicate reaction, the dependence of the amount of La-silicate layer on W film thickness is measured by XPS for TiN(10 nm)/W(0-10 nm)/La$_2$O$_3$(3 nm)/n-Si structures. Figure 4.7 shows the Si 1s spectra of the samples with and
without post metallization annealing at 800 °C for 2 s measured at a photoelectron take-off angle of 80°. Here, Si 1s spectral intensities arising from the Si substrate are adjusted to be equal to each other in order to indicate the changes in the La₂O₃/Si interface. The as-deposited sample of the TiN/W (0 nm) electrode shows nearly no silicate reaction. On the other hand, the increase in the number of La-O-Si bonds with the thickness of the W film indicates that silicate reaction could be controlled by changing the thickness of the W film [4.6, 4.7].
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

**Figure 4.6** EOT dependence on annealing temperature for TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/n-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed for 2 s. An increase in EOT after annealing is effectively suppressed by thinning the W thickness.

**Figure 4.7** Si 1s photoelectron spectra arising from TiN(10 nm)/W(0, 3 and 10 nm)/La$_2$O$_3$(3.5 nm)/n-Si structure annealed at 800 °C for 2 s.
4.3 Effect of W electrode thickness on electrical characteristics

C-V characteristics of TiN(40 nm)/W(6 or 12 nm)La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed at 800 °C for 2 s is shown in figure 4.8. A larger right-handed hysteresis window is observed for thinner W electrode capacitor. The hysteresis of $C-V$ curve suggests the existence of traps in the gate dielectric. The windows of the hysteresis in the $C-V$ curves for TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/n-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/n-Si gate stack capacitors annealed for 2 s are summarized in Figure 4.9. It is confirmed that thinner W layer capacitors represent a larger right-handed hysteresis and need further higher-temperature annealing to reduce the hysteresis.

![Figure 4.8](image_url)  
*Figure 4.8 C-V characteristics of TiN(40 nm)/W(6 or 12 nm)La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed at 800 °C for 2 s. A larger hysteresis window is observed with capacitor of thinner W film.*
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

Figure 4.9 Hysteresis window dependence on annealing temperature for TiN(40 nm)/W(6 or 12 nm)La$_2$O$_3$(3.5 nm)/n-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed for 2 s. A ramp rate of measurement is 0.25 V/s. Hysteresis window becomes large when the W film is thin.

As described in chapter 3.3.3, high temperature annealing reduces the traps in the dielectric, which induce the generation of hysteresis. Moreover, this relationship indicates that electron traps are formed near the La$_2$O$_3$/La-silicate interface and in La$_2$O$_3$ [4.8, 4.9], where the distance from the Si substrate has a positive correlation with the amount of oxygen supplied. This implies that $C$-$V$ characteristics with a small EOT as well as a small hysteresis can be obtained by optimization of annealing.
temperature and W film thickness. A TEM image of a TiN(45 nm)/W(3 nm)/La$_2$O$_3$(2.5 nm)/n-Si gate stack capacitor annealed at 800 °C for 2 s reveals that the direct contact of high-k material to the Si structure is obtained (Figure 4.10). An extremely small EOT of 0.43 nm with an average dielectric constant ($k_{av}$) of 22.7 is obtained.

![Figure 4.10 Cross-sectional TEM image of TiN (40 nm)/W(3 nm)/La$_2$O$_3$(2.5 nm)/n-Si capacitor annealed at 800 °C for 2 s. A direct contact structure of high-k/Si is confirmed.](image-url)
The $V_{fb}$-EOT plot measured for TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$/n-Si and W(60 nm)/La$_2$O$_3$/n-Si gate stack capacitors annealed at 800 °C for 2 s is shown in Fig. 4.10. The slopes in the $V_{fb}$-EOT relation show nearly the same trend for all W film thicknesses. However, a negative parallel shift in $V_{fb}$, depending on the thickness of the W film, is observed. Given the result shown in figure 4.7, it can be anticipated that the formation of the La-silicate layer induces the formation of oxygen vacancies or positive fixed charges. Actually, the formation of positive fixed charges in the La-silicate layer due to the metal diffusing from the gate electrode is reported [4.10, 4.11].

![Figure 4.11](image-url)

**Figure 4.11** $V_{fb}$-EOT plot of TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/n-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/n-Si capacitors annealed at 800 °C for 2 s. A parallel $V_{fb}$ shift accompanied with the silicate formation is observed, indicating the formation of positive fixed charges.
Figure 4.11 shows the $C-V$ characteristics of TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/$n$-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/$n$-Si gate stack capacitors annealed at 800 °C for 2 s. A correlation between the hump shapes at the weak inversion region, which are caused by interfacial trap density [4.12], and the amount of the La-silicate layer is revealed. There is a possibility that electron traps in the La-silicate layer contribute to the hump shapes and cause the degradation of $D_{it}$.

![Figure 4.12](image)

**Figure 4.12** $C-V$ characteristics of TiN(40 nm)/W(6 or 12 nm)/La$_2$O$_3$(3.5 nm)/$n$-Si and W(60 nm)/La$_2$O$_3$(3.5 nm)/$n$-Si capacitors annealed at 800 °C for 2 s (inset: scale-up hump shapes at weak inversion region). Smaller hump is obtained for thinner W film capacitor.
To explain the origin of hysteresis, $V_{fb}$ shift and hump shapes observed in figure 4.9, 4.11, and 4.12, a model is proposed as is shown in figure 4.13. In the study of Hf-based oxides, difference of oxygen vacancy energy level between HfO$_2$ and Hf-silicate is reported [4.13, 4.14]. In the band diagrams shown in figure 4.13, assuming oxygen vacancy level in La$_2$O$_3$ is different from that of La-silicate as an analogy from Hf-based oxide, oxygen vacancy levels at flat-band condition in La$_2$O$_3$ are located at a higher energy than Fermi-level ($E_f$) and those in La-silicate are aligned lower than $E_f$. When a positive voltage is applied to the gate to accumulation, electrons are trapped in the oxygen vacancy level in La$_2$O$_3$ or La$_2$O$_3$/La-silicate interface. The trapped electrons generate negative charges which results in right-handed hysteresis, where the hysteresis window degrades as oxygen supply becomes deficient. When a negative voltage is applied to the gate to depletion, electrons at oxygen vacancy levels near $E_f$ in La-silicate respond to AC signal. As a result, a capacitance connected in parallel to depletion capacitance increases and the hump shapes at the weak inversion region is observed.
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

La-silicate
La$_2$O$_3$
Si-substrate
Metal

Trap due to $V_o^{2+}$

Metal induced defects (origin of $V_{fb}$ shift)

Origin of hysteresis

Flat-band condition

Accumulation condition

Origin of humps

Electrons respond to AC signal

Depletion condition

Figure 4.13 Conceivable band diagram model of flat-band, accumulation and depletion conditions.
4.4 MOSFET characteristics with thin W film

Figures 4.14 show the $C_{gc}$-$V_g$ characteristics of TiN(40 nm)/W(3 or 12 nm)/La$_2$O$_3$(3 nm)/$n$-MOSFETs. For a W(3 nm) FET, a small EOT of 0.50 nm is extracted from $C_{gc}$. A $C_{gc}$ of W(12 nm) FET reveals an EOT of 0.71 nm. In the case of the MOSFET fabrication process, it is confirmed that oxygen supply control by changing the thickness of the oxygen-containing metal is also effective. In addition, the threshold voltage ($V_{th}$) relation with W film thickness coincides with the result of capacitors shown in figure 4.11.

![Figure 4.14](image)

**Figure 4.14** $C_{gc}$-$V_g$ characteristics of TiN(40 nm)/W(3 or 12 nm)/La$_2$O$_3$(3 nm)/$n$MOSFETs. EOT and $V_{th}$ relations with W film thickness coincide with the results of capacitors.
Figure 4.15  $I_{ds}$-$V_g$ characteristics of TiN(40 nm)/W(3 or 12 nm)/La$_2$O$_3$(3 nm)/nMOSFETs. The relationship of SS value corresponding to hump shapes of capacitors is obtained.

Figure 4.16  $\mu_{eff}$ of TiN(40 nm)/W(3 or 12 nm)/La$_2$O$_3$(3 nm)/nMOSFETs.
Figure 4.15 shows $I_{ds}$-$V_{g}$ characteristics of TiN(40 nm)/W(3 or 12 nm)/La$_2$O$_3$(3 nm)/$n$MOSFETs. The relationship of subthreshold slope (SS) corresponding to hump shapes of $C$-$V$ curves (figure 4.12) is confirmed. An appropriate transistor operation at an EOT of 0.5 nm is confirmed for W(3 nm) $n$MOSFET annealed at 800 °C for 2 s, as shown in figure 4.16. However, degradation due to EOT scaling is observed for the thinned W film. The lower $\mu_{\text{eff}}$ of thinner W MOSFET where amount of oxygen supplied is small indicates that defects caused by oxygen vacancies in La$_2$O$_3$ degrade $\mu_{\text{eff}}$. Thus, reduction of oxygen vacancies is important to improve mobility, which is discussed in chapter 5 and 6.
4.5 Conclusion

To achieve an EOT of 0.5 nm using La$_2$O$_3$ gate dielectric, a control method for silicate reaction has been proposed. The amount of supplied oxygen atoms, which trigger the formation of the silicate layer, is controlled by changing the thickness of an oxygen-containing metal such as W. Almost no change in EOT from the as-deposited condition was observed for the TiN/W(6 nm)/La$_2$O$_3$(3.5 nm)/$n$-Si capacitor annealed for 2 s, and an EOT of 0.51 nm is achieved with 800 °C annealing. The relationships between the amount of formed silicate and the hysteresis window of the C-V curve, the humps at the weak inversion region, and $V_{fb}$ shift have been explained by the defect energy levels in the silicates and La$_2$O$_3$ and at the La$_2$O$_3$/La-silicate interface. An appropriate transistor operation at an EOT of 0.5 nm has been confirmed for TiN(40 nm)/W(3 nm)/La$_2$O$_3$(3 nm)/$n$MOSFETs annealed at 800 °C for 2 s.
Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction

References


Chapter 4. Selection of Metal Electrode for Controlling Silicate Reaction


Chapter 5

Thin Si Insertion at Metal Gate/High-k Interface

5.1 Introduction

5.2 Electrical characteristics for MOS capacitors

5.3 Electrical characteristics for MOS transistors

5.4 Quantitative understanding for mobility improvement

5.5 Conclusion

References
5.1 Introduction

At a region of EOT>1.5 nm, a fairly nice interfacial property with a peak effective mobility of over 300 cm²/Vs has been reported with La₂O₃ dielectrics. Also, La₂O₃ gated MOSFETs with EOT of ~0.5 nm were achieved by using W electrode as a source of oxygen atoms supply as described in chapter 4. However, degradations in the mobility have been observed when the thickness of La₂O₃ is thinned down. Figure 5.1 shows the peak $\mu_{\text{eff}}$ of La₂O₃ gated MOSFETs as a function of EOT. The mobility degradation accompanied with EOT scaling can be confirmed, especially at EOT below 1.3 nm.

<table>
<thead>
<tr>
<th>EOT (nm)</th>
<th>$\mu_{\text{eff}}$ (cm²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>150</td>
</tr>
<tr>
<td>1.0</td>
<td>200</td>
</tr>
<tr>
<td>1.5</td>
<td>250</td>
</tr>
<tr>
<td>2.0</td>
<td>300</td>
</tr>
</tbody>
</table>

**Figure 5.1** Peak $\mu_{\text{eff}}$ of La₂O₃ gated MOSFETs as a function of EOT. The mobility degradation accompanied with the EOT scaling is observed.
The negative shifts in $V_{th}$ as well as $V_{fb}$ are also observed as the EOT below approximately 1.3 nm as shown in figure 5.2. Thus, the cause of mobility degradation is considered to be fixed charges ($Q_{fix}$) in gate dielectric. However, the origin of fixed charges generation in gate dielectric is still under discussion. For example, formation of positive fixed charges in the dielectrics caused by diffused metal from the gate electrode is proposed [5.1]. In addition, the defect segregation and enhanced diffusion of oxygen vacancies induced by grain boundaries, which result in generation of positive fixed charges, are also reported (Figure 5.3) [5.2, 5.3].

**Figure 5.2** $V_{fb}$ and $V_{th}$ trend of W/La$_2$O$_3$ gated MOSFETs as a function of EOT, showing negative shift below EOT of ~1.3 nm.
Possible models for $Q_{\text{fix}}$ generation

Grain boundaries with oxygen vacancies

Fixed charges induced by gate metal

Figure 5.3 Reported models for fixed charge generation. The oxygen vacancies segregated at grain boundaries and metal atoms diffusion from gate metal are taken into account as an origin of fixed charges in this chapter.
Actually, the diffusion of W atoms from gate metal to gate dielectric is confirmed by electron energy loss spectroscopy (EELS) measurement as shown in figure 5.4. In any case, the fixed charges play an important role for the mobility degradation. In this study, a thin amorphous La-silicate layer formed by Si insertion at the interface of W and La$_2$O$_3$ has been conducted, anticipating formation of the amorphous La-silicate layer at the metal-gate/La$_2$O$_3$ interface eliminate the grain boundaries. Then, its effect on the electrical characteristics at scaled EOT has been observed.
Figure 5.5 shows the fabrication process of MOS devices discussed in this chapter. Si was \textit{in situ} deposited with a rate of \textasciitilde0.2 nm/min on some samples by RF sputtering to form a thin La-silicate layer at the top of La$_2$O$_3$ dielectrics. A 12-nm-thick W layer was also deposited by RF sputtering. The wafers were not exposed to air until W layer was formed.

\textbf{Figure 5.5} Fabrication process of La$_2$O$_3$ gated MOS devices used in this chapter.
5.2 Electrical characteristics for MOS capacitors

Figure 5.6 shows $C-V$ characteristics of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$(3 nm) gate stack capacitors annealed at 800 °C for 2 s. A small EOT of 0.62 nm was obtained with the Si inserted capacitor while the EOT of that without Si insertion was 0.71 nm. Moreover, a positive shift in $V_{fb}$ was observed with Si insertion. The EOT dependence on the annealing temperature is summarized in figure 5.7. An increase of the EOT accompanied with annealing temperature is suppressed for Si inserted capacitors annealed at from 700 to 900 °C for 2 s.

Figure 5.6 $C-V$ characteristics of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$(3 nm)/n-Si capacitors annealed at 800 °C for 2 s. La$_2$O$_3$ of 3 nm dielectrics with and without Si insertion are deposited at once. Smaller EOT is obtained for Si inserted capacitor.
Figure 5.7 EOT dependence on annealing temperature for TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$(3 nm)/n-Si capacitors annealed for 2 s. La$_2$O$_3$ of 3 nm dielectrics with and without Si insertion are deposited at once.

It can be considered that formation of amorphous La-silicate layer at the interface of W/La$_2$O$_3$ inhibits the diffusion of oxygen atoms thorough grain boundaries and formation of La-silicate layer at the La$_2$O$_3$/Si substrate interface is suppressed. $V_{fb}$-EOT plot measured for TiN/W/Si(0.3 nm)/La$_2$O$_3$(2.5-3.1 nm) and TiN/W/La$_2$O$_3$(2.7-3.3 nm) gate stack capacitors annealed at 800 °C for 2 s is shown in figure 5.8. A positive $V_{fb}$ shift by ~150 mV is obtained for Si inserted capacitors, indicating the suppression of positive fixed charges generation. A formation of positive fixed charges in the dielectrics caused by diffused metal from the gate
electrode and the defect segregation and enhanced diffusion of oxygen vacancies induced by grain boundaries, which result in generation of positive fixed charges, are reported [5.3-5.6]. The formation of the amorphous La-silicate layer at the metal-gate/La$_2$O$_3$ interface might eliminate the grain boundaries. As a result, the amount of diffused metal in dielectrics or oxygen vacancies segregated at the grain boundaries are reduced, resulting in the suppression of positive fixed charge generation.

Figure 5.8 $V_{fb}$-EOT plot of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$/n-Si capacitors annealed at 800 °C for 2 s. A negative $V_{fb}$ shift is suppressed by Si insertion.
5.3 Electrical characteristics for MOS transistors

Next, Si insertion effect on the electrical properties of FETs was performed. Figure 5.9 shows the gate-to-channel capacitance ($C_{gc}$) of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$(3 nm) gate stack nFETs annealed at 800 ºC for 2 s. Compared to EOT of 0.68 nm for nFET without Si insertion, a smaller EOT of 0.58 nm is obtained for Si inserted nFET, consistent with the capacitor experiment. A positive shift in the threshold voltage is also observed for Si inserted nFET.

![Diagram of C$_{gc}$–V$_g$ characteristics](image)

**Figure 5.9** C$_{gc}$–V$_g$ characteristics of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$(3 nm) gate stack nMOSFETs annealed at 800 ºC for 2 s. EOT relation with existence or non-existence of Si insertion coincides with result of capacitors.
Figure 5.10 shows EOT dependence of $V_{th}$ measured for TiN/W/Si(0.3 nm)/La$_2$O$_3$(2.5-3.0 nm) and TiN/W/La$_2$O$_3$(2.7-3.3 nm) gate stack nFETs annealed at 800 °C for 2 s. The positive $V_{th}$ shift by ~150 mV is confirmed for Si inserted nFETs as well as the positive $V_{th}$ shift of capacitor (fig. 5.8), implying the reduction of positive fixed charges.

**Figure 5.10** $V_{th}$ dependence on EOT of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s. $V_{th}$ relation with existence or non-existence of Si insertion coincides with $V_{fb}$ of capacitors.
Effective mobility of TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s as a function of E$_{\text{eff}}$ is shown in figure 5.11. It can be seen that even EOT of Si inserted nMOSFET is smaller than that of nMOSFET without Si insertion, higher $\mu_{\text{eff}}$ is achieved with Si inserted FET at all E$_{\text{eff}}$ region. Figure 5.12 shows $\mu_{\text{eff}}$ at peak value around E$_{\text{eff}}$ of 0.3 MV/cm for TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s as a function of EOT. The same degradation trend in the $\mu_{\text{eff}}$ caused by EOT scaling is observed for nFETs with and without Si insertion. However, when compared at the same EOT, a large improvement can be
**Figure 5.12** $\mu_{\text{eff}}$ at peak value around $E_{\text{eff}}$ of 0.3 MV/cm for TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s as a function of EOT. A large improvement of peak $\mu_{\text{eff}}$ is confirmed by Si insertion.

**Figure 5.13** $\mu_{\text{eff}}$ at $E_{\text{eff}}$ of 1 MV/cm for TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s as a function of EOT. A large improvement of $\mu_{\text{eff}}$ at $E_{\text{eff}}$ of 1 MV is confirmed by Si insertion.
confirmed for $\mu_{\text{eff}}$ at peak value with Si inserted nFETs. Considering the reduction of positive fixed charges with Si insertion as is seen in figure 5.8 and 5.10, the improvement of peak $\mu_{\text{eff}}$ can be explained by the suppression of remote charge scattering (RCS) which is dominant in low $E_{\text{eff}}$ region [5.7]. Then, figure 5.13 shows $\mu_{\text{eff}}$ at $E_{\text{eff}}$ of 1 MV/cm for TiN/W/Si(0 or 0.3 nm)/La2O3 gate stack nMOSFETs annealed at 800 °C for 2 s as a function of EOT. An improvement can be also confirmed for $\mu_{\text{eff}}$ at $E_{\text{eff}}$ of 1 MV/cm with Si inserted nFETs. The improvement in the high $E_{\text{eff}}$ region is considered to be due to the suppression of surface roughness scattering which is dominant at high $E_{\text{eff}}$. La-silicate has various compositions as stable phase, including La2SiO5, La0.33Si6O26 and La2Si2O7 [5.8], and its dielectric constant changes as its composition varies. As shown in figure 5.7 and 5.9, the formation of amorphous La-silicate layer at the metal gate/La2O3 interface might suppress the diffusion of oxygen atoms, resulting in the formation of La-rich silicate with higher k-value at the surface of Si substrate. Consequently, electrical roughness sensed by carriers might become small with Si inserted nFETs. Figure 5.14 summarizes the Si insertion effect.

Figure 5.15 shows gate leakage current density-EOT plot for TiN/W/Si(0 or 0.3 nm)/La2O3 gate stack nFETs annealed at 800 °C for 2 s. A fairly nice $J_g$ of 3.3 A/cm² at $V_g$=1 V, which is $\sim 10^3$ times smaller with respect to the requirement in the ITRS 2009 roadmap, is achieved. Approximately same value of $J_g$ even the EOT of Si inserted nMOSFET is smaller can be explained by suppression of PF current which flow through the traps in the dielectric as discussed in chapter 3.2.
Figure 5.14 Reduction of fixed charges which cause RCS and formation of La-rich silicate at Si substrate interface by formation of amorphous silicate layer at metal gate/high-k interface.
Figure 5.15 $J_g$ at $V_g$ of 1 V for TiN/W/Si(0 or 0.3 nm)/La$_2$O$_3$ gate stack nMOSFETs annealed at 800 °C for 2 s as a function of EOT. $J_g$ of approximately $10^3$ times smaller with respect to the requirement in the ITRS 2009 roadmap, is achieved.
5.4 Quantitative understanding for mobility improvement

As described in previous chapter, RCS induced by fixed charges in the dielectric is suppressed by Si insertion and improvement in mobility at low electric field region is observed. However, $V_{fb}$ and $V_{th}$ behavior, parallel shift of ~150 mV by Si insertion, and mobility improvement by suppression of RCS is explained only qualitatively. Then, $V_{fb}$ and $V_{th}$ behavior and mobility improvement by suppression of RCS is quantitatively studied. For simplicity, fixed charge in the dielectric is assumed to be sheet charge. The influence of RCS depends on the distance from fixed charge to Si substrate and fixed charge density ($N_{fix}$). In this chapter, difference of RCS effect for FETs with and without Si insertion is expressed as distance of fixed charges and Si substrate, conforming the value of $N_{fix}$ of FETs with Si insertion to that without Si insertion.

Figure 5.16 Schematic illustration of parameters used in this chapter.
Chapter 5. Thin Si Insertion at Metal Gate/High-κ Interface

Following Matthiessen’s rule, different contributions to the mobility is given by

\[
\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \ldots
\]  

(5.1)

where \(\mu_1, \mu_2\) and \(\mu_3\) correspond to the limited components of mobility such as the lattice and impurity scattering 5.9. Then eq. 5.1 can be rewritten to

\[
\frac{1}{\mu} = \frac{1}{\mu_{\text{without RCS}}} + \frac{1}{\mu_{\text{RCS}}}
\]  

(5.2)

where \(\mu_{\text{without RCS}}\) is limited components of mobility without RCS and \(\mu_{\text{RCS}}\) is the mobility component limited by RCS. The reported mobility at low electric field region with La\(_2\)O\(_3\) gate dielectric is saturated at \(~300\ \text{cm}^2/\text{Vs}\) for EOT>1.5 nm. Thus \(\mu_{\text{without RCS}}\) can be considered to be \(300\ \text{cm}^2/\text{Vs}\) for La\(_2\)O\(_3\) gated MOSFET. The value of \(V_{\text{fb}}\) and \(V_{\text{th}}\) shift is

\[
\Delta V_g = \frac{qN_{\text{fix}} EOT_{\text{charge}}}{\varepsilon_{\text{ox}}}
\]  

(5.3)

where \(q\) and \(\varepsilon_{\text{ox}}\) denote the electronic charge and permittivity of SiO\(_2\) respectively. EOT\(_{\text{charge}}\) corresponds to the EOT between gate electrode and fixed charges. Considering the \(V_{\text{fb}}\) and \(V_{\text{th}}\) shift of \(150\ \text{mV}\) observed in figure 5.8 and 5.10, eq. (5.3) gives

\[
\Delta V_{g_{\text{w/oSi}}} - \Delta V_{g_{\text{w/Si}}} = \frac{qN_{\text{fix}} EOT_{\text{charge w/oSi}}}{\varepsilon_{\text{ox}}} - \frac{qN_{\text{fix}} EOT_{\text{charge w/Si}}}{\varepsilon_{\text{ox}}} = 0.15 \ [\text{V}]
\]  

(5.4)

where EOT\(_{\text{charge w/oSi}}\) and EOT\(_{\text{charge w/Si}}\) are the electrical distance between gate electrode and fixed charges of FET without and with Si insertion, respectively. Then, the eq. (5.2) can be calculated by using the equation of \(\mu_{\text{RCS}}\) reported in reference [5.10], adjusting the parameters to satisfy the eq. (5.4). The calculated parameters and mobility are shown in figure 5.17. The EOT\(_{\text{charge}}\) for Si inserted nFETs is revealed to be smaller than that for nFETs without Si insertion. It can be
Effective diffusion length of gate metal atoms is suppressed by Si insertion. Thus, the model for suppression of fixed charges ingressio is proposed. However, detailed analysis and experiment are necessary for future works.
5.5 Conclusion

A thin amorphous La-silicate layer formed by Si deposition at the W/La₂O₃ interface is conducted and its effect on the electrical characteristics of MOS capacitors and transistors is examined. A suppression of increase in EOT indicates the diffusion of oxygen atoms thorough grain boundaries are inhibited by the formation of an amorphous La-silicate at the W/La₂O₃ interface, resulting in reduction of La-silicate layer at the La₂O₃/Si substrate interface. In addition, positive shifts in Vₜb and Vₜh with Si insertion implies the formation of amorphous La-silicate layer at the W/La₂O₃ interface reduces positive fixed charges induced by diffused metal atoms or oxygen vacancies segregated at grain boundaries. Consequently, a large improvement in mobility has been confirmed for both at peak value and at high E_{eff} of 1 MV/cm with Si inserted nFETs. Although a degradation trend on EOT scaling has been observed, the insertion of thin Si layer is effective in pushing the scaling limit and might be applicable for other metal/high-k gate stack such as Hf-based dielectrics.
References


Chapter 6

Influence of Annealing Ambient during Silicate Formation on Electrical Characteristics

6.1 Introduction
6.2 Electrical characteristics with capacitors
6.3 Results with transistors
6.4 Conclusion
References
Chapter 6. Influence of Annealing Ambient during Silicate Formation

6.1 Introduction

Thus far, all samples are subjected to post-metallization annealing in F.G. ambient to form high-quality silicate layer with various temperature and time. However it can be considered that an annealing ambient also has a profound effect on electrical characteristics of MOS devices. Therefore, examining the influence of the annealing ambient on electrical characteristics is important to achieve high performance MOS devices. Figure 6.1 shows C-V characteristics of a capacitor with HfO$_2$-based gate dielectric [6.1]. The capacitors are annealed in F.G. ambient which is reducing condition and in oxidizing condition. The $V_{fb}$ is shifted positive and negative direction in sequence by simply switching the annealing ambient from reducing to oxidizing and

![C-V characteristics of MOS devices with HfO$_2$-based gate dielectric. The reversibility of the $V_{fb}$ shift by reducing and oxidizing ambient is confirmed. [6.1]](image)

*Figure 6.1 C-V characteristics of MOS devices with HfO$_2$-based gate dielectric. The reversibility of the $V_{fb}$ shift by reducing and oxidizing ambient is confirmed. [6.1]*
vice versa. This $V_{fb}$ behavior can be understood by the change of amount of oxygen vacancies in gate dielectric. Whereas the annealing in oxidizing condition reduces oxygen vacancies and $V_{fb}$ shifts positive, the annealing in F.G., reducing condition, forms oxygen vacancies and $V_{fb}$ shifts negative.

Figure 6.2 C-V characteristics of MOS devices with La$_2$O$_3$ gate dielectric. The no-reversibility of the $V_{fb}$ shift by reducing and oxidizing ambient is confirmed. [6.2]

On the other hand, C-V characteristics of La$_2$O$_3$ gated capacitors annealed in the oxidizing and reducing ambient is shown in figure 6.2 [6.2]. In the case of La-silicate, negative shift of $V_{fb}$ by annealing in reducing condition doesn’t occur, whereas positive $V_{fb}$ shift by oxidizing condition is observed. A different behavior of $V_{fb}$ between HfO$_2$-based and La-silicate dielectric can be explained by existence of
covalent bond in La-silicate. The electrical instability of HfO$_2$ for annealing ambient is due to material nature associated with ionic bond. On the other hand, in La-silicate layer, oxygen atoms are covalently-bonded with silicon atoms, resulting in no-reversibility of the $V_{fb}$ shift by reducing and oxidizing ambient. However, oxygen atoms in La$_2$O$_3$, which a lot exists soon after deposition, are ionically-bonded. Therefore, in the case of annealing in F.G. ambient during silicate formation, it is anticipated that oxygen vacancy is formed in gate dielectric. In this chapter, fabricated samples are subjected to annealing in F.G. or N$_2$ ambient, investigating the
Chapter 6. Influence of Annealing Ambient during Silicate Formation

effect of annealing ambient on electrical characteristics. Figure 6.3 shows fabrication process of La$_2$O$_3$ gated MOS devices used in this chapter. After the deposition of gate electrode, samples are *in-situ* annealed in F.G. or N$_2$ ambient. Until the end of silicate formation annealing, samples are not exposed to the air.
6.2 Electrical characteristics with capacitors

$C$-$V$ characteristics of TaN/W/La$_2$O$_3$/n-Si capacitors annealed at 900 °C for 30 min in F.G. and N$_2$ ambient are shown in figure 6.4. The EOTs of the two capacitors are aligned to same value of 1nm. Although the hysteresis and hump shapes of $C$-$V$ curves are same, a difference in $V_{fb}$ is observed.

![Graph showing C-V characteristics of TaN/W/La$_2$O$_3$/n-Si capacitors annealed in F.G. and N$_2$ ambient with an EOT of 1 nm. A difference of $V_{fb}$ is observed.](image)

**Figure 6.4** $C$-$V$ characteristics of TaN/W/La$_2$O$_3$/n-Si capacitors annealed in F.G. and N$_2$ ambient with an EOT of 1 nm. A difference of $V_{fb}$ is observed.

Figure 6.5 shows $V_{fb}$-EOT plot of TaN/W/La$_2$O$_3$/n-Si capacitors annealed at 900 °C for 30 min in F.G. and N$_2$ ambient. The positive $V_{fb}$ shift of ~200 mV is observed for capacitors annealed in N$_2$ ambient. These results indicate that the positive fixed charges in gate dielectric are reduced by annealing in N$_2$ ambient. As described in chapter 6.1, the annealing in F.G. ambient, which is reducing condition, is anticipated
Figure 6.5 $V_{fb}$-EOT plot of TaN/W/La$_2$O$_3$/n-Si capacitors annealed in F.G. and N$_2$ ambient. A suppression of negative $V_{fb}$ shift is observed for N$_2$ annealing, indicating the reduction of oxygen vacancies.

to form the oxygen vacancies, positive fixed charges, in La$_2$O$_3$ including ionic bonds. Then, there is a possibility that mobility is improved by annealing in N$_2$ ambient due to suppression of RCS [6.3]. Next, electrical characteristics of transistors are discussed to examine the influence of RCS.
6.3 Results with transistors

Effective mobility of TaN/W/La2O3 gate stack transistors annealed in F.G. and N2 ambient with the EOT of 0.72 nm as a function of $E_{eff}$ is shown in figure 6.6. It can be confirmed that higher $\mu_{eff}$ is achieved for FET annealed in N2 ambient at all $E_{eff}$ region. Figure 6.7 shows the effective electron mobility at (a) $E_{eff}$ of 0.3 MV/cm and (b) $E_{eff}$ of 0.8 MV/cm for TaN/W/La2O3 gate stack transistors annealed at 900 °C for 30 min in F.G. and N2 ambient as a function of EOT. The same degradation trend in the $\mu_{eff}$ caused by EOT scaling is observed for both annealing ambient.

![Figure 6.6](image_url)

*Figure 6.6* $\mu_{eff}$-$E_{eff}$ characteristic of TaN/W/La2O3 gate stack transistors annealed in F.G. and N2 ambient. Mobility improvement is observed for transistor annealed in N2 ambient, especially at low electric region.
Figure 6.7 $\mu_{\text{eff}}$ at (a) $E_{\text{eff}}$ of 0.3 MV/cm and (b) 0.8 MV/cm, respectively as a function of the EOT. The mobility improvement is observed for $N_2$ annealing, especially at low electric field region, indicating suppression of RCS.
However, when compared at the same EOT, a large improvement can be confirmed for $\mu_{\text{eff}}$, notably at low electric field of 0.3 MV/cm. Considering the reduction of positive fixed charges with annealing in N$_2$ ambient as shown in figure 6.7, the improvement of $\mu_{\text{eff}}$ at low $E_{\text{eff}}$ can be explained by the suppression of RCS which is dominant in low $E_{\text{eff}}$ region.

For a quantitative understanding, the effect of RCS on the mobility is examined with the similar approach as shown in chapter 5.4. For simplicity, fixed charge in the dielectric is assumed to be sheet charge. Here, the effective length between the gate electrode and fixed charges are supposed to be 1 nm for both annealing in F.G. and N$_2$ ambient. Considering the $V_{\text{fb}}$ shift of 200 mV observed in figure 6.5, eq. (5.3) gives

$$
\Delta V_{g,\text{FG}} - \Delta V_{g,\text{N2}} = \frac{qN_{\text{fix,FG}}EOT_{\text{charge}}}{\varepsilon_{\text{ox}}} - \frac{qN_{\text{fix,N2}}EOT_{\text{charge}}}{\varepsilon_{\text{ox}}}
$$

$$
= 0.2 \ [V] 
$$

(6.1)

where $N_{\text{fix,FG}}$ and $N_{\text{fix,N2}}$ correspond to the fixed charge density of FET annealed in F.G. and N$_2$ ambient, respectively. Then, the eq. (5.2) can be calculated by using the equation of $\mu_{\text{RCS}}$ reported in reference [6.4], adjusting the parameters to satisfy the eq. (6.1). The calculated parameters and mobility are shown in figure 6.8. The $N_{\text{fix}}$ in FET with N$_2$ annealing and that with F.G. annealing are revealed to be $3.8 \times 10^{13}$ cm$^2$ and $6.1 \times 10^{13}$ cm$^2$.

Thus, it is confirmed that the annealing in reducing ambient during silicate formation forms oxygen vacancies in gate dielectric due to ionic bonds of La$_2$O$_3$, resulting in degradation of mobility at low $E_{\text{eff}}$ region. This mobility degradation can be prevented by splitting the annealing process in annealing for silicate formation and
that for dangling bond termination. The annealing for silicate formation shouldn’t be taken place in reducing ambient and that for dangling bond termination should be taken place in F.G. ambient.

Figure 6.8 C-V characteristics of TaN/W/La$_2$O$_3$/n-Si capacitors annealed in F.G. and $N_2$ ambient with an EOT of 1 nm.
Figure 6.9 Benchmark of this work for effective electron mobility at (a) $E_{\text{eff}}$ of 0.5 MV/cm and (b) 1 MV/cm respectively. A slightly higher mobility is achieved, especially at low electric region.
Figure 6.9 shows the benchmark of effective electron mobility at (a) $E_{\text{eff}}$ of 0.5 MV/cm and (b) $E_{\text{eff}}$ of 1 MV/cm. The results of Hf-oxides reported in IEDM might be record mobility with scaled EOT at the time of writing [6.5]. The $\text{La}_2\text{O}_3$ gated FETs with annealing at 900 °C for 30 min in $\text{N}_2$ ambient fabricated in this chapter achieve slightly higher mobility than that of Hf-based oxide, especially at low electric field region. This indicates the potentiality of amorphous La-silicate dielectric fabricated with appropriate process.
6.4 Conclusion

In this chapter, fabricated samples are subjected to annealing in F.G. or N₂ ambient, investigating the effect of annealing ambient during silicate formation on electrical characteristics. It is confirmed that the annealing in reducing ambient during silicate formation forms oxygen vacancies in gate dielectric due to ionic bonds of La₂O₃, resulting in degradation of mobility at low E_{eff} region. This mobility degradation can be prevented by splitting the annealing process in annealing for silicate formation and that for dangling bond termination. The annealing for silicate formation shouldn’t be taken place in reducing ambient and that for dangling bond termination should be taken place in F.G. ambient. The La₂O₃ gated FETs with annealing at 900 °C for 30 min in N₂ ambient achieve slightly higher mobility than that of record data, especially at low electric field region. This indicates the potentiality of amorphous La-silicate dielectric fabricated with appropriate process.
References


Chapter 6. Influence of Annealing Ambient during Silicate Formation

Chapter 7

Conclusions
In this thesis, the ways to fabricate the MOSFET with extremely small EOT of 0.5 nm and to prevent the effective mobility degradation accompanied with EOT scaling is proposed for the scaling of MOS devices. In this chapter, the studies are summarized below.

a) Selection of High-k Gate Dielectrics with Annealing Process (Chapter 3)

In order to suppress the increase in EOT after annealing, using CeOx which forms silicate with high dielectric constant as a gate dielectric and short time annealing are investigated. It is revealed that SiO$_2$-IL changes to LaCe-silicate layer, whose dielectric constant is higher than that of SiO$_2$, by depositing La$_2$O$_3$ on CeO$_x$, although the formation of SiO$_2$-IL is confirmed with CeO$_x$ dielectric. Suppression of an increase in EOT and fairy nice interfacial property are confirmed with CeO$_x$ insertion. Moreover, it is confirmed that short time annealing at high temperature is suitable to obtain better electrical property of MOSFETs in terms of EOT, interfacial trap density, fixed charge, and gate leakage current.

b) Selection of Metal Gate Electrode for Controlling Amount of Oxygen Atom Supply (Chapter 4)

A novel control method for silicate reaction is proposed to achieve an EOT of 0.5 nm using La$_2$O$_3$ gate dielectric. The amount of supplied oxygen atoms, which trigger the
formation of the silicate layer, is controlled by changing the thickness of an oxygen-containing metal such as W. Almost no change in EOT from the as-deposited condition was observed for the thin W electrode capacitor annealed for 2 s, and an EOT of 0.51 nm is achieved with 800 °C annealing. In addition, the reduction of EOT is observed with TiN capping due to oxygen diffusion from the gate dielectric to the TiN electrode. On the other hand, larger hysteresis is observed for thin W film capacitor, needing high temperature annealing to reduce the hysteresis. These imply that $C-V$ characteristics with a small EOT as well as a small hysteresis can be obtained by optimization of annealing temperature and W film thickness. Moreover, the hysteresis of the $C-V$ curve, the humps at the weak inversion region, and $V_{th}$ shift can be explained by the defect energy levels in the dielectric and La$_2$O$_3$/La-silicate interface. Then, an appropriate transistor operation at an EOT of 0.5 nm is confirmed for $n$MOSFETs with W of 3 nm annealed at 800 °C for 2 s.

c) Thin Si Insertion at Metal Gate/High-k Interface (Chapter 5)

A novel structure for eliminating grain boundaries at the top of La$_2$O$_3$ is proposed. A thin amorphous La-silicate layer formed by Si deposition at the W/La$_2$O$_3$ interface is conducted and its effect on the electrical characteristics of MOS devices is examined. A suppression of increase in EOT indicates that the diffusion of oxygen atoms thorough grain boundaries are inhibited by the formation of an amorphous La-silicate at the W/La$_2$O$_3$ interface, resulting in reduction of La-silicate layer at the La$_2$O$_3$/Si substrate interface. In addition, positive shifts in $V_{th}$ and $V_{th}$ with Si insertion implies
the amorphous La-silicate layer at the W/La$_2$O$_3$ interface reduces diffused metal atoms or oxygen vacancies induced by grain boundaries. Consequently, a large improvement in mobility is confirmed for both at peak value and at high $E_{\text{eff}}$ of 1 MV/cm with Si inserted $n$FETs. The Si insertion technique proposed in this study is effective in pushing the scaling limit.

d) Influence of Annealing Ambient during Silicate Formation (Chapter 6)

The effect of annealing ambient during silicate formation on electrical characteristics is investigated. It is confirmed that the annealing in reducing ambient during silicate formation forms oxygen vacancies in gate dielectric, resulting in degradation of mobility at low $E_{\text{eff}}$ region. This mobility degradation can be prevented by splitting the annealing process in annealing for silicate formation and that for dangling bond termination. The annealing for silicate formation shouldn’t be taken place in reducing ambient and that for dangling bond termination should be taken place in F.G. ambient. According to the annealing guideline above, the La$_2$O$_3$ gated FETs is fabricated and achieve slightly higher mobility than that of record data with Hf-based oxide, especially at low electric field region. This indicates the potentiality of amorphous La-silicate dielectric fabricated with appropriate process.
Finally, I would like to propose the fabrication process obtained from studies noted above to achieve the MOSFET with high performance and small EOT (Figure 7.1).

![fabrication process diagram]

**Figure 7.1** Guideline obtained from this thesis for MOSFET with high performance and small EOT.
[Publications]


[Invited Talk]


[International Presentations]


[Dominic Presentations]


Publications and Presentations


Acknowledgments

First of all, I would like to express my gratitude to my supervisor Prof. Hiroshi Iwai for his continuous encouragement and advices for my study. He also gave me many chances to attend conferences. The experiences are precious for my present and future life.

I deeply thank to Prof. Takeo Hattori, Prof. Kenji Natori, Prof. Nobuyuki Sugii, Prof, Akira Nishiyama, Prof. Kazuo Tsutsui, Prof. Yoshinori Kataoka, Associate Prof. Parhat Ahmet, and Associate Prof. Kuniyuki Kakushima for useful advice and great help whenever I met difficult problem.

I also thank research colleagues of Iwai Lab. for their friendship, active many discussions and many of encouraging words.

I would like to appreciate the support of secretaries, Ms. Nishizawa and Ms. Matsumoto.

I would like to thank Mr. Koyanagi who is lonely man and Mr. Shigemory who is thai for their passion.

I also express the appreciation to Mr. Monkichi, Ms. Koume, Ms. Jiko, and Ms. Makie for giving me much healing.

Finally, I would like to thank my parents Mikio and Kumiko and my sister Nanami for their endless support and encouragement.

Daisuke Kitayama

February, 2012