Master Thesis

Effects of Flash Lamp Anneal processing on Electrical Characteristics of MOS Devices

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1.1 Background of this study

Today’s high-tech such as the internet, mobile phones, game machines, and entertainment robots can never be realized without the recent tremendous progress of the integrated circuits (IC). The progress of electronic circuits has been accomplished by the downsizing of components such as vacuum tubes 40 years ago and transistors since then, as shown in Fig. 1.1. [1]

To downsize the components equal to decrease its capacitance, resulting in the increase of the circuit operating speed and decrease of its power consumption. The components size reduction brought increment in the number of the components in the circuit, resulting in another increase in the circuit speed. The downsizing rate of the component is really tremendous. In fact, its dimension has reduced 1 million times in the production level for the past 100 years. This dimensional scaling has progressed along the Moore's Law, increasing transistor performance year over year has become more difficult. [2] The importance of the dimensional scaling will be expected to further increase in intelligent society. It is considered that the dimensional scaling will reach the ultimate limit in near future, as shown in Fig. 1.2.

Now, sub-32 nm gate length MOSFETs are used for commercially available CMOS LSIs. [3] Anyone in 100 years could imagine that circuits composed of billions of electronic components would be realized and control the operation of our human society. Future downsizing trends have been predicted by International Technology Roadmap for Semiconductors (ITRS). However, the roadmap has to be renewed every two years, because semiconductor product suppliers develop the scaling technology and provide downscaled products every two years ahead of the roadmap. Thus, CMOS downsizing has been accelerated very aggressively in these years.
Fig. 1.1 Evolution of electronic devices

Fig. 1.2 Past and future downsizing trend
1.2 Device Scaling method for Si based MOSFET

The performance of Si based CMOS products depend on the capability of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) which is core part of LSI systems. In order to obtain high performance devices, it is necessary to miniaturize the MOSFET with the scaling method. The scaling method is based on reducing the device dimension in both lateral and vertical. A simple description of miniaturization with scaling factor of $k$ is shown in Fig. 1.3 and Fig. 1.4. To gain $k$ times of the device performance, the physical device dimensions are reduced by $k$ times, while the electrical parameters are increased by $k$ times.

![MOSFET Scaling parameters](image)

Fig. 1.3 MOSFET Scaling parameters
1.3 Scaling limits of SiO$_2$ Gate dielectric

1.3.1 Leakage current

Silicon dioxide (SiO$_2$) is the most common materials as gate insulator film. However, a big hurdle is confronted to miniaturize the MOSFET size as in the past with keeping high performance and high integration. From ITRS 2009 roadmap which shown in Fig. 1.5, Planer type bulk MOSFETs Equivalent Oxide Thickness (EOT) will be required sub 0.5 nm level in near future. [4] On the other hand, one of the main problems of SiO$_2$ gated dielectric film’s scaling limitations is leakage current. Depending on the physical thickness of the SiO$_2$, leakage current is too increasing to be neglected as shown in Fig. 1.6. Therefore, SiO$_2$ gate insulator film is to be replaced with an alternative material, which can be suppressed leakage current.
Fig. 1.5 International Technology Roadmap for Semiconductors (ITRS) roadmap in 2009.

Fig. 1.6 Relations between gate leakage current and physical thickness of SiO₂ dielectric film.
1.3.2 Short channel effect

As expressed even with the section before, another problem of SiO₂ gated dielectric film’s scaling limitation is Short Channel effect. Short Channel effect is phenomenon in which the current control by a gate electrode becomes difficult with the scaling gate length (\(L_g\)), shown in Fig. 1.7. The thickness of gate dielectrics must scale with lateral MOSFET devices at each technology node to preserve the long-channel behavior; otherwise the device suffers from severe short channel effects such as dropping off the threshold voltage. [5] In addition, it is reported that it causes the increase of the off current (consumed power) and degradation of variation tolerance.

Fig. 1.7 Relations between gate length(L) and carrier(electron) distribution by computer simulation.
1.4 Introduction of High-k gate dielectrics

I explained the difficulties of MOSFET with SiO₂ gated dielectrics to realize the further scaling. Therefore, attention is focused on the materials which have higher dielectric constant (k) than SiO₂ dielectrics. The materials are so-called high-k materials. Even if high-k dielectrics which have smaller physical thickness than SiO₂ dielectrics are used in Si-MOSFET, the high-k dielectrics can get more capacitance than SiO₂ one thanks to the larger k-value as shown in Fig.1.8. Therefore, the high-k dielectrics are effective for suppressing the leakage current. In addition, short channel effect can be suppressed by employing high-k material because thick physical thickness of dielectric film is accepted. At the same time, as the introduction of high-k materials into gated dielectric film, the term of equivalent oxide thickness (EOT) has been in use. It is useful index in comparing the high-k materials, which have different k-values and EOT can be written as

\[ EOT = \frac{\varepsilon_{SiO₂} t_{physical}}{\varepsilon_{high-k}} \]

where \( \varepsilon_{SiO₂} \) and \( \varepsilon_{high-k} \) are respectively the permittivity of SiO₂ dielectrics. So, permittivity of high-k gated dielectrics film is important index for EOT scaling.

Fig. 1.8 Advantage of the High-k gated dielectric film.
The key guidelines for selecting an alternative gate dielectric material are high dielectric constant, large band gap and band alignment to silicon, thermodynamic stability, film morphology, interface quality, process compatibility, and reliability. Among them, high dielectric constant and large band gap are the minimum required characteristics to suppress the gate leakage current. Fig. 1.9 shows possible candidates of several high-k gated dielectric films relationship of k-value on band-gap.

![Diagram showing possible candidates of several high-k gated dielectric films.](image)

**Fig. 1.9 Possible candidates of several high-k gated dielectric films.**

Lanthanum oxide (La$_2$O$_3$) material shows good physical properties, high dielectric constant of 27, wide band-gap of 5.6 eV, symmetrical band offset for electrons and holes of more than 2 eV, and good thermal stability in contact with silicon.

From the viewpoint of electrical characteristics, SiO$_2$ interfacial layer is required between the high-k dielectrics and Si-substrate for improving interfacial characteristics. However, SiO$_2$ (lower-k) interfacial layer is harmful for further EOT scaling. It is reported that La$_2$O$_3$ can
achieve an EOT below 1 nm with fairly nice performance by forming La-silicate layer at Si interface [6]. As shown in Fig. 1.10, La-silicate is reactively formed and direct contacted by heat treatment and it also has high k-value ranging from 8 to 14 depending on the amount of silicon composition. Therefore, It also remarked gate oxide thanks to its advantage of leakage current, which means that this material can realize smaller EOT.

From the above things, La$_2$O$_3$ is one of the potential candidates of the high-k gated dielectric film for the next generation gate dielectric technology. We especially focused on this high-k material and doing research.

Fig. 1.10 TEM image of the W/La$_2$O$_3$/n-Si structure which conducted the PMA 500°C for 30 minutes.
1.5 Problems of High-k gated dielectric film

Degradation in the electrical properties with EOT scaling is one of the major problems for most of the gated dielectric film. La$_2$O$_3$ also suffers from this problem. For example, it is reported that the negative shift in the flat-band voltage ($V_{fb}$) are observed below an EOT of about 1.3 nm as shown in Fig. 1.11. One of the reasons of the degradation can be considered as the generation of defects in the dielectrics. It is reported that the metal gate induced fixed charge generation and the electrical properties degrade. [7] In this case, fixed charge is generated by W gate electrode which diffuses W atoms toward gated dielectric films during the Post Metallization Annealing (PMA) process as shown in Fig. 1.12. PMA process is needed for forming La-silicate layer at the interface of dielectric film and Si substrate which improving the interfacial properties. Actually, this phenomenon is observed by physical analysis “EELS” for TiN/W/La$_2$O$_3$/n-Si which conducted PMA process as shown in Fig. 1.13. [8] Therefore, mechanism for preventing the fixed charge generation is required.

So far, I described the problems of fixed charge generation with the EOT scaling. One of the solution for suppressing the W diffusion (fixed charge generation) is forming the amorphous La-silicate layer on the top of the dielectric film by heat treatment as shown in Fig. 1.14. W atoms near the Si channel also cause the serious mobility degradation with the thickness scaling by Remote coulomb scattering. Therefore, there is the possibility of the improvement of the electrical characteristics of MOS devices by forming the La-silicate layer on the top of the dielectric film.
Fig. 1.11 EOT on Flat-band voltage ($V_{fb}$) and Threshold voltage ($V_{th}$) of W/La$_2$O$_3$/Si n- capacitors and MOSFET.

Fig. 1.12 Schematic illustrations of the mechanism of W diffusion.
Fig. 1.13 Electron Energy-Loss Spectroscopy (EELS) spectrums for TiN/W/La$_2$O$_3$/n-Si structure which conducted PMA process.

Fig. 1.14 Schematic illustrations of the solution for suppressing the W diffusion.
1.6 Properties of Flash Lamp Annealing

I proposed the solution for suppressing the W diffusion (fixed charge generation) by forming the amorphous La-silicate layer on the top of the dielectric film using some heat treatment. One of the candidates for forming La-silicate layer on the top of the dielectric film is considered the Flash Lamp Annealing.

Flash Lamp Annealing has the characteristics of ultimate short-time annealing which is in the order of the milisecond and consecutive spectrum with the wavelength of 200 to 800 nm. So, it is the equipment which realizes more nearly high-speed annealing by hitting a flash glint of light with hundreds of thousands times as much energy as the flash light used for a digital camera etc. to the semiconductor surface. It is used for activation of the extension (S/D) of the integrated circuit (IC). At the viewpoint of the spectrum of the wavelength, there is a valuable characteristic because of the difference of the intensity of light absorption with the materials as shown in Fig.1.15. [9] [10] It is also confirmed that the Xe Flash Lamp Annealing matches to the light absorption of Si which has the two states of crystal Si (Si-substrate) and PVD-Si. Crystal Si and PVD-Si have differences of the intensity of light absorption characteristics toward the Xe Flash Lamp Annealing. Therefore, this can be applied to use as the heat treatment on the top of the La$_2$O$_3$ film especially for suppressing the W diffusions as shown in Fig. 1.16.
Fig. 1.15 Intensity of the light absorption characteristics with the wavelength for some materials.

Fig. 1.16 Schematic illustrations of the applications of the Flash Lamp Annealing as the heat treatment.
1.7 Purpose of this study

All the previous discussion, I took particular notes about fixed charge generation as the high-k gated dielectric film’s problem. In other words, we need to consider how to balance the EOT Scaling and suppress the fixed charge generation. I try to decide following approaches for solving these problems.

Firstly, we introduce Flash Lamp Annealing method for High-k gate dielectrics. Because it is one of the most short time annealing methods and it matches the light absorption quality of various Si. This method is already applied to the S/D extension. Therefore, we need to examine the effects of Flash Lamp Annealing to the high-k gated dielectric film for gate last process.

Secondly, we employ the Si/La$_2$O$_3$/n-Si structure as the gated dielectric film. Because, it is well known that La-silicate is amorphous and forming the amorphous La-silicate layer at High-k/Metal gate interface for preventing the metal diffusion from gate electrode. Capped Si layer can effectively absorb Flash Lamp Annealing energy because it matches the light absorption quality of PVD-Si than crystal-Si by Fig. 1.15.

Therefore, purpose of this study is examines the effects of Flash Lamp Annealing on electrical characteristics of MOS device with Si/La$_2$O$_3$/n-Si structure for suppressing the fixed charge generation as shown in Fig. 1.17.

![Fig. 1.17 Schematic illustrations of my approach.](image-url)
References


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  2.1.2.2 Flash Lamp Annealing
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2.2.1 C-V measurement
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2.2.3 Conductance method for $D_{it}$ (Density of Interfacial Trap)
2.1 Experimental procedures

2.1.1 Silicon surface cleaning

Before deposition of high-$k$ gate dielectric films for fabrication of MOS device process, the ultra-pure surface of a bare Si-substrate should be chemically cleaned to remove particles contamination, such as metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness. It is considered that this substrate cleaning process is very important to realize desirable device operation and its reproducibility.

In this paper, the method of surface cleaning process was used a typical processing using hydrofluoric acid, which is usually called RCA cleaning method, was proposed by W. Kern et al. But some steps were reduced.

Firstly, silicon substrates were dipped in SPM solution, mixed 4 parts H$_2$SO$_4$ (96 %) with 1 part H$_2$O$_2$ (30 %) at 100 degrees, generating heat helping organic materials oxidize. And then, dipped in hydrofluoric acid diluted at 1 % to remove chemical or natural oxide layers and obtain hydrogen-terminated surface. Hydrogen-terminated surface is stable and a preventive oxidation. Schematic illustration of silicon surface cleaning process is shown in Fig. 2.1.
2.1.2 All in-situ deposition and annealing process

2.1.2.1 E-beam evaporation

There are many ways to deposit high-k dielectric films on Si substrate. Various deposition methods have been proposed. These include CVD, ALD, PLD and E-beam evaporation. In this study, E-beam evaporation method was employed. High-k materials were deposited in ultra high vacuum chamber as shown in Fig. 2.2. La$_2$O$_3$ were subsequently heated by the e-beam which was located near the high-k material source. E-beam was controlled by a magnetic sweep controller. The base pressure of the E-beam chamber is maintained at $10^{-8}$ Pa by TMP, when high-k was deposited the pressure inside the chamber changes to $10^{-6}$ Pa. Then, since the chamber is maintained at the ultra high vacuum state, the La$_2$O$_3$ molecule begins to evaporate. While deposition, the physical thickness of each high-k film was measured by crystal oscillator.
and the sample folder was rotated. Average deposition rate was set to be around 0.2 ~ 0.3 nm/s, was important for the film quality.

![Diagram of E-beam evaporation method](image)

**Fig. 2.2** Schematic illustrations of E-beam evaporation method.

2.1.2.2 Flash Lamp Annealing

Flash Lamp Annealing is equipment which realizes more nearly high-speed annealing by hitting a flash glint of light with hundreds of thousands times as much energy as the flash light used for a digital camera etc. to the semiconductor surface. It is used for activation of the extension (S/D) of the integrated circuit (IC). [1] Although it was common to have used a halogen lamp as for the annealing, if it is going to heat a wafer at not less than 1000 °C which the doped ion activates, in a halogen lamp, it will take the time for several seconds. The doped dopant will diffuse it, so that Drain connects with Source too rapidly the transistor with which gate length was made detailed by tens of nm by the annealing time for only several of the
seconds. Flash lamp annealing is rising temperature at the speed of per second hundreds of thousands of degrees which does not give the spare time which the doped ion diffuses. The ion doped without this hardly causing ion diffusion is activable. This annealing technology is used for general purpose CPU after 65nm. [2]

If setting voltage (900 V), pulse width (0.9 ms), and luminescence mode (short pulse mode) were set up in a control part, setting part sets up the waveform of a pulse signal, and a pulse generator generates a pulse signal according to the waveform. In this case maximum energy density of Flash Lamp Annealing is approximately 25 J/cm². Flash Lamp Annealing is performed in a diluted oxygen ambient (N₂:O₂ = 95:5) under 10 Pa and it is assisted by substrate heater which was set several temperatures. While a pulse generator outputs a pulse to the gate of a switching element, specific wave-like current flows into the circuit containing the flash lamp by impressing trigger voltage to a trigger electrode. Using an array of flash lamps which are ignited by a high voltage pulse it allows annealing for times in the range 0.1 ~ 10 mili-seconds by using light flashes. Schematic illustrations of the Flash Lamp Annealing method are shown in Fig. 2.3.
2.1.2.3 RF magnetron sputtering

Gate metal (W : tungsten) was deposited by RF magnetron sputtering method. In the chamber filled with the Argon gas, the high voltage is applied in high frequency between the target (W) side and the sample side. The flow rate of gases is (10 sccm) controlled by mass flow. The RF power supply system has auto impedance matching equipment and its capability of power supply is ~ 150W.

The Argon molecules are divided into Argon ions and electrons because of the difference of mass. Because the sample side keeps conductive and the target side keeps dielectric, the electrons gathered on the sample side can flow into the circuit but those on the target side are kept gathered. The target side has the minus bias and Argon ions with momentum crash to the
target. By the crush, the particles of the target are emitted and deposited on the wafer.

![Fig. 2.4 Schematic illustrations of RF magnetron sputtering method.](image)

2.1.2.4 Composition of all in-situ process

So far, it is explained concerning E-beam deposition method and Flash Lamp Annealing method and RF magnetron sputtering method. As a matter of fact, the equipment of these deposition and heat treatment process can be performed in all in-situ (vacuum part). Here, the summary of this all in-situ process equipment is explained briefly.

Schematic illustration of the all in-situ system is shown in Fig. 2.5. LL chamber can be taken the samples by breaking the vacuum. Each of LL, E-beam, Sputtering, and Flash Lamp Annealing chambers are equipped with Turbo Molecular Pump (TMP). Therefore, it can change into a vacuum state easily. Each chamber can make the samples transfer automatically by a
robot arm in a vacuum state. Therefore, it is possible to perform deposition and heat treatment, maintaining a high vacuum state without returning to the atmosphere.

Fig. 2.5 Schematic illustrations of the all in-situ system.

2.1.3 Photolithography

The process flow of photolithography is shown in Fig. 2.6. Electrical hotplate is used for baking purposes. The spin-coated layer photoresist was aligned and exposed through tungsten coated e-beam patterned hard-mask with high-intensity ultraviolet (UV) light at 405 nm wavelength. The exposure duration was set to 1.2 seconds. After that, exposed wafers were developed using the specified developer called NMD-3 (Tokyo Ohka Co. Ltd.) after dipped into the solvent for 2 minute and baked at 130 °C for 3 minutes.
Coating photoresist

Baking at 115 °C for 5 min by Hot plates.

Exposure (capacitor : 1.2 s)

Development (NMD3 2 min)

Baking at 130 °C for 3 min by Hot plates.

Fig. 2.6 Photolithography process flow.

2.1.4 Dry and wet etching

Reactive ion etching (RIE) is one of the dry etching methods. The gas in the chamber is plasmanized and crashed to the samples. But, in the RIE process, not the physical crash but the chemical reaction between the ions and samples is important.

W combined with F- and forms WF₆, which boiling point is 18°C. WF₆ is evaporated and eliminated from the sample. Therefore, in this experiment, SF₆ is used as etching gas for W etching. On the other hand, photoresist, which is attached to the sample by the photolithography, reacts with not SF6 but O₂ to be eliminated. This phenomenon is called ashing. O₂ is used as the etching gas of the resist. Fig. 2.7 shows the schematic illustration of the RIE process. HCl and buffered HF (BHF) were used for the wet etching. BHF is the mixture liquid of HF, NH₄F and H₂O. HCl dissolves La₂O₃ (sometimes Ar gas was used by RIE for etching the La₂O₃ layer) and BHF dissolves SiO₂. However, both HCl and BHF don’t dissolve the resist. The resist is dissolved by the acetone. By these chemical reactions, the dielectrics are etched.
2.1.5 Rapid Thermal Annealing (RTA)

Rapid Thermal Annealing (RTA) method was employed for the heat treatments after deposition of dielectric films and metal gate. The annealing process is indispensable to improving defects in dielectric film and at the interface. The schematic illustrations of RTA system are shown in Fig. 2.8. The samples with gate dielectric were put on silicon susceptor and inserted into heat-treating furnace. The ambience in furnace was vacuumed adequately by rotary pump for highly-pure forming gas substitution. And then, forming gas was provided and the samples were annealed at atmospheric pressure. In order to improve the electrical characteristics of MOS devices, the post metallization annealing (PMA) condition were set 420 °C for 30 minute.
2.1.6 Thermal evaporation method

Thermal evaporation method is employed for deposition of the Al electrode on the back side of the substrates. Fig. 2.9 shows the schematic illustrations of the thermal evaporation method. Al is placed on W boat, and current is flown in the circuit connected with W boat. Large current is flown, and then Al is vaporized by joule heat because the boiling point of Al is lower than the melting point of W. Therefore, vaporized Al is deposited on the substrates.
2.2 Measurement methods

2.2.1 C-V measurement

C-V characteristic measurements were performed with various frequencies (1 kHz ~ 1 MHz) by precision LCR Meter (HP 4284A, Agilent). The energy band diagram of an MOS capacitor on a p-type substrate is shown in Fig. 2.10 [4]. The intrinsic energy level $E_i$ or $\phi$ potential in the neutral part of device is taken as the zero reference potential. The surface potential $\phi_s$ is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV}$$

(2.1)

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurements, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at an MOS capacitor from the gate, $C = \frac{dQ_G}{dV_G}$, where $Q_G$ and $V_G$ are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge,

$$Q_G = -(Q_S + Q_a)$$

where $Q_s$ is the semiconductor charge, $Q_a$ the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor.

This gives,

$$V_G = V_{FB} + V_{ox} + \phi_s$$

Where $V_{FB}$ is the flat-band voltage, $V_{ox}$ the oxide voltage, $\phi_s$ and the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = \frac{dQ_s + dQ_p}{dV_{ox} + d\phi_s}$$

(2.2)

The semiconductor charge density $Q_S$, consists of hole charge density $Q_p$, space-charge region bulk charge density $Q_b$, and electron charge density $Q_n$. With $Q_S = Q_p + Q_b + Q_n$, Eq.
(2.2) becomes
\[
C = -\frac{1}{\frac{dV_{ox}}{dQ_s + dQ_o} + \frac{d\phi}{dQ_p + dQ_b + dQ_n + dQ_{it}}} \quad (2.3)
\]

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes
\[
C = -\frac{1}{\frac{1}{C_{ax} + \frac{1}{C_p + C_b + C_n + C_{it}}}} = \frac{C_{ax} \left( C_p + C_b + C_n + C_{it} \right)}{C_{ax} + C_p + C_b + C_n + C_{it}} \quad (2.4)
\]

The positive accumulation \( Q_p \) dominates for negative gate voltages for \( p \)-substrate devices. For positive \( V_G \), the semiconductor charges are negative. The minus sign in Eq. (2.3) cancels in either case. Eq. (2.4) is represented by the equivalent circuit in Fig. 2.11 (a). For negative gate voltages, the surface is heavily accumulated and \( Q_p \) dominates. \( C_p \) is very high approaching a short circuit. Hence, the four capacitances are shorted as shown by the heavy line in Fig. 2.11 (b) and the overall capacitance is \( C_{ax} \). For small positive gate voltages, the surface is depleted and the space-charge region charge density, \( Q_n = -qN_dW \), dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of \( C_{ax} \) in series with \( C_b \) in parallel with \( C_{it} \) as shown in Fig. 2.11 (c). In weak inversion \( C_n \) begins to appear. For strong inversion, \( C_n \) dominates because \( Q_n \) is very high. If \( Q_n \) is able to follow the applied ac voltage, the low-frequency equivalent circuit (Fig. 2.11 (d)) becomes the oxide capacitance again.

When the inversion charge is unable to follow the ac voltage, the circuit in Fig. 2.11 (e) applies in inversion, with \( C_b = K \varepsilon_0 / W_{inv} \) with \( W_{inv} \) the inversion space-charge region width. The flat-band voltage \( V_{FB} \) is determined by the metal-semiconductor work function difference \( \phi_{MS} \) and the various oxide charges through the relation
\[
V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ax}} - \frac{Q_n(x)}{C_{ax}} - \frac{1}{C_{ax}} \int_0^L \rho_n(x) dx - \frac{1}{C_{ax}} \int_0^{t_{ox}} x \rho_{ox}(x) dx \quad (2.5)
\]

where \( \rho(x) = \) oxide charge per unit volume. The fixed charge \( Q_f \) is located very near the
Si-SiO₂ interface and is considered to be at that interface. \( Q_s \) is designated as \( Q_s(\rho_s) \), because the occupancy of the interface trapped charge depends on the surface potential. Mobile and oxide trapped charges may be distributed throughout the oxide. The \( x \)-axis is defined in Fig. 2.10. The effect on flat-band voltage is greatest, when the charge is located at the oxide-semiconductor substrate interface, because then it images all of its charge in the semiconductor. When the charge is located at the gate-insulator interface, it images all of its charge in the gate and has no effect on the flat-band voltage.

In the study, principally, EOT values and flat-band voltage were extracted from C-V characteristics by using the NCSU CVC modeling program. EOT values were calculated with taking quantum effect into account.

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![Fig. 2.10 Cross-section and potential diagram of an MOS capacitor.](image-url)
2.2.2 $J_{g-V}$ measurement

One of the main concepts of replacing the high-k gate dielectrics with SiO$_2$ is to suppress the gate leakage current. Thus, it is enormously important to measure the gate leakage current-voltage ($J_{g-V}$) characteristics. In addition, the properties of high-k films, such as the barrier height, effective mass, are obtained by analyzing the carrier transport mechanisms from the leakage current. To investigate the voltage and temperature dependence of gate leakage current, it is able to identify the carrier conduction mechanisms experimentally [3]. $J-V$ characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hewlett-Packard Co. Ltd.). Additionally, The Schottky, Poole-Frenkel and F-N leakage emission, which are known as major leakage mechanism, were discussed.
2.2.3 Conductance method for $D_{it}$ (Density of Interfacial Trap)

The conductance method, proposed by Nicosia and Goetzberger in 1967, is one of the most sensitive methods to determine $D_{it}$ [4]. Interface trap densities of $10^9$ cm$^{-2}$ eV$^{-1}$ and lower can be measured. It is also the most complete method, because it yields $D_{it}$ in the depletion and weak inversion portion of the band gap, the capture cross-sections for majority carriers, and information about surface potential fluctuation. The technique is based on measuring equivalent parallel conductance $G_p$ of an MOS capacitor as a function of bias voltage and frequency. The conductance, representing the loss mechanism due to interface trap capture and emission of carriers, is a measure of the interface trap density.

The simplified equivalent circuit of an MOS capacitor appropriate for the conductance method is shown in Fig. 2.12(a). It consists of the oxide capacitance $C_{ox}$, the semiconductor capacitance $C_s$, and the interface trap capacitance $C_{it}$. The capture-emission of carriers by $D_{it}$ is a lossy process, represented by the resistance $R_{it}$. It is convenient to replace the circuit of Fig. 2.12 (a) by that in Fig. 2.12 (b), where $C_p$ and $G_p$ are given by

$$C_p = C_s + \frac{C_{it}}{1 + (\omega \tau_{it})^2} \tag{2.6}$$

$$\frac{G_p}{\omega} = \frac{q \omega \tau_{it} D_{it}}{1 + (\omega \tau_{it})^2} \tag{2.7}$$

Where $C_{it} = q^2 D_{it}$, $\omega = 2\pi f$ ($f$ = measurement frequency) and, $\tau_{it} = R_{it} C_{it}$ the interface trap time constant, given by $\tau_{it} = \left[ v_{th} \sigma_p^2 N_A \exp(-q\phi_s / kT) \right]^{-1}$. Dividing $G_p$ by $\omega$ makes Eq. (2.7) symmetrical in $\omega \tau_{it}$. Eq. (2.6) and (2.7) are for interface traps with a single energy level in the band gap. Interface traps at the SiO$_2$-Si interface, however, are continuously distributed in energy throughout the Si band gap. Capture and emission occurs primarily by traps located
within a few kT/q above and below the Fermi level, leading to a time constant dispersion and giving the normalized conductance as

\[
\frac{G_p}{\omega} = \frac{qD_u}{2\omega\tau_u} \ln\left[1 + \left(\omega\tau_u\right)^2\right] \quad (2.8)
\]

Equations (2.7) and (2.8) show that the conductance is easier to interpret than the capacitance, because Eq. (2.7) does not require \(C_s\). The conductance is measured as a function of frequency and plotted as \(G_p / \omega\) versus \(\omega\). \(G_p / \omega\) has a maximum at \(\omega = 1 / \tau_u\) and at that maximum \(D_u = 2G_p / q\omega\). For Eq. (2.8) one can find

\[
\omega = \frac{1}{\tau_u} \quad \text{and} \quad D_u = \frac{2.5G_p}{q\omega}
\]

at the maximum. Hence one can determine \(D_u\) from the maximum \(G_p / \omega\) and determine \(\tau_u\) from \(\omega\) at the peak conductance location on the \(\omega\) axis. \(G_p / \omega\) versus \(f\) plots, calculated according to Eq. (2.7) and (2.8).

Experimental \(G_p / \omega\) versus \(\omega\) curves are generally broader than predicted, attributed to interface trap time constant dispersion caused by surface potential fluctuations due to non-uniformities in oxide charge and interface traps as well as doping density. Surface potential fluctuations are more pronounced in \(p\)-Si than in \(n\)-Si. Surface potential fluctuations complicate the analysis of the experimental data. When such fluctuations are taken into account, Eq. (2.8) becomes

\[
\frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_u}{\omega\tau_u} \ln\left[1 + \left(\omega\tau_u\right)^2\right]P(U_s)dU_s \quad (2.9)
\]

where \(P(U_s)\) is a probability distribution of the surface potential fluctuation given by

\[
P(U_s) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp\left(-\frac{(U_s - \overline{U}_s)^2}{2\sigma^2}\right) \quad (2.10)
\]

With \(\overline{U}_s\) and \(\sigma\) the normalized mean surface potential and standard deviation, respectively.
An approximate expression giving the interface trap density in terms of the measured maximum conductance is

\[ D_{it} \approx \frac{2.5}{q} \left( \frac{G_p}{\omega} \right)_{\text{max}} \quad (2.11) \]

Capacitance meters generally assumed the device to consist of the parallel \( C_m - G_m \) combination in Fig. 2.12 (c). A circuit comparison of Fig. 2.12 (b) to 2.12(c) gives \( G_p / \omega \) in terms of the measured capacitance \( C_m \), the oxide capacitance, and the measured conductance \( G_m \) as

\[ \frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad (2.12) \]

assuming negligible series resistance. The conductance measurement must be carried out over wide frequency range. The portion of the band gap probed by conductance measurements is typically from flat-band to weak inversion. The measurement frequency should be accurately determined and the signal amplitude should be kept at around 50mV or less to prevent harmonics of the signal frequency giving rise to spurious conductance. The conductance depends only on the device area for a given \( D_{it} \). However, a capacitor with thin oxide has a high capacitance relative to the conductance, especially for low \( D_{it} \) and the resolution of the capacitance meter is dominated by the out-of-phase capacitive current component. Reducing \( C_{ox} \) by increasing the oxide thickness helps this measurement problem.
Fig. 2.12 Equivalent circuits for conductance measurement;

(a) MOS-capacitor with interface trap time constant \( \tau_i = R_i C_i \)

(b) simplified circuit of (a)

(c) measured circuit

References


Chapter 3 Properties of Flash Lamp Annealing

3.1 Introduction
3.2 Estimation of Flash Lamp Annealing energy
   3.2.1 Experimental procedure
   3.2.2 Effect of Flash Lamp Annealing on sheet resistance
3.1 Introduction

Firstly, we need to examine the energy of the Flash Lamp Annealing. Because its thermal energy is not clearly known yet. Therefore I want to know this thermal energy to compare other heat treatment methods and applying the High-k gated stacks.

In this chapter, I would like to investigate the function of Flash lamp annealing and its thermal energy physically as heat treatment.

3.2 Estimation of Flash Lamp Annealing energy

3.2.1 Experimental procedure

One of the techniques to estimate the annealing temperature or thermal energy as heat treatment is reported. [1] [2] This technique shows the difference in the sheet resistance depending on the annealing temperature for Ni/Si multiply stacked layer (red line) as shown in Fig. 3.1. Here, I explain the experimental procedure and how to estimate the Flash Lamp Annealing thermal energy.

I apply this technique for estimating the Flash Lamp Annealing energy. Schematic illustrations of the experimental procedures are shown in Fig. 3.2. Same as those which were reported Ni/Si(0.5nm/1.9nm) structure was cyclically stacked for 8 times was deposited on the n-Si(100) substrate by RF-magnetron sputtering. The samples were annealed in N₂ ambient at various temperatures by Rapid Thermal Annealing (RTA) for 1 minutes or Flash Lamp Annealing for 0.9 mili second as following condition. The sheet resistance was measured by four point probe measurements. Finally, Flash Lamp Annealing energy was estimated by comparing the sheet resistance of the samples with RTA and with Flash Lamp Annealing.
Fig. 3.1 Sheet resistance of the film on annealing temperature. [2]

Fig. 3.2 Schematic illustrations of the experimental procedure of the estimation for Flash Lamp Annealing energy.
3.2.2 Effect of Flash Lamp Annealing on sheet resistance

Results of the effect of Flash Lamp Annealing and RTA on sheet resistance for Ni/Si multiply stacked layer is shown in Fig. 3.3.

Same as those which were reported in Fig. 3.1, relationship that the sheet resistance was changed by RTA temperature is observed. Each Flash Lamp Annealed samples were changed the sheet resistance. From this result, Flash Lamp Annealing was demonstrated that this method had certainly worked as heat treatment.

In addition, sheet resistance value were measured 340 (\(\Omega/sq\)) which was conducted Flash Lamp Annealing at 30 °C and 100 (\(\Omega/sq\)) which was conducted Flash Lamp Annealing at 200 °C. There was observed a greatly difference in Flash Lamp Annealed sample’s sheet resistance by substrate temperature. From these results, thermal budget of the Flash Lamp Annealing which conducted at 200 °C was equal to RTA at 420 °C for 1 minute. Assisting the Flash Lamp Annealing energy by substrate heater temperature was well known method. [3] In this study, I employing this method for playing the Flash Lamp Annealing effectively.
Fig 3.3 Effect of the Flash Lamp Annealing on sheet resistance for Ni/Si multiply stacked film.

References


Chapter 4 Effect of Flash Lamp Annealing on electrical characteristics of MOS Devices

4.1 Introduction

4.2 Influence of Flash Lamp Annealing condition on electrical characteristics of without PMA MOS devices
   4.2.1 Fabrication process of MOS capacitors
   4.2.2 Number of Flash Lamp Annealing times on $CV$ characteristics
   4.2.3 Flash Lamp Annealing assisted by substrate temperature on $CV$ characteristics
   4.2.4 Discussion about effect of Flash Lamp Annealing

4.3 The necessity of PMA on Flash Lamp Annealed MOS devices

4.4 Effect of Flash Lamp Annealing on electrical characteristics of MOS devices
   4.4.1 Fabrication process of MOS capacitors
   4.4.2 Effect of Flash Lamp Annealing on $CV$ characteristics
   4.4.3 Model of Flat-band Voltage shifts equation
   4.4.4 Discussion of model equation
   4.4.5 Effect of Flash Lamp Annealing on leakage current
   4.4.6 Discussion about leakage current
   4.4.7 Effect of Flash Lamp Annealing on $D_{it}$
4.1 Introduction

In this chapter, the effects of Flash Lamp Annealing on electrical characteristics of MOS device were investigated. First of all, I just tried to optimize the Flash Lamp Annealing condition by changing numbers of the Flash Lamp Annealing times and assisting substrate temperature. Finally, I examined the effect of Flash Lamp Annealing on electrical characteristics of MOS device with PMA device and discussed about reasons of the differences by conducting Flash Lamp Annealing.

4.2 Influence of Flash Lamp Annealing condition on electrical characteristics of without PMA MOS devices

4.2.1 Fabrication process of MOS capacitors

La$_2$O$_3$ films with thickness ranging from 3 to 3.5 nm were deposited as gate dielectrics by e-beam evaporation on a HF-last $n$-Si(100) substrates. The substrate temperature during the depositions was set to 250 °C. The samples were transferred to a sputtering chamber without breaking the vacuum and a 1.5-nm-thick Si film was deposited by RF magnetron sputtering. Then, Flash Lamp Annealing was performed in a diluted oxygen ambient (N$_2$:O$_2$ = 95:5) under 10 Pa for 0.9 milisecond. In this case, the maximum energy density of Flash Lamp Annealing was approximately 25 J/cm$^2$. [1] Flash Lamp Annealing was conducted at substrate temperature of 30 ~ 200 °C. After Flash Lamp Annealing, post deposition annealing (PDA) in a forming gas ambient at 420 °C for 15 minutes was carried out as the recovery annealing. A 30-nm-thick W film was in situ deposited as a gated electrode by RF magnetron sputtering. The films were patterned by reactive-ion etching (RIE) using a SF$_6$ chemistry to form the gate electrodes.
Because I just want to investigate the effects of Flash Lamp Annealing, wafers didn’t conduct the post metallization annealed (PMA). Finally, an Al contact layer on the backside of the substrate was deposited by thermal evaporation. The schematic illustration of the process flow is shown in Fig. 4.1.

Fig. 4.1 Experimental procedures of MOS capacitors process. (4.2)

4.2.2 Number of Flash Lamp Annealing times on $CV$ characteristics

First of all, I would like to examine the difference in the number of Flash Lamp Annealing times on $CV$ characteristics.

Fig. 4.2 shows the number of Flash Lamp Annealing times on EOT. EOT of 0.05 nm increment was observed by once Flash Lamp Annealing. Same characteristics can be said the Flash Lamp Annealing times of five times and ten times.
Fig. 4.3 declared that the schematic illustrations of the effects of Flash Lamp Annealing times. It is considered that 0.2 nm thick La-silicate was formed by once Flash Lamp Annealing. Profile of the La-silicate layer is changed by the numbers of Flash Lamp Annealing times.

Fig. 4.4 shows the number of Flash Lamp Annealing times on $CV$ characteristics. This result denoted capacitance was not obviously changed by the number of Flash Lamp Annealing times. On the other hand, flat-band voltage strongly depends on the Flash Lamp Annealing times. In addition, there are large hump and $CV$ hysteresis.

Fig. 4.5 shows the number of Flash Lamp Annealing times on relationship of EOT versus flat-band voltage. Same characteristics were observed as $CV$ characteristics.

![Graph showing number of Flash Lamp Annealing times on EOT.](image-url)
Fig. 4.3 Schematic illustrations of the effects of number of Flash Lamp Annealing times.

Fig. 4.4 Numbers of Flash Lamp Annealing times on $CV$ characteristics.
4.2.3 Flash Lamp Annealing assisted by substrate temperature on $CV$ characteristics

In this chapter, I investigated the effect of Flash Lamp Annealed substrate temperature on $CV$ characteristics.

Fig. 4.6 shows the effect of Flash Lamp Annealed substrate temperature on EOT. It indicates the sample’s EOT is strongly depended on the Flash Lamp Annealed substrate assisted temperature.

Fig. 4.7 shows the effect of Flash Lamp Annealed substrate temperature on $CV$ characteristics. EOT was increased by rising the Flash Lamp Annealed substrate temperature. Flat-band voltage also depends on the Flash Lamp Annealed substrate temperature. Besides, Flash Lamp Annealing conducted at 30 °C samples were observed large hump and $CV$ hysteresis. However
Flash Lamp Annealed at 200 °C and over samples were fairly improved. Flash Lamp Annealing assisted by substrate temperature is effective method for recovering $CV$ curves than numbers of the annealing time by comparing to Fig. 4.4.

Fig. 4.8 shows the effect of Flash Lamp Annealed substrate temperature on relationship of EOT versus flat-band voltage. Same characteristics were observed as Fig. 4.7.

**Fig. 4.6 Flash Lamp Annealed substrate temperature on EOT.**

**Fig. 4.7 Flash Lamp Annealed substrate temperature on $CV$ characteristics.**
It also shows that differences between conducted at 30 °C and 200 °C are EOT increment and negative flat-band voltage shifts. However there is a difference between conducted at 200 °C and 300 °C is only EOT increment. Therefore it can be said that Flash Lamp Annealing conducted at 300 °C and over act excess low k-value silicate formation and it is not suitable for EOT scaling. Flash Lamp Annealing conducted at 200 °C is balanced condition for improving electrical characteristics of MOS devices.

![Graph](image)

**Fig. 4.8 Flash Lamp Annealed substrate temperature on EOT vs. $V_{\text{fb}}$.**

4.2.4 Discussion about effect of Flash Lamp Annealing

Fig. 4.2 ~ Fig. 4.8 demonstrated the effects of Flash Lamp Annealing at several conditions. In common, these results show EOT increment and flat-band voltage shifts to negative direction.

Fig. 4.9 shows the schematic illustrations of the effects of Flash Lamp Annealing. It indicates the La-silicate formation. Degradation of the k-value is generation of the La-silicate which has
lower k-value layer. In addition, it is considered that the reason for the negative V_{fb} shift is due to the formation of the La-silicate layer which contains the positive fixed charges at the interface of the Si/La-silicate and La-silicate/n-Si. [2]

It is found that Flash Lamp Annealing conducted at 200 °C is a useful method for promoting the reaction of Si/La₂O₃/n-Si layer and preventing samples from excess lower k-value silicate formation. From the above results, Flash Lamp Annealing condition is fixed substrate temperature at 200 °C in this paper as shown in Fig. 4.10.

![Fig. 4.9 Schematic illustrations of the effect of Flash Lamp Annealing process.](image1)

<Optimized Flash Lamp Annealing condition>
5%O₂ under 10 Pa, 900V, 0.9 ms (25 J/cm²)
substrate temperature at 200 °C

![Fig. 4.10 Optimized Flash Lamp Annealing process condition in this paper.](image2)
4.3 The necessity of PMA on Flash Lamp Annealed MOS devices

In this chapter, I examined the effect of Post Metallization Annealing (PMA) on optimized Flash Lamp Annealing condition (substrate temperature at 200 °C) samples.

Fig. 4.11 shows the $CV$ characteristics of Flash Lamp Annealed samples with and without PMA. $CV$ hysteresis and hump structure which indicates the low interfacial properties were improved by PMA. [3]

Fig. 4.12 shows flat-band voltage dependence on EOT about with and without PMA MOS capacitors. Compare with to without PMA samples, only 0.1 V negative flat-band voltage shift and 0.1 nm EOT increment were observed by conducting PMA. So, Flash Lamp Annealed samples were recovered $CV$ characteristics of MOS device with a small trade-off by PMA. Therefore, I will perform the PMA for Flash Lamp Annealed samples to improve electrical characteristics in this paper.

![Fig. 4.11 CV characteristics of the Flash Lamp Annealed samples with and without PMA.](image-url)
4.4 Effect of Flash Lamp Annealing on electrical characteristics of PMA performed MOS devices

4.4.1 Fabrication process of MOS capacitors

La$_2$O$_3$ films with thickness ranging from 3 to 3.5 nm were deposited as gate dielectrics by e-beam evaporation on a HF-last $n$-Si(100) substrates. The substrate temperature during the depositions was set to 250 °C. The samples were transferred to a sputtering chamber without breaking the vacuum and a 1.5-nm-thick Si film was deposited by RF magnetron sputtering. Then, Flash Lamp Annealing was performed in a diluted oxygen ambient ($N_2$:$O_2 = 95:5$) under 10 Pa for 0.9 milisecond. In this case, the maximum energy density of Flash Lamp Annealing was approximately 25 J/cm$^2$. [1] In this section, Flash Lamp Annealing was conducted at only substrate temperature of 200 °C. After Flash Lamp Annealing, post deposition annealing (PDA) in a forming gas ambient at 420 °C for 15 minutes was carried out as the recovery annealing. A 30-nm-thick W film was in situ deposited as a gated electrode by RF magnetron sputtering. The
films were patterned by reactive-ion etching (RIE) using a SF$_6$ chemistry to form the gate electrodes. Wafers were then post metallization annealed (PMA) using a rapid thermal annealing (RTA) furnace in forming gas (FG)(N$_2$:H$_2$= 97%:3%) ambient at 420 °C for 30 min for improving the electrical characteristics of MOS devices. Finally, an Al contact layer on the backside of the substrate was deposited by thermal evaporation. The schematic illustration of the process flow is shown in Fig. 4.13.

Fig. 4.13 Experimental procedures of MOS capacitors process. (4.4)
4.4.2 Effect of Flash Lamp Annealing on $CV$ characteristics

In this chapter, I studied the effect of Flash Lamp Annealing on $CV$ characteristics of the capacitors with PMA.

Fig. 4.14 shows the effect of Flash Lamp Annealing on $CV$ characteristics of the capacitors which performed PMA at the EOT of 1.0 nm. However each samples has same EOT (capacitances), there is a clear difference in the flat-band voltage. Flat-band voltage changed about 400 mV by conducting Flash Lamp Annealing.

Fig. 4.15 shows the effect of Flash Lamp Annealing on EOT vs. flat-band voltage of the capacitors with PMA. It also shows that with Flash Lamp Annealing and without Flash Lamp Annealing samples were demonstrated the flat-band voltage roll-off and roll-up behavior, respectively. [A.3] These characteristics were also observed La$_2$O$_3$/silicate MOS devices typically. [2] It can be said that the slope of flat-band voltage on EOT relation should indicate the net fixed charges at the interface. In addition, roll-up turning point was gone to the negative direction by performing the Flash Lamp Annealing. Therefore improvement of the electrical characteristics which changed the flat-band voltage to the positive direction was observed at the EOT of below and including 1.0 nm by conducting Flash Lamp Annealing. From these results, Flash Lamp Annealing can be said that it is one of the effective methods for improving flat-band voltage at the EOT of sub 1 nm region.
Fig. 4.14 Effect of Flash Lamp Annealing on CV characteristics of the capacitors with PMA.

Fig. 4.15 Effect of Flash Lamp Annealing on EOT vs. flat-band voltage of the samples with PMA.
4.4.3 Model of Flat-band Voltage shifts equation

In this chapter, I would like to discuss the mechanism of the flat-band voltage shift to the positive direction and difference in the roll-off and roll-up characteristics by Flash Lamp Annealing as shown in Fig. 4.14 and Fig. 4.15.

I propose the model of the Flat-band voltage shifts for W/Si/La$_2$O$_3$/n-Si structures by assuming the several fixed charges as shown in Fig. 4.16. $Q_0$ is the positive fixed charges at the La-silicate/Si interface and $Q_{add}$ is also positive fixed charges into the La-silicate layer generated by diffusing the W atoms from gate electrode. Phenomenon of the W diffusion is described by complementary error function. In addition, dielectric film is defined the La-silicate layer by several annealing process and top of the La-silicate layer is Si-rich. And ‘$t$’ is the fitting parameters of the Flat-band voltage roll-off and roll-up characteristics. From this model, Flat-band voltage relationship is expressed by equation (1). Turning point from roll-off to roll-up is fitted by ‘$t$’, total physical thickness of the dielectric film is changed for expressing roll-off and roll-up characteristics.
4.4.4 Model of Flat-band Voltage shifts equation

From the equation (1), roll-off and roll-up characteristics were fitted by ‘t’ as shown in Fig.4.17. Fitting is conducted for matching the experimental data and ‘t’ is obtained. It shows the turning point of the roll-off and roll-up characteristics was changed by Flash Lamp Annealing. Shift of the turning point is indicated the increment of ‘t’. I already demonstrated the Flash Lamp Annealing is promoted the La-silicate formation at the Si/La₂O₃ interface. Therefore, it is involved the shift of roll-up point by Flash Lamp Annealing. Q₀ and C₀ were obtained by fitting EOT on Flat-band voltage characteristics. In case of without Flash Lamp Annealing samples were ‘t’ = 2, Q₀ = -5.7x10¹², C₀ = 1.73x10¹⁴. Flash Lamp Annealed samples were ‘t’ = 3, Q₀ = -2.6x10¹², C₀ = 1.27x10¹⁴ obtained by fitting eq. (1). There is not critical change in Q₀ and C₀ by Flash Lamp Annealing. At the viewpoint of ‘t’, it shows the thickness of La-rich La-silicate. In the case of the total film thickness is 4 nm, schematic illustrations of this model is shown in Fig. 4.18. It shows the distance of the Qadd to La-silicate/n-Si interface was changed.
by Flash Lamp Annealing. From these results, it is considered that the total amount of the
diffused W atoms were not so changed, but the distance of these diffused atoms were suppressed
by performing the La-silicate layer before PMA process. Therefore, improvement of the
Flat-band voltage and suppression of the Remote Coulomb Scattering (RCS) were expected by
bearing off the W atoms toward the La-silicate/n-Si interface.

![Graph showing the relationship between EOT and Flat-band voltage](image_placeholder)

*Fig. 4.17 Fitted EOT on Flat-band voltage characteristics by eq.(1).*
4.4.5 Effect of Flash Lamp Annealing on leakage current

Fig. 4.19 shows the effects of Flash Lamp Annealing on EOT vs. leakage current characteristics of the capacitors with PMA at gate bias voltage of 1.0 V. Flash Lamp Annealed samples had effectively suppressed the leakage current density about single figure and over at same EOT region. Therefore Flash Lamp Annealing can effectively suppress the leakage current density.
4.4.6 Discussion about leakage current

In this chapter, I want to discuss about the reasons of the improvement of leakage current by performing Flash Lamp Annealing as shown in Fig. 4.19.

Fig. 4.20 shows the relationship of gate voltage on leakage current for three times measured at EOT of 1.08 nm. In first time measurement, sample without Flash Lamp Annealing had experienced the breakdown at the gate bias voltage of around 2.8 V. After this measurement, leakage current had obviously increased as shown in left hand side figure. It indicates the new leakage pass generation by first time measurement. On the other hand, sample with Flash Lamp Annealing has highly I-V characteristics stability at same EOT.

Fig. 4.21 shows the schematic illustrations of the reason of the leakage pass generation. This improvement is considered that diffused W atoms make grain boundary in dielectric film and generate a new leakage path during the deposition or PMA process. It is reported that grain
boundary driven leakage path formation. If there are few amount of W atoms in dielectric films by Flash Lamp Annealing than without, inhibition of leakage current can be said that less probability of leakage pass formation. Therefore preventing the samples from diffusing the W atoms is also effective method for suppressing the leakage current density.

![Leakage current density vs Gate Voltage graph](image)

**Fig. 4.20 Relationship of gate voltage on leakage current for three times measured at EOT of 1.08 nm.**

![Schematic Illustrations](image)

**Fig. 4.21 Schematic illustrations of the reason of the leakage path generation.**
4.4.7 Effect of Flash Lamp Annealing on $D_{it}$

In this chapter, I investigated the effect of Flash Lamp Annealing on interfacial properties.

Fig. 4.22 shows the effect of Flash Lamp Annealing on density of interfacial trap ($D_{it}$) value calculated by conductance method. $D_{it}$ had slightly improved by Flash Lamp Annealing at the EOT of 1.08 nm.

Fig. 4.23 shows the effect of Flash Lamp Annealing on $CV$ hump structure at EOT of 1.08 nm. Comparing each $CV$ characteristics, hump structure had decreased by Flash Lamp Annealing. Magnitude of the hump structure accommodates to the $D_{it}$ value. [3]

<table>
<thead>
<tr>
<th>EOT (nm)</th>
<th>w/o FLA</th>
<th>w FLA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_{it}$ (/eV cm$^2$)</td>
<td>$6.29 \times 10^{13}$</td>
<td>$3.01 \times 10^{13}$</td>
</tr>
</tbody>
</table>

Fig. 4.22 Effect of Flash Lamp Annealing on Density of interfacial trap ($D_{it}$).

Fig. 4.23 Effect of Flash Lamp Annealing on $CV$ hump structure.
References

[1] USHIO Inc.


Chapter 5 Conclusion

5.1 Conclusion of this study
5.2 Future issues
5.1 Conclusion of this study

This study is examined the effects of Flash Lamp Annealing on electrical characteristics of MOS device with Si/La$_2$O$_3$/n-Si structure for balancing the EOT scaling and suppressing the fixed charge generation.

First of all, I confirmed the Flash Lamp Annealing had certainly worked as heat treatment for Si based stack. And thermal budget of Flash Lamp Annealing performed at 200 °C equals to RTA at 420 °C for 1 minute.

Secondly, I examined the effects of Flash Lamp Annealing on electrical characteristics of MOS device. Flash Lamp Annealing condition was optimized by assisting substrate temperature. In addition, it promoted the La-silicate formation at the interface of the Si/La$_2$O$_3$ and La$_2$O$_3$/n-Si. Positive flat-band voltage shift was observed the samples with PMA at the EOT of sub 1.0 nm by Flash Lamp Annealing. It is considered that the amorphous La-silicate layer formed by Flash Lamp Annealing process had effectively suppressed the distance of the diffused W atoms from gate electrode during the PMA process by modeling the Flat-band voltage roll-off and roll-up characteristics. Leakage current and interfacial properties were improved by Flash Lamp Annealing. One of the reasons for the suppression of leakage current is thought to be preventing the dielectric film from diffusing the W atoms had it reduced the probability of leakage path formation.

5.2 Future issues

In this thesis, I described about the application of the Flash Lamp Annealing to the High-k gate stack annealing for the first time and obtained the possibility of improving electrical properties.
of MOS devices.

In the future, we needed to investigate the electrical characteristics of MOS devices with Flash Lamp Annealing closely at the EOT of sub 1.0 nm region. In addition, optimization of La-silicate composition and gate electrode structure and heat treatment condition are required for going together the electrical properties and further EOT scaling.
Appendices

A.1 Relationship between pulse width and Flash Lamp Annealing Energy
A.2 The light absorption quality of Si for Xe Flash Lamp Annealing
A.3 Flat-band voltage roll-off and roll-up behavior of La$_2$O$_3$/silicate MOS capacitors
A.1 Relationship between pulse width and Flash Lamp Annealing Energy

So far, I discussed about the thermal energy and the application of the Flash Lamp Annealing. However, it can be said that Flash Lamp Annealing energy is decided by its multiplication of the pulse power and pulse width (time). [1] Therefore we need to know the dependence on these factors.

There is a relationship between pulse width and Flash Lamp Annealing energy as the parameters of the applied voltage which shown in Fig. A.1. [2] Flash Lamp Annealing Maximum energy density depends on the applied voltage and pulse width. From this relationship, Flash Lamp Annealing condition (which applied 900 V and pulse width is 0.9 milisecond) has maximum energy density of around 25 J/cm².

Fig. A.1 Relationship between pulse width and Flash Lamp Annealing Energy.
A.2 The light absorption quality of Si for Xe Flash Lamp Annealing

Fig. A.2 shows the radiant spectrum of the xenon Flash Lamp and optical coefficient of Si. [3]
The radiant peak of the xenon Flash Lamp is in the range from 300 to 800 nm. And it also
shows that Flash Lamp Annealing has a consecutive spectrum. Since the absorption edge of Si
is approximately 1100 nm, Si substrate can be effectively heated by the xenon flash lamp.
Therefore Si/La$_2$O$_3$/n-Si structure is also considered to be effectively heated by Flash Lamp
Annealing.

Fig. A.2 Radiant spectrum of the xenon flash lamp and optical coefficient of Si.
A.3 Flat-band voltage roll-off and roll-up behavior of La$_2$O$_3$/silicate MOS capacitors

Fig. A.3 shows the flat-band voltage on EOT relation of capacitors with various La$_2$O$_3$ thicknesses after PMA. It shows three regions (a), (b), (c) can be observed and flat-band voltage roll-off and roll-up behavior. [4]

Linear relationships between flat-band voltage and EOT observed in (a) is a typical sign of fixed charges located at the interface. In these cases, the fixed charges with densities of $Q_{\text{La}_2\text{O}_3/\text{silicate}}$ and $Q_{\text{silicate}/\text{Si}}$ are located at interfaces of La$_2$O$_3$/silicate and silicate/Si substrate, respectively.

In the region (b), an enhanced generation of fixed charges with $Q_{\text{fix}}$ can be extracted as the slope becomes steeper, when a linear fitting is carried out. However, considering the work function difference and the potential offset at the interfaces, one must interpret an enhanced generation of positive fixed charges at smaller EOT in region (b). The enhanced generation of fixed charges is reported to degrade the effective electron mobility and the $D_{it}$ of MOS devices. [5]

In the region (c), the flat-band voltage start to shift toward positive direction. Considering the thickness of the initially deposited La$_2$O$_3$, it is reasonable to think that all the La$_2$O$_3$ film was converted into silicate. From the slope in the region (c), positive charges with $Q_{\text{silicate}/\text{Si}}$ can be extracted to be located silicate/Si interface with a linear fitting.

The slope of flat-band voltage on EOT relation should indicate the net fixed charges at the interface.
Fig. A.3 Relationship of the EOT on flat-band voltage of La$_2$O$_3$/La-silicate capacitors after PMA performed.

(a) at the EOT range from 1.8 to 1.2 nm

(b) at the EOT range from 1.2 to 0.9 nm

(c) at the EOT below 0.9 nm

References


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