Master thesis

Thermally Resistant InGaAs Schottky Diodes using NiSi$_2$ Electrodes

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Introduction
1.1 Background of this study

Scaling technology of semiconductor devices is critical for continuing trend of more functionality in a chip. One of the major factors of the technology developments has been integrated large scale integrated circuits (LSI) high density. Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is a factor of LSI and very important device for the sophisticated integrated circuits (IC). MOSFET scaling has been proceeded for integrated LSI and is useful to progress with many device parameters for the scaling assumptions in Table 1-1, so that improve the performances of high density, high speed performance and low power consumption. Scaling size trends of DRAM and MPU are shown in figure 1-1.
Table 1-1 Device circuit parameter as a function of the scaling factor

<table>
<thead>
<tr>
<th>Interconnection Parameter</th>
<th>Scaling Factor (k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnection dimensions</td>
<td>1/k</td>
</tr>
<tr>
<td>Line resistance</td>
<td>k</td>
</tr>
<tr>
<td>Line capacitance</td>
<td>1/k</td>
</tr>
<tr>
<td>Interelectrode capacitance</td>
<td>1/k</td>
</tr>
<tr>
<td>Line response time</td>
<td>1</td>
</tr>
<tr>
<td>Line voltage drop</td>
<td>1</td>
</tr>
<tr>
<td>Line current density</td>
<td>k</td>
</tr>
</tbody>
</table>

Figure 1-1 the International Technology Roadmap for DRAM and MPU
1.2 Properties of Compound Semiconductor Materials

Currently, the increase in drive currents for faster switching speeds at lower supply voltages is largely at the expense of an exponentially growing leakage current, which leads to a large standby power dissipation. To address the scaling challenge, both industry and academia have been investigating alternative device architectures and materials, among which III-V compound semiconductor transistors stand out as promising candidates for future logic applications because their light effective masses lead to high electron mobilities (table 1-2) and high on-currents, which should translate into high device performance at low supply voltage. Recent innovations on III-V transistors include sub-100nm gate-length; high performance InGaAs buried channel and surface channel MOSFETs. Alternative channel material with high electronic mobility such as InGaAs has been studied to extend the performance in sub-10 nm devices.
### Channel Material Properties at 295K

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>GaAs</th>
<th>In$<em>{53}$Ga$</em>{47}$As</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electron Mobility</td>
<td>600</td>
<td>4,600</td>
<td>7,800</td>
<td>20,000</td>
<td>30,000</td>
</tr>
<tr>
<td>(cm$^2$V$^{-1}$s$^{-1}$)</td>
<td></td>
<td></td>
<td>n$_0$=1x10$^2$/cm$^3$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electron Saturation</td>
<td>1.0</td>
<td>1.2</td>
<td>0.8</td>
<td>3.5</td>
<td>5.0</td>
</tr>
<tr>
<td>Velocity ($10^7$ cm/s)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ballistic Mean Free Path</td>
<td>28</td>
<td>80</td>
<td>106</td>
<td>194</td>
<td>226</td>
</tr>
<tr>
<td>(nm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Energy Band-gap</td>
<td>1.12</td>
<td>1.42</td>
<td>0.72</td>
<td>0.36</td>
<td>0.18</td>
</tr>
</tbody>
</table>

Table 1·2 Channel material properties at 295 K
1.3 Schottky Diode

In the case of metal and silicon contact, the potential that is called Schottky barrier height is formed metal and silicon interface that is the commutation characteristics of pn junction. The work function of metal and semiconductor is $\phi_m$ and $\phi_o$ respectively, and the electron affinity is $\chi$. When the relationship is defined $\phi_m > \phi_o > \chi$, the Schottky barrier height is

$$\phi_B = \phi_m - \chi \quad (2.1)$$

The commutation is appeared from this potential. But, in fact the Schottky barrier height is measured that dose not depend against metal work function $\phi_m$. In generalization, the dependence on work function is small against ideal it. That reason is existence interfacial trap and interfacial layer. A lot of model are suggested in relationship among Fermi level pinning. In this case, the only ideal case is considered. The transportation structure pass through thermal electron emission obtains over the potential and tunneling structure pass through Schottky potential as shown in figure 1-2.
Figure 1-2 Schematic illustration of Schottky diode band diagram
1.4 Requirement Metal Schottky Source/Drain Junction

Although devices with InGaAs as the channel have achieved highest mobilities on nMOSFETs, source/drain (S/D) formation still faces problems. Metal Schottky S/D junction is one of the candidates to solve these problems. Because Metal Schottky S/D is a prospect technology to replace the conventional doping junction due to its atomically abrupt junction, low parasitic resistance, reduced channel doping type of concentration and low temperature process capability. These features make this type of junction especially of interest for III-V semiconductor devices because of their low dopant solubility which limits potential scaling capability.

1.5 Purpose of this study

InGaAs MOSFET is one of the promising candidates for next generation devices. However, III-V channel needs to overcome the problems. In this study, we attempted to fabricate Schottky S/D junction with III-V materials and investigate the diode characteristics of metal (Ni, TiN and stacked structure of Ni/Si)/InGaAs Schottky diodes.
Chapter 2.

Fabrication and Characterization Method
2.1 Fabrication Process of InGaAs Schottky Devices

Fabrication process of metal/InGaAs Schottky devices is shown in figure 2-1. The devices were fabricated on p-type $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrate, epitaxially grown on a p-type InP (100) substrate. The InGaAs layer thickness was at 100 nm doped at a density of $5.2 \times 10^{17}$ with Zn. The buffer InP layer below the InGaAs layer had thickness of 300 nm with a $1.1 \times 10^{18}$ Zn dopant density. III-V substrates were first degreased by acetone and ethanol. Subsequently, samples were dipped in concentrated hydrofluoric acid to removal native oxides and finally rinsed by de-ionized water. RF sputtering method was used to deposit metals and gates were patterned using lift-off method. Ni (10 nm), TiN (10 nm) and stacked structure of Ni(0.5 nm)/Si(1.9 nm) were chosen as gate electrodes. Post-metalization annealing was performed in N$_2$ gas ambient from 300 ºC to 500 ºC for 1 min. Finally, a 50-nm-thick Al contact layer on the backside of the substrates was deposited by thermal evaporation. The device structure is shown in figure 2-2.
Metal/In$_{0.53}$Ga$_{0.47}$As/$p$InP (100)
300 nm thick In$_{0.53}$Ga$_{0.47}$As on $p$InP wafer

- Acetone and ethanol cleaning
- Hf 20% (2min) treatment
- Photoresist coating and photolithography
- Metal deposition by sputtering
- Lift-off
- Annealing in N$_2$ ambient from 300°C to 500°C for 1 min
- Backside Al contact

Electrical Characterization

Figure 2-1 Fabrication process flows of metal/InGaAs Schottky devices

(a) (b)

Metal (Ti, Ni, TiN)

$\text{Si} 1.9\text{nm}$

$\text{Ni} 0.5\text{nm}$

$p$In$_{0.53}$Ga$_{0.47}$As (100)
$p$InP

Al

Figure 2-2 (a) Fabricated Schottky devices of metal/InGaAs. (b) Stacked structure Schottky devices of Ni/Si/InGaAs.
2.2 Fabrication Methods

2.2.1 Substrate Cleaning

In this study, the III-V substrates were cleaned by using acetone, ethanol and DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination.

III-V substrates were first cleaned by acetone and ethanol in ultrasonic environment. Subsequently, the substrates were dipped in concentrated hydrofluoric acid (HF, 20 %) for 2 minutes until a clean and uniform surface was achieved. Then samples were rinsed in DI water. Finally, the cleaned III-V substrates were loaded to photolithography apparatus as soon as it was dried by air gun.
2.2.2 Photolithography

After cleaned by chemicals, the substrates were coated by positive photo-resist. Positive photo-resist layers were deposited by spin coating followed by baking samples at 115 °C for 3 minutes on a hot plate. The photo-resist layered samples were aligned and exposed through e-beam patterned hard-mask with high intensity ultraviolet (UV) light at 405 nm wavelength.

Figure 2-3 The photo of photolithography apparatus
2.2.3 RF Sputtering of Gate Electrode and Metal Gate Etching

After photolithography, Schottky devices such as Ni/InGaAs, TiN/InGaAs and stacked structure NiSi/InGaAs were formed by an UHV-sputtering system shown in figure 2-4 and structure of the system is shown in figure 2-5. Sputtering is one of the vacuum processes used for depositing gate metals on substrates. Ni (10 nm), TiN (10 nm) and 8-sets of Ni(0.5 nm)/Si(1.9 nm) cyclically stacked were chosen as gate electrodes. A high voltage across a low-pressure gas (usually argon at about 20 mTorr) is applied to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the “target,” composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to, and bond with the substrate. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2-1 is attached for reference.

After the metal gate depositing, photoresist layer and top of metal gate were removed by acetone for 3 minutes in ultrasonic environment.
Figure 2-4 Photo of UHV Multi Target Sputtering System ES-350SU

Figure 2-5 Structure of UHV Multi Target Sputtering System ES-350SU
2.2.4 Thermal Annealing Process

Thermal annealing was used post gate electrode formation. The annealing process is a must to minimize defects in dielectric film at the interface or channel lattice recovery. In this study, low temperature (between 300°C-500°C) thermal treatments utilizing infrared lamp typed rapid thermal annealing (RTA) system were used. The ambience in furnace was vacuumed adequately prior to every annealing cycle and then N₂ gas was provided with flow rate of 1.5 l/min while preserving the furnace pressure at atmospheric pressure. All annealed samples were removed from the chamber under 100 °C.
2.2.5 Thermal Evaporation of Al Contact Layer

In this study, backside electrodes were formed with Al. Al was deposited by thermal evaporation method in a vacuum chamber at a background pressure up to $1.0 \times 10^{-3}$ Pa. A tungsten (W) filament is used to hold highly pure Al wires. Chamber pressure during evaporation was kept under $4 \times 10^{-3}$ Pa. The illustration in figure 2-6 shows the experimental setting.

![Figure 2-6 The schematic illustration of Al deposition](image)
2.3 Characterization Method

2.3.1 Capacitance-Voltage (C-V) Characteristics

$C$-$V$ characteristic measurements of Schottky devices were performed by precision LCR meter (HP 4284A, Agilent). The energy band diagram of a Schottky diode on a p-type substrate is shown in figure 2-7. The intrinsic energy level $E_i$ or potential $\phi$ in the neutral part of the device is taken as the zero reference potential. The surface potential $\phi_s$ is measured from this reference level. The capacitance is defined as

$$C = \frac{dQ}{dV} \quad (2.1)$$

It is the change of charge due to a change of voltage and is most commonly given in units of farad/units area. During capacitance measurement, a small-signal ac voltage is applied to the device. The resulting charge variation gives rise to the capacitance. Looking at a MOS capacitor from the gate, $C = \frac{dQ_G}{dV_G}$, where $Q_G$ and $V_G$ are the gate charge and the gate voltage. Since the total charge in the device must be zero, assuming no oxide charge, $Q_G = (Q_S + Q_{it})$, where $Q_S$ is the semiconductor charge, $Q_{it}$ the interface charge. The gate voltage is partially dropped across the oxide and partially across the semiconductor. This gives $V_G = V_F + V_{ox} + \phi_s$, where
VFB is the flat band voltage, $V_{ox}$ the oxide voltage, and $\phi_s$ the surface potential, allowing Eq. (2.1) to be rewritten as

$$C = \frac{dQ_s + dQ_n}{dV_{ox} + d\phi_s} \quad (2.2)$$

The semiconductor charge density $Q_S$ consists of hole charge density $Q_p$, space-charge region bulk charge density $Q_b$, and electron charge density $Q_n$. With $Q_S = Q_p + Q_b + Q_n$, Eq. (2.2) becomes

$$C = \frac{1}{dQ_S + dQ_n} \frac{d\phi_s}{dQ_p + dQ_b + dQ_n + dQ_n} \quad (2.3)$$

Utilizing the general capacitance definition of Eq. (2.1), Eq. (2.3) becomes

$$C = \frac{1}{C_{ox} + C_p + C_b + C_n + C_{it}} \frac{C_{ox}(C_p + C_b + C_n + C_{it})}{C_{ox} + C_p + C_b + C_n + C_{it}} \quad (2.4)$$

The positive accumulation $Q_p$ dominates for negative gate voltages for p-substrate devices. For positive $V_G$, the semiconductor charges are negative. The minus sign Eq. (2.3) cancels in either case. Eq. (2.4) is represented by the equivalent circuit in figure 2-8 (a). For negative gate voltages, the surface is heavily accumulated and $Q_p$ dominates. $C_p$ is very high approaching a shot circuit. Hence, the four capacitances are shorted as shown by the heavy line in figure 2-8 (b) and the overall capacitance is $C_{ox}$. For small positive gate voltages, the surface is depleted and the space-charge region charge density, $Q_b = qN_AW$, dominates. Trapped interface charge capacitance also contributes. The total capacitance is the combination of $C_{ox}$ in series with $C_b$ in parallel with $C_{it}$ as shown in figure
2-8 (c). In weak inversion $C_n$ begins to appear. For strong inversion, $C_n$ dominates because $Q_n$ is very high. If $Q_n$ is able to follow the applied ac voltage, the low-frequency equivalent circuit (figure 2-8 (d)) becomes the oxide capacitance again. When the inversion charge is unable to follow the ac voltage, the circuit in figure 2-8 (e) applies in inversion, with $C_h = K_s e_0 / W_{inv}$ where $W_{inv}$ is the inversion space-charge region width.

![Figure 2-7 The energy band diagram of a MOS capacitor on p-type substrate](image)
Figure 2-8 Capacitances of a MOS capacitor for various bias conditions
2.3.2 Evaluation of Schottky Barrier Height Based $C\cdot V$ Characteristics

Schottky barrier height biased reverse voltage work as capacitance against small AC signal because the charge in depletion region changes if depletion-layer width is changed by bias voltage. The charge in depletion region is expressed Eq. (2.5).

$$Q = qN_Dd = \sqrt{2q\varepsilon_s\varepsilon_0N_D(V_D + V)}$$  \hspace{1cm} (2.5)

Depletion capacitance is defined

$$C = \frac{dQ}{dV} = \sqrt{\frac{q\varepsilon_s\varepsilon_0N_D}{2(V_D + D)}}$$  \hspace{1cm} (2.6)

$1/C^2$ is calculated by Eq. (2.7)

$$\frac{1}{C^2} = \frac{2}{q\varepsilon_s\varepsilon_0N_D}(V_D + V)$$  \hspace{1cm} (2.7)

$1/C^2$ can be lined straight against reverse voltage $V$ as shown figure 2-10. Diffusion voltage $V_D$ is got from the point of $1/C^2=0$. The slope is $\frac{2}{q\varepsilon_s\varepsilon_0N_D}$ and $\varepsilon_s$ is a constant defined by a material of semiconductor, so $N_D$ is calculated by the slope. Eq. (2.7) is defined per a unit area and divided by a sample space $A$ equals Eq. (2.8).

$$\frac{\Delta(1/C^2)}{\Delta V} = \frac{2}{A^2q\varepsilon_s\varepsilon_0N_D}$$  \hspace{1cm} (2.8)
$N_D$ is

$$N_D = \frac{2}{A^2 q \varepsilon_c \varepsilon_0 \frac{\Delta(1/C^2)}{\Delta V}} \quad (2.9)$$

$E_C - E_F$ is got from Eq. (2.10)

$$n = N_C \exp \left\{ - \frac{(E_C - E_F)}{kT} \right\} \quad (2.10)$$

Schottky barrier height is expressed Eq. (2.11)

$$\phi_b = qV_D + (E_C - E_F) \quad (2.11)$$

The band structure of Schottky contact was shown as figure 2·9.

Figure 2-9  $1/C^2$-$V$ graph of Schottky contact
2.3.3 Leakage Current Density-Voltage (J-V) Characteristics

To measure the leakage current density, J-V characteristics are measured using semiconductor-parameter analyzer (HP4156A, Hwelett-Packard Co. Ltd.). The Schottky devices were measured from -1 V to 1 V.
2.3.4 Evaluation of Schottky Barrier Height Based $J$-$V$ Characteristics

When the case of $V \gg kT/q$, the index term is larger than 1, it can be ignored. The current density ($J$) of Schottky contacts is defined

$$J = J_0 e^{qV/\eta kT}$$ (2.12)

However, the current density of obtaining actual characteristics increases the index function against bias voltage. The increasing rate is less than (2.12). Therefore, the ideal factor ($n$) is used as same as pn junction

$$J = J_0 e^{qV/nkT}$$ (2.13)

If $n$ is equal to 1, (2.13) accords with (2.12), and the current density flows along theory, but usually $n > 1$.

Another, $J_0$ is expressed

$$J_0 = A^* T^2 e^{-\phi_B/kT} = \frac{4\pi q m^* k}{h^3} T^2 e^{-\phi_B/kT}$$ (2.14)

$A^*$, $k$ and $m^*$ are Richardson constant, Boltzmann constant and effective mass. From (2.14), $\phi_B$ can be obtained from $J_0$. 

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Chapter 3.

Electrical Characteristics of In_{0.53}Ga_{0.47}As Schottky Devices
3.1 Introduction

In this study, we investigated electrical characteristics of Ni/InGaAs, TiN/InGaAs and stacked structure NiSi/InGaAs Schottky diodes. $J-V$ and $C-V$ characteristics of Schottky diodes were measured at various annealing temperatures ranging from $300 \, ^\circ C$ to $500 \, ^\circ C$ and Schottky barrier height was calculated using $1/C^2$ versus applied voltage.
3.2 Electrical Characteristics and Evaluation of Schottky Barrier Height

3.2.1 Ni (10 nm)/p-type InGaAs Schottky Devices

A 10-nm-thick Ni layer was deposited on p-type InGaAs substrates. Rapid thermal post-metallization annealing (PMA) was performed in N\textsubscript{2} ambient gas ambient in the range of 300 – 500 °C for 1 min. Figure 3-1 and 3-2 show current-voltage (J-V) characteristics of Ni/p-type InGaAs Schottky diodes at as-depo condition and annealing temperatures from 300 °C to 500 °C. On/Off current ratio obtained at as-depo condition and 300 °C annealing temperature have high thermal stability window compared with annealing temperatures of 400 °C and 500 °C. Hole Schottky barrier height was calculated using 1/C\textsuperscript{2} versus applied voltage characteristics (figure 3-3 and 3-4). Figure 3-5 shows the effect of the annealing temperature on Ni/p- InGaAs diode \( \phi_{bp} \). The highest value for hole Schottky barrier height of 0.72 (eV) is achieved at as-depo condition. However, the lowest value is 0.50 (eV) at 400 °C annealing temperature.
Figure 3-1 Current-Voltage characteristics of Ni (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature.
Figure 3-2 Current-Voltage characteristics of Ni (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C
Figure 3-3 $1/C^2$ versus applied voltage of Ni (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature.
Figure 3.4 $1/C^2$ versus applied voltage of Ni (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C
Figure 3-5 Schottky barrier height versus annealing temperature of Ni deposited on InGaAs substrate extracted from $1/C^2-V$. 

Ni (10 nm)/InGaAs
N$_2$, 1 min anneal
3.2.2 TiN (10 nm)/p-type InGaAs Schottky Devices

A 10-nm-thick TiN was stacked in p-InGaAs substrates. Deposition using RF sputtering system was performed in Ar and N₂ (Ar:N₂=8:2) ambient gas.

Figure 3-6 and 3-7 show $J-V$ characteristics of TiN/p-InGaAs Schottky diodes at as-depo condition and annealing temperatures from 300°C to 500°C. On/Off current ratio obtained at as-depo condition and 300 °C annealing temperature have high thermal stability window compared with annealing temperatures of 400 °C and 500 °C. Hole Schottky barrier height was calculated using $1/C^2$ versus applied voltage characteristics (figure 3-8 and 3-9). Figure 3-10 shows the effect of the annealing temperature on TiN/p-InGaAs diode $\phi_{bp}$. The highest value for hole Schottky barrier height of 0.74 (eV) is achieved at 400 °C annealing temperature. However, the lowest value is 0.60 (eV) at 300 °C annealing temperature.
Figure 3-6 Current-Voltage characteristics of TiN (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature.
Figure 3-7 Current-Voltage characteristics of TiN (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C
Figure 3-8 $1/C^2$ versus applied voltage of TiN (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature.
Figure 3-9 $1/C^2$ versus applied voltage of TiN (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C
Figure 3-10 Schottky barrier height versus annealing temperature of TiN deposited on InGaAs substrate extracted from $1/C^2-V$
A 8-sets of Ni(0.5 nm)/Si(1.9 nm) were cyclically stacked in p-InGaAs substrates. Annealing was performed in N\textsubscript{2} ambient gas at the range of 300\textdegree C - 500\textdegree C for 1 min. Figure 3-11 and 3-12 show J-V characteristics of stacked structure NiSi/p-InGaAs Schottky diodes. NiSi stacked structure has high thermal stability window due to the fact that J-V statistical dispersion is low in a wide annealing temperature range. Hole Schottky barrier height was calculated using $I/C^2$ versus applied voltage characteristics (figure 3·13 and 3·14). Figure 3-15 shows the effect of the annealing temperature on stacked structure Ni/Si/p-InGaAs diode $\phi_{bp}$. The structure achieved stable values at the range of 300 – 500 \textdegree C.
Figure 3-11 Current-Voltage characteristics of NiSi (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature
Figure 3-12 Current-Voltage characteristics of NiSi (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C.
Figure 3-13 $1/C^2$ versus applied voltage of NiSi (10 nm)-InGaAs Schottky diodes at as-depo condition and 300 °C annealing temperature.
Figure 3.14 $1/C^2$ versus applied voltage of NiSi (10 nm)-InGaAs Schottky diodes at annealing temperatures of 400 °C and 500 °C
Figure 3-15 Schottky barrier height versus annealing temperature of NiSi deposited on InGaAs substrate extracted from $1/C^2-V$. 

NiSi (10 nm)/InGaAs 
N$_2$, 1 min anneal
Chapter 4.

Conclusion
4.1 Conclusion of this Study

We have investigated the electrical properties of metal/InGaAs diodes using Ni, TiN and a multilayer stacked Ni/Si structure. The effect on anneal temperature on the changes in On/Off current ratio and Schottky barrier height of metal/InGaAs diodes in various annealing temperatures are measured. It is shown that the largest On/Off current ratio can be achieved in Ni/Si stacked structure. This On/Off ratio is reduced in Ni or TiN gated diodes. Moreover the Ni/Si structure shows a stable ratio despite increasing the annealing temperature. Furthermore the highest value for hole Schottky barrier height of 0.78 (eV) is achieved in Ni/Si stacked diodes and this value is only marginally affected by anneal temperature, which suggests a stable interface with the InGaAs substrate. X-ray photoelectron spectroscopy of these structures revealed that the reaction of substrate in all three elements of As, Ga, and In were significantly suppressed by incorporating the Ni/Si stacked structure.
4.2 Extension of this Study

In this study, we measured metal/InGaAs Schottky diode characteristics and evaluated Schottky barrier height in order to apply for InGaAs-based MOSFETs with metal S/D region. Controlling the reaction of metal and substrate by changing the type of metal is a key factor in stabilizing the Schottky contact in various thermal treatment temperatures. High On/Off ratio of Ni/Si structure and it's low barrier height for electrons could be utilized in enhancing both mobility and drive current of InGaAs-based MOSFETs.
References

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[2.1] Dieter K. Schroder, Semiconductor Material and Device Characterization 3rd
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