Doctorial Thesis

A Study on Interfacial Properties of \( \text{La}_2\text{O}_3 \) Gate Dielectrics with Thickness Scaling

A Dissertation Submitted to the Department of Electronics and Applied Physics Interdisciplinary Graduate School of Science and Engineering Tokyo Institute of Technology

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Abstract

Aggressive scaling of Si-based metal-oxide-semiconductor field-effect-transistors (MOSFETs) has led to the replacement of gate oxide from SiO₂ to high dielectric constant (high-k) material in order to enable continuous down-scaling. Poor interface between high-k material and Si-substrate results in degradation of the device performance. Also achieving a direct high-k/Si-sub contact has been a major issue in the device research field as the EOT of the high-k gate insulator becomes small. In this thesis, we have investigated the interfacial properties and scaling potential of gate stacks with La₂O₃ as the gate oxide insulator. Direct contact between La₂O₃ and Si substrate is capable forming La-rich silicate interfacial layer with high dielectric constant and good electrical properties. In order to achieve such a desirable La-rich silicate, in-situ high-temperature annealing was conducted to control the silicate composition. Electrical characterizations such as capacitance-voltage and conductance method were employed to evaluate the La₂O₃/ La-silicate/Si interfaces. Also process guidelines were developed to minimize the defect sites within the La₂O₃ gate insulator after heat treatment. Remote Coulomb Scattering (RCS) plays an important role on the effective mobility degradation of La₂O₃ gate MOSFETs with small EOT. The location of the charges which cause Remote Coulomb Scattering (RCS) of the MOSFET channel carriers was analyzed.
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<td>Celsius temperature</td>
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<td>$T_{\text{ox}}$</td>
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<td>Oxide thickness</td>
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<td>$T_{\text{silicate}}$</td>
<td>$[\text{nm}]$</td>
<td>La-silicate thickness</td>
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<tr>
<td>$T_{\text{Phys}}$</td>
<td>$[\text{nm}]$</td>
<td>Physical thickness of gate oxide</td>
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<td>Al</td>
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<td>Aluminum</td>
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<tr>
<td>Si</td>
<td></td>
<td>Silicon</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td></td>
<td>Silicon oxide</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td></td>
<td>Lanthanum oxide</td>
</tr>
<tr>
<td>W</td>
<td></td>
<td>Tungsten</td>
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<tr>
<td>TaN</td>
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<td>Tantalum nitride</td>
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<th>Description</th>
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<tr>
<td>ITRS</td>
<td>International technology roadmap for semiconductors</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal-oxide-semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>LSI</td>
<td>Large-scaled-integrated circuit</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very-large-scaled-integrated circuit</td>
</tr>
<tr>
<td>ULSI</td>
<td>Ultra-large-scaled-integrated circuit</td>
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<tr>
<td>EOT</td>
<td>Equivalent oxide thickness</td>
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<td>E-beam</td>
<td>Electron-beam</td>
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<td>High-k</td>
<td>High dielectric permittivity materials</td>
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<td>F.G</td>
<td>Forming gas</td>
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<td>IL</td>
<td>Interfacial layer</td>
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<tr>
<td>PMA</td>
<td>Post-metallization annealing</td>
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<td>RTA</td>
<td>Rapid thermal annealing</td>
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<td>RIE</td>
<td>Reactive-ion etching</td>
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<td>RF</td>
<td>Radio-frequency</td>
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<tr>
<td>DIW</td>
<td>Diluted-ion water</td>
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<td>UHV</td>
<td>Ultra-high vacuum</td>
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<td>FT</td>
<td>Fourier transform</td>
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<td>FTIR</td>
<td>Fourier transform of infrared spectroscopy</td>
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<td>LO</td>
<td>Longitudinal optical phonon mode</td>
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<td>TO</td>
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<td>TEM</td>
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<td>XRD</td>
<td>X-ray diffraction</td>
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<td>BE</td>
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Figure 6.6  Flat band voltage as a function of the thickness of W metal gate in La\(_2\)O\(_3\)/Si MOS capacitors with \textit{in-situ} PMA in F.G for 30 min at 800 °C.

Chapter 7

Figure 7.1  Schematic cross-section of La\(_2\)O\(_3\) gate stacked MOSFET

Figure 7.2  Calculated RCS-limited electron mobility versus inversion charge density.

Figure 7.3  Measured \( C-V \) characteristics for the fabricated MOS capacitors after PMA 800 °C in F.G for 30 min; (a) EOT dependence of capacitance value; (b) Capacitance dependence on measurement frequency; in both figures, the solid lines refer to the ideal curve.
and the symbols refer to measurement data

Figure 7.4 EOT versus the thickness of the deposited La$_2$O$_3$ film. The closed symbols correspond to the total EOT extracted from the $C$-$V$ measurement; the solid line refers to the fitting curve, considering the formation of interfacial silicate layer ($T_{La$-silicate}$) within La$_2$O$_3$ layer ($T_{La$-oxide}$)

Figure 7.5 The measured electrical characterizations of W/La$_2$O$_3$ gate stacked MOSFETs annealed at 800°C in F.G for 30 minutes; (a) $I_d$-$V_d$ characteristics, and (b) Gate-to-channel ($C_{gc}$), and gate-to-body ($C_{gb}$) capacitance characteristics

Figure 7.6 Mobility versus inversion layer charge density; (a) measured effective electron mobility, and (b) extracted additional scattering-limited electron mobility for samples with PMA 800°C in F.G for 30 min; the measured device size is $L/W = 10/10 \ \mu$m and measurement frequency is 100 kHz

Figure 7.7 Mobility versus the thickness of La$_2$O$_3$ layer. $T_{La$-oxide}$ is extracted from the total EOT by considering the formation of La-silicate layer. The closed symbols correspond to the measurement data
of \( \mu_{\text{eff}} \) at \( E_{\text{eff}} = 0.3 \text{ MV/cm} \). The solid line refers to theoretical modeling.

Figure 7.8 Conductance spectra for W/La\(_2\)O\(_3\)/Si MOS capacitors with PMA 800 °C in F.G for 30 min. The dark and light symbols correspond to samples with EOT = 0.8 nm and EOT = 1.2 nm, respectively. The conductance spectra were measured with \( E-E_i \) range from -0.5 to -0.8 eV.
Chapter 1 Introduction

Since the invention of the first bipolar transistor in 1947 [1], and the realization of the first integrated circuit in 1958 [2], semiconductor device dimensions have continuously shrunk and their performance has dramatically improved. In this chapter, at first the history of semiconductor devices is briefly summarized. The major driving force behind the semiconductor technology, i.e. the Scaling Law, is explained. The necessity for introduction of high-k dielectrics into MOSFET gate insulator and the related integration issues are explained. Finally, the objective of this thesis is described.

1.1 Brief History of Semiconductor Devices

In 1906, L. D Forest invented the first vacuum tube which was used for rectifying, amplifying, and switching electrical signals [3]. Before the advent of the semiconductor transistor, vacuum tubes had been widely applied to electrical devices, and had played an important role in the development of electronics. However, even small vacuum tubes have dimensions of several cubic centimeters and substantially consume a larger amount of power.
In 1925, J.E. Lilienfeld proposed a field-effect-transistor (FET) [4]. In 1947, J. Brattain and W. Bardeen invented the first point-contact junction transistor [1, 5], and in 1948 W. Shockley proposed bipolar junction transistor (BJT) [6]. These three scientists received the Nobel Physics Prize in 1956 for their research on semiconductors and their discovery of the transistor [7]. The term ‘bipolar’ means that the operation involves both electron and hole carriers. In contrast, the FET is a ‘unipolar’ transistor that involves only one type of carriers for its operation. In 1951, W. Shockley invented junction field-effect transistor (JFET) [8]. JFET was a revolutionary replacement of the vacuum tube by a solid-state device, and it paved the way for smaller and cheaper electronic devices. In 1958, J. Kilby realized the first integrated circuit and received the Nobel Physics Prize for his innovation and pioneering work [9]. In 1960, D. Kahng fabricated metal-oxide-semiconductor field-effect transistors (MOSFETs) on Si-substrate using SiO$_2$, for the first time [10]. MOSFETs rapidly replaced the JFET and had a profound effect on microelectronics [11]. However, MOSFETs suffered from large standby power dissipation due to their single-polarity. In 1963 the complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET), which uses both $n$-and $p$-type MOSFETs, brought major breakthrough to the integrated circuits [12]. In 1970, large scale integrated circuits (VLSIs) were realized, and transistor dimensions
shrunk to a several micrometers. By the year 2000, transistors were only a several hundred nanometers in size. As shown in Figure 1.1, the size of transistor in a microprocessor has shrunk nearly 100,000 times within 40 years, and as of 2011 an advanced microprocessor included as many as 3.1 billion transistors [13].

Transistors which are the fundamental building elements of the modern VLSI, are used in almost every electronic device these days, playing a crucial role in every aspect of modern human life. The recent advances in information technology (Mini Laptop, iPhone, the Internet, and satellite etc.) demand an ever higher operational speed, lower power consumption, smaller size, and lighter weight. Electronics and information
technology based on VLSI has brought great convenience and comfort to life, and also has greatly contributed to the development of modern industry [15].

1.2 MOS Device Scaling

The continuous progress of VLSI performance has been made possible by the downsizing of transistors or “scaling”. The device feature size decreases by approximately 0.7x in every two or three years and the number of transistors on a VLSI chip doubled in every two years as shown in Figure 1.1. This trend is called as “Moore’s Law” which was first stated by Gordon Moore [16]. As shown in table 1.1, by the scaling rule, when the device dimension is scaled down with factor \( \alpha \), the supply voltage of MOSFETs should be reduced by the same factor \( \alpha \). The doping concentration should be increased by the same factor \( \alpha \), keeping the electric field in MOSFETs constant. Moreover, power dissipation per circuit is reduced by \( \alpha^2 \). By the scaling method and Moore’s Law, transistor size has shrunk to obtain higher performance and low fabrication costs.

As the result of continuous reduction of the SiO\(_2\) layer thickness, the physical thickness of SiO\(_2\) has already reached less than 1.2 nm, and the gate leakage current caused by direct-tunneling exceeds 1A/cm\(^2\) at 1 V as shown in Figure 1.2 [17]. Thus,
the stand-by power consumption is remarkably increased. In order to suppress the power consumption caused by leakage current, the conventional dielectric layer of SiO₂ is needed to be replaced by new type of materials.

Table 1.1 Scaling rules for constant-field scaling

<table>
<thead>
<tr>
<th>MOSFET device parameters</th>
<th>Multiplicative factor (α &gt;1)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scaling assumption</strong></td>
<td></td>
</tr>
<tr>
<td>Device dimension ($t_{ox}$, $L$, $W$)</td>
<td>1/α</td>
</tr>
<tr>
<td>Supply voltage ($V$)</td>
<td>1/α</td>
</tr>
<tr>
<td>Doping concentration ($N_{d}$, $N_{a}$)</td>
<td>α</td>
</tr>
<tr>
<td><strong>Behavior of device parameters</strong></td>
<td></td>
</tr>
<tr>
<td>Electric field</td>
<td>1</td>
</tr>
<tr>
<td>Carrier velocity</td>
<td>1</td>
</tr>
<tr>
<td>Capacitance ($C = εA/t_{ox}$)</td>
<td>1/α</td>
</tr>
<tr>
<td>Drift current ($I$)</td>
<td>1/α</td>
</tr>
<tr>
<td><strong>Behavior of circuit parameters</strong></td>
<td></td>
</tr>
<tr>
<td>Power density ($P/A$)</td>
<td>1/α²</td>
</tr>
<tr>
<td>Power dissipation ($\propto IV$)</td>
<td>$α^2$</td>
</tr>
<tr>
<td>Circuit density ($\propto 1/A$)</td>
<td>$α^2$</td>
</tr>
<tr>
<td>Circuit speed</td>
<td>$α$</td>
</tr>
</tbody>
</table>

Figure 1.2 Leakage current increases as EOT thinning [17].
1.3 High-k Gate Dielectric materials

High-k dielectric constant (high-k) materials are widely studied for continuing the scaling trend of MOSFETs. In this section, an introduction of high-k dielectrics is explained and their related issues are described. Also, the published results for high-k gate technology are summarized.

1. Introduction of high-k dielectrics

1) Replacement of SiO₂ gate oxide with high-k dielectrics

It is necessary to replace SiO₂ by high-k materials in order to suppress the gate leakage current for the further downscaling of MOSFETs. By using the high-k materials, the gate leakage current is suppressed at smaller EOT values as shown Figure 1.3 [18]. The relation between EOT and the thickness of the high-k layer is expressed as:

\[
EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} T_{high-k}, \quad (1.1)
\]

where \( \varepsilon_{SiO_2}, \varepsilon_{high-k} \) are the dielectric constants of SiO₂ and high-k dielectrics. \( T_{high-k} \) is the physical thickness of high-k dielectrics gate oxide.

2) Requirements for high-k gate dielectrics

The guidelines for selecting an alternative gate dielectric material includes a number of
Table 1.2 Parameters of mostly used high-k dielectrics and SiO2

<table>
<thead>
<tr>
<th>Material</th>
<th>Dielectric constant</th>
<th>Band gap [eV]</th>
<th>Interface trap density [cm⁻²/eV]</th>
<th>Phase status</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>3.9</td>
<td>8.9</td>
<td>≤1×10¹⁰</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Gd₂O₃</td>
<td>12</td>
<td>5</td>
<td>1.2×10¹¹ [19]</td>
<td>Crystal (T &gt; 400 °C)</td>
</tr>
<tr>
<td>Al₂O₃</td>
<td>12.5</td>
<td>8.8</td>
<td>4.1×10¹¹ [20]</td>
<td>Amorphous (T &lt; 700 °C) [21]</td>
</tr>
<tr>
<td>Y₂O₃</td>
<td>15</td>
<td>6</td>
<td>1.3×10¹² [22]</td>
<td>Crystal (T &gt; 400 °C) [23]</td>
</tr>
<tr>
<td>CeO₂</td>
<td>20-26</td>
<td>5.5</td>
<td>2×10¹¹</td>
<td>Crystal (T &gt; 400 °C) [24]</td>
</tr>
<tr>
<td>HfO₂</td>
<td>22</td>
<td>5.6</td>
<td>1×10¹¹ [25]</td>
<td>Crystal (T &gt; 700 °C)</td>
</tr>
<tr>
<td>ZrO₂</td>
<td>24</td>
<td>4.7 – 5.7</td>
<td>3×10¹¹ [26]</td>
<td>Crystal (T &gt; 400 °C)</td>
</tr>
<tr>
<td>Ta₂O₅</td>
<td>25</td>
<td>4.4</td>
<td>2×10¹¹ [27]</td>
<td>?</td>
</tr>
<tr>
<td>La₂O₃</td>
<td>27</td>
<td>5.8</td>
<td>1.6×10¹¹ [28]</td>
<td>Amorphous</td>
</tr>
</tbody>
</table>

Factors such as a higher dielectric constant value, a large band gap and high band offset to silicon conduction or valence bands, thermodynamic stability, interface quality, process compatibility, and reliability. Table 1.2 compares dielectric constant, band gap,
and interface state density of SiO₂ gate oxide insulator with commonly used high-k dielectrics.

2. Main problems in the high-k dielectrics

Some semiconductor companies such as Intel have already successfully introduced high-k dielectric materials in their products. However, the EOT value needs to be reduced in every new generation of the products, and there are many issues facing further EOT scaling. To solve these problems, many researchers have been performed in the world. Some of the notable results are introduced in the following.

1) Interfacial quality

Compared to conventional SiO₂ MOSFETs, high-k dielectric gate stacked MOSFETs have degraded interfacial properties in general. Lai et al. proposed a scheme of “hybrid” HK/MG integration for high performance 28 nm CMOSFETs. For high quality interfacial layer (IL) oxide/Si interface, IL oxide was formed with high/medium thermal process [29]. They achieved a low leakage current density in the device treated with a high temperature and optimizing HfO₂ high-k dielectrics by TiN metal and LaOₓ capping layer. They also achieved a 30 % performance improvement and a low threshold voltage ($V_{th}$) of 0.25 V for PFET by gate last process.

2) Flat band voltage suppression and threshold voltage control
In the high-k dielectric gate stacked MOSFETs, flat band voltage ($V_{FB}$) shift and $V_{th}$ shift are widely observed compared to conventional SiO$_2$ MOSFETs. Brunet et al. reported that HfO$_2$ and HfZrO oxide suffer large $V_{th}$ instabilities up to 230 mV when transistor channel width is scaled down to 80 nm [30]. Morooka et al. reported that reduction of Mg/La atoms in bulk high-k dielectric layer and piling Mg/La atoms up near the high-k dielectrics/IL interface and modulation of La/Mg diffusion from high-k dielectric layer can suppress the increase in $V_{th}$ instability. They achieved a $V_{th}$ reduction over 400 mV [31]. Meanwhile, Maeng et al. demonstrated interface state density ($D_{it}$) improvement and $V_{FB}$ by capping TiO$_2$ layer over HfO$_2$ gate dielectrics [32].

3) Ultrathin EOT devices

Ando et al. for the first time realized extremely scaled nMOSFETs with high-k/metal gate (HK/MG) stacks using a gate-first process. [33] They capped the HfO$_2$ layer by La and Al, followed by TiN as a gate electrode. Finally, they doped some scavenging elements in TiN. By their remote interfacial layer scavenging technique, they were able to fabricate a device with EOT of 0.42 nm. Meanwhile, they observed no extrinsic mobility degradation in the case of La capping over HfO$_2$. By depositing La$_2$O$_3$ on a thin CeO$_2$, Kakushima et al. realized LaCe-silicate MOSFET with EOT of 0.64 nm and extremely low gate leakage current of 0.65 A/cm$^2$ [34].
4) Leakage current suppression

By employing bottom interfacial SiO$_x$ layer modification techniques such as k-boosting capping, TaN-alloy gate electrode, and effective work function tuning techniques, Choi et al. successfully demonstrated extremely thin FET devices with EOT of 0.55 nm, leakage current of 0.6 A/cm$^2$, and $T_{inv}$ of 0.95 nm [35]. Xiong et al. showed that band gap, conduction band offset and conduction band minimum are simultaneously increased by doping Gd in HfO$_2$ gate dielectrics with reduction of oxygen vacancies. Also the leakage current density was reduced by almost an order of magnitude. They obtained the EOT of 0.81 nm and leakage current of 0.9 mA/cm$^2$ at 1 V gate voltage [36].

5) Mobility degradation

It is widely observed that carrier mobility in the channel of inversion mode MOSFETs with high-k dielectrics is largely degraded compared to the conventional MOSFETs with SiO$_2$ dielectric. Robertson showed that mobility value is largely reduced (to less than 110 cm$^2$/Vs) in HfO$_2$ and HfSiO dielectric layer MOSFETs [37]. Therefore, he suggested that the effect of complete gate stack and its thickness must be considered for a gate dielectric with a higher dielectric constant than HfO$_2$.

6) Suppress Fermi level pinning
Liu and Robertson showed that adding group III elements such as La, Y, Sc and Al can passivates oxygen vacancies in the HfO$_2$, ZrO$_2$ and suppress Fermi level pinning [38]. They also showed that Effective Work Function (EWF) can be suppressed by adding La or Al into HfO$_2$ which passivates oxygen vacancies.

7) Thermal stability

Thermal stability is also one of the most important factors that should be considered. Kwon and Chabal showed that Ta-O bonds in TaN layer of the gate stacks (TaN/high-k/SiO$_2$/Si) are very sensitive to the annealing temperature during post deposition annealing (PDA) [39]. Zafari et al. showed that gate stacks with high-k dielectric layers such as oxide/HfO$_2$ and oxide/Al$_2$O$_3$, are inherently instable due to the oxygen vacancies which exist in the HfO$_2$ layer. These oxygen vacancies lead to $V_{th}$ instability due to the charge trapping, negative bias temperature instability, hot carrier stressing, de-trapping kinetics and transient charge trapping effects [40].

8) Parasitic gate charge

In ultra-thin high-k dielectric gate stacked MOSFETs, parasitic gate charge is a major issue. Komaragiri et al. demonstrated that the drain current performance is highly improved by using a $p$-type poly gate instead of an $n$-type poly gate in an nMOSFET [41].
9) **Permittivity and barrier height**

In high-k dielectrics, permittivity has a trade-off relation with conduction or valance band barrier height. Thus the permittivity value of the chosen high-k material must be chosen accordingly to control the gate leakage current density [42].

**1.4 Lanthanum Oxide (La$_2$O$_3$) Gate Dielectrics**

Various high-k materials have been investigated as gate oxide insulator, including Gd$_2$O$_3$ [43], CeO$_2$ [44], Y$_2$O$_3$ [45-46], Al$_2$O$_3$ [47], TiO$_2$ [48], ZrO$_2$ [49], HfO$_2$ [50] and silicates of Hf, Zr, and Y [51-53]. However, there is a tradeoff relationship between dielectric constant value of a high-k material and its band offset as shown in Figure 1.4 [16]. La$_2$O$_3$ is considered as one of the most promising candidate for high-k dielectrics for the following reasons:

1) Lanthanum oxide (La$_2$O$_3$), has a wide band gap ($E_g = 5.6$ eV) and a relatively high dielectric constant ($\varepsilon_{La_2O_3} = 23.4$) (Figure 1.4).

2) La$_2$O$_3$ can form a direct contact with Si-substrate without formation of SiO$_2$ layer at the Si-substrate interface [55]. A silicate layer at the La$_2$O$_3$/Si-substrate interface is formed after annealing as shown in Figure 1.5. Both TEM image and XPS spectra confirm the formation of a La-silicate Interfacial Layer (IL) with a high dielectric
constant (8~14), as shown in Figure 1.6. This is in contrast with HfO$_2$-based oxides which promote the formation of a SiO$_x$ IL (Figure 1.7). Recent theoretical studies have explained the physical nature of La-silicate formation in La$_2$O$_3$ and SiO$_2$ formation in HfO$_2$ [56].

**Figure 1.4** Band gap versus dielectric constants [54].

**Figure 1.5** After annealing a La-silicate interfacial layer formed between La$_2$O$_3$ and Si-substrate.
However, like most of the high-k materials, the La$_2$O$_3$ exhibit higher surface states, $D_{it} \sim 10^{11-12}$ cm$^{-2}$eV [28], and large flatband voltage shift due to high fixed charge density in the dielectric layer [18], depending on the process condition. These high surface states and fixed charges lead to degradation of the device performance. Therefore, interfacial
property improvement is one of the important issues for the development of La₂O₃ gate
MOSFETs with small EOT.

1.5 Objective of This Study

The purpose of this thesis is to study the interfacial properties of La₂O₃ gate dielectrics
and provide guidelines for improving their performance. Mobility degradation
mechanism, including Remote Coulomb Scattering effects, in thin-EOT MOSFETs with
La₂O₃ gate dielectrics is studied.

Figure 1.8 shows the outline of this thesis. The following are the brief descriptions of
each chapter:

In Chapter 1, a brief history of transistors is given and the scaling law for the
MOSFETs is summarized. Then, the problem of the conventional SiO₂ gate insulator
thinning is explained and the necessity of the introduction of high-k gate dielectrics as
the solution is described. After the review of the recent high-k gate insulator research,
purpose of the thesis research is described.

In Chapter 2, the fabrication processes of MOS capacitors and MOSFETs with high-k
gate insulator are explained. Then, methods for the physical and electrical
characterization of the above MOS samples are described.
In Chapter 3, the results of the study on the formation mechanism of La-silicate interfacial layer (IL) at the La$_2$O$_3$/Si interface are described. From the analyses using TEM and XPS techniques, the formation of the La-silicate IL with high dielectric constant value (8 ~ 14) was confirmed. EOT increment by increasing the annealing temperature was evaluated. The results of Fourier Transform Infrared (FTIR) spectroscopy indicate that high temperature annealing above 600 °C is necessary for...
relaxing the stretch of the SiO\textsubscript{4} tetrahedral network in the La-silicate layer so as to improve the interfacial properties.

In Chapter 4, the results of the investigation on the electrical characteristics of MOS devices with La\textsubscript{2}O\textsubscript{3} gate dielectrics are given. A novel interpretation of the conductance spectra was developed in order to analyze the location of the trapping sites. Two distinct peaks in the conductance spectra revealed that a large number of slow trap states exists within the gate insulator. It was found that Post Metallization Annealing (PMA) in the forming gas ambient is not effective for reducing this type of the number of the slow traps which are mainly located at the La\textsubscript{2}O\textsubscript{3}/La-silicate interface.

In Chapter 5, the results of the study on the effect of PMA on the interfacial properties of the La\textsubscript{2}O\textsubscript{3}/La-silicate MOS capacitor are shown. Samples treated with \textit{in-situ} annealing result in smaller EOT in comparison with the samples treated with \textit{ex-situ} annealing. The results indicate that \textit{in-situ} annealing is preferable for reducing the EOT of La\textsubscript{2}O\textsubscript{3} gate stack MOS capacitors.

In Chapter 6, the results of the study on the effect of the choice of gate-electrode metal material as well as that of the metal thickness on the interfacial silicate layer formation and the interfacial property are described. According to the experiments, W gate electrode devices showed better interfacial properties compared with those of TaN.
Moreover, it was found that increasing the W physical thickness is effective for lowering the interfacial state density. Controlling the amount of oxygen supplied from the gate electrode metal during the thermal process is considered the key for obtaining the good quality of the gate oxide and its interface.

In Chapter 7, the results of the investigation on the effect of RCS on the electron mobility are described. It was confirmed that RCS by charges located near the metal gate/high-k interface cause mobility degradation in La$_2$O$_3$ gate stacked MOSFETs with small EOT. It was shown that suppressing the diffusion of gate metal atoms into the gate oxide high-k insulator is effective for suppressing RCS.

Finally, in Chapter 8, summary and conclusions of the thesis research are given.
References


Chapter 2 Fabrication and Characterization Methods

In this chapter, sample fabrication and characterization methods for MOS capacitors and nMOSFETs used in this study are described.

2.1 Fabrications of MOS Capacitors and MOSFETs

The process fabrication of MOS capacitors and MOSFETs involves the steps of surface cleaning of Si-substrate, oxide layer deposition, gate electrode deposition, thermal annealing, patterning and contacting of electrodes.

1) Fabrication process for MOS capacitors

Two types of Si wafers were used in our experiments. 1: Commercially available wafer with a 400 nm thick thermally grown SiO$_2$ layer on both sides (front and back) of the Si (1 0 0) substrate. 2: plane Si (1 0 0) wafer.

In Figure 2.1, fabrication process flow for MOS capacitors is shown. SiO$_2$ (400 nm)/Si-sub with doping concentration of $3 \times 10^{15} \ cm^{-3}$ were first degreased by acetone and ethanol. Substrates were then patterned by photo lithography for gate electrodes and the SiO$_2$ layer of the gate area was etched away. Standard SPM and
diluted-HF (1%) cleaning was performed on gate areas. Substrates were loaded to an ultra-high vacuum chamber equipped with electron-beam (E-beam) guns. High-k thin films were deposited on the Si-substrate using E-beam evaporation at controlled rate and pressure. Metal gate electrodes were formed by Radio Frequency (RF) sputtering system. Metal gate electrodes were patterned by photo lithography and the gate area was formed by reactive ion etching (RIE). This was followed by heat treating devices in a Rapid Thermal Annealing (RTA) unit. Finally, Al metal was deposited by thermal evaporating to form back contact. The experimental conditions and parameters for these fabrication processes will be described in detail in the following sections.

2) Fabrication process for MOSFETs

Figure 2.2 shows the fabrication flow of nMOSFETs. First, $p$-type Si (1 0 0) substrates with pre-formed source and drain were cleaned by SPM, and diluted-HF treatment. The
substrate doping concentration is $3 \times 10^{16}$ cm$^{-3}$. High-k layer and metal gate electrode were deposited by E-beam evaporation system and RF sputtering system, respectively. Metal gate area was patterned by RIE. Thermal annealing was conducted in a RTA system. Next, high-k and 400 nm thick SiO$_2$ layers which cover the source/drain were removed by RIE and wet etching. Al contacts for source/drain as well as backside contact were deposited by thermal evaporation.

![Fabrication process flow for nMOSFETs](image)

Figure 2.2 Fabrication process flow for nMOSFETs.

3) Surface cleaning of substrates

Surface cleaning of substrates is an important step in MOS device fabrication process. The sources and the related effects on device performance of the Si-substrate contaminations are shown in table 2.1.
Table 2.1 Sources and related effects of various contaminations

<table>
<thead>
<tr>
<th>Contamination</th>
<th>Possible source</th>
<th>Effects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Particles</td>
<td>Equipment, ambient, gas, DIW, chemical</td>
<td>Low oxide breakdown (BKD); Poly-Si and metal bridging-induced low yield;</td>
</tr>
<tr>
<td>Metal</td>
<td>Equipment, chemical, reactive ion etching, implantation, ash removing</td>
<td>Low BKD field; Junction leakage; $V_{th}$ shift;</td>
</tr>
<tr>
<td>Organic</td>
<td>Vapor in room, residue of photo-resister, storage containers, chemical</td>
<td>Change in oxidation rate;</td>
</tr>
<tr>
<td>Micro roughness</td>
<td>Initial wafer material, chemical</td>
<td>Low oxide BKD field; Low mobility of carrier;</td>
</tr>
<tr>
<td>Native oxide</td>
<td>Ambient moisture, DIW, rinse</td>
<td>Degraded gate oxide; High contact resistance; Poor siliside formation;</td>
</tr>
</tbody>
</table>

Figure 2.3 shows the processes flow for Si wafer cleaning. First, the Si wafer is rinsed with Diluted Ion Water (DIW) for 5 minutes. Next, the Si wafer is rinsed in SPM ($\text{H}_2\text{O}_2:\text{H}_2\text{SO}_4 = 1:4$) solution followed by a HF (1%) solution dip. This step results in hydrogen termination of substrate’s surface (HF-last) and is effective for reducing defects at oxide/Si-sub interface.

4) Gate oxide deposition by electron-beam evaporation system

In this study La$_2$O$_3$ dielectric film is deposited by the E-beam evaporation method in the ultra high vacuum deposition chamber, as shown in Figure 2.4. There are eight
compartments to allocate various solid high-k material sources at the bottom of the chamber. The Si-substrate is heated and its temperature is maintained at 250 to 300 °C during La$_2$O$_3$ deposition. Electron beam is accelerated at 5 kV and focused towards the La$_2$O$_3$ source which results in its evaporation. During evaporation process, the base pressure inside growth chamber is maintained at $10^{-6} - 10^{-7}$ Pa. The physical thickness of the deposited La$_2$O$_3$ thin film is controlled and monitored by a crystal oscillator. To ensure a better uniformity of the deposited film layer, the sample holder is rotated during La$_2$O$_3$ layer deposition.

![Figure 2.4 Schematic illustration of E-beam evaporation system.](image)

5) Gate electrode deposition by radio frequency sputtering system

Tungsten (W) and tantalum nitride (TaN) were deposited by RF sputtering system on top of the La$_2$O$_3$ layer. Figure 2.5 shows the schematic illustration for RF magnetron
sputtering system. This equipment deposits metal film by means of physical sputtering that occurs in a magnetically-confined RF plasma discharge of an inert argon (Ar) gas ambient. The base pressure during sputtering process is $10^{-5}$ Pa. The thickness of the sputtered W (or Ta) metal layer was controlled by deposition time, and the thickness of the La$_2$O$_3$ layer was confirmed by spectroscopic ellipsometer measurements.

![Schematic illustration of RF sputtering system](image)

*Figure 2.5 Schematic illustration of RF sputtering system [1].*

6) Reactive ion etching for gate electrode and gate dielectrics

RIE is one of the methods to etch the patterned films [2]. It is similar to RF magnetron sputtering, but it is used by not only physical but also chemical reaction. The schematic illustration of RIE system is shown in Figure 2.6.

The etching gases for metal gate, high-k layer (La$_2$O$_3$) and resistor ash are sulfur hexafluoride (SF$_6$) gas, Ar gas, and O$_2$ gas, respectively. Table 2.2 shows RIE gases for
etching contaminations in the gate stacks. First, the gas used to etch the film, turns to plasma. In the plasma status, ionized radicals of cations and anions exist in the process chamber. Chemical reaction occurs when the ionized radicals are absorbed on the substrates, and the unprotected part of the sample is removed from the substrates. Meanwhile, as a physical etching process, collisions of cations with the substrates occur due to the electric field.

**Figure 2.6** Schematic illustration of RIE system [3].

**Table 2.2** Etching methods for gate metal and dielectric layers in the gate stacks

<table>
<thead>
<tr>
<th>Contamination</th>
<th>Etching method</th>
<th>conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>Wet etching in BHF solution</td>
<td>at 23 °C</td>
</tr>
<tr>
<td>W</td>
<td>RIE by SF₆ gas</td>
<td>Gas flow 30 sccm, RIE power 30 W at 23 °C</td>
</tr>
<tr>
<td>Ta</td>
<td>RIE by SF₆ gas</td>
<td>Gas flow 30 sccm, RIE power 30 W at 23 °C</td>
</tr>
<tr>
<td>TaN</td>
<td>RIE by SF₆ gas</td>
<td>Gas flow 30 sccm, RIE power 30 W at 23 °C</td>
</tr>
<tr>
<td>La₂O₃</td>
<td>RIE by Ar gas</td>
<td>Gas flow 15 sccm, RIE power 50 W at 23 °C</td>
</tr>
<tr>
<td>Resistor ash</td>
<td>RIE by O₂ gas</td>
<td>Gas flow 99 sccm, RIE power 30 W at 23 °C</td>
</tr>
<tr>
<td>Al</td>
<td>Wet etching in NMD-3 (2.38%)</td>
<td>at 23 °C</td>
</tr>
</tbody>
</table>
7) Thermal annealing process

Thermal annealing process is used in modern semiconductor fabrication for defects recovery, lattice recovery or impurity electrical activation of doped or ion implanted wafers. During the thermal annealing process there is a possibility for ingredients of each layer in MOS structure to diffuse into other layers. A proper thermal annealing process must be selected to acquire the desired device performance. In this thesis, we studied both \textit{in-situ} annealing and \textit{ex-situ} annealing approaches. \textit{In-situ} annealing process is when wafers are directly loaded into thermal annealing system after metal gate deposition without exposing the wafers to the air. In contrast, \textit{ex-situ} annealing process is when the wafers are taken out from metal gate deposition system and exposed to air in order to transfer into a thermal annealing unit. In this study, thermal treatment utilizing infrared lamp typed rapid thermal anneal (RTA) system was applied. For \textit{ex-situ} annealing, QHC-P610CP RTA system (ULVAC Co.) is applied for post metallization annealing (PMA) in forming gas (F.G) (H$_2$:N$_2$ = 3%:97%). Figure 2.7 illustrates the schematic drawing for ULVAC QHC-P610CP [4].

For \textit{in-situ} annealing, prior to every annealing cycle, residual gas species inside the anneal chamber and gas lines were pumped out and purged to minimize possibility of contamination of other existence gases or particles.
8) Vacuum pumps

Vacuum components play an important role in semiconductor technology, especially in MOS device fabrication processes. A schematic of turbo and rotary pump connection settings are shown in Figure 2.8. Table 2.3 shows vacuum pumps and their usages applied in this study.

![Figure 2.7 Schematic illustration for QHC-P610CP RTA system.](image1)

![Figure 2.8 Schematic illustration of a vacuum process chamber for fabrication of MOS devices.](image2)
Table 2.3 Vacuum pumps and their classification for MOS device processes

<table>
<thead>
<tr>
<th>Vacuum levels</th>
<th>Type of pumps</th>
<th>Vacuum levels</th>
<th>Usages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low level vacuum</td>
<td>Rotary pump</td>
<td>$10^{3}$-$10^{4}$ Pa</td>
<td>Rough pumping</td>
</tr>
<tr>
<td></td>
<td>Diffusion pump</td>
<td>$10^{-2}$-$10^{-5}$ Pa</td>
<td>When contaminations are not critical</td>
</tr>
<tr>
<td>High level vacuum</td>
<td>Turbo molecular pump</td>
<td>$10^{-2}$-$10^{-8}$ Pa</td>
<td>When contaminations are concerned</td>
</tr>
</tbody>
</table>

2.2 Physical Characterization of Gate Dielectrics

The physical characterization of deposited La$_2$O$_3$ films consisted of spectroscopic ellipsometry measurements for physical thickness determination (of as-deposited samples or La$_2$O$_3$ without annealing), transmission electron microscopy (TEM) for the imaging of the structures and X-ray photoelectron microscopy (XPS), and also Fourier transform infrared (FTIR) spectroscopy measurements for the analyzing of characteristics of the chemical bondings at the interfaces created between La$_2$O$_3$ and silicon-substrate. In this paragraph, an introduction for these measurement methods was briefly described.

1) Ellipsometry measurement

Ellipsometry is a technique for analyzing the properties of a material (include in thin films and semiconductors) from the characteristics of light reflected from its surface. In this thesis, the initial physical thickness of the deposited La$_2$O$_3$ thin film was optically
extracted by Photal FE-5000 ellipsometer (OTSUKA Electronics) using a Cauchy model and a single layer approximation [5]. As seen in Figure 2.9, the incident light angle ($\theta_0$) was fixed at 70°. The wavelength of the incident light was varied from 300 to 800 nm.

In the ellipsometry measurement technique, a linearly polarized incident light changes polarization state when it reflected from the film surface. The name ‘Ellipsometer’ is related to the fact that the reflected light is elliptically polarized. The polarization can be described by the $\sigma$ (light polarized perpendicular to the plane of incidence) and $\pi$ (light polarized parallel to the plane of incidence) components of the electric field component of the propagating light. The polarized light can be measured by a detector and the complex ratio of the two reflection coefficients of $\pi$ and $\sigma$ polarized lights

*Figure 2.9 Schematic illustration of ellipsometer [6].*
\[
P = \frac{P_\pi}{P_\sigma} = \tan(\varphi)e^{i\Delta}, \quad (2.1)
\]

is the basic equation in ellipsometry measurement. Where \( \varphi \) and \( \Delta \) are two important parameters as functions of the complex refractive index of the film material.

Film thickness can be determined by three phase optical system consisting of air/film/substrate structure. The reflection and transmission of the incident wave in the air/film/substrate optical system is depicted in Figure 2.9. The incident angle for the wave from the air (medium 0) to film is \( \theta_0 \). The incident wave is partially reflected at the boundary and partially transmitted through the film (medium 1) at angle of \( \theta_1 \). The transmitted part of the incident wave propagates through medium 1, again partially reflected and partially transmitted through substrate (medium 2) at an angle of \( \theta_2 \). By analyzing the reflection and transmission coefficients of \( \sigma \) and \( \pi \) polarized light, the film thickness, \( d \), can be expressed as [7]:

\[
d = \frac{1}{2\pi} \cdot \frac{\lambda \beta}{\bar{n}_i \cos(\theta_1)}. \quad (2.2)
\]

Where \( \lambda \) is wave length, \( \bar{n}_i \) is complex refractive index of the film. \( \beta \) is phase change
due to the propagation of the light wave through the medium 1, and can be related to the reflection of the light from the medium 1 by an expression of [7]

\[
P = \frac{P_{\pi}}{P_{\sigma}} = \frac{\rho_{12,\pi} \rho_{01,\sigma} \rho_{12,\sigma} e^{-j4\beta} + (\rho_{01,\pi} \rho_{01,\sigma} \rho_{12,\sigma} + \rho_{12,\pi}) e^{-j2\beta} + \rho_{01,\pi}}{\rho_{01,\pi} \rho_{12,\pi} \rho_{12,\sigma} e^{-j4\beta} + (\rho_{01,\pi} \rho_{12,\pi} \rho_{01,\sigma} + \rho_{12,\sigma}) e^{-j2\beta} + \rho_{01,\sigma}}.
\]  \hspace{1cm} (2.3)

Where \( \rho_{01,\pi} , \rho_{01,\sigma} , \rho_{12,\pi} , \rho_{12,\sigma} \) are complex reflection coefficients related to the complex refractive indexes, \( \tilde{n}_0 , \tilde{n}_1 , \tilde{n}_2 \) for medium 0, 1, and 2 respectively. If a set of ellipsometric parameters are measured at a given angle of incidence \( \theta_0 \) and a given wavelength \( \lambda \), by solving eq. (2.1) and (2.3) for the phase change \( \beta \), the film thickness of a sample can be determined by eq. (2.2).

2) Transmission electron microscope

Transmission electron microscope (TEM) uses a high voltage electron beam for creating images instead of using the visible light (wavelength of 400 -700 nm). Using TEM enables the observation of objects in the order of a few nanometers.
The imaging process of the TEM is illustrated in a schematic Figure 2.10. Electrons are emitted by an electron gun, and the electron beam is accelerated by an anode typically at $+100$ keV (generally 40 to 400 keV) with respect to the cathode. The accelerated electrons focused by electrostatic and electromagnetic lenses, and transmitted through the specimen. The electrons transmitted through the specimen, carries information about the structure of the specimen that is magnified by the objective lens system of the microscope. The spatial variation in this information of the specimen may be viewed by projecting the magnified electron image onto a fluorescent viewing screen coated with a phosphor or scintillator material such as zinc sulfide. Alternatively, the image can be photographed by charge-coupled device (CCD) camera. The image detected by the CCD is displayed on a monitor.

The smallest distance between two points that we can resolve by our eyes is about 0.1-0.2 mm [8]. This distance is the resolution of our eyes. The Rayleigh criterion defines the resolution of light microscope as [8]:

$$\delta = \frac{0.61\lambda}{n \sin \beta}, \quad (2.4)$$
where $\lambda$ is the wavelength of the radiation, $n$ is the refractive index of the view medium and $\beta$ is the semi-angle of collection of the magnifying lens. For the green light with the wave length 550 nm, the resolution of light microscope gives around 0.3 $\mu$m. 

Based on wave-particle duality, if an electron is accelerated by an electrostatic potential drop $V$, the electron wavelength can be described as [9]:

$$
\lambda = \frac{h}{mv} = \frac{h}{\sqrt{2m_0eV[1 + eV/(2m_0c^2)]}}.
$$

(2.5)

Where $h$ is Planck constant, $m_0$ is electron rest mass of electron, and $c$ is the speed of light. If we take the potential as 100 keV, the wavelength is 0.0371 Å. From eq. (2.4) and (2.5), the higher accelerating rate of the electron beam, the higher resolution can be obtained [10].

3) X-ray photoelectron spectroscopy

XPS is a well established technique for surface analyses of composition, and nature of oxygen bonding and also oxidation state of the cations in the thin films.
XPS spectra are obtained by irradiating material with a beam of X-ray and simultaneously measuring the kinetic energy and the number of escaped photoelectrons from the ionized atoms by the X-ray irradiation. The process of electron emission is shown schematically in Figure 2.11, where an electron from the K shell is ejected from the atom (a 1s photoelectron). The relation between the energy of the incident photon and escaped electrons from the material is expressed as [11]:

\[ \hbar \omega = E_{\text{kin}} + E_{\text{bind}} + \phi_{\text{work}} , \quad (2.6) \]

\[ E_{\text{bind}} = E_{\text{ion}} - E_{\text{atom}} . \quad (2.7) \]

Where \( \hbar \omega \), \( E_{\text{kin}} \), \( E_{\text{bind}} \), and \( \phi_{\text{work}} \) are energy of incident photon, kinetic energy of
escaped electron from material, binding energy of atoms in material, and work function of the spectrometer. Binding energy is representing the difference in energy between the ionized and neutral atoms.

XPS spectra are plots of the measured numbers of the detected electrons versus the kinetic energy of the detected photons. Different elements have different characteristic set of peaks in their XPS spectra. The characteristics peaks refer to electron configuration of the electrons within the atoms, for instance, 1s, 2s, 2p, 3s, etc. The peak area determines the amount of elements within the area irradiated by X-rays. The electronic state of the atom can affect the value of binding energy. When an atom is bonded to another atom, the binding energy of the electron may increase or decrease. The change in the binding energy can be applied to indentify the final electronic state of
the atoms in the sample. Figure 2.12 shows XPS core-level of O 1s spectra for HfO$_2$ layer [12]. The binding energy for O 1s shifts to higher energy side with the increase of the thickness of the HfO$_2$ layer. Table 2.4 summarized binding energy of gate dielectrics applied in this study.

<table>
<thead>
<tr>
<th>Bonds</th>
<th>Electronic state</th>
<th>Binding energy [eV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si$^0$</td>
<td>Si 2$p_{3/2}$</td>
<td>99.25 [13]</td>
</tr>
<tr>
<td>Si$^{4+}$</td>
<td>Si 2$p_{3/2}$</td>
<td>103.15 [13]</td>
</tr>
<tr>
<td>CeO$_2$</td>
<td>O 1$s$</td>
<td>530.4 [14]</td>
</tr>
<tr>
<td></td>
<td>Ce 3$d_{3/2}$</td>
<td>904.2 [15]</td>
</tr>
<tr>
<td></td>
<td>Ce 3$d_{5/2}$</td>
<td>898.8, 885.9 [15]</td>
</tr>
<tr>
<td>Ce$_2$O$_3$</td>
<td>O 1$s$</td>
<td>530.7 [14]</td>
</tr>
<tr>
<td></td>
<td>Ce 3$d_{3/2}$</td>
<td>901.0, 907.5, 916.8 [15]</td>
</tr>
<tr>
<td></td>
<td>Ce 3$d_{5/2}$</td>
<td>882.2, 888.2, 898.5 [15]</td>
</tr>
<tr>
<td>Hf-O</td>
<td>O 1$s$</td>
<td>531.3 [12]</td>
</tr>
<tr>
<td>Si-O-Si</td>
<td>O 1$s$</td>
<td>533.45 [15]</td>
</tr>
<tr>
<td>Hf-O-Si</td>
<td>O 1$s$</td>
<td>531.8 [12]</td>
</tr>
<tr>
<td></td>
<td>Si 2$p$</td>
<td>103.3 [12]</td>
</tr>
<tr>
<td>La-O-Si</td>
<td>O 1$s$</td>
<td>531.70 [15]</td>
</tr>
<tr>
<td>La-O-La</td>
<td>O 1$s$</td>
<td>529.56 [16]</td>
</tr>
<tr>
<td></td>
<td>La 3$d_{5/2}$</td>
<td>835.7, 839.2 [17]</td>
</tr>
</tbody>
</table>

4) Fourier-transform infrared spectroscopy measurement

FTIR is a vibrational spectroscopy measurement method based on the absorption of infrared photons that excite vibrations of molecular bonds. As shown in Figure 2.13,
FTIR spectroscopy measurement method first collects an interferogram of a sample using an interferometer and detector, then performs a Fourier transform (FT) on the interferogram to obtain the spectrum. The FTIR spectra of La$_2$O$_3$ thin film was obtained by JASCO FT/IR-4200 spectrometer.

Infrared spectroscopy exploits the fact that molecules absorb specific frequencies that are characteristic of their structure. These absorptions are resonant frequencies, i.e., the frequency of the absorbed radiation matches the vibration frequency of the bond or group in the chemicals. Molecules only absorb infrared light at those frequencies where the infrared light affects the dipolar moment of the molecule. In a molecule, the differences of charges in the electronic fields of its atoms produce the dipolar moment of the molecule. Molecules with a dipolar moment allow infrared photons to interact with the molecule causing excitation to higher vibrational states. The homo-polar diatomic molecules do not have a dipolar moment since the electronic fields of its atoms are equal. Monatomic molecules do not have a dipolar moment since they only have one

![Figure 2.13 Schematic illustration of FTIR measurement system.](image)
atom. Therefore, molecules with homo-polar diatomic or with monatomic do not absorb infrared light. For instance, the homo-polar diatomic (H₂, N₂, O₂, etc.) molecules and the monatomic (He, Ne, Ar, etc.) molecules do not absorb infrared light.

When an infrared light interacts with the matter, a chemical functional group tends to adsorb infrared radiation in a specific wave number range regardless of the structure of the rest of the molecule. For example, the C = O stretch of a carbonyl group appears at around 1700 cm⁻¹ in a variety of molecules.

When an interferogram is Fourier transformed, a single beam spectrum is generated. A single beam spectrum is a plot of raw detector response versus wave number. A single beam spectrum obtained without a sample is called a background spectrum, which is induced by the instrument and the environments. Characteristic bands around 3500 cm⁻¹ and 1630 cm⁻¹ are ascribed to atmospheric water vapor and the bands at 2350 cm⁻¹ and 667 cm⁻¹ are attributed to carbon dioxide. The single beam spectrum of the sample must be normalized against the background spectrum. Consequently, a transmittance spectrum is obtained as follows:

\[
T = \frac{I}{I_0}, \quad (2.8)
\]
where $T$ is transmittance, $I$ is the intensity measured with a sample in the beam, and $I_o$ is the intensity measured from the background spectrum. The absorbance spectrum can be calculated from the transmittance spectrum using the following equation.

$$A = -\log_{10} T, \quad (2.9)$$

where $A$ is the absorbance.

2.3 Electrical Characterization of MOS Devices

In this section, electrical characterization methods for MOS capacitors and MOSFETs, such as estimation of interface trap states by conductance method, effective mobility extraction by drain current measurement and split C-V method are described.

1) Trap states estimation by conductance technique

In this study, conductance method is used to estimate interface trap state density ($D_{it}$). Conductance method is an approach which we replace the measurement circuit of MOS capacitor with equivalent circuit models and calculate $D_{it}$. Figure 2.14(a) shows an equivalent circuit model of MOS capacitor [18], where $C_{ox}$ is the oxide capacitance per
unit area, $C_s$ is the silicon capacitance per unit area, $R_{it}$ and $C_{it}$ are the resistance and capacitance components per unit area related to interface trap, and $G_{it}$ is tunnel conductance per unit area related to leakage current. On the other hand, the measurement circuit is shown in Figure 2.14(b), where $C_m$ and $G_m$ are the measured capacitance and conductance per unit area. And the equivalent parallel circuit is shown in Figure 2.14(c), where $C_p$ and $G_p$ are the equivalent parallel capacitance and conductance per unit area. The reason why it is changed like that can be expressed that $G_p$ has only interface trap information not including $C_s$ when the circuit is converted. $C_p$ and $G_p$ are given by

$$C_p = C_s + \frac{qD_{it}}{1 + (\omega \tau_{it})^2}, \quad (2.10)$$

$$\frac{G_p}{\omega} = \frac{q\omega \tau_{it} D_{it}}{1 + (\omega \tau_{it})^2}, \quad (2.11)$$

where $C_{it} = qD_{it}$, and $\tau_{it} = C_{it}R_{it}$. $D_{it}$ is interface state density and $\tau_{it}$ is interface trap time constant here. These two equations are for interface traps with a single energy level in the band gap.

On the other hand, the capacitance and conductance are measured from the circuit in
Figure 2.14(b). By using equivalent circuit in Figure 2.14(c) $G_p/\omega$ can be calculated as:

\[
\frac{G_p}{\omega} = \frac{\omega(G_m - G_t)C_{OX}^2}{(G_m - G_t)^2 + \omega^2(C_{OX} - C_m)^2}. \tag{2.12}
\]

By considering the fluctuation of surface potential due to the inhomogeneities in oxide charge and interface charge [19], and by assuming that the surface potential fluctuation follows normal distribution, thus eq. (2.11) becomes

\[
\frac{G_p}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\sqrt{\omega \tau_{it}}} \ln \left[ 1 + (\omega \tau_{it})^2 \right] P(\psi_S) d\psi_S, \tag{2.13}
\]

\[
P(\psi_S) = \frac{1}{\sqrt{2\pi\sigma^2}} \exp \left( - \frac{(\psi_S - \bar{\psi}_S)^2}{2\sigma^2} \right). \tag{2.14}
\]
2) Threshold voltage and subthreshold slope determination

The threshold voltage \((V_{th})\) is one of the most important characteristics of a MOSFET because it determines the switching characteristic of the device. \(V_{th}\) is defined as the gate voltage necessary to form an inversion layer in the channel region. A common measurement technique for determining \(V_{th}\) is the linear extrapolation method with the drain current \((I_d)\) measured as a function of gate voltage \((V_g)\). Drain voltage \((V_d)\) in this case is typically 50 -100 mV [18]. Due to the deviation of the \(I_d\) curve from a straight line at the \(V_g\) below \(V_{th}\), generally the maximum slop of the \(I_d-V_g\) curve determined by the maximum point in the trans-conductance curve. As shown in Figure 2.15, \(V_{th}\) can be determined from the intersection point of the vertical line with the \(I_d-V_g\) curve and extrapolating \(I_d-V_g\) curve linearly to \(I_d = 0\).

![Image of the graph showing the determination of threshold voltage by the linear extrapolation technique](image)

*Figure 2.15 Determination of threshold voltage by the linear extrapolation technique.*
The maximum slope of $I_d-V_g$ curve is usually expressed as the Subthreshold Slope (S.S) as shown in Figure 2.16. S.S is a parameter that shows the gate control over channel. In the experiment, the S.S is defined as the gate voltage required for decreasing the drain current by one decade, and is given by

$$S.S = \left( \frac{d(\log_{10} I_d)}{dV_g} \right)^{-1} = 2.3 \frac{kT}{q} \left( 1 + \frac{C_{dm}}{C_{ox}} \right),$$

(2.15)

where $k$ is the Boltzmann’s constant, $T$ is absolute temperature of the system, $q$ is the electronic charge, $C_{dm}$ is depletion-layer capacitance. If the density of interface trap states is high, the subthreshold slope may be degraded due to the interface trap capacitance which is in parallel with the depletion-layer capacitance [20, 21].

*Figure 2.16* $I_d-V_g$ characteristics in logarithmic scale for typical MOSFETs.
3) Effective mobility measurement by split C-V method

The effective mobility ($\mu_{\text{eff}}$) of carriers in the inversion layer of MOSFETs is an important parameter for device analysis, characteristics and design.

$\mu_{\text{eff}}$ is defined by the measured $I_d$, and the inversion layer charge density ($Q_{\text{inv}}$) at a low $V_d$ in the linear region as [22]:

$$\mu_{\text{eff}} = \frac{L}{W} \cdot \frac{I_d}{V_d} \cdot \frac{1}{Q_{\text{inv}}(V_g)} = \frac{L}{W} \cdot g_d(V_g) \cdot \frac{1}{Q_{\text{inv}}(V_g)}, \quad (2.16)$$

where $g_d(V_g) = I_d(V_g)/V_d$ is the channel conductance. To obtain an accurate value of the $\mu_{\text{eff}}$, it is necessary to determine accurate values for $g_d$ and $Q_{\text{inv}}$ in eq. (2.16). Figure 2.17 shows $g_d-V_g$ and $I_d-V_g$ characteristics of the fabricated La$_2$O$_3$ gate dielectric MOSFETs.
with PMA at 800 °C in F.G for 30 min.

\[ g_d = \frac{\partial I_D}{\partial V_D} \bigg|_{V_g = \text{const}}. \]  \hspace{1cm} (2.17)

The split C-V measurement technique is well known for accurate measurement of the carrier charge density in the channel. In the split C-V measurement, the capacitance measured between the gate and the channel and between the gate and the substrate as illustrated in Figure 2.18 [20]. The characteristics of gate-to-channel capacitance \( C_{gc} \) and gate-to-body capacitance \( C_{gb} \) are illustrated in Figure 2.19. In order to avoid the error from the non-linear dependency of the inversion layer charge density on the gate voltage above the threshold voltage [23], a direct evaluation of inversion charge density by integrating \( C_{gc} \) is applied [24]. Therefore, \( Q_{\text{inv}} \) can be written as:

\[
Q_{\text{inv}} = \int_{V_{th}}^{V} C_{gc}(V_g) dV_g.
\]  \hspace{1cm} (2.18)

Similarly, as shown in Figure 2.19 (b), the depletion layer charge \( Q_b \) is also obtained by integrating \( C_{gb} \) from \( V_{FB} \) towards the inversion condition.
Figure 2.18 Schematic configurations for (a) gate-to-channel and (b) gate-to-body capacitances measurements for nMOSFETs [20].

![Schematic configurations](image)

Figure 2.19 Characteristics for (a) gate-to-channel and (b) gate-to-body capacitances for nMOSFET.

\[ Q_b = \int_{V_{FB}}^{V_G} C_{gb}(V_G) dV_G. \]  

(2.19)

Then, the effective electric field \( E_{eff} \) can be expressed as [25]:

53
\[ E_{\text{eff}} = \frac{1}{\varepsilon_{\text{Si}}} (\eta Q_{\text{inv}} + Q_{b}) , \]  

(2.20)

where \( \eta \) are 1/2 for electrons and 1/3 for holes.

### 2.4 Summary

In this chapter, fabrication processes for MOS capacitors and MOSFETs are briefly illustrated. Measurement techniques of Ellipsometry and FTIR for physical characterization of gate dielectric layer, and the extraction methods of interface state density and effective electron mobility for the electrical characterization of fabricated MOS devices are briefly introduced.
References


[2] Nishioka K, Reactive ion etching of Si and SiO$_2$,


409(1986).


Chapter 3 Interfacial Silicate Layer Formation

One of the advantages of the La\textsubscript{2}O\textsubscript{3} gate dielectrics is that a direct high-k contact with Si-substrate can be realized by forming a La-silicate Interfacial Layer (IL) at the La\textsubscript{2}O\textsubscript{3}/Si-substrate interface. In this chapter, characterization of the La-silicate IL and effect of annealing temperature on the La-silicate IL formation are described.

3.1 Introduction

For MOS devices with EOT less than 0.7 nm, a direct high-k dielectrics contact with Si-substrate is necessary. La\textsubscript{2}O\textsubscript{3} based dielectrics have been widely studied for gate insulator application [1-7], and recently, Kakushima et al. realized direct La\textsubscript{2}O\textsubscript{3}/Si-substrate contact structure by forming La-silicate IL, which has a relatively high dielectric constant [8]. Formation of La-silicate IL instead of SiO\textsubscript{x} at the La\textsubscript{2}O\textsubscript{3}/Si-substrate interface during the thermal annealing process without employing any complex fabrication process makes this material an attractive choice from the fabrication point of view. In the following sections, formation mechanism of the silicate IL and the effect of thermal annealing on the IL formation are analyzed.
3.2 Kinetics of Silicate Reaction

In this section, kinetics of the silicate reaction is described. La-silicate IL is formed by increasing the PMA temperature, and the thickness of the layer is modeled by activation energy in eq. (3.1) as [8]:

\[
    t_{silicate} = C_o \exp \left( -\frac{E_a}{kT} \right),
\]

where \( C_o \) is the concentration of radical oxygen atoms at the La\(_2\)O\(_3\)/La-silicate interface.

Figure 3.1 shows the extracted EOTs and the estimated thickness of the interfacial La-silicate layer versus the annealing temperature. The activation energy of silicate formation \( E_a \) is 0.115 eV and dielectric constants of La\(_2\)O\(_3\) and La-silicate layers are assumed to be 23 and 7, respectively.

Silicate reaction is promoted by the presence of the radical oxygen atoms at the surface of Si-substrate. Diffusion of oxygen atoms through gate oxide causes the reaction of silicate formation [8]. Two factors for limiting the reaction rate can be considered: (1) preventing the oxygen supply from the metal gate electrode, and (2) deactivation of oxygen atoms in the silicate layer. Since the PMA time is 30 min for all the samples, the oxygen atoms contained in W gate seem not to be a limiting factor for
EOT increment by the PMA temperature. Therefore, the deactivations of radical oxygen atoms play important role in the silicate reaction mechanism.

Concentration of radical oxygen atoms in the La$_2$O$_3$ gate stack can be expressed by mass transfer equation as [9]:

$$C(z) = C_0 \exp\left(-\frac{z}{\sqrt{D\tau}}\right).$$ (3.2)

Where $D$ and $\tau$ are diffusion constant and the life time of the radical oxygen atoms due to the effect of deactivation in the silicate layer. $C_0$ is the concentration of radical oxygen atoms at the W/La$_2$O$_3$ interface as shown in Figure 3.2.
In eq. (3.2) the term $\tau_D$ can be considered as a characteristic length of radical oxygen atoms from La$_2$O$_3$/La-silicate interface, and it is proportional to the ionic conductivity $\sigma$ of the La-silicate layer. $\sigma$ can be expressed in terms of the activation energy $E_a$ and the temperature $T$ as:

$$\sigma(T) = \sigma_0 \exp\left(-\frac{E_a}{kT}\right)$$

where $\sigma_0$ is the pre-exponential factor and $k$ is the Boltzmann constant.

**Figure 3.2** Schematic illustration of concentration of oxygen atoms in the gate oxide [10].

**Figure 3.3** Arrhenius plot of the formed silicate layer thickness and annealing temperature [8].
energy $E_a$ for La-silicate formation and pre-exponential factor $\sigma_0(r)$. The activation energy can be determined by Arrhenius plot of the formed La-silicate layer. Figure 3.3 shows the thickness of silicate layers in samples annealed at 300 and 500 °C, where the thicknesses are extracted from TEM [8]. The activation energy for La-silicate formation is the slope of the $t_{\text{sili}}/T$ line.

### 3.3 FTIR Spectroscopy Analyze for La-silicate Formation

Previous researches by XPS [11], Rutherford backscattering [12] and TEM equipped with electron energy-loss spectroscopy [13] have investigated the atomic distribution of silicon within the formed La-silicate layer. The results of these works show that there is a gradual compositional change of La-silicate in the direction normal to the Si-substrate. XPS study of O 1s core level has revealed the existence of La-O-Si bonding, with a binding energy (BE) located in between that of La-O-La and Si-O-Si bonding [5, 14 and 15]. Generally, La-silicate takes the form of an amorphous structure within the temperature range of semiconductor fabrication process (~1000 °C) [16]. However it is possible for La-silicate layer to have a crystalline structure in the form of $\text{La}_2\text{SiO}_5$ which has a tetrahedron SiO$_4$ network [17]. The SiO$_4$ network is connected through Si-O bonds, where the oxygen atoms are called bridging oxygen (BO). When La atom is
diffused into the silicate layer, La atom breaks the Si-O bond and forms a La-O bond; in this case the oxygen atom is called non-bridging oxygen (NBO). Due to the differences in electro-negativity and binding energy, an increase in the amount of NBO decreases the amount of BO [18, 19]. It is reported that the decrease in binding energy is the reason for gradual compositional change of silicate structure [20].

![FTIR absorption spectroscopy of samples annealed at temperatures of 200 to 800 °C and also as-deposited for W/La$_2$O$_3$ structure.](image)

**Figure 3.4** FTIR absorption spectroscopy of samples annealed at temperatures of 200 to 800 °C and also as-deposited for W/La$_2$O$_3$ structure.

FTIR spectroscopy can provide information about vibration modes of the bonding states in the dielectric layer. Figure 3.4 shows the absorption intensity of the photoelectrons in the samples annealed at various temperatures. Two absorption peaks, one for longitudinal optical (LO) phonon, and the other for transverse optical (TO)
phonon, are observed. The absorption peaks gradually shift to the low frequency as the annealing temperature increases. For annealing temperatures higher than 600 °C, the vibration frequency of the LO remains constant at around 1248 cm$^{-1}$. This is a typical value for Si-O bonds in tetrahedral SiO$_4$ network. Therefore, the LO phonon vibration mode corresponds to the Si-O asymmetric stretch of SiO$_4$ network.

![Figure 3.5](image_url)  
*Figure 3.5 Annealing temperature dependency of absorption peaks in FTIR spectra.*

Figure 3.5 shows the dependency of absorption peak values on the annealing temperature in FTIR spectra. The peak position is stationary at a value around 1248 cm$^{-1}$ for annealing temperatures higher than 600 °C. This result indicates that the stretch of the SiO$_4$ network is relaxed by high temperature annealing (600 °C or higher).
3.4 Characterization of La-silicates

In this section, the results of characterization of La-silicates by XPS spectra are described.

1) Sample preparation

High-k thin films were deposited by e-beam evaporation in an ultrahigh vacuum chamber at a base pressure of $10^{-7}$ Pa from high-k oxide pressed targets. Substrates used in this study were $n$-type Si (1 0 0) wafers with a doping density of $3 \times 10^{15}$ cm$^{-3}$. Substrates were chemically cleaned and dipped in an HF solution prior to the oxide deposition. The substrate temperature was 300 $^\circ$C and the deposition rate was 0.2 nm/min. In order to avoid any moisture absorption from air, SiO$_2$ film was capped on top of the high-k surface.

XPS analysis is carried out for the samples with the structure of SiO$_2$/La$_2$O$_3$/Si and annealed in F.G ambient at 300 $^\circ$C, 500 $^\circ$C and 700 $^\circ$C. The XPS measurement was carried out at SPring-8 with BL46XU using an X-ray light source of 7940 eV at a take-off angle (TOA) of 85$^\circ$ [22].

Grazing incident X-ray diffraction (GI-XRD) study was carried out by Grazing X-ray spectrometer for two kinds of samples: a single layer of La$_2$O$_3$(4 nm), HfO$_2$(4 nm); and a double layers of La$_2$O$_3$(3 nm)/HfO$_2$(1 nm), La$_2$O$_3$(2 nm)/HfO$_2$(2 nm), and
HfO$_2$(2 nm)/Sc(2 nm). All these samples were annealed in F.G ambient at 500 °C for 30 min. The wavelength of the incident ray is converted into wavelength of 1.54 Å of Cu-K$\alpha$.

2) La-silicate characterization by XPS

O 1s spectra obtained from as deposited and annealed samples are shown in Figure 3.6. La-silicate IL with two different compositions was formed at the interface of La$_2$O$_3$/Si. The estimated band gaps of these La-silicate ILs are around 5.8 and 6 eV, respectively. Expression (3.3) shows the possible silicate structures by reaction of oxygen atoms with La$_2$O$_3$ dielectrics and Si-substrate.

\[
\text{La}_2\text{O}_3 + \text{Si} + \text{O}_2 \rightarrow \text{La}_2\text{SiO}_5, \text{La}_{0.33}\text{Si}_6\text{O}_{26}, \text{La}_2\text{Si}_2\text{O}_7, \ldots \quad (3.3)
\]

Densities of the La$_2$O$_3$ layer and La-silicate IL were extracted from GI-XRD spectra. Figure 3.7 shows the detected intensities of GI-XRD versus incident angles of incident X-rays. The measured data were fitted by least squares method, and the extracted values of densities for each layer are shown in table 3.1. A value of 5.43 g/cm$^3$ was obtained for density of La-silicate IL.
Figure 3.6 O 1s spectra for samples of as deposited and annealed at 300–900 °C for SiO₂/La₂O₃/nSi structure.

Figure 3.7 Trend of reflective X-ray intensity versus irradiating angle by GI-XRD
Table 3.1 Densities and thickness of each layer in SiO$_2$/La$_2$O$_3$/La-silicate/Si sample by XRD method

<table>
<thead>
<tr>
<th>Material</th>
<th>Density [g/cm$^3$]</th>
<th>Thickness [nm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$</td>
<td>1.92</td>
<td>17.8</td>
</tr>
<tr>
<td>La$_2$O$_3$</td>
<td>6.57</td>
<td>3.78</td>
</tr>
<tr>
<td>La-silicate</td>
<td>5.43</td>
<td>1.33</td>
</tr>
<tr>
<td>Si</td>
<td>2.33</td>
<td>0.00</td>
</tr>
</tbody>
</table>

Figure 3.8 Grazed incident XRD spectra for La$_2$O$_3$ and HfO$_2$ gate stacked layers after thermal annealing at 500°C in F.G ambient.

Figure 3.8 shows GI-XRD spectra for La$_2$O$_3$ and HfO$_2$ gate stacked layers after thermal annealing at 500°C in F.G ambient for 30 min. Distinct crystallization peaks were observed at $\theta = 25.8^\circ$ and $\theta = 29.6^\circ$ for the single layers of both La$_2$O$_3$(4 nm) and HfO$_2$(4 nm), respectively. These spectra suggest the presence of hexagonal and monoclinic crystal phases for La$_2$O$_3$ and HfO$_2$ dielectrics [23]. For La$_2$O$_3$(3 nm)/HfO$_2$(1 nm), La$_2$O$_3$(2 nm)/HfO$_2$(2 nm), HfO$_2$(2 nm)/Sc(2 nm) structures, the crystallization peaks are notably suppressed. These results indicate that fabricating
high-k films composed of more than one rare earth element, is an effective method to prevent crystallization of the high-k dielectrics due to thermal treatment.

3.5 Advantage of La$_2$O$_3$ Gate Dielectrics over CeO$_x$

In this section, interface reactions of a Ce-oxide layer with Si (1 0 0) wafers are studied by XPS analyses.

1) Sample preparation

Two kinds of samples were fabricated; 1: samples with 2- or 3-nm-thick Ce oxide layers on Si-substrates, 2: a capacitor structure with a W layer on top of a 3-nm-thick Ce oxide layer. The former set of samples is used to extract the photoelectron spectra of Ce atoms from Ce-silicate and also to characterize the band alignment with respect to Si-substrates. To promote the Ce oxides reaction with Si-substrates, high temperature annealing at 900 °C for 2 sec was performed. For the MOS structure sample, 8-nm-thick W layer was deposited by sputtering. The metal layers were deposited on the Ce oxide layer without breaking the vacuum to avoid any contamination and water absorption from the air. The capacitors were then annealed at 500 °C for 30 min in F.G ambient. XPS measurement was carried out at SPring-8 with BL46XU using an X-ray source of 7940 eV at a TOA of 85° [22]. As the inelastic mean free paths (IMFP) of the
photoelectrons in the W metal arising from Ce 3d_{5/2} and Si 1s core levels are 6.9 and 6.4 nm respectively [24], the chemical bonding states can be probed through the 8-nm-thick W layer [25].

2) Band alignment of cerium silicate on Si (1 0 0)

Ce 3d_{5/2} and Si 1s spectra obtained from 2- and 3-nm-thick Ce oxide samples, which were annealed at 900 °C are shown in Figure 3.9. Both spectra were normalized by the intensity of the photoelectrons arising from the un-oxidized Si-substrate component in the Si 1s spectra. The Ce 3d_{5/2} spectra showed no change in the shape except for the intensity with the ratio of 1 to 1.3, which indicates that the Ce atoms are in the same bonding states for the two samples. On the other hand, the photoelectrons arising from the oxidized Si atoms in the Si 1s spectra revealed three oxide components with
different bonding states; a sub-oxide (Si\(^{1+}\)) component with a peak intensity at an energy of 1841.8 eV, a Ce-silicate signal at 1842.7 eV and an SiO\(_2\) bonding at 1844.0 eV [26].

As the photoelectron intensity of Si\(^{1+}\) and SiO\(_2\) spectra showed no difference between the two samples, these bondings should locate at the interface between the Ce-silicate and the Si-substrate with the same amount. The formation of a thin SiO\(_2\) layer by a Ce-oxide layer is in contact with Si-substrate is in a good agreement with previous report [27]. As the photoelectron intensity ratio of the Ce-silicate components in Si 1s spectra between the samples was 1 to 1.3, one can conclude that the reactively formed Ce-contained layers are compositionally uniform Ce-silicates.

The loss spectra in the O 1s core level and the valence band (VB) spectra with respect to the Si-substrate Fermi level (\(E_F\)) are shown in Figure 3.10. Two peaks observed in the

**Figure 3.10** (a) O 1s and (b) VB spectra of Ce-silicates on Si (1 0 0).
O 1s spectra indicate the formation of Ce-silicate and SiO2 interfacial layer. The difference in the O 1s spectra of the 2- and 3-nm-thick samples by subtraction showed a single spectrum with peak energy of 530.83 eV, suggesting that the thickness of the SiO2 layers were the same, which is in good agreement with the Si 1s spectra. The photoelectrons obtained around 3.5 eV below the $E_F$ can be assigned as the Ce 4f\(^{1}\) initial state, which is fully localized within the bandgap [28, 29]. Moreover, two peaks observed at energies of 6.7 and 9.0 eV below the $E_F$ are the O 2p arising from the interfacial SiO2 layer. Therefore, further subtracting the VB spectrum of SiO2, a VB offset of 4.35 eV at Si-substrate and Ce-silicate layer can be determined [30]. Finally, the conduction band (CB) offset of Ce-silicate and Si-substrate can be calculated as 2.20 eV.

3) Valence number transition in W/CeO\(_x\) MOS capacitors by annealing

To observe the valence number transition of the Ce atoms in the Ce oxides before and after the PMA, Ce 3d\(_{5/2}\) and Si 1s spectra were measured from Ce oxide capacitors with W gate electrodes. Figure 3.11 shows the Ce 3d\(_{5/2}\) spectra of as-deposited state and after annealing at 500 °C for 30 min. Compound spectra indicate the presence of Ce\(^{3+}\) and Ce\(^{4+}\) as well as Ce-silicate components in the oxide film [31].

Using the first set of samples as a reference spectrum of Ce-silicate component, each
component of Ce$^{3+}$ and Ce$^{4+}$ can be extracted from the two Ce 3$d_{5/2}$ spectra by constructing linear equations. By comparing the photoelectron intensities in each spectrum, 47 and 19 % of the Ce atoms were in Ce$^{3+}$ and Ce$^{4+}$ states, respectively, and 34 % of the Ce atoms were in the silicate state at as-deposited sample. Upon annealing, the portion of Ce$^{4+}$ and silicate increased up to 26 and 48 %, respectively, and the Ce$^{3+}$ was found to decrease down to 26 %. CeO$_2$ is known to promote oxidation of Si-substrates by reducing the state from Ce$^{4+}$ to Ce$^{3+}$, producing Ce$_2$O$_3$ in the oxide and SiO$_2$ layer at the Si-substrate interface [32]. By further supplying of oxygen atoms from environment to react with the SiO$_2$ layer, the reaction advances to oxidize the Ce$^{3+}$ to Ce$^{4+}$ and leaving Ce-silicates at the Ce-oxide/SiO$_2$ interface. The source of oxygen, which triggers the reaction, is originated from the sputter-deposited W gate electrode, which is a metal known to contain oxygen atoms [8].

The growth of Ce-silicate layer is also confirmed from Si 1$s$ spectra, as shown in Figure 3.12 (a), where the photoelectron intensity of the silicate component increased by 2.4 times. The discrepancy in the increased ratio of silicates observed in Ce 3$d_{5/2}$ and Si 1$s$ spectra can be understood from the formation of Si-rich phase, which including Ce$_2$Si$_2$O$_7$ phase, after annealing. By subtracting the two Si 1$s$ spectra, formation of SiO$_2$ layer is observed during PMA annealing. Assuming a density of 5.78 g/cm$^3$ (PDF
48-1588) [33] and IMFP of 10.1 nm for Si-rich Ce-silicate, the thickness of the silicate can be calculated as 1.3 nm after annealing, which fairly matches with a thickness of 1.4 nm observed from TEM image, as shown in Figure 3.12 (b). In the same way, the thickness of SiO$_2$ layers can be calculated to increase from 0.44 to 0.96 nm after annealing, which is also observed in the TEM image.

Promotion of Si oxidation under the presence of Ce and O atoms is known to take place owing to two reactions; oxidation of Ce$^{3+}$ to Ce$^{4+}$ and reduction of Ce$^{4+}$ to Ce$^{3+}$ states [32]. The valence number transitions of oxidation of Ce atoms can be expressed as:

$$
\text{Ce}^{3+} + m\text{Si} + n\text{O} \rightarrow (\text{Ce}^{4+}) \rightarrow x\text{Ce}_{\text{silicate}}^{3+} + (1-x)\text{Ce}^{4+},
$$

Figure 3.11 Measured and deconvoluted Ce 3d$_{5/2}$ spectra obtained from capacitor structure: (a) before and (b) after annealing.
where $m$ and $n_1$ is the number of Si and O atoms required for reaction and $x$ is the ratio of Ce$^{3+}$ atoms that is converted into silicate ($0 < x < 1$), so that the ratio of Ce atoms in Ce$^{4+}$ state is $(1-x)$. At the same time, a part of the Ce atoms in Ce$^{4+}$ states are reduced to Ce$^{3+}$ states by oxidizing Si atoms to form SiO$_2$ as:

$$\text{Ce}^{4+} + y\text{Si} + n_2\text{O} \rightarrow y\text{Ce}^{3+} + (1-y)\text{Ce}^{4+} + y\text{SiO}_2, \tag{3.5}$$

where $y$ is the ratio of Ce$^{3+}$ atoms that is reduced back from Ce$^{4+}$ state and to form SiO$_2$ at interface, and $n_2$ is number of oxygen atoms required to proceed the reaction. The created Ce atoms in Ce$^{3+}$ state again follow the first reaction until the thermal equilibrium is reached. By combining the two reactions, we can obtain the following
reaction as:

\[
\text{Ce}^{3+} + \frac{m + (1-x)y}{1-(1-x)y} \text{Si} + \frac{n_{1} + (1-x)_{1}n_{2}}{1-(1-x)y} \text{O} \rightarrow \frac{x}{1-(1-x)y} \text{Ce}_{\text{silicate}}^{3+} + \frac{(1-x)(1-y)}{1-(1-x)y} \text{Ce}^{4+} \\
+ \frac{(1-x)y}{1-(1-x)y} \text{SiO}_2.
\]  

(3.6)

The Ce 3d\text{5/2} spectra indicated that the reacted Ce atoms in Ce\text{3+} states were converted into Ce- silicates and Ce\text{4+} states with a ratio of 2 to 1, so that the following equation can be derived.

\[
\frac{x}{1-(1-x)y} = 2 \frac{(1-x)(1-y)}{1-(1-x)y}.
\]  

(3.7)

On the other hand, assuming that newly created SiO\text{2} layer after annealing is grown only by the reduction of Ce atoms, another equation can be derived from the ratio of increased photoelectrons in Si 1s spectra, shown in Figure 3.12 (a), as:

\[
1.4 \frac{x}{1-(1-x)y} = \frac{(1-x)y}{1-(1-x)y}.
\]  

(3.8)

Solving the two equations, we can obtain \( x = 0.34 \) and \( y = 0.74 \).
4) **Advantage of La$_2$O$_3$ over CeO$_x$**

XPS analyses show that Ce-silicate and SiO$_2$ layers are formed at Si (1 0 0) interface with CeO$_x$ gate dielectric during PMA. Valance number transition analysis in CeO$_x$ show that oxidation of Si atoms is stronger than the formation of silicate. La$_2$O$_3$ gate oxide on the other hand, promotes silicate formation rather than SiO$_2$ at the interface.

### 3.6 Summary

In this chapter, the effect of the PMA on La-silicate IL is described. The EOT increment with annealing temperature is caused by La-silicate IL formation due to the chemical reaction of La, Si and O atoms at the La$_2$O$_3$/Si-substrate interface. Fourier Transform Infrared Spectroscopy results indicate that high temperature annealing is required to relax the stretch of SiO$_4$ network of the La-silicate layer and thus preventing crystallization of the high-k film. Wide band gap value of ~6 eV and physical density value of 5.43 g/cm$^3$ was obtained for La-silicate layer based on GI-XRD analysis. XPS spectra results for CeO$_x$ show SiO$_2$ interfacial layer formation at Ce-oxide/Si-substrate interface due to valance number transition.
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Chapter 4 Evaluation of Interface and Oxide Trap States in 

La$_2$O$_3$/La-Silicate Capacitors

In this chapter, origin of the trap states in La$_2$O$_3$ gate stacks is studied. A novel interpretation of observed two peaks in the conductance spectra of La$_2$O$_3$/La-silicate capacitors has been proposed.

4.1 Introduction

Formation of the La-silicate IL with higher dielectric constants (8–14) instead of SiO$_2$ IL is one of the advantages of using La$_2$O$_3$ as a gate dielectrics for further downscaled MOS devices [1, 2]. However, previous works show that $D_{it}$ at the interface of La-silicate/Si-substrate is still in the order of $10^{12}$ cm$^{-2}$/eV and sensitive to the annealing temperature [3]. This is due to high number of defects in La$_2$O$_3$ dielectric and also the chemical reaction between La$_2$O$_3$ and Si-substrate. Therefore, it is necessary to reduce the interface trap state densities in the La$_2$O$_3$/Si MOS devices. Another typical feature of La$_2$O$_3$ gate stacked MOS capacitors is that their $C$-$V$ spectra show frequency-dependent humps near the flat-band condition as shown in Figure 4.1. It is also important to
identify the physical origin of the traps responsible for this behavior. This would help with improving the La$_2$O$_3$/Si-substrate interfacial properties.

4.2 Conductance Spectra of La$_2$O$_3$ Gated MOS Capacitors

Figure 4.2 shows the measured conductance spectrum as a function of the voltage frequency for both La$_2$O$_3$ and SiO$_2$ MOS capacitors. The measured conductance spectrum in depletion condition for SiO$_2$-based capacitor shows only a single peak in the high frequency region. However, two distinct peaks are observed in the conductance spectrum of La$_2$O$_3$-based capacitor at the frequency region of 100 Hz ~ 2 MHz. The conductance-frequency peaks in the low frequency region are nearly an order of magnitude lower for La$_2$O$_3$ than for SiO$_2$.

Figure 4.1 Capacitance versus gate bias for a sample annealed at 600°C. The dots correspond to the measured capacitances for the frequency range from 1 kHz to 1 MHz, and the solid line corresponds to the ideal curve of SiO$_2$.
magnitude higher than the conductance-frequency peaks in the high frequency region. Moreover, the conductance peaks at the low frequency region are less dependent on the electron energy, whereas the conductance peaks at high frequency region change with the electron energy.

Figure 4.2 $G_p/\omega$ as a function of frequency. The left y-axis is for La$_2$O$_3$ gate stack capacitor, which is annealed at 600°C. The solid lines correspond to the fitting curves by our modified model with the fitting parameters of $\tau_{c1} \sim 10^{-3}$s, $\tau_{c2} \sim 10^{-7}$s, $\sigma \sim 10^{-4}$. The right y-axis is for SiO$_2$ capacitor. The conductance data for both La$_2$O$_3$ and SiO$_2$ sample correspond to the $\psi_c = -0.11$eV. All data are taken by the measured voltage amplitude of 100 mV.

Figure 4.3 shows the trap time constants estimated from these conductance peaks. The conductance-frequency peaks in the high frequency region (100 kHz ~ 2 MHz), show a shorter trap time constant for the capture and emission process, and their value vary
significantly with the surface potential. On the other hand, the conductance-frequency peaks in the low frequency region (100 Hz ~ 10 kHz), show a longer trap time constant for the capture and emission process, and vary marginally in their values with the surface potential. Conductance-frequency peaks in the high frequency region can be considered to be caused by interface trap states. This means that the trap centers are located at/or near the oxide/Si interface. The conductance-frequency peaks in the low frequency region are assumed to be caused by trap states other than interface traps. We have assigned the low frequency conductance peaks to slow traps, meaning the electron capturing time is slower than the electron capturing time for the typical interface trap.

**Figure 4.3** Interface trap time constant ($\tau_{it}$) and slow trap time constant ($\tau_{slow}$) versus electron energy; the closed dots represent $\tau_{it}$ and the closed triangles represent $\tau_{slow}$. 
states. In the following sections, we attempt to clarify the origins of these slow traps in the La$_2$O$_3$ gate dielectric MOS capacitors.

### 4.3 A Proposed Method for La$_2$O$_3$/Si Trap States Characterization

Generally, $G_{p, it}$ for interface traps with continuum energy level in the band gap can be expressed by $D_{it}$ and time constant ($\tau_{it}$) by a statistical Gaussian model based on surface potential fluctuation as eq.(4.1) and (4.2).

\[
\frac{G_{p, it}}{\omega} = \frac{q}{2} \int_{-\infty}^{\infty} \frac{D_{it}(\psi_s)}{\omega \tau_{it}(\psi_s)} \ln \left[ 1 + \left\{ \frac{\omega \tau_{it}(\psi_s)}{2} \right\}^2 \right] P(\psi_s) d\psi_s, \tag{4.1}
\]

\[
P(\psi_s) = \frac{1}{\sqrt{2\pi}\sigma^2} \exp \left\{ - \frac{(\psi_s - \overline{\psi})^2}{2\sigma^2} \right\}, \tag{4.2}
\]

where $q$, $\omega$, $\overline{\psi}$, and $\sigma$ are the electronic charge, angular frequency, the normalized mean surface potential and standard deviation, respectively [4]. By setting proper values for $D_{it}$, $\tau_{it}$ and $\sigma$, the conductance spectrum shown in Figure 4.2 for SiO$_2$ and the fast traps with La$_2$O$_3$ capacitors can be reproduced as shown with solid line. Since $\tau_{it}$ and $\sigma$ showed little difference between two gate oxide materials, the basic mechanism for the
carrier trappings can be assumed identical. Therefore, we can conclude that the fast
traps which peak at a frequency of 800 kHz can be related to $D_{it}$ located at the
La-silicate/Si-substrate interface. The decreasing trend of $D_{it}$ towards Si mid-gap as
shown in Figure 4.3, is a typical feature of interface trap states in Si (1 0 0)-orientated
substrate.

![Figure 4.4](image)

*Figure 4.4 Energy distribution of the $D_{it}$ and $D_{slow}$ within the band gap of Si.*

On the other hand, the slow traps in the conductance spectrum ($G_{p,slow}$) have a single
time constant ($\tau_{slow}$) and a single trapping energy level, expressed in eq. (4.3)

$$G_{p,slow} = \frac{q \omega \tau_{slow} D_{slow}}{\omega} \frac{1}{1 + (\omega \tau_{slow})^2}. \quad (4.3)$$
Since $\tau_{\text{slow}}$ is larger than $\tau_{\text{it}}$, the physical origin of these slow traps can be considered either at deep energy levels within the bandgap of silicon or inside oxide layer. The former possibility can be eliminated since the capacitors are biased in depletion condition. Surface potential fluctuation in depletion condition should broaden the spectrum by convolution of Gaussian distribution expressed in eq. (4.2). Traps in oxide are known to behave like slow-states to generate low frequency ($1/f$) noise in SiO$_2$ case. M. J. Uren et al. reported that the traps in the oxide with a time constant of $\tau_{\text{ox}}$ and trap state density ($D_{\text{ox}}$) can be expressed as eq. (4.4)

$$\frac{G_{p,\text{ox}}}{\omega} = \frac{qD_{\text{ox}}}{2}\left\{\pi - 2\tan^{-1}(\omega\tau_{\text{ox}})\right\}.$$  \hspace{1cm} (4.4)

A plateau in the conductance spectra can be observed at low frequency region, typically below 100 kHz [5]. In a real device, traps are distributed both spatially and energetically in the oxide. This results in the broadening of the spectrum. Therefore, the observed slow traps here should be located at the same distance or distributed with a certain distance from Si-substrate. Indeed, the fact that the capture cross-section of the slow traps ($\sigma_{\text{slow}}$) show a strong dependency on the distance from the substrate, which can be explained by the tunneling probability for trapping, also supports our model. This will
be discussed in more detail in the next section.

The slow-state traps should be energetically distributed at a fixed level, since the amount of these traps is almost constant even considering the surface potential fluctuation. Here we propose that the physical origin of the traps can be considered to be at the interface of La$_2$O$_3$ and La-silicate layer. La$_2$O$_3$ is known to react with Si-substrate to form a La-silicate interfacial layer. The thickness of the La-silicate layer is dependent on the annealing process; oxygen partial pressure and temperature. The atomic bonding in La$_2$O$_3$ is known to be of ionic nature and in La-silicate layer more of a covalent nature. It is reported that at the boundary of two materials with ionic and covalent bonds, a large amount of oxygen vacancies are presented [6]. These vacancies can be

---

**Figure 4.5** Band diagram representing the proposed interpretation of the location of trap sites for La$_2$O$_3$ gated MOS capacitors.
eliminated by low-temperature oxidation. However, they can also be easily created by annealing in reducing ambient [7]. The localized traps at ionic-HfO$_2$ and covalent SiO$_2$ have been reported to be probed by charge-pumping measurement [8]. Therefore, it is plausible to consider the slow traps to be located at La$_2$O$_3$ and La-silicate interface. The proposed interpretation of the interface and slow traps is schematically illustrated in Figure 4.5.

4.4 Effect of Annealing Temperature on Trap States in La$_2$O$_3$ Gate Stacks

In this section, the dependency of $D_{it}$ and $D_{slow}$ on PMA temperature is investigated.

In Figure 4.6 (a), (b), and (c) show PMA temperature dependencies of the trap states, capture cross sections and the flat band voltage shifts due to the slow trap states, respectively. Both $D_{it}$ and $D_{slow}$ decrease with higher annealing temperature, in which a large decrease by two orders of magnitude is achieved with $D_{it}$, as shown in Figure 4.6 (a). On the other hand, only a slight decrease by half in $D_{slow}$ indicates that the traps located at La$_2$O$_3$ and La-silicate layer is hardly improved by annealing process. The capture cross-section of interface trap states ($\sigma_{it}$) and slow trap states $\sigma_{slow}$ dependencies on the annealing temperature are shown in Figure 4.6 (b). The decrease in $\sigma_{it}$ with annealing temperature up to 500 °C can be considered as the effect of hydrogen atom
passivation of dangling bonds at the Si substrate. $\sigma_{t}$ stays almost constant at annealing temperature over 600 °C. On the other hand, $\sigma_{\text{slow}}$ is showed continuous decrements with the annealing temperature. Based on our assignment that $D_{\text{slow}}$ is located at the interface between La$_2$O$_3$ and La-silicate layers, the $\sigma_{\text{slow}}$ should follow

$$\sigma_{\text{slow}} = \sigma_0 \exp\left(-\frac{t_{\text{silicate}}}{\lambda}\right),$$

(4.5)

where $\sigma_0$ and $\lambda$ are the capture cross-section pre-factor and attenuation wave function coefficient related to tunnel probability extracted from WKB approximation [9]. Therefore, the $\sigma_{\text{slow}}$ values on the annealing temperature can be obtained from eq. (3.1) and (4.5) as

$$\log_{10}(\sigma_{\text{slow}}) = \frac{1}{\ln 10} \left\{ \sigma_0 - \frac{1}{\lambda} \exp\left(-\frac{E_a}{kT}\right) \right\}. $$

(4.6)

The calculated $\sigma_{\text{slow}}$ in Figure 4.6 (b) with $\sigma_0$ and $\lambda$ of $7 \times 10^{-14}$ cm$^2$ and 0.8 nm, respectively, shows fairly nice agreement with the obtained data. This also supports our interpretation of the slow traps to be the traps located at La$_2$O$_3$ and La-silicate interface.
When the gate voltage is biased over $V_{FB}$ to accumulation region, conductance spectra cannot be obtained due to excess majority carriers [5]. However, the electron trapping into slow traps, still occurs while increasing the gate voltage. When the $C$-$V$ curves are fitted with ideal curves at the accumulation region, we see a discrepancy near $V_{FB}$, a stretch-out behavior. As most of the interface trap states are occupied by the electrons, the shift can be mainly considered as the contribution of the slow traps. Indeed, suppose

Figure 4.6 Dependencies of (a) $D_{it}$ and $D_{slow}$, (b) capture cross-sections, and (c) $\Delta V_{FB}$ on annealing temperature.

When the gate voltage is biased over $V_{FB}$ to accumulation region, conductance spectra cannot be obtained due to excess majority carriers [5]. However, the electron trapping into slow traps, still occurs while increasing the gate voltage. When the $C$-$V$ curves are fitted with ideal curves at the accumulation region, we see a discrepancy near $V_{FB}$, a stretch-out behavior. As most of the interface trap states are occupied by the electrons, the shift can be mainly considered as the contribution of the slow traps. Indeed, suppose
all the trappings beyond $V_{FB}$ to the accumulation region are to be due to slow traps with a constant $D_{slow}$, one can estimate the shift in the $V_{FB}$ from the ideal value by $t_{silicate}$. The shifts in the $V_{FB}$ ($\Delta V_{FB}$) at each annealing temperature with $D_{slow}$ of $2.8 \times 10^{13} \text{ cm}^{-2}$/eV are shown in Figure 4.6 (c). We can see that the $\Delta V_{FB}$ can be well reproduced with our model, which also supports our interpretation of slow traps. Also, it is worth to note that the energy distribution of $D_{slow}$ is still constant even at the energy range out of the bandgap of Si-substrate.

4.5 Summary

Conductance spectra of La$_2$O$_3$ dielectrics MOS capacitors were analyzed. Based on observed experimental results, a novel interpretation of the two peaks in the conductance spectra of La$_2$O$_3$/La-silicate gate dielectric capacitors has been proposed. The fast-state response is assigned to the interface trap state as is commonly observed with SiO$_2$ gate oxide. The slow-state response is assigned to trapping at the La$_2$O$_3$/La-silicate interface for the following reasons: (1) The spectra have shown a single-level trapping without statistical surface potential fluctuation; (2) Capture cross-sections of the traps can be modeled by tunneling probability with the thickness of silicate IL; (3) The trapped charges are in good agreement with the shift in the $V_{FB}$. 

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References


Chapter 5 Interfacial Properties and Effect of Annealing

In this chapter, the effect of Post Metallization Annealing (PMA) on the interfacial properties of La$_2$O$_3$ MOS capacitor is described. First, the effect of thermal treatment timing on the La-silicate IL formation is discussed. The difference between *in-situ* and *ex-situ* annealing approaches are compared by device characteristics. Finally, the effect of the annealing temperature on the La-silicate formation is discussed.

5.1 Introduction

Radical oxygen within La$_2$O$_3$ gate dielectric insulator, promotes La-silicate formation at the substrate interface. An excess amount of oxygen atoms results in the excess formation of the La-silicate IL. On the other hand, an insufficient oxygen supply can lead to formation of oxygen vacancies in La$_2$O$_3$ layer. These oxygen vacancies, which being as Coulomb scattering centers, lead to mobility degradation of carriers in the channel of MOSFETs [1]. Therefore, a careful annealing approach to maintain precise control over the oxygen supply without degrading the electrical characteristics of MOSFETs is required.
There are a number of works done to prevent EOT increment during the PMA process. Kawanago et al. proposed a method of capping a Si layer on the metal gate to prevent absorption of the oxygen atoms into the metal gate [2]. Meanwhile, Kitayama et al. proposed a thin Si layer insertion between metal gate and La$_2$O$_3$ dielectric layer [3]. In the latter case, by thermal annealing, an interfacial amorphous La-silicate layer is formed between metal gate W and La$_2$O$_3$ layer. This amorphous interfacial layer inhibits the diffusion of oxygen atoms through the dielectric grain boundaries and suppresses the formation of the La-silicate IL at the La$_2$O$_3$/Si-substrate interface. In the approach of Kawanago et al., extra steps are needed for patterning the gate electrode and source/drain area. In the approach of Kitayama et al., the inserted Si layer turns to La-silicate at the metal/La$_2$O$_3$ interface thus increasing the EOT of the gate stack. As shown in Figure 5.1, in our method, an *in-situ* annealing approach is used in order to

*Figure 5.1 Schematic diagram of preventing oxygen atoms diffusing into La$_2$O$_3$ gate dielectrics.*
avoid exposing devices to the air.

**5.2 The Effect of Air Exposure**

In this section, effect of delaying the PMA time on the EOT of the gate oxide insulator is discussed. Due to the absorption of oxygen atoms into the metal gate W [4], these atoms can diffuse into the gate oxide insulator during thermal treating process. The amount of the oxygen atoms in the metal gate affects the formation of the La-silicate IL and interfacial properties of the gate stack.

In order to observe the effect of oxygen on the formation of the La-silicate IL, samples were deliberately left in room temperature and pressure for a certain amount of time before carrying out PMA process. The delay time for PMA is defined as the time interval between deposition of gate metal and carrying out PMA. A delay time of few hours, one day, two days, one week, and three weeks was investigated. The rest of the fabrication flow was the same for all samples.

Figure 5.2 (a) and (b) show the dependence of measured capacitance and EOT on the delay time for PMA, respectively. The results show that both the capacitance and EOT decrease for longer delay times. The increment in EOT can be explained by contribution of the oxygen atoms absorbed in W metal gate layer [4, 5]. The solid line in the Figure
5.2 (b) is fitting curve. The linear trend of increment in EOT can be attributed to a linear dependency of the silicate thickness on the amount of oxygen concentration at the W/La2O3 interface [6].

These results indicate that it is preferable to avoid exposing devices to oxygen containing environments after gate metal deposition. By in-situ annealing approach, the thermal annealing process is applied without exposing the wafers to the air. Hence, in-situ annealing approach can effectively avoid EOT increment.

5.3 In-situ Post Metallization Annealing

In the previous section, it was shown that delaying the PMA timing contributes to the EOT increment. In this section, in-situ annealing approach for minimizing oxygen diffusion into W gate metal is described.

Figure 5.2 (a) measured capacitance variance with PMA delay time; (b) EOT variance with PMA delay time.
Figures 5.3 (a) and (b) show measured capacitance and EOT for the samples with in-situ and ex-situ PMA, respectively. For the MOS capacitors with similar La$_2$O$_3$ gate dielectric insulator and gate metal thickness, a smaller EOT value was obtained with in-situ annealing approach compared to ex-situ annealing approach. In Figure 5.3 (b), solid lines show the theoretical fitting lines. For samples with in-situ PMA, EOT increment is saturated when the initial deposition thickness is larger than 4.5 nm. This result indicates that La$_2$O$_3$ layer with a certain thicknesses remains in the gate stack and does not turn to La-silicate. This is due to lack of sufficient oxygen supply.

5.4 Annealing Temperature Effects on Interfacial Property

In the previous sections, it was shown that in-situ PMA is an effective method for suppressing EOT increase due to thermal treatment. In this section, we will discuss the
effect of PMA temperature on the interfacial properties of the MOS capacitors with W/La$_2$O$_3$/Si-substrate structure.

Figures 5.4 (a), (b), and (c) compare the C-V characteristics of three MOS capacitors with in-situ PMA treatment in various temperatures. For PMA temperature of 700 °C or lower, device C-V curves have frequency-dependent humps in flatband condition. These humps disappear by increasing the PMA temperature and the measured C-V approach ideal curve. These results indicate that high temperature PMA improves the interfacial properties of MOS capacitors with La$_2$O$_3$ gate dielectric insulator.

5.5 Summary

In this chapter, effects of PMA temperature on the electrical characteristics of MOS capacitors were described. It was found that in-situ PMA is an effective method in order
to suppress EOT increase due to thermal treatment. Suppressing the promotion of silicate reaction at La$_2$O$_3$/Si-substrate interface by preventing the absorption of oxygen atoms in the metal gate is considered to be the reason for this result. High temperature PMA of 800 °C or more was found to be important for improving the interfacial properties of La$_2$O$_3$ gate stacked MOS capacitors.
References


Chapter 6 Impact of Metal Gate on Interfacial Properties

In this chapter, the impact of metal gate on the interfacial properties of La$_2$O$_3$ gate stacked MOS capacitors is described. Effects of the physical thickness and material nature of the metal gate on the formation of La-silicate interfacial layer are discussed.

6.1 Introduction

For the high-k gate dielectric gate stacked MOS devices, performance improvement cannot be solved solely from the improvement of the properties of the high-k dielectric layer [1]. Impact of metal gate on the overall properties of the MOS device is also an important factor for improving the performance of MOS devices with metal gate/high-k structure. Several metal gate electrodes such as W/TiN, Mo, Ta, TaN, TiN and TaSi$_x$N$_y$ have been studied as a replacement for poly-Si gate. Metal gates must have a suitable work function, thermal and chemical stability with underlying gate dielectric insulator [2]. Tungsten (W) has been explored extensively as a gate metal for CMOS technology because of its low resistivity and near mid-gap work function [3-4]. However, for W metal gates with HfO$_2$ and ZrO$_2$ gate insulator, the increase in the EOT of gate dielectric
layer was observed due to the formation of interfacial SiO$_2$ layer during thermal annealing process [5-7]. For La$_2$O$_3$ gate dielectric insulators with W metal gate, the increment of EOT also observed due to the silicate IL formation at the interface of La$_2$O$_3$/Si-substrate [8]. In these works, the formation of the IL at the high-k/Si-substrate interface is believed due to the oxygen involvement in the oxidation of the interface of high-k/Si-substrate, and the W metal gate layer is considered the source of the oxygen. Observed results showed that oxygen atoms were absorbed in W metal layer during sputtering deposition process. The source of this oxygen was considered to be the impurities contained in Ar gas lines which were used during the deposition process. As discussed in chapter 5, in our experiments, exposing the devices to room temperature and pressure after gate deposition, was the main cause of oxygen absorption into W metal film. These oxygen atoms promote silicate reaction at the interface of La$_2$O$_3$/Si-substrate when PMA is conducted. The formation of the La-silicate IL at the La$_2$O$_3$/Si-substrate interface, effects the interfacial properties of the gate stack and also increases EOT of gate dielectric layer in MOS devices.

In the following sections, the effects of the physical thickness and material nature of metal gate are explored as a mean to control the amount of oxygen atoms within the gate stack. Figure 6.1 shows the schematic illustration of our approach.
6.2 Effect of Metal Gate Material on Interfacial Properties

In this section, the effect of metal gates with the medium work function, such as tungsten (W) and tantalum nitride (TaN), on the interfacial property of La$_2$O$_3$ MOS capacitors is described.

Figure 6.2 shows $C-V$ characteristics for TaN(45 nm), W(60 nm), and TaN(45 nm)/W(5 nm) metal gated La$_2$O$_3$ MOS capacitors with similar fabrication process. Sample with TaN metal gate shows a distinct hump in the $C-V$ characteristics, whereas no humps are observed in the $C-V$ characteristics of other samples. TaN gate electrodes contain less oxygen atoms compared to the W gate electrode. Low oxygen concentration of TaN gate electrode results in only a partial La-silicate transformation at
the $\text{La}_2\text{O}_3$/Si-sub interface while the regions close to the metal gate remain in the form of $\text{La}_2\text{O}_3$.

![C-V characteristics](image)

**Figure 6.2** C-V characteristics of (a) TaN/$\text{La}_2\text{O}_3$/Si, (b) W/$\text{La}_2\text{O}_3$/Si, and (c) TaN/W/$\text{La}_2\text{O}_3$/Si MOS capacitors.

As shown in Figure 6.2 (c), the TaN capped sample shows less $V_{FB}$ shift compared to the TaN, and W metal gate capacitors. When EOT value is less than 0.8 nm, no humps can be observed, and the C-V curve is closer to the ideal curve. This implies that the
interfacial (La-silicate/Si-substrate) property of the gate stack has improved by capping TaN on W metal gate. However, a relatively large negative $V_{FB}$ shift is observed when EOT value is around 1.0 nm. The negative shift in $V_{FB}$ implies that the net positive charges at the interfaces of La$_2$O$_3$/La-silicate and La-silicate/Si-substrate increase with the La$_2$O$_3$ layer thickness.

![Figure 6.3](image)

**Figure 6.3** EOT dependence of flat band voltage for (a) TaN, (b) W, and (c) TaN/W metal gated La$_2$O$_3$ MOS capacitors with PMA in F.G for 30 min at 800 °C.
Figure 6.3 shows EOT dependence of $V_{FB}$ for TaN, W, and TaN/W metal gated La$_2$O$_3$ MOS capacitors. $V_{FB}$ of the sample with the TaN metal gate (Figure 6.3 (a)) shows a relatively large value compared to the sample with the W metal gate (Figure 6.3 (b)). On the other hand, $V_{FB}$ of the sample with the TaN/W metal gate (Figure 6.3 (c)) shows the smallest value. Both W and TaN/W metal gates show $V_{FB}$ roll-off behavior at EOT around 0.8 nm and 0.9 nm, respectively. In the case of TaN metal gate, $V_{FB}$ roll-up is observed at EOT around 1.3 nm. $V_{FB}$ shifts with EOT can be explained by fixed charges located inside the gate oxide [9]. Therefore, from the slope of $V_{FB}$ the net charge concentrations at the La$_2$O$_3$/La-silicate and La-silicate/Si-substrate interfaces can be qualitatively estimated.

### Table 6.1 Estimated net charge concentrations at the interfaces of La$_2$O$_3$ gate stacks

<table>
<thead>
<tr>
<th>Sample</th>
<th>EOT [nm]</th>
<th>$Q_{net}$ [cm$^{-2}$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>W(60 nm)/La$_2$O$_3$(2–5 nm)/Si</td>
<td>EOT&lt;0.9</td>
<td>-3.19×10$^{12}$</td>
</tr>
<tr>
<td></td>
<td>EOT&gt;0.9</td>
<td>1.24×10$^{13}$</td>
</tr>
<tr>
<td>TaN(45 nm)/La$_2$O$_3$(2–5 nm)/Si</td>
<td>EOT&lt;1.3</td>
<td>8.65×10$^{12}$</td>
</tr>
<tr>
<td></td>
<td>EOT&gt;1.3</td>
<td>-8.20×10$^{12}$</td>
</tr>
<tr>
<td>Ta(45 nm)/W(5 nm)/La$_2$O$_3$(2–5 nm)/Si</td>
<td>EOT&lt;0.8</td>
<td>-1.71×10$^{12}$</td>
</tr>
<tr>
<td></td>
<td>EOT&gt;0.8</td>
<td>2.42×10$^{13}$</td>
</tr>
</tbody>
</table>

Table 6.1 shows the estimated net charge concentrations at the interfaces of La$_2$O$_3$ gate stack. The net charge is the sum of all charges located at the La$_2$O$_3$/La-silicate and
La-silicate/Si-substrate interface. Judging by $V_{FB}$, both W and TaN/W metal gate samples show a large decrease in the net positive charges for $0.9 \text{ nm} < \text{EOT} < 1.3 \text{ nm}$. Whereas a small increase in the net positive charges for the sample with TaN metal gate is observed.

The negative shift of the $V_{FB}$ for EOT over 1.3 nm (as shown in Figure 6.3 (a)) can be explained by the negative polarity of the net charges. The charges at the silicate/Si-substrate interface are considered as positive because of the silicate formation reaction includes oxidation of the Si atoms [10]. Therefore, the charges at the La$_2$O$_3$/La-silicate should be negative since the bonding nature of oxygen atoms in the La$_2$O$_3$ layer is different from the bonding of oxygen atoms in the La-silicate layer. Oxygen atoms are negatively charged ($O^{2-}$) in the La$_2$O$_3$ layer, and neutral ($O^0$) in the La-silicate layer. This bonding state of oxygen atoms in the La$_2$O$_3$ and La-silicate layers leads to negatively charged electrons trapped at the La$_2$O$_3$/La-silicate interface [11]. When EOT is between 0.9 and 1.3 nm, the net positive charges increase due to the metal diffusion or oxygen vacancies induced by metal atoms [12]. When EOT is less than 0.9 nm, the roll-off behavior can be explained by the net positive charge increase due to the phase changes of La-silicate layer [13].
6.3 Effect of the Metal Gate Thickness on Interfacial Properties

In the previous section, MOS capacitor with W metal gate had a better interfacial property compared to MOS capacitor with TaN metal gate electrode. In this section, the effect of metal gate thickness on the interfacial property of MOS capacitors with W and TaN/W metal gate electrodes will be discussed.

Figures 6.4 (a) and (b) show C-V characteristics for W(60 nm)/La₂O₃(4 nm)/Si and W(8 nm)/La₂O₃(4 nm)/Si MOS capacitors, respectively. The capacitor with W(60 nm) metal gate electrode shows a smaller hump in C-V curves compared to the capacitor with thinner W metal gate, indicating that higher concentration of oxygen atoms are contained in the thicker W gate electrode. This result implies that an appropriate thickness for the W metal gate in respect with La₂O₃ thickness should be selected.

---

**Figure 6.4** C-V characteristics for samples with (a) W(60 nm), and (b) W(8 nm) metal gate electrodes.
It is reported that oxygen atoms in the W gate electrode diffuse into the oxide layer, and participate in silicate formation reaction at the La$_2$O$_3$ and Si-substrate interface [9]. XPS results for La$_2$O$_3$ gate dielectric layer with different physical thickness of W metal gate show that the interfacial silicate formation is strongly affected by the thickness of the metal gate [15].

Figure 6.5 shows $C-V$ characteristics for TaN/W/La$_2$O$_3$/Si MOS capacitors with in-situ PMA in FG for 30 min at 800 $^\circ$C. Figure 6.5 shows $C-V$ characteristics for La$_2$O$_3$ MOS capacitors with TaN/W (2 ~ 20 nm) metal gate. Due to TaN capping of the W film, the amount of oxygen atoms in the W metal layer is mainly determined by the thickness of the W metal layer. The oxygen atoms initially absorbed into the W metal layer, start to diffuse into the gate oxide layer during in the PMA process [3]. These oxygen atoms compensate oxygen defects in the La$_2$O$_3$ layer and also promote the silicate reaction at the
La$_2$O$_3$/Si-substrate interface. For W metal gate thickness of less than 5 nm, the capacitance decreases at a constant $V_{FB}$. This means that all the diffused oxygen atoms participate in silicate formation. Above a certain value of the thickness of W metal layer (thicker than 5 nm), the capacitance is largely decreased while the $V_{FB}$ shifts to the negative direction due to some amounts of the oxygen atoms contribute to the fixed charges located at the interface and inside of the gate oxide layer. These results are consistent with reports that a 10 nm thick W metal gate is sufficient to compensate oxygen deficiency in the La$_2$O$_3$ layer [16].

**Figure 6.6** Flat band voltage as a function of the thickness of W metal gate in La$_2$O$_3$/Si MOS capacitors with in-situ PMA in FG for 30 min at 800 °C.

Figure 6.6 shows the experimental and fitting results for $V_{FB}$ as a function of the thickness of the W metal layer in TaN/W/La$_2$O$_3$/Si gate stacked MOS capacitors. The experimentally observed $V_{FB}$ values largely shift to a negative direction with the
increasing of the W metal layer thickness. The experimental results are well fitted to the exponential decay curve of the $V_{FB}$ dependence on the W layer thickness. This indicates that the concentration of the oxygen atoms inside the gate oxide layer is exponentially decayed [17].

6.4 Summary

The impacts of metal gate material and the physical thickness of the metal gate on the interfacial properties of La$_2$O$_3$ gate stacked MOS capacitors were discussed. It was shown that by a combination of TaN (as oxygen free metal) and W (as metal containing oxygen) silicate reaction at the substrate interface can be controlled. Balancing the thickness of each metal is a key factor for preventing excess or deficiency of oxygen atoms within the gate stack which would lead to degradation in device characteristics.
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Chapter 7 Effective Mobility Analyses Based on Remote Coulomb Scattering Model

In this chapter, the analysis of effective mobility for thin La$_2$O$_3$ gate MOSFETs is described.

7.1 Introduction

Mobility degradation is one of the main concerns in MOSFETs with high-k gate stacks [1-6]. A number of models were proposed for clarify the mechanism of mobility degradation in the ultrathin gate oxide MOSFETs [7-15], and these models suggested that remote scattering mechanisms such as RCS [8-11], RSR [12-15], and RPS [16] contribute to the mobility degradation in ultrathin gate oxide MOSFETs. At the room temperature, effect of RPS on the electron mobility can not be reduced due to the intrinsic characteristics of the high-k gate dielectrics. Hence, RCS and RSR scattering are considered can be reduced by optimizing device fabrication process. Effects of RCS and RSR on the electron mobility in the channel of MOSFETs can be separated by their
low and high electric field dependency, respectively [17-18]. In this study, the effect of RCS on the electron mobility in La$_2$O$_3$ gate stacked MOSFETs was studied.

For ultrathin MOSFETs that La$_2$O$_3$ direct contacting on Si-substrate, Kakushima et al. have reported that for EOT thicker than 1.3 nm, reduction of electron mobility value can be considered relatively small and the mobility reduction becomes more significant when EOT is smaller than 1.3 nm. This degradation can be explained by an additional scattering from RCC due to the diffusion of metal atoms from gate electrode into the La$_2$O$_3$ dielectric layer [19]. In the following paragraphs, the effect of charges located near W/La$_2$O$_3$ interface on the electron mobility in the channel of MOSFETs was discussed. Remote scattering from the Coulomb charges was evaluated on La$_2$O$_3$-based MOSFETs with EOT scaled from 1.2 to 0.8 nm.

### 7.2 Remote Charge Scattering Model

In this paragraph, RCS Model is briefly described.

The electron transport in an $n$-type inversion layer formed at a Si (100) surface of a MOSFET with structure of W/La$_2$O$_3$/Si (as shown in Figure 7.1) was considered. Based on the previous work [19], a silicate IL formation between La$_2$O$_3$ layer and Si-substrate was suggested. RCC were assumed mainly located at near the interfaces of the W/La$_2$O$_3$
and $La_2O_3$/silicate layers, and the charge distribution follows a delta function. The electrons in the Si inversion layer were considered as a two-dimensional electron gas.

$\mu_{RCS}$ can be calculated from the relaxation time approximation, as follows:

$$\mu_{RCS} = e < \tau_{RCS} > / m_t^*,$$ \hspace{1cm} (7.1)

where $m_t^*$ is the transverse effective mass of the electron and $< \tau_{RCS} >$ is the averaged relaxation time over the kinetic energy of the electron. The relaxation time can be solved from a perturbation potential by a method proposed by Saito et al [10]. Using Fermi’s golden rule, $\tau_{RCS}$ can be obtained by the following expression:
\[
< \tau_{RCS} > = \frac{\sum_k E(k) \tau_{RCS}[-\partial f / \partial E(k)]}{\sum_k E(k)[-\partial f / \partial E(k)]}, \tag{7.2}
\]

where \( f = f(E, E_F, T) \) is the Fermi-Dirac distribution function, and \( E_F \) is Fermi energy of the electron. The relaxation time is simplified as follows:

\[
\frac{1}{\tau_{RCS}(\varepsilon)} = \frac{2\pi m_i^*}{h^3} \int_{-\infty}^{2\pi} d\theta \int_{-\infty}^{\infty} dz_0 N_{RCS}(z_0) |< A_q(z_0) >|^2 (1 - \cos \theta), \tag{7.3}
\]

where \( \langle \rangle \) is a scattering potential averaged over the inversion charge distribution.

\( A_q(z_0) \) is the Fourier-Bessel transformation of the scattering potential \( \phi(\vec{r}, z; z_0) \). In the calculation of the perturbation potential, the screening effect was included using Thomas-Fermi approximation with considering the quantum fluctuation as derived by Pirovano et al. [20-21].

In the numerical calculation, the transverse and longitudinal effective mass of the electrons were take as \( m_t / m_0 = 0.916 \), and \( m_l / m_0 = 0.2 \), respectively. The dielectric constants of the La_2O_3 layer, the interfacial silicate layer, and Si-substrate were take as \( \varepsilon_{La_2O_3} = 23.4 \), \( \varepsilon_{silicate} = 8 \) and \( \varepsilon_{Si} = 11.7 \), respectively. The EOT value was considered as ranges of 0.7 \( \sim \) 1.5 nm.
Figure 7.2 shows that the numerically (Appendix) calculated $\mu_{\text{RCS}}$ in the channel of La$_2$O$_3$ gate stacked MOSFETs decreases with EOT. This result implies that the RCS potential increases as the location of RCC approaching closer to the inversion layer.

![Figure 7.2 Calculated RCS-limited electron mobility versus inversion charge density.](image)

### 7.3 RCS Induced Mobility Degradation Mechanism

In this paragraph, mobility degradation in the La$_2$O$_3$ gate stacked MOSFETs was discussed.

1) **Experimental details**

nMOS capacitors and nMOSFETs with W/La$_2$O$_3$/Si structure were fabricated on the (1 0 0)-oriented Si-substrates with doping densities of $3 \times 10^{15}$ cm$^{-3}$ and $3 \times 10^{16}$ cm$^{-3}$, respectively. The wafers were cleaned by sulfuric acid hydrogen peroxide mixture (SPM) and HF (1%) solution. After deposition of the La$_2$O$_3$ film by E-beam deposition,
the samples were transferred *in-situ* into a high vacuum chamber and a 60 nm thick W film was deposited by RF-sputtering method. Then, the samples were transferred into a thermal processing chamber and PMA at a temperature of 800 °C for 30 min was carried out in F.G ambient. In order to avoid absorptions of oxygen and moisture from the air, all the fabrication and annealing processes described above were performed in a multi-chamber system, without exposing the samples to the air. After patterning the gate electrodes by RIE, Al thin film was thermally evaporated to form source/drain and backside electrode contacts. In Figure 7.1, a Schematic structure of the samples is shown.

Capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements have been performed by Agilent E4980A precision LCR meter and Agilent 4156C semiconductor parameter analyzer, respectively. The capacitance was measured in the frequency range from 1 kHz to 1 MHz, and the area of the capacitors was $10 \times 10 \mu m^2$. EOT was extracted from the *C-V* data using the NCSU CVC modeling program [22]. Conductance measurements were done in frequency range from 100 Hz to 2 MHz, and the area of the capacitors was $50 \times 50 \mu m^2$. Effective electron mobility was extracted from the data of $I_d-V_d$ and split *C-V* measurements. Both the gate length and gate width
of the measured MOSFETs were 10 μm. Additional scattering mobility was evaluated using Matthiessen’s rule.

2) Observation of mobility degradation

Figure 7.3(a) shows typical 100 kHz C-V curves measured for the fabricated MOS capacitors with EOT down to 0.8 nm. Small humps are observed (Figure 7.3(b)) near the $V_{FB}$ at frequencies of 1 kHz and 10 kHz. These humps indicate the existence of interfacial state density at La-silicate/Si-substrate interface [23].

![Figure 7.3](image)

**Figure 7.3** Measured C-V characteristics for the fabricated MOS capacitors after PMA 800 °C in FG for 30 min; (a) EOT dependence of capacitance value; (b) Capacitance dependence on measurement frequency; in both figures, the solid lines refer to the ideal curve and the symbols refer to measurement data.

Figure 7.4 shows EOT dependence of MOS capacitors on the physical thickness of deposited La$_2$O$_3$ gate dielectrics. Considering the formation of La-silicate at the
oxide/Si-substrate interface [24], the total EOT of the capacitor is determined by the sum of the thicknesses of the La-silicate and La$_2$O$_3$ layers.

\[ EOT = EOT_{\text{La-oxide}} + EOT_{\text{La-silicate}} \]  \hspace{1cm} (7.4)

Where $EOT_{\text{La-oxide}}$ and $EOT_{\text{La-silicate}}$ are equivalent oxide thicknesses for La$_2$O$_3$ and La-silicate layers. The thickness of La-silicate layer formed at La$_2$O$_3$/Si-substrate interface can be extracted from the relation between the estimated EOT and the deposited physical thickness of La$_2$O$_3$ dielectric layer. A best fit (with standard deviation of 0.02 nm) leads to the value of 1.55 nm for silicate IL. The formation of silicate IL at the interface of La$_2$O$_3$/Si-substrate during the thermal annealing process was confirmed by XPS analyses [24]. The fitting also gives the values of dielectric constants $\varepsilon_{\text{La-silicate}} = 8.1$ for silicate IL, and $\varepsilon_{\text{La-oxide}} = 22.3$ for the La$_2$O$_3$ layer. These obtained values are well agreed with the reported $k$ values that are calculated from the oxide thickness determined by TEM images [19, 25]. Assuming the silicate IL thickness at the interface depends only on the annealing temperature, the increment of the measured EOT can be explained simply by the increment in the thickness of La$_2$O$_3$ layer.
Figure 7.4 EOT versus the thickness of the deposited La$_2$O$_3$ film. The closed symbols correspond to the total EOT extracted from the C-V measurement; the solid line refers to the fitting curve, considering the formation of interfacial silicate layer ($T_{La\text{-silicate}}$) within La$_2$O$_3$ layer ($T_{La\text{-oxide}}$).

Figure 7.5 The measured electrical characterizations of W/La$_2$O$_3$ gate stacked MOSFETs annealed at 800 °C in FG for 30 minutes; (a) $I_d$-$V_d$ characteristics, and (b) Gate-to-channel ($C_{gc}$), and gate-to-body ($C_{gb}$) capacitance characteristics.

Figure 7.5(a) shows the $I_d$-$V_d$ characteristics of the fabricated W/La$_2$O$_3$/Si gate stacked MOSFETs. The gate-to-channel capacitance has no
hysteresis, while the gate-to-body capacitance shows a small hysteresis, as shown in Figure 7.5(b). These results suggest that a fairly nice La-silicate/Si-substrate interface is achieved with a negligible amount of local trap states existing near the valance band of the silicon.

**Figure 7.6** Mobility versus inversion layer charge density; (a) measured effective electron mobility, and (b) extracted additional scattering-limited electron mobility for samples with PMA 800 °C in FG for 30 min; the measured device size is L/W = 10/10 μm and measurement frequency is 100 kHz.

Figure 7.6(a) shows EOT dependency of the measured $\mu_{\text{eff}}$ for the fabricated MOSFETs. The $\mu_{\text{eff}}$ decreases with the decrement of EOT. By using Matthiessen’s rule, an additional scattering-limited mobility ($\mu_{\text{add}}$) factor was extracted from $\mu_{\text{eff}}$ of MOSFETs with EOT of 1.2 and 0.8 nm. As shown in Figure 7.6(b), a relation of $\mu_{\text{add}} \propto N_s^{-0.60}$ was observed in the low electric field region ($N_s < 5.5 \times 10^{13}$ cm$^{-2}$). The
power dependency of $\mu_{add}$ on $N_s$, $\mu_{add} \propto N_s^{+0.60}$, suggests that the RCS is the main cause for the mobility degradation [18].

3) Proposed model for explaining mobility degradation by RCS

The obtained $\mu_{eff}$ values at the effective electric field of 0.3 MV/cm for MOSFETs with EOT from 1.2 to 0.8 nm are plotted against the thickness of La$_2$O$_3$ layer in Figure 7.7. The decrease in $\mu_{eff}$ value with the thickness of La$_2$O$_3$ layer can be attributed to at least two kinds of RCC: one originating from La$_2$O$_3$/La-silicate interface and the other from W/La$_2$O$_3$ interface.

![Figure 7.7 Mobility versus the thickness of La$_2$O$_3$ layer. T$_{La$-oxide} is extracted from the total EOT by considering the formation of La-silicate layer. The closed symbols correspond to the measurement data of $\mu_{eff}$ at $E_{eff} = 0.3$ MV/cm. The solid line refers to theoretical modeling.](image)

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Figure 7.8 shows the experimentally observed conductance spectra for the fabricated MOS capacitors. The conductance peaks are roughly constant regardless of both EOT and the electron energy. These conductance peaks can be assigned to RCC centers due to slow traps located at the La$_2$O$_3$/La-silicate interface [26]. This implies that an approximately same amount of RCC is distributed at the La$_2$O$_3$/La-silicate interface despite the changes in the total EOT. Therefore, the observed mobility degradation at smaller EOT can be considered as the result of scattering from the RCC located near the W/La$_2$O$_3$ interface. The small negative shift of $V_{FB}$ with the increment of EOT in Figure 7.3(a) indicates a small reduction of the negative charges. This can be understood due to the increase of the total positive charges as a result of a thicker La$_2$O$_3$ layer. These positive charges are generally attributed to the metal induced [18, 27] and oxygen defects [28] in the gate oxide layer. Given the facts above, it is reasonable to assume that, approximately same amount of RCC is distributed near to the W/La$_2$O$_3$ interface. Therefore, the relation between $\mu_{\text{eff}}$ and the thickness of the La$_2$O$_3$ layer can be modeled using RCS potential intensity at MOSFET channel with different EOT [16]. RCS potential decreases by the $\exp(-2k_F T_{ox})$ factor, with increasing oxide thickness. Where $k_F$ is the Fermi wave number of the channel carriers and $T_{ox}$ is the thickness of the oxide layer. The measured electron mobility, $\mu$ can be expressed as [16]:
\[
\frac{1}{\mu} = \frac{1}{\mu_R} \exp(-2k_F T_{\alpha}) + \frac{1}{\mu_{\text{other}}},
\] 
(7.5)

where \( \mu_R \) is the pre-factor mobility representing the scattering from a high-k dielectric, and \( \mu_{\text{other}} \) is the mobility in the gate-oxide from other contributions. The inset in Figure 7.7 shows an exponential decay trend of RCS potential intensity for RCC located at the La\(_2\)O\(_3\)/silicate interface and near W/La\(_2\)O\(_3\) interface. The RCC distributed at the La\(_2\)O\(_3\)/silicate interface with the density of \( 5.4 \times 10^{12} \text{ cm}^{-2} \) and near W/La\(_2\)O\(_3\) interface with the density of \( 7.9 \times 10^{12} \text{ cm}^{-2} \) results the best calculated fit of \( \mu_{\text{eff}} \) to the experimental value, as shown in Figure 7.7 (solid line). It should be noted that the

Figure 7.8 Conductance spectra for W/La\(_2\)O\(_3\)/Si MOS capacitors with PMA 800° C in FG for 30 min. The dark and light symbols correspond to samples with EOT = 0.8 nm and EOT = 1.2 nm, respectively. The conductance spectra were measured with E-E\(_i\) range from -0.5 to -0.8 eV.
assumed value of charge density located at the La₂O₃/La-silicate interface is consistent with the experimental value of slow trap density extracted by conductance method [26]. The agreement between the calculated and experimentally obtained mobility suggests that the RCC located near to the W/La₂O₃ interface plays an important role in causing the mobility degradation in MOSFETs with thin La₂O₃ dielectrics. Our result suggest that in order to improve the mobility in MOSFETs with thin La₂O₃ gate dielectrics, it is necessary to reduce the RCS potential by reducing the amount of RCC located near W/La₂O₃ interface. This result is consistent with the result reported by Kitayama et al. [29], where a thin Si layer was inserted at the interface between the W and La₂O₃ to reduce the positive fixed charges which induced by the metal electrode, and consequently an improvement in the electron mobility was observed.

7.4 Suggestion to Improve Mobility

Mobility degradation in W/La₂O₃/Si MOSFETs with EOT from 1.2 to 0.8 nm was studied. The obtained results show that RCC located near W/La₂O₃ interface has a dominant role in the mobility degradation as EOT scaled smaller than 1 nm. Our results suggest that in order to achieve a higher mobility in the MOSFETs with thin La₂O₃ gate dielectrics, it is necessary to reduce the RCC located near W/La₂O₃ interface.
References


mobility in Si MOSFET’s: Part I – effects of substrate impurity concentration,


Chapter 8 Summary

In this chapter, summaries of all chapters and future prospects of this thesis are described.

8.1 Summaries of This Thesis

In this thesis, interfacial properties of La$_2$O$_3$ gate dielectrics, and effect of RCS on electron mobility in the La$_2$O$_3$ gate stacked MOSFETs are experimentally investigated.

In the first chapter, high-k dielectrics are introduced and current status of high-k dielectrics in particular La$_2$O$_3$, are summarized. In the second chapter, fabrication process for MOS capacitors and MOSFETs with La$_2$O$_3$ gate stacks and electrical characterization methods are described. Below are the summaries of the remaining chapters:

a) La-silicate interfacial layer formation (Chapter 3)

In chapter 3, realization of direct high-k contact with Si is described. Effect of PMA on the silicate formation mechanism is also investigated. The main findings and contributions of this work are summarized as below:
La$_2$O$_3$ is a suitable candidate to achieve direct high-k contact with Si because of its material nature to form a La-silicate IL at La$_2$O$_3$/Si-substrate interface. Both TEM image and XPS spectra confirm La-silicate IL formation. Measurement and calculation results show that by increasing of the annealing temperature EOT becomes larger due to the formation of La-silicate IL. It was also observed from FTIR spectra that at PMA temperatures of 600 °C and higher, stretch of La-Si-O bonds within the silicate structure start to saturate. This indicates a complete transformation of La$_2$O$_3$ to La-silicate.

b) **Interface and oxide trap states estimation (Chapter 4)**

In chapter 4, the electrical characteristics of MOS devices with La$_2$O$_3$ as gate dielectrics are investigated. Based on the observed two distinct peaks in the conductance spectra for the La$_2$O$_3$ gate dielectrics, a novel interpretation for conductance method to evaluate interface and oxide trap state density has been proposed. The observed result assigned that the amount of the slow trap centers located at the La$_2$O$_3$/La-silicate interface can not be reduced by PMA in the F.G ambient. The estimated value of the order of $10^{13}$ cm$^{-2}$/eV for the slow traps at the La$_2$O$_3$/La-silicate interface indicates that a W/La-silicate/Si structure is preferable for fabrication of devices with low interfacial traps.

c) **Interfacial properties and effect of annealing (Chapter 5)**
In chapter 5, process-based approach for interfacial properties is described. Effect of PMA temperature on the electrical characteristics of La$_2$O$_3$ gate stack capacitors was investigated. The result shows that \textit{in-situ} PMA is an effective method in order to suppress EOT increase due to thermal treatment. High temperature PMA of 800 °C or more was found to be important for improving the interfacial properties of La$_2$O$_3$ gate stacked MOS capacitors.

d) Impact of metal gate on interfacial properties (Chapter 6)

In chapter 6, the impact of the metal gate material and physical thickness of the metal gate on the interfacial properties of La$_2$O$_3$ MOS capacitors by reducing the amount of oxygen atoms in the metal gate were discussed. The result shows that the silicate reaction at the substrate interface can be controlled by a combination of TaN (as oxygen free metal) and W (as metal containing oxygen). Balancing the thickness of each metal is a key factor for preventing excess or deficiency of oxygen within the gate stack which would lead to degraded device characteristics.

e) Effective mobility analyses based on RCS model (Chapter 7)

In chapter 7, mobility degradation in W/La$_2$O$_3$/Si MOSFETs with EOT from 1.2 to 0.8 nm was studied. The obtained results show that RCS from Coulomb charges located near the metal gate/high-k interface has a dominant role in the mobility degradation as
EOT scaled down less than 1 nm. Our result suggests that in order to achieve a higher mobility in the MOSFETs with thin La$_2$O$_3$ gate dielectrics, it is necessary to prevent or reduce the amount of RCC located near W/La$_2$O$_3$ interface by reducing the RCS potential.

8.2 Recommendations for Further Study

Based on this study, further study of high-k/metal gate stacks with La-silicate is described. Interfacial properties improvement and mobility degradation are two of the main concerns in performance improvement of the downscaled devices. In this work, La-silicate IL formation and its effects on interfacial properties of La$_2$O$_3$ gate dielectrics were studied. The silicate reaction is basically triggered by the presence of oxygen atoms. The controlling of the amount of oxygen atoms corresponds to the controlling of silicate reaction. Further EOT scaling may be achieved by systematic study including spectral analysis for the chemical bonds at the interface and in the gate oxide. The amount of oxygen atoms in the gate stacks should be investigated by spectral analyses. The MOSFET performance can be improved by preventing metal diffusion and reducing oxygen defects. As previously mentioned in this study, RCS from Coulomb charges within high-k layer near to the metal gate/high-k interface become an important
factor in mobility degradation for ultrathin MOSFETs with high-k dielectrics. Further studying of RSR scattering is also necessary to improve device performance. Especially, effects of these two remote scattering mechanisms are expected to reduce by optimizing device fabrication process.

In conclusion, this thesis provides useful information and further understanding for high-k/metal gate system. These studies are also expected to contribute to the future progress of LSIs.
Publications and Presentations

a) Publications (3 papers accepted for publication)


b) International Presentations (2 oral presentations)

1) M. Mamatrishat, M. Kouda, T. Kawanago, K. Kakushima, P. Ahmet, A. Aierken, K.


c) Domestic Presentations (3 oral presentations)


3) M. Mamatrishat, M. Kouda, K. Kakushima, P. Ahmet, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, and H. Iwai, Remote Coulomb scattering limited mobility in MOSFET with CeO$_2$/La$_2$O$_3$ gate stacks, 70$^{th}$ Japan Society of Applied
Physics (JSAP), Japan, Sept. 2009.

d) Domestic Presentations (5 posters)


e) Other contributions (3 international and 4 domestic conferences)


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Appendix

A. MATLAB code for RCS-limited electron mobility calculation

The RCS-limited electron mobility was calculated based on the work of S. Saito (*J. Appl. Phys.*, 98, 113706(2005)).

The MATLAB code was written by the author Mamat Mamatrishat.

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--------------Physical constants-------------------

Clear

fid=fopen('77K-La2O3-La-sil.txt','w+'); % open a data file

double E;
double Z_o;

h=6.63*10^(-34); % Planck’s constant [JS]
h_p=h/(2*pi); % Reduced Planck’s constant [JS]
e=1.6*10^(-19); % Electron charge [C]
m_o=9.1*10^(-31); % Electron mass [kg]
m_p=0.19*m_o; % Effective mass in interface direction
m_z=0.916*m_o; % Effective mass motion in z direction
V=1; % Voltage unit
g_v=2; % Degeneracy factor for spin
k=1.38*10^(-23); % Boltzmann constant [J/K]
E_o=3.1*e*V; % Lowest subband energy 3.1eV
E_f=4.56*e*V; % Fermi energy (refer to vacuum level)
k_f=sqrt(2*m_p*E_f)/h_p; % Wave vector corresponding to E_f
T_1=300; % Room temperature 300 K

% Densities in gate stack
N_depl=3*10^20; % Depletion charge density
N_inv=2.5*10^12; % Inversion charge density
% Permittivities in gate stack
E_Si=11.7;  % Dielectric constant of silicon (or 11.5)
E_SiO2=3.9;  % Dielectric constant of SiO2
E_La-sili=10;  % Dielectric constant of La-silicate
E_Al2O3=11.5;  % Dielectric constant of Al2O3 (or 9.3)
E_La2O3 = 23;  % Dielectric constant of La2O3

% Thickness of layers in the gate stack
\text{t}_{SiO2_1} = 0.7 \times 10^{-9} \text{ nm};  \%
\text{0.7nm, 0.9nm, 1.5nm, 2.7nm}
t_{Al2O3} = 2.0 \times 10^{-9} \text{ nm};  \%
\text{Physical thickness of Al2O3}
t_{phys_1} = 2.7 \times 10^{-9} \text{ nm};  \%
\text{Total physical thickness}

%-------------------------------------Parameter P_0 and P_av-------------------------------------
b_alpha=48\pi m_z e^2;  % Pre-factor of the b

step=E_meas;  % Effect field (unit in V/m)
Low_E=Low_E;
Up_E=Up_meas;

E_eff = Low_E:step:Up_E;  % Effect field (unit in V/m)
b=(b_alpha*(E_Si*E_eff/e-5*N_inv/32)/(h_p^2)).^(1/3);  % Variation factor

\text{--------------------------Screening parameter determination --------------------------}
eta=(E_f-E_o)/(k*T_1);
mahraj=(1+exp(-eta))*log(1+exp(eta));
q_so=(N_inv*e^2)/(2*E_Si*k*T_1*mahraj);
Fermi = @(E) 1/(1+exp((E-E_f)/(k*T_1)));  % Fermi distribution function
q_s = @(E) q_so/(2*Fermi(E_o))/(sqrt(E/4));

%--------------------------------- Parameter beta ---------------------------------------------------

\text{beta1}=(E_Si-E_La-sili)/(E_Si+E_La-sili);
\text{beta2}=(E_La-sili-E_Al2O3)/(E_La-sili+E_Al2O3);
\text{beta3}=(E_Al2O3-E_gate)/(E_Al2O3+E_gate);

%--------------------------------- Parameter gamma-----------------------------------------------------

Yegin_1=[]
gam_40_1=[]
gam_4_1=[]
gam_1_1=[]
gam_2_1=[]
gam_3_1=[]
gam_4_1=[]
gam_5_1=[]
Yegin_1 = @(E)(beta2*exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_SiO2_1)+beta3*... exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_phys_1);
gam_40_1 = @(E)((beta2)*(beta3)*exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_phys_1)+... exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_SiO2_1).*(1+beta1*Yegin_1(E));
gam_4_1 = @(E) (1./gam_40_1(E));
beta=beta1*beta2*beta3;
gam_1_1 = @(E) ((gam_4_1(E)).*(beta*exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_phys_1)+... exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_SiO2_1).*(beta1+Yegin_1(E))));
gam_2_1 = @(E) (gam_4_1(E).*(exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_SiO2_1)+... beta2*beta3*exp(-2*2*sqrt(2*m_p*E/h_p^2)*t_phys_1)));
gam_3_1 = @(E) (gam_4_1(E).*(exp(-2*2*sqrt(2*m_p*E/h_p^2)*... t_SiO2_1).*Yegin_1(E)));
gam_5_1 = @(E) (gam_4_1(E)*beta3.*exp(-2*2*sqrt(2*m_p*E/h_p^2)... *t_phys_1));
%--------------------------------------Average scattering potential-------------------------------
Z_o_1=-0.7*10^(-9); % Position of test charge (0.7~2 nm)
Z_e = e * A_N; % Atomic number of fixed charge in gate
mm1=(1-beta1)*Z_e;
denominator1_1 = @(E) (2*sqrt(2*m_p*E/h_p^2)+... q_s(E).*(P_av(E)+gam_1_1(E).*P_o(E).*P_o(E)));
surat1_1 = @(E)

% subplot(2,2,1) plot(E_eff,A_av1,'--rs')
%-------------------------------------- Scattering rate ---------------------------------------------
Z_o=[];
Pref=(2*pi*m_z)*(2*pi)/(h_p^3); % Integral constants
N_ofix=N_depl; % Fixed charge (FC) to cause the RCS
\[ N_{rcs\_1} = @Z_o (N_{ofix} * \exp(-2*\sqrt{2*m_p*E/h_p^2})*Z_o); \]

% Exponential distribution of FC

\[ F1 = @Z_o ((N_{rcs\_1}(Z_o)).*((A_{av1}(E)).*(A_{av1}(E)))); \]

\[
\text{integ1} = \text{quadv}(F1, -d\_limit, u\_limit); \quad \% \text{Double integral part}
\]

\[ f_{rcs1} = \text{Pref} \* \text{integ1}; \]

subplot(2,2,2)

plot(E\_eff, f_{rcs1},'--rs')

%--------------------------------------------------------------- Average scattering time -------------------------------

\[ E= []; \]

\[ D_f = @(E) -1/(k*T_1)*(1-\text{Fermi}(E)).*\text{Fermi}(E); \quad \% \text{Derivative of the Fermi function} \]

\[ D_s = g_v*m_p/(\pi*(h_p)^2); \quad \% \text{Density of states}(E>E_{c\_min}=3.1eV) \]

\[ S11 = @(E) (-D_s*E*(D_f(E))./f_{rcs1}); \]

\[ \text{Surat\_integ1} = \text{quadv}(S11, d\_limit, u\_limit); \quad \% \text{Integral of S11} \]

\[ M1 = @(E) (D_s*E.*\text{Fermi}(E)); \]

\[ \text{Mahraj\_integ1} = \text{quadv}(M1, d\_limit, u\_limit); \]

\[ tao_{rcs1} = \text{Surat\_integ1}./\text{Mahraj\_integ1}; \quad \% \text{Average RCS time} \]

subplot(2,2,3)

plot(E\_eff, tao_{rcs1},'--rs');

%---------------------------- Remote charge scattering limited mobility -------------------------------

\[ u_{rcs1} = e*tao_{rcs1}/m_p; \]

subplot(2,2,4)

plot(E\_eff, u_{rcs1},'--rs');

\[ E\_eff1 = E\_eff; \]

fprintf(fid,'%10.4e%10.4e%10.4e
',E\_eff1, A_{av1}, u_{rcs1});

end