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Schottky Barrier Heights Extraction of an Atomically Flat Ni-silicide/Si Interface with Dopants through Diode Characteristics and X-ray Photoelectron Spectroscopy

Supervisor: Prof. Hiroshi Iwai
Supervisor: Associate Prof. Kuniyuki Kakushima

Tokyo Institute of Technology
Department of Electrical and Electronic Engineering

07_29178 Ryo Yoshihara
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It is important to exactly measure a Schottky barrier height of metal/semiconductor with an atomically flat interface. In this study, we drew on the individualistic Ni-silicide process for the ideal interface, and incorporated B and P to the silicide interface. Then we extracted the Schottky barrier heights ($\phi_{BM}$) of the Ni-silicide/Si through $J-V$ and $C-V$ Schottky characteristics and X-ray photoelectron spectroscopy (XPS). In the result, we have been able to indicate achievement of an atomically flat interface by the individualistic Ni-silicide process, and effectiveness as no infection from parasitic element.
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Introduction

1 Introduction

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1.1 Introduction of CMOS scaling

Continuous shrinking CMOS device into 16 and 11 nm technology nodes is facing tremendous difficulties, including severe short channel effects, degraded driving current, dopant penetrations and poly-silicon depletion, high-field effects, direct gate tunneling current and high series resistance [1.1]. Keeping the Moore’s law way encounters unprecedented difficulties. Among them, source/drain region receives considerable attentions as a key component in MOSFET structure, as traditional source/drain with p-n junctions faces inevitable deficiencies, such as complicated process, large parasitic capacitors and tight compromises between thermal budgets and parasitic resistance [1.2]. One solution is to use Schottky barrier contacts, usually implemented with metal silicides, which can have low parasitic resistance and abrupt interface. In addition, Schottky barrier source/drain process can be achieved with low annealing temperature [1.3].

1.2 Issues of Schottky junction

The issues of Schottky barrier source/drain include the control of $\phi_{Bn}$, under-lapping and over-lapping to the gate and narrow process temperature window [1.4]. Additionally, the surface morphology and interface roughness induce variability in $\phi_{Bn}$, and degrade the sheet resistance and the ideality factor ($n$-factor) [1.5, 1.6].
1.3 Purpose of this study

In this paper, we propose a novel stacked-silicide process for an atomically flat Ni-silicide/Si interface without consumption Si from substrate. Moreover, we measure the $\phi_{Bn}$ of the silicide diodes.

Chapter 1 summarizes the background and the purpose of this study. Chapter 2 expresses the experimental principles and the procedures. In chapter 3, composition and morphology of the stacked-silicide are evaluated, and an atomically flat interface is confirmed. In chapter 4, measurement of $\phi_{Bn}$ through diode characteristics and XPS were conducted, and we examined the effect of dopants incorporation. Chapter 5 summarizes this study.
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Experiment setup

2 Experimental setup

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2.1 Device fabrication

2.1.1 Radio frequency magnetron sputtering

Thin films are the subject of matter for many applications and have got significant importance in physical sciences and engineering. Sputtering is one important technique used for thin film deposition. Radio frequency (RF) magnetron sputtering is an enhanced sputter method which enables a higher deposition rate at low operating pressure together with the possibility to obtain high quality films at low as well as high substrate temperatures. In this study, the surface contact metals were deposited by RF magnetron sputtering using the Ar gas. In the chamber filled with the Ar gas, the high voltage is applied in high frequency between the target side and the sample side. The surface atoms of target material are removed and deposited on a substrate by bombarding the target with the ionized Ar atoms. The magnet, located behind the target, enhances ionization and effectively directs the sputtered atoms towards the substrate, and the samples are not damaged by the plasma. Schematic diagram of this method is shown in fig. 2.1.

![Schematic diagram of RF magnetron sputtering.](image)

Fig. 2.1 Schematic diagram of RF magnetron sputtering.
2.1.2 Rapid thermal annealing

Rapid thermal annealing (RTA) was used for produce of Ni-silicide. The heat chamber was vacuum and filled in nitrogen gas, so that the effect of prevention oxidation of the sample. The samples were annealed by infrared ray for 1 minute.

2.1.3 Vacuum evaporation

Al was used for backside contact of Schottky diodes. Al was deposited by vacuum evaporation method which is suitable for deposition of metallic thin films onto cool surface. A suitable material (the source), in this study using Al, is placed inside the vacuum chamber with a heater. When the temperature reaches the evaporation temperature of the source, atoms or molecules start to leave the surface of the source and travel in a more or less straight path until they reach another surface (substrate, chamber wall, instrumentation). Since these surfaces are at much lower temperatures, the molecules will transfer their energy to the substrate, lower their temperature and condense. The schematic diagram of this method is shown in fig. 2.2.

Fig. 2.2 Schematic diagram of vacuum evaporation.
2.2 Four-point method

In a planar IC technology, it is useful to define a quantity, called the sheet resistivity ($\rho_{sh}$). That is because the thickness of conducting regions is uniform and normally much less than both the length and width of the regions. $\rho_{sh}$ of the sample was measured by four-point method. In this method, put four probes on the sample in a straight line, and the resistance is obtained by measuring difference of potential between the two inner probes when a small current is passed through the two outer probes as shown fig. 2.3.

![Fig. 2.3 Schematic illustration of four-point method.](image)

2.3 Transmission electron microscopy

Transmission electron microscopy (TEM) is one of the electron microscopes. In this study, observations of silicide cross section surface were using TEM. By irradiating electrons to the thin sample, some electrons are scattered and others are transmitted.
Because the amount of transmitted electrons depends on the structure or component of each portion, the image is generated by the interference of the transmitted electrons. In TEM, the specimen shape and surface structure in addition to information of the internal material which is the degree of cohesion, crystalline patterns, presence of lattice defect, and such as orientation directions of the crystal can be known by observing the internal structure of the sample. Typically a TEM consists of three stages of lensing as shown fig. 2.4. The stages are the condenser lenses, the objective lenses, and the projection lenses. The condenser lenses are responsible for primary beam formation, whilst the objective lenses focus the beam that comes through the sample itself. The projection lenses are used to expand the beam onto the fluorescent screen or other imaging device, such as film.

![Organizational illustration of the TEM.](image-url)
2.4 Electrical characteristics

2.4.1 $J$-$V$ characteristics

2.4.1.1 Thermionic emission theory

Current characteristics of Schottky diodes ($J$-$V$) were measured by semiconductor parameter analyzer. In this study, the method of analyzing $J$-$V$ data used thermionic emission (TE) theory. Thermionic-field emission (TFE) and generation current from depletion don’t been considered, as these effects are negligible in the prepared samples in this study. From the TE theory,

\[
J = A^* T^2 \exp\left( -\frac{q \phi_{Bn}}{kT} \right) \left[ \left( \frac{q V_{app}}{nkT} \right) - 1 \right],
\]

(2.1)
can be obtained where $A^*$ is the effective Richardson constant, $T$ is the absolute temperature, $q$ is the electronic charge, $\phi_{Bn}$ is the Schottky barrier height, $k$ is the Boltzmann’s constant, $V_{app}$ is the applied voltage, and $n$ is the ideality factor ($n$-factor) which is related to the slope. $\phi_{Bn}$ and $n$-factor can be obtained by fitting of $J$-$V$ characteristics. $A^*$ can be obtained from temperature characteristics. If the Schottky diode is applied values of reverse voltage greater than $3kT/q$, eq. 2.1 can be reduced to

\[
J = A^* T^2 \exp\left( -\frac{q \phi_{Bn}}{kT} \right)
\]

(2.2)

and if eq. (2.2) is multiplied by $T^2$, we obtain

\[
\ln \left( \frac{J}{T^2} \right) = -\frac{q \phi_{Bn}}{kT} + \ln(A^*)
\]

(2.3)

Thus the intercept at y-axis ($1/T = 0$) yields $A^*$ as shown fig. 2.5 [2.1].
2.4.1.2 Image-force-induced barrier lowering

Image-force is the interaction due to the polarization of the conducting electrodes by the charged atoms of the sample. The image-force effect causes the energy barrier for electron transport across a metal-silicon interface to be lowered by

\[ \Delta \phi_{Bn} = \sqrt{\frac{qE}{4\pi\varepsilon_{si}}} \]  

(2.4)

where \( E \) is the electric field and \( \varepsilon_{si} \) is the permittivity of Si. The actual energy barrier for electron transport in a Schottky barrier diode is \( (q\phi_{Bn} - q\Delta \phi_{Bn}) \) [2.2].

2.4.2 C-V characteristics

Capacitance characteristics of Schottky diodes were measured by (E4980AC) LCR meter. \( \phi_{Bn} \) can also be determined by the capacitance measurement. The relationship

Fig. 2.5 Extraction of \( A^* \) from a plot of \( \ln(J/T^2) \) versus \( 1/T \).
between $C$ (depletion-layer capacitance per unit area) and $V_{app}$ is given by

$$C = \sqrt{\frac{q\varepsilon_{si}N_d}{2(\psi_{bi} - V_{app})}}$$  \hspace{1cm} (2.5)

where $N_d$ is the donor impurity density and $\psi_{bi}$ is the built-in potential. Fig. 2.6 shows a typical result where $1/C^2$ on $V_{app}$. The intercept at the voltage axis gives $\psi_{bi}$ from which $\phi_{Bn}$ can be determined:

$$\phi_{Bn} = \psi_{bi} + E_c - E_f$$  \hspace{1cm} (2.6)

where $E_c$ is the conduction band and $E_f$ is the Fermi level [2.1].

![Graph showing the extraction of $\psi_{bi}$ from a plot of $C^{-2}$ versus $V_{app}$](image.png)
2.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is one of the most effective method of determining the elements, which composing the sample. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from the material being analyzed. The relation of the energies can be expressed:

\[ h \nu = E_k + E_b \]  

(2.7)

where \( h \nu \) is the energy of the x-ray, \( E_k \) is the kinetic energy of the emitted electron and \( E_b \) is the binding energy of the emitted electron. Because the value of \( h \nu \) is constant, \( E_b \) is determined by measuring \( E_k \). The \( E_b \) is peculiar to each element and the elements consisting of the sample is also determined. In this study, the chemical composition of the sample was measured by hard XPS at Spring-8 BL46XU as shown fig.2.7 [2.3], and the relative displacement of \( \phi_Bn \) was calculated by the measure results. The mean free path of excited electrons is about 10 nm, so this is sufficiently smaller than the thickness of the depletion layer is about 300 nm. Therefore, we can analyze near the surface and compare each \( \phi_Bn \).
2.6 Conclusions

This chapter showed the principles and structures of the experimental apparatus, and the measurement of $\phi_{\text{lin}}$. 

Fig. 2.7 Diagrammatic illustration of the XPS system.
References


Chapter 3
Composition and morphology of Ni-silicide films

3 Composition and morphology of Ni-silicide films

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References
3.1 Process of Ni-silicide

The wafers used in this study were n-type Si(100) with a doping density of \(3 \times 10^{15}\) cm\(^{-3}\). A set of Si/Ni(1.9nm/0.5nm) was cyclically stacked [3.1] for 8 times and 3-nm-thick, and 5.5-nm-thick Ni thin film was deposited by RF magnetron sputtering system after SPM (H\(_2\)O\(_2\):H\(_2\)SO\(_4\) = 1:4) cleaning and HF treatment of the substrates as shown fig. 3.1. The values of Si/Ni layers thickness correspond to atomic concentration of 2 to 1.

3.2 Measurement of sheet resistance

The samples of deposition film were annealed in nitrogen gas at annealing temperature ranging from 200 to 900 °C for 1 minute, and measured \(\rho_{sh}\) using four-point method. Fig. 3.2 shows \(\rho_{sh}\) of the films on annealing temperature. \(\rho_{sh}\) of the stacked-layer showed a gradual decrease with annealing up to 875 °C, where Ni-5.5nm and Ni-3.0nm were found to degrade at lower temperature (500 and 800 °C, respectively). We can be inference that the silicide with stacked-layer is NiSi\(_2\), because \(\rho_{sh}\) of stacked-layer indicated nearly characteristics.
3.3 Observation of cross-section surface

Cross-section surfaces of the staked-layer as-deposited and annealed at 500 °C were observed by TEM. As shown in fig. 3.3, TEM images revealed no change in the thickness, so this consequence indicate that the stacked-layer silicide achieved an atomically flat interface and surface before and after annealing at 500 °C.
3.4 Analysis of the chemical composition

Ni $2p_{3/2}$ spectra of the samples annealed at various temperatures are shown in Fig. 3.4. The binding energy at the peak intensity was found to shift to higher energy from pure Ni, which was obtained by the as-deposited 3.0-nm-thick sample. At an annealing temperature of 250 °C, the spectrum indicates the main composition is Ni-rich phase, which is in good agreement with the $\rho_{sh}$ as high resistivity is reported for Ni-rich phase. As the sample with 5.5-nm-thick-Ni showed a single peak at 500 °C annealing, it corresponds to the NiSi phase. The spectrum obtained a single peak when the sample with was annealed at 800 °C. This peak indicate NiSi$_2$ phase. When the sample with stacked-layer was annealed at 500 °C, the spectrum showed two single peaks have small and large one. The small and large peaks corresponded to NiSi and NiSi$_2$ phase, respectively.
3.5 Conclusions

\( \rho_{sh} \) of the stacked-layer was indicated the same characteristic of the NiSi\(_2\) by the as-deposited 3.0-nm-thick sample. Using TEM revealed that the interface of the stacked-layer was an atomically flat. The stacked-layer which was composed NiSi\(_2\) was confirmed by XPS. Therefore, we achieved the process of NiSi\(_2\) which has an atomically flat interface.

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Chapter 4
Measurement of Schottky barrier heights

4 Measurement of Schottky barrier heights

4.1 Process of Schottky diodes

4.2 Comparing stacked-layer with single-layer diodes

4.2.1 \(J-V\) characteristics

4.2.2 \(C-V\) characteristics

4.2.3 X-ray photoelectron spectroscopy

4.3 Schottky barrier height control with B and P incorporation

4.3.1 Incorporation process

4.3.2 \(J-V\) characteristics

4.3.3 \(C-V\) characteristics

4.3.4 X-ray photoelectron spectroscopy

4.4 Conclusions

References
4.1 Process of Schottky diodes

Fig. 4.1 shows the fabrication flow of Schottky diodes. Schottky diodes were fabricated on HF-last n-type Si (100) substrates with a doping density of $3 \times 10^{15}$ cm$^{-3}$. SiO$_2$ were etched and buffered HF (BHF) after lithographical patterning. The surface contact metals were sputtered as chapter 3.1. An Al film was formed as a backside contact using vacuum evaporation after resist was eliminated. The schematic illustration of Schottky diodes is shown fig. 4.2.

![Fig. 4.1 Experimental procedure of Schottky diode process.](image1)

![Fig. 4.2 Schematic illustration of fabricated Schottky diode.](image2)
4.2 Comparing stacked-layer with single-layer diodes

4.2.1 $J$-$V$ characteristics

For calculating $A^*$, we measured temperature characteristics of the stacked-layer diode from 26 °C to 80 °C after annealed the diode at 500 °C as shown fig. 4.3. The value of $A^*$ was $112 \text{ A/cm}^2\cdot\text{K}^2$ by the ordinate intercept at $1/T = 0$ in $V_{app} = -1 \text{ mV}$. This value is similar to the value of literature which is $110 \text{ A/cm}^2\cdot\text{K}^2$.

Fig. 4.3 Plot of $\ln(J/T^2)$ versus $1/T$ at $V_{app}$ from -0.01 to -1 V.

$J$-$V$ characteristics of the Schottky diodes with the Si/Ni stacked, Ni(3.0nm) and Ni(5.5nm) layer annealed at 500 °C measured, and fitted by TE theory as shown Fig. 4.4. The diode $J$-$V$ characteristics of stacked-layer showed almost ideal reverse current and single-layer showed declinations from ideal curves.
Fig. 4.4 $J-V$ characteristics of the diodes with thin and thick Ni and stacked Si/Ni.

Reverse current density at $V_{app} = -1$ mV measured at varied areas of 20×20, 50×50, 100×100 and 200×200 µm$^2$ as shown fig. 4.5. The Schottky diode with stacked-layer indicated low values and little or nothing dispersion. The single-layer diode indicated dispersions which may were caused by effecting around current. When the electrically active area was larger, the dispersions were lower.

Fig. 4.5 Reverse current density of the diodes at $V_{app} = -1$ mV on area.
Fig. 4.6 shows $\phi_{Bn}$ and $n$-factor extracted $J$-$V$ characteristics of the Schottky diodes on various annealing temperature. The Schottky diode with stacked-layer indicated stable values of $\phi_{Bn}$ within 0.59–0.63 eV and $n$-factor lower 1.1 until 700 °C. The single-layer diodes showed scattered values in $\phi_{Bn}$ and $n$-factor. Therefore, stacked-layer diode achieved ideally sable interface.

![Graph showing $\phi_{Bn}$ and $n$-factor vs. annealing temperature.]

Fig. 4.6 $\phi_{Bn}$ and $n$-factor of the diodes on annealing temperature.

### 4.2.2 $C$-$V$ characteristics

Schottky barrier heights of the diodes were also obtained by $C$-$V$ characteristics. Fig. 4.7 shows plot of $C^2$ of the diodes on applied voltage from -2.0 to 0 V for calculating $\psi_{Si}$. As a result, $E_c - E_f = 0.234$ eV was determined by the donor impurity density. The values of $\phi_{Bn}$ of the diodes with Si/Ni stacked, Ni(3.0nm) and
Ni(5.0nm) layer were obtained 0.62, 0.47 and 0.49 eV, respectively. $\phi_{Bn}$ of the diode with stacked-layer by $C-V$ characteristic is almost similar by $J-V$ characteristic. $\phi_{Bn}$ of the diodes with single-layer by $C-V$ characteristics have a little difference by $J-V$ characteristics, because the $J-V$ characteristics were additionally measured around current.

![Figure 4.7](image)  
**Fig. 4.7** $C^2$ of the diodes versus applied voltage.

The capacitance of the diodes with stacked-layer measured at varied areas of 20×20, 50×50, 100×100 and 200×200 µm² as shown in fig. 4.8. The smaller the value of area increases the value of the intercept on the voltage axis. This is likely because of the parasitic capacitance of SiO₂ around electrode. Therefore, in order to give a more accurate $\phi_{Bn}$ may be larger in area.
4.2.3 X-ray photoelectron spectroscopy

Si 1s spectra of the samples with the Si/Ni stacked, Ni(3.0nm) and Ni(5.5nm) silicide were analyzed by XPS as shown fig. 4.9. The differences of Si substrate peaks Ni(3.0nm) and Ni(5.5nm) silicide from stacked-silicide were 0.15 and 0.18 eV, respectively. The difference of Ni(3.0nm) from stacked-layer is much the same difference of $\phi_{Bn}$. The difference of Ni(5.5nm) from stacked-layer is lack of accuracy as relative displacement of $\phi_{Bn}$, because peak of NiSi is distinct from NiSi$_2$. 

Fig. 4.8 $C^{-2}$ of the diodes versus applied voltage of various areas.
Fig. 4.9 Si 1s spectra of the silicide films with (a) Si/Ni stacked, (b) Ni(3.0nm) and (c) Ni(5.0nm).
4.3 Schottky barrier height control with B and P incorporation

4.3.1 Incorporation process

Using B and P incorporation is expected a wide change of $\phi_{bn}$, as predicted theoretically [4.1]. Fig. 4.10 shows schematic illustration of inserting B and P at the silicide/substrate interface of the sample. In P case, a 0.68-nm-thick-Ni$_3$P layer was deposited instead of the first Ni layer. The 0.68-nm-thick-Ni$_3$P corresponded to the same Ni atomic concentration of a 0.5-nm-thick-Ni. In B case, a 0.13-nm-thick-B layer was deposited. The 0.13-nm-thick-B corresponded to the same P atomic concentration of the 0.68-nm-thick-Ni$_3$P.

Fig. 4.10 (a) B and (b) P incorporation schemes for stacked-silicide process.
Cross-section surfaces of B and P incorporated stacked-layer were observed by TEM as shown fig. 4.11. The images revealed no change in the morphology and atomically flat interface were maintained.

Fig. 4.11 TEM images of (a) B and (b) P incorporated stacked-layer diodes.

4.3.2 $J$-$V$ characteristics

Fig. 4.12 shows $J$-$V$ characteristics of the diodes annealed at 500 °C, where large shift in the reverse current was observed for both case. In B case, the reverse current decreased, and in P case, the reverse current increased. The extracted $\phi_{bn}$ was 0.68 and 0.36 eV for B and P, respectively. $J$-$V$ characteristic of P incorporation obtained nearly ohmic characteristic. This shift of $J$-$V$ characteristics supposably occurred due to changing the work function of Ni-silicide by B and P incorporation, or dipoles caused by electron transfer at interface.
On annealing temperature up to 800 °C, $\phi_{Bn}$ and $n$-factor were extracted from $J$-$V$ characteristics of the diodes as shown fig. 4.13. $\phi_{Bn}$ of B and P incorporation up to 700 °C annealing were within 0.67–0.70 eV and 0.37–0.41 eV, respectively. The $n$-factor of P incorporation did not been extracted, because $J$-$V$ characteristic of P incorporation was nearly ohmic characteristic.
4.3.3 C-V characteristics

Fig. 4.14 shows $C^2$ of the diodes with B and P incorporation on applied voltage from -2.0 to 0 V. The capacitance of the diode with P incorporation could not be measured, because the diode resistivity was too small. The value of $\phi_{BN}$ of the diode with B incorporation was obtained 0.73 eV which was different from $\phi_{BN}$ of $J-V$ characteristic, because the incorporated B atom at surface diffused by breaking and forming bond configurations in SiO$_2$ networks, and exchanged Si atom affected lowering $\phi_{BN}$ of $J-V$ characteristic as shown fig. 4.15 [4.2].
Fig. 4.14 $C^2$ of the stacked-silicide with B incorporation versus applied voltage.

Fig. 4.15 Scheme illumination of diffused B atom in SiO₂, to induce errors for $C-V$ measurement.

4.3.4 X-ray photoelectron spectroscopy

Analysis of Si 1s spectrum by XPS is the way of measurement relative $\phi_{Ba}$ in no band bending, and then $\phi_{Ba}$ of the stacked-silicide with P incorporation can be exactly obtained in contrast to $J-V$ and $C-V$ characteristics. Fig. 4.16 shows Si 1s spectra of
the silicide films with B and P incorporation. The differences of Si substrate peaks B and P incorporation from stacked-silicide were 0.12 and 0.33 eV, respectively. The difference of B incorporation from stacked-layer is much the same difference of $\phi_{\text{Bi}}$. Each of the band shape of the diodes were assumed by the relative $\phi_{\text{Bi}}$ as shown Fig. 4.17.

![Si 1s spectra](image)

Fig. 4.16 Si 1s spectra of the silicide films with
(a) Si/Ni stacked, (b) B and (c) P incorporation.
4.4 Conclusions

We extracted $\phi_{Bn}$ through $J-V$ and $C-V$ characteristics. The values were swayed by parasitic element. Then we estimated the relative $\phi_{Bn}$ by XPS, and declared the effectiveness as no infection from parasitic element.
References


Chapter 5
Conclusions
A novel stacked-silicide process has achieved an atomically flat silicide and silicon interface. The existence of NiSi$_2$ phase has been confirmed at low temperature annealing and the surface has shown resistant up to 800 °C, which is in good agreement with change in the sheet resistivity. The diode characteristics have shown ideal characteristics as no Si consumption from substrate. Extraction of $\phi_{nn}$ through diode characteristics and XPS have demonstrated the effectiveness of measurement which don’t been affected by parasitic elements.
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