Interface state density measurements of 3D silicon channel by conductance method

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Introduction
Silicon metal-oxide-semiconductor (MOS) field-effect transistors (FETs) with three-dimensional channels, such as Fin FET, Tri-gate and Si nanowire FET, have attracted a strong interest owing to their excellent properties. Performance of 3D-channel devices is largely dependent on MOS interface which has kinds of surface orientations. Therefore, understanding the interface state density (Dit) of every surface in 3D channel device, especially corners, is becoming increasingly important. We found an increase of Dit in 3D-channel fins compared with planar devices. One suppose of this result is that the corners of 3D-channel device have high-index surfaces which have higher Dit than planar devices. In this work, we investigated Dit distribution of corners of fins using fins and planar devices.

Experimental
Fins with height of 75nm and 50nm and (100)-oriented planar were respectively fabricated on silicon bulk wafers. Line structures (fin) were formed with lithography and dry-etching process. After SPM cleaning and HF treatment, a dry oxidation process (1000 °C for 30 min) was performed to form a gate oxide of 34.5 nm. A tungsten film was deposited by RF magnetron sputtering, followed by gate electrode lithography. Aluminum contacts were formed at the back contact by thermal evaporation. Finally, the sample was annealed in forming gas(N2/H2: 97/3) ambient at 420 °C for 30 minutes. (fig.1) C-V characteristics of fins and planar were measured at room temperature. Dit values for devices were determined from peaks in conductance spectra (Gp/ω) by conductance-voltage measurements, so that the energy distribution of Dit can be extracted. The cross-sectional SEM image of a line pattern in figure 1 showed the top (100) surface, the two (110) sidewalls and the junction corners between sidewalls and etching surfaces which serve as channels.

Results and Discussion
We observed higher capacitance density for 3D-channel devices than planar devices (fig.2). It was supposed that parts of oxidation thickness in 3D-channel devices became thinner due to the shape of corners. We also found that the frequency where peak of Gp/ω appeared in 3D-channel devices had a higher value at Ei than at Ei+0.2eV. Next, Dit of 3D-channel devices became higher from Ei to Ec and from Ei-0.2eV to Ev (fig.3), which is very like the distribution of (111)-oriented surface[1].

References