Master thesis

Wire-size dependent Ni silicidation for Si nanowires and a proposal for its complete suppression

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1.1 Background of This Study

Nowadays, Ultra-Large Scale Integrated circuits (ULSIs) constructed from complementally metal-oxide-semiconductor (CMOS) structures, are really indispensable components for our human society. Obviously, almost all the human activities, such as living, production, financing, telecommunication, transportation, medical care, education, entertainment, etc. cannot work without the help of the CMOS VLSI operation. Also, it should not be forgotten that CMOS semiconductor industry is one of big driving force of world economy, which is not limited to semiconductor fields but also includes many different kinds industries of materials, equipments, and software’s required for the integrated circuits. The continuous progress of CMOS technologies in terms of high-performance operation and low power consumption have been and will be very important because of the following three reasons.

At first, under the rapid progress of aging population and falling birth rate, we need to accelerate the replacement of some of the human jobs by intelligent machines – such as human type robot for elderly-care, for example. For the penetration of such intelligent robots to the daily family use, much higher intelligence and much lower power consumption than those of today are required. Therefore the development of CMOS integrated circuits with much more high performance and low power consumption are indispensable.

Secondly, our society is now facing the global warming. The reduction of the CO$_2$ gas release is a critically urgent issue for the earth. Continuous progress of CMOS technologies contributes to the ‘cooling of the earth’ in two ways. One is direct contribution to the power reduction for IT (Information Technology) devices. Explosive increase of energy consumption at office and home are demanded to be suppressed by so called ‘Green IT’ procedure. This can be done by the development of
low power and high performance CMOS devices used to data centers, routers and terminals, together with the high-efficient DC power feeding technology. Another contribution of the CMOS technology is to save the total power consumption of any kinds of systems – from those for entire city transportation traffic to those for individual car operation – by the optimum power saving control of the operation by intelligent CMOS processors.

Thirdly, continuous progress of CMOS technology is critically important from the semiconductor industry point of view, as well as from the global economical point of view. Because of the merits in performance and power consumption from 65 to 45 nm node logic devices, and because of the high-density or cost merit from 16 to 64 Gbit flash memories, LSI products are sold well in the market every 2 or 3 years to replace the products of previous generations. In case if there is no more progress in the CMOS technologies, semiconductor industry will face a disaster, and hence, the world economy will be in a crisis.

1.2 CMOS ultimate scaling

It is well known that the progress of CMOS LSI has been accomplished by the downsizing of metal-oxide-semiconductor field effect transistors (MOSFETs). In the past, there were many downsizing limits predicted already from the 0.8 micron-meter generation since 1970's. It was fortunate, however, it has been proven that those forecasts are not true by the fabrication of smaller dimension MOSFETs and confirmation of their excellent electric characteristics. However, it has been predicted by most of the engineers now, that the downsizing would reach its limit probably about the gate length of 5 nm around the year of 2020. There is less than ten years until 2020, but there is no sufficiently clear image for the world after CMOS reaches its scaling
limit.

It is expected that about 5 nm is the limit of the downsizing of the gate length, because there are four main reasons; A) Difficulty in off-current suppression, B) Difficulty in the on-current increase, C) Difficulty in the increase of MOSFETs speed, D) Production and development cost increase.

**A. Difficulty in off-current suppression**

With decrease in gate length, off-current – the subthreshold and direct-tunneling leakage currents between source and drain – becomes significant at the gate length of 5~3 nm. From the consideration of the integration of huge number of MOSFETs in a chip, and resulted huge entire off-leakage current, probably, around 5 nm could be regarded as the limit of the gate length reduction. It might be even 10 nm or 3 nm, depending on the number of MOSFET integrations. Below 3 nm, the direct-tunneling leakage current increases very significantly and it is almost impossible to suppress the off-leakage current.

**B. Difficulty in the on-current increase**

Already the conduction of the drain current enters in the semi-ballistic region and thus, no significant increase of the drain saturated current or on-current is expected by reducing the gate length below 5 nm. Also, increase in source/drain resistance of small geometry MOSFETs tends to suppress the on-current.

**C. Difficulty in the increase of MOSFETs speed**

One of the scaling merits is to reduce the gate capacitance, $C_g$, because the switching time of MOSFETs is defined by $C_gV_{dd}/I_d$, where $I_d$ is the drain on-current
and $V_{dd}$ is power voltage. However, $C_g$ will not decrease in proportion to the gate length because of gate electrode sidewall capacitance component and that of drain/source-to-gate electrode overlap. These capacitance components are very difficult to be reduced because the gate electrode thickness and source/drain areas are very difficult to be further reduced.

D. Production and development cost increase

It is expected that the structure and manufacturing process of such small dimension MOSFETs with huge number of integration on a chip becomes very complicated and the development and production cost of the CMOS LSI would become to expensive to retain the profit for the production.

E. Possible solution after that

It is not sure exactly at what gate length and exactly at what year, the downsizing of MOSFETs reach its limit, but most of the engineers are expected that it would be happen around at the gate length of 5 nm and around in the year of 2020, although it could be 10 nm in 2015 or 3 nm in 2030.

Then, what will be the world after we reached the limitation. Unfortunately, at this moment, there are no candidates among the so-called ‘beyond CMOS’ or ‘Post Si’ new devices, which are believed to really replace CMOS transistors used for the products of highly integrated circuits within 20 years. Our opinion is that we need to still continue CMOS based transistors with ‘More Moore’ approach with combining that of ‘More than Moore.’ Then, what is ‘More Moore’ approach after we reached the downsizing limit or with no more decrease in gate length? Because the number of the transistors in
a chip is limited by the power consumption, we could continue the ‘More Moore’ law for certain period by replacing current CMOS transistors by NW or nanotube MOSFETs with which the suppression of off-leakage current and increase of on-current under low voltage could be realized because of its nature such as quasi-one-dimensional conduction, multi- quantum channel per wire/tube and high-density integration of wire/tube in multi-layers. Figure 1.1 shows our roadmap for wire and tube MOSFETs after 2020.

![Roadmap for wire and tube MOSFETs](image)

**Figure 1.1** Roadmap for wire and tube.
1.3 Silicon Nanowire Field Effect Transistor

1.3.1 Structure and features

Si nanowire FET is considered as one of the promising candidates for further extending the device downsizing, owing to its gate-all-around (GAA) structure which enables better gate control capability than planar transistors [1-2]. Figures 1.2 show schematic image of Si NW FET with GAA structure. Moreover, advantage in ballistic conduction from quasi-one-dimensional (Q1D) structure can be achieved [3]. Therefore, high \( I_{\text{on}}/I_{\text{off}} \) ratio can be achieved with sufficient low power consumption. Figure 1.3 shows comparison of the requirement to the bulk Si, the ultra-thin body fully depleted (UTB FD) SOI and the double-gate (DG) MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes [4-10]. Si NW FETs have already been obtained higher \( I_{\text{on}}/I_{\text{off}} \) ratio than any planer transistors.

Si NW FET has been fabricated by several techniques including, Si Fins are patterned by lithography and etching followed by the oxidation (Figure 1.4 (a) shows Top-down method) or Methods using CVD, MBE and other processes to grow Si NW with better controllability of the size of the wire (Figure 1.4 (b) shows Bottom-up method) [11-12].

The electrical characteristics of Si NW FET are not yet completely understood and should be clarified. Fabrication guideline for the shape control of Si NW must be facilitated the interface characteristic of the insulator on it, the geometry intolerances and surface roughness created by the Top-down processing, the strain, influence the transistor characteristic (mobility and threshold). In addition, another concern on Si NW FET is the increase in parasitic resistance at source and drain region, which eventually reduces the on-state current.
Figures 1.2 Schematics of Si NW FET with GAA structure.

Figure 1.3 Comparison of the requirement to the bulk Si, UTB FD SOI, and DG MOSFET in ITRS2008 with previously reported data on Si NW FET fabricated using CMOS compatible processes.
1.3.2 The reason for the silicidation of source and drain regions

One of the concerns is the degradation in the performance of Si NW FETs due to parasitic resistances located at source and drain (S/D) contact [13]. To effectively reduce the S/D resistance, Ni silicide technology has been investigated intensively [11,14-16].

In MOSFET fabrication, silicide often has been used for the materials of source/drain regions and gate electrodes. There are many kinds of metals (Ni, Ti, Co, Mo, W, Pt and so on…) for silicides. Especially, Ni-, Co-, and Ti- silicides with low resistivity have been studied for a long time. In addition to its relatively low resistivity, less contaminated interface can be obtained, resulting in the suppression of the variability. Though TiSi$_2$ was used in sub-micron era, it has relatively large sheet resistance when the line width becomes thin. Therefore, Ni and Co-silicides are used in 100 nm- or smaller generations. Although CoSi$_2$ has very good electrical properties, its high Si consumption and junction spiking problems limit its application to deep sub-micrometer devices [17]. Therefore, Ni is a promised material of metal-silicide, because of its relatively low resistivity (typically 10.5 $\mu\Omega$ cm), relatively low
temperature and relatively small Si consumption during the formation for application to nano-scale structure [18-22]. The study on Ni silicide started to become an active research area in the 1970’s and the silicide technology in MOSFET fabrication process since 1980's [23-25].

1.4 Nickel silicidation for Si nanowire

1.4.1 Ni silicidation in Si-Ni binary system

Ni silicide is formed at relatively low temperature with relatively small Si consumption during the reaction for the application to nano-electronic devices. Moreover, Ni silicide has low resistivity, in particular the value of NiSi is as low as 10.5-18 $\mu\Omega\text{cm}$. Therefore, this material formation has been investigated intensively and its complex phases have been reported. Table 1.1 is previously reported fundamental data of Ni silicide formation on bulk Si [18,26-27]. And, Figs. 1.5 [28] and 1.6 [29] show the reaction temperature dependent Ni silicide phase which is mainly appeared in bulk Si case.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Resistivity ($\mu\Omega\cdot \text{cm}$)</th>
<th>Crystal structure</th>
<th>Density (g/cm$^3$)</th>
<th>$T_{\text{silicide}} / T_{\text{Ni}}$</th>
<th>Si consumption / $T_{\text{Ni}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ni</td>
<td>7-10</td>
<td>Cubic</td>
<td>8.91</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Ni$_3$Si</td>
<td>80-90</td>
<td>Cubic</td>
<td>7.87</td>
<td>1.31</td>
<td>0.61</td>
</tr>
<tr>
<td>Ni$<em>3$Si$</em>{12}$</td>
<td>90-150</td>
<td>Hexagonal</td>
<td>7.56</td>
<td>1.40</td>
<td>0.71</td>
</tr>
<tr>
<td>Ni$_2$Si</td>
<td>24-30</td>
<td>Orthorhombic</td>
<td>7.51</td>
<td>1.47</td>
<td>0.91</td>
</tr>
<tr>
<td>Ni$_3$Si$_2$</td>
<td>60-70</td>
<td>Orthorhombic</td>
<td>6.71</td>
<td>1.75</td>
<td>1.22</td>
</tr>
<tr>
<td>NiSi</td>
<td>10.5-18</td>
<td>Orthorhombic</td>
<td>5.97</td>
<td>2.20</td>
<td>1.83</td>
</tr>
<tr>
<td>NiSi$_2$</td>
<td>34-50</td>
<td>Cubic</td>
<td>4.80</td>
<td>3.61</td>
<td>3.66</td>
</tr>
<tr>
<td>Si</td>
<td>Dopant dependent</td>
<td>Cubic</td>
<td>2.33</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Table 1.1 Fundamental data of Ni silicide on bulk Si.
Figures 1.5 Silicidation temperature dependent sheet resistances and the appeared Ni silicide phase on bulk Si [28]. Deposited Ni thickness is 12 nm.

Figures 1.6 Schematic of silicidation temperature dependent mainly appeared Ni silicide phase on bulk Si [29].
1.4.2 Lateral growth of Ni silicide for Si nanowires

In partial or selective Ni silicidation for Si NWs, excessive lateral growth of Ni silicide into NWs has been reported [30-31]. Figures 1.7 show a schematic view of the silicidation of Si nanowire. During the silicidation, not only the Si portion on which Ni is directly deposited, but the edge of the NW covered with SiO$_2$ are silicided. We refer this silicidation of NW edge covered with SiO$_2$ ‘lateral growth of silicide’ in this thesis. Figures 1.8 show a SEM and a TEM image of the lateral growth of Ni silicide for NW. The NW with a diameter of 30 nm was covered with a SiO$_2$ with thickness of 50 nm in this case. In SEM image, a brighter contrast of the NW near the oxide edge indicates the formation of Ni silicide in this region. The figure on the right hand side shows the plane TEM image of the formed Ni silicide in the NW. In TEM image, Ni silicide corresponds to a darker portion, and this figure also indicates the lateral growth of Ni silicide into the NW. Here, it can be confirmed that there is no volume expansion due to the incorporation of Ni in the Si NW and Ni silicide and Si NW are smoothly connected. When it comes to its influence on the NW transistor characteristics, this lateral growth phenomenon may lead to junction leakage of S/D as well as uncontrollable effective channel length modulation.

In order to reduce the excessive lateral growth, some measures have been investigated in this laboratory: the 2-step annealing method [31] and the nitrogen incorporation method [32]. The results of suppression which have been achieved from the two methods are indicated in Figs. 1.9 and 1.10. Although it has been revealed that these methods are effective to suppress the lateral growth of silicide, there still exists the lateral growth as long as 50nm. In addition to that, the growth mechanism has not been understood yet.
Figure 1.7 Schematic figures of lateral growth of Ni silicide for SiO₂-covered NW structure.

Figure 1.8 Over view SEM and TEM images of lateral growth of Ni Silicide for SiO₂-covered NW.
Figure 1.9 Schematic figure of 2-step annealing and suppression of growth length of Ni silicide by 2-step annealing.


Figure 1.10 Suppression of growth length of Ni silicide by using Ni with N₂ incorporation.
1.5 Purpose of this thesis

Si NW FETs have been expected as future high performance devices. One of the concerns is the degradation in the performance due to parasitic resistances located at S/D contact. To effectively reduce the S/D parasitic resistance, Ni silicide technology has been investigated intensively. However, excessive lateral growth of Ni silicide into Si NW has been reported and the lateral growth has to be suppressed and controlled. By 2-step annealing and N₂ incorporation into Ni films, the growth with length of 50 nm or more remained and controllability was not sufficient. The 50 nm lateral growth is long enough to lead to the short circuit of S/D for sub-100 nm NW FETs.

Therefore, in this work, the physical insight of the lateral growth of Ni silicide for NW structures was investigated with respect to the influence of SiO₂ cover on the nano-structure. For that purpose, the lateral growth for SiO₂-covered Si NW structure with width ranging from sub-10 nm to 50 nm was investigated compared to bare Si NW (Fin) structure. And, the dependence of the lateral growth on wire width and annealing conditions were studied intensively. From the conclusion that the lateral growth of Ni silicide is governed by the Ni diffusion into the structure, a new process concept in which the formation of Ni silicide is formed without Ni diffusion, is proposed and confirmed its usefulness.
References


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Fabrication and Characterization Method

2.1 Experimental procedure

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2.2 Measurement methods

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2.2.2 Transmission Electron Microscope (TEM)
2.1 Experimental procedure

Figure 2.1 shows main experimental procedure of Ni silicidation for Si Fin and NW structures. The following subsections explain in detail the process and used equipments.

![Figure 2.1 Process flow of Ni silicidation for Si Fin and NW structures.](image)

2.1.1 Fabrication of Fin-structures substrate

Narrow Si Fin-structures were fabricated on a 30-nm-thick Silicon-on-insulator (SOI) wafer with ranging from 15 to 60 nm by dry etching. The direction of the Fin structures was aligned to <110>.
2.1.2 Substrate cleaning process

At first, the experiments using high quality thin films require ultra clean surface of Si Fin structures without particle contamination, metal contamination, organic contamination, ionic contamination, water absorption, native oxide and atomic scale roughness.

One of the most important chemicals used in Si substrate cleaning is DI (de-ionized) water. DI water is highly purified and filtered to remove all traces of ionic, particulate, and bacterial contamination. The theoretical resistivity of pure water is 18.25 MΩ·cm at 25°C. Ultra-pure water (UPW) system used in this study provided UPW of more than 18.2 MΩ·cm at resistivity, fewer than 1 colony of bacteria per milliliter and fewer than 1 particle per milliliter.

In this study, the Si Fin-structures substrate was cleaned on a basis of RCA cleaning process, which was proposed by W. Kern et al. But some steps were reduced. The first step, which use a solution of sulfuric acid (H₂SO₄) and hydrogen peroxide (H₂O₂) (H₂SO₄:H₂O₂=4:1), was performed to remove any organic material and metallic impurities. After dipping in the chemicals to clean the substrate, the clean wafer was dipped in DI water to rinse away the chemicals. The process dipping the wafer in DI water after dipping the wafer in chemicals with each cycle is important. Then, the native or chemical oxide was removed by 1% diluted hydrofluoric acid (HF). Finally, the cleaned Fin substrate was loaded to chamber to deposit as soon as it was dried by air gun.

2.1.3 Thermal oxidation process

The SiO₂-covered Si NW structures were fabricated by thermal oxidation of the Si Fin-structure substrate. Thermal oxidation is accomplished by using an oxidation
furnace (or diffusion furnace, since oxidation is basically a diffusion process involving oxidant species), which provides the heat needed to elevate the oxidizing ambient temperature. A furnace typically consists of: 1) a cabinet; 2) a heating system; 3) a temperature measurement and control system; 4) fused quartz process tubes where the wafers undergo oxidation; 5) a system which transfers process gases into and out of the process tubes; and 6) a loading station used for loading (or unloading) wafers into (or from) the process tubes.

The heating system usually consists of several heating coils that control the temperature of the furnace tubes. The wafers are placed in quartz glassware known as boats, which are supported by fused silica paddles inside the process tube. A boat can support many wafers. The oxidizing agent (oxygen or steam) then enters the process tube through its source end, subsequently diffusing to the wafers surface where the oxidation occurs. In this study, the dry oxidation furnace shown in Fig. 2.2 was used.

Depending on oxidant species used (O\textsubscript{2} or H\textsubscript{2}O), the thermal oxidation of SiO\textsubscript{2} may either be in the form of dry oxidation (wherein the oxidant is O\textsubscript{2}) or wet oxidation (wherein the oxidant is H\textsubscript{2}O). The reactions for dry and wet oxidation are governed by the following equations:

1) for dry oxidation:  \[ \text{Si (solid)} + \text{O}_2 \text{(vapor)} \rightarrow \text{SiO}_2 \text{(solid)}; \]

2) for wet oxidation:  \[ \text{Si (solid)} + 2\text{H}_2\text{O} \text{(vapor)} \rightarrow \text{SiO}_2 \text{(solid)} + 2\text{H}_2 \text{(vapor)}. \]

Figure 2.3 shows the dry thermal oxidation rate using bulk p-Si substrate and SOI substrate which has 51-nm-thick SOI, 137.8-nm-thick BOX layer. The figure indicate that SiO\textsubscript{2} thickness increases and residual SOI thickness decreases as increasing oxidation time.
In this study, the thermal oxidation was performed by dry process at 1000 °C for 20 min, which results in formations of Si NWs covered by about 20-nm-thick SiO₂ with diameters ranging from 5 to 50 nm.

**Figure 2.2** Oxidation furnace.

**Figure 2.3** Rate of dry oxidation.
2.1.4 Photolithography process

The process flow and a photo of the photolithography apparatus used throughout this study are shown in Fig. 2.4. The apparatus is MJB4 of Karl Süss contact-type mask aligner. At first, the substrates were coated with positive type photoresists by spin-coating method. The thicker photoresist called S1818 and thinner one called S1818 were used to selectively deposit Ni films on Fin-structures substrate and partially remove SiO₂ coverage from SiO₂-covered NWs substrate, respectively. Secondly, the coated photoresists were baked at 115 °C for over 5 min by using electrical hotplate. Then, spin-coated photoresist layers were exposed through e-beam patterned hard-mask with high-intensity ultraviolet (UV) light with the wavelength of 405 nm. The exposure duration was set to 1.5 sec and 3.8 sec for thinner photoresist and thicker one, respectively. Finally, exposed wafers were developed using the specified tetra-methyl-ammonium-hydroxide (TMAH) developer called NMD-3 (Tokyo Ohka Co. Ltd.). The wafers were dipped into the solvent for 1~2 minute. In the case of SiO₂-covered NW structures, the SiO₂ coverage was partially removed by dipping into buffered HF (BHF) in order to expose Si core regions.
2.1.5 RF magnetron-sputtering process

After cleaning wafers or selectively protecting by photoresist and additional partially etching by chemicals, film structures such as M/Ni/Si, Ni/M/Si (Here M is a metal additive layer) and Ni/Si were formed by an ultra-high-vacuum (UHV) sputtering system.

Sputtering is one of the vacuum processes used to deposit ultra thin films on substrates. A high voltage across a low-pressure gas (usually argon at about 5 mTorr) is applied to create a “plasma,” which consists of electrons and gas ions in a high-energy state. Then the energized plasma ions strike the “target,” composed of the desired coating material, and cause atoms of the target to be ejected with enough energy to travel to the substrate surface.

In this study, Ni films with thickness of 20, 80, and 100 nm were deposited on Si Fin-structures and SiO$_2$-covered Si NWs substrates by RF magnetron-sputtering in
argon ambient. As RF magnetron-sputtering system, UHV Multi Target Sputtering System ES-350SU shown in Fig. 2.5 was used and its schematic structure is shown in Fig. 2.6. The rotating function of target positioning is developed, enabling this system to sputter 5 targets by means of DC & RF power sources by using a single electrode. The substrate holder can be rotated and its speed can be selected. For other details, Table 2.1 is attached for reference.

In the case of Si Fin-structures substrate, after depositing Ni films on the substrate, lift-off process was performed. The lift-off is the process which selectively removes deposited Ni films by photolithography in advance of Ni deposition and ultrasonic cleaning of left photoresist after Ni deposition.

![Figure 2.5](image)

**Figure 2.5** Photo of UHV Multi Target Sputtering System ES-350SU.
Figure 2.6 Schematic internal structure of UHV sputtering system.

Table 2.1 Specifications for UHV Multi Target Sputtering System ES-350S.

<table>
<thead>
<tr>
<th>Growth chamber</th>
<th>1. Ultimate pressure</th>
<th>$1.5 \times 10^8$Pa</th>
</tr>
</thead>
<tbody>
<tr>
<td>2. Substrate size</td>
<td>2 inch in diameter</td>
<td></td>
</tr>
<tr>
<td>3. Heating temperature</td>
<td>600°C</td>
<td></td>
</tr>
<tr>
<td>4. Heater type</td>
<td>Lamp type heater</td>
<td></td>
</tr>
<tr>
<td>5. Target</td>
<td>3 inch x 5 pieces (motor-driven)</td>
<td></td>
</tr>
<tr>
<td>Load lock chamber</td>
<td>6. Vacuum pumps</td>
<td>TMP 500L/sec and RP 250L/min</td>
</tr>
<tr>
<td></td>
<td>7. Ultimate pressure</td>
<td>$6.6 \times 10^5$Pa</td>
</tr>
<tr>
<td></td>
<td>8. Vacuum pumps</td>
<td>TMP60L/sec and RP90L/min</td>
</tr>
<tr>
<td></td>
<td>9. Substrate holder with cooling function / Substrate holder with heating function / Cleaning function / Radical beam source</td>
<td></td>
</tr>
</tbody>
</table>
2.1.6 Thermal rapid annealing process

After formation of thin films of Ni/Si, Ni/M/Si, or M/Ni/Si by UHV sputtering system, these structures were transferred to annealing furnace to perform thermal process. The thermal process leads to the reaction between Ni and Si, or among Ni, M, and Si.

In this study, the thermal rapid annealing (RTA) process was performed for Ni films /Si Fin- or NW structures and led to Ni silicidation for Fin and NW structures. The silicidation was performed by using infrared image furnace in nitrogen ambient. The annealing temperature and time ware varied from 450 to 600 °C and from 30 sec to 15 min, respectively.

The equipment for annealing used in this study is QHC-P610CP (ULVAC RIKO Co. Ltd). Figure 2.7 is the photo of the infrared image furnace, whose schematic illustration was shown in Fig. 2.8. The annealing was performed by six infrared lamps surrounding the sample stage made of carbon coated by SiC. The heating temperature was controlled by thermocouple feedback.

In the case of SiO₂-covered NW structures, after the silicidation, the unreacted Ni was removed by dipping the substrate in a heated mixed solution of H₂SO₄ and H₂O₂ at 150 °C for over 15 min.
Figure 2.7 Photo of infrared image furnace.

Figure 2.8 Schematic internal configuration of infrared image furnace.
2.2 Measurement Methods

2.2.1 Scanning Electron Microscope (SEM)

The formed Ni silicides in Fin and NW structures were observed by scanning electron microscope (SEM). The observation was mainly performed by overhead viewing.

Figure 2.9 shows Scanning Electron Microscope (SEM) system which is S-4800 (HITACHI High-Technologies Corporation) and its schematic internal configuration is shown in Fig. 2.10. The “Virtual Source” at the top represents the electron gun, producing a stream of monochromatic electrons. The stream is condensed by the first condenser lens. This lens is used to both form the beam and limit the amount of current in the beam. It works in conjunction with the condenser aperture to eliminate the high-angle electrons into a thin, tight, coherent beam. A user selectable objective aperture further eliminates high-angle electrons from the beam. A set of coils then scan or sweep the beam in a grid fashion and make the beam dwell on points for a period of time determined by the scan speed. The final lens, the Objective, focuses the scanning beam onto the part of the specimen desired. When the beam strikes the sample, interactions occur inside the sample and are detected with various instruments, interactions. Before the beam moves to its next dwell point these instruments count the number of interactions and display a pixel on a display whose intensity is determined by this number. This process is repeated until the grid scan is finished and then repeated, the entire pattern can be scanned 30 times per second.
Figure 2.9 Photograph of SEM equipment.

Figure 2.10 Schematic view of internal configuration of SEM equipment.
2.2.2 Transmission Electron Microscope (TEM)

Cross-section transmission electron microscope (TEM) image is the most important analysis method to characterize physical thickness, film quality and interface condition.

Figure 2.11 shows internal configuration of TEM system. First, focus lenses change convergent angle and beam size. The electron beam transmitted through the thin fragment sample passes objective lens and projective lens, and finally projected on fluorescent screen. Recording of the image is performed by direct exposure on exclusive films for electron microscope use located below the fluorescent screen.

Electron interacts strongly with lattice by scattering. Thus, sample has to be very thin fragment. Required thickness of the sample is 5 to 500 nm at 100 kV. TEM images are obtained in very high resolution such as 0.2 to 0.3 nm at 200 kV.

![Schematic internal configuration of TEM equipment.](image)

**Figure 2.11** Schematic internal configuration of TEM equipment.
Chapter 3
Wire-Size Dependent Ni Silicidation for Si Fin and Nanowire Structures

3.1 Result and Discussion

3.1.1 SEM images of Ni silicides formed in Si Fin and NW structures

3.1.2 Wire-size dependent lateral growth of Ni silicide

3.1.3 RTA time dependent lateral growth of Ni silicide

3.1.4 RTA temperature dependent lateral growth of Ni silicide

3.1.5 Consideration for the mechanisms of Ni atoms diffusion

3.2 Conclusion of this section

Reference
3.1 Results and discussion

3.1.1 SEM images of Ni silicides formed in Fin and NW structures

Figures 3.1 show SEM images of Ni silicides formed in (a) Si Fin and (b) SiO₂-covered Si NW structures. Ni films with a thickness of 80nm were deposited on the substrates and RTA was performed at 500 °C for 3 min. The width of the structures is 20 nm for both cases. The bright regions and the dark regions correspond to Ni silicide and Si, respectively. Therefore, it was easy to measure the lateral growth length in both structures. Figure 3.1(a) shows that the lateral growth length of Ni silicide in Si Fin structures varied from 1062 nm to 1396 nm even among neighboring ones. On the other hand, Fig. 3.1(b) shows that the lateral growth into SiO₂-covered NW structures varied from 432 nm to 478 nm among neighboring ones. Therefore, Figs 1 indicate that the growth length in SiO₂-covered NWs is much shorter than that in Fins and the uniformity in the lateral growth in SiO₂-covered structures is much better than that in Fins case.
Figures 3.1 Over view SEM images of laterally formed Ni silicides in (a) Si Fin and (b) SiO$_2$-covered Si NW structures.
3.1.2 Wire-size dependent lateral growth of Ni silicide

The width dependent lateral growth of Ni silicide in Si Fin and SiO$_2$-covered Si NW structures was measured as shown in Figs. 3.2 and 3.3. Deposited Ni films thickness was set to be 20 nm and 80 nm. RTA was performed at 500 °C for 3 min in both cases. For both cases, the growth length in Fin structures are scattered for whole width region, but good uniformity of the growth length is clearly observed in SiO$_2$-covered NW structure. And, SiO$_2$-covered NW structures show decreasing trend of the lateral growth for narrower NW width.

However, the major difference of the growth length between each Fin structure was observed. It may be considered that the supply Ni is not sufficient for the Fin structure case of 20-nm-thick Ni. Meanwhile, the lateral growth length in SiO$_2$-covered NWs is almost the same for 20nm and 80nm Ni cases. It is assumed that a mechanism other than Ni supply limits the growth in case of SiO$_2$-covered NWs. Actually, it was clearly observed that the lateral growth length in Fins is larger than the case of SiO$_2$-covered NWs in Fig.3.3. This is in agreement with the previous report showing the difference of lateral growth of Ni silicide for 50 nm wide NWs with or without SiO$_2$ coverage in ref. 1. Figure 3.3 reveals that this trend is observed for NW width from 50 nm to even less than 10 nm. Interestingly, the growth length in SiO$_2$-covered NWs with the width less than 8 nm is very small and clear decreasing trend by the reduction of the width. Regarding the width dependency of the growth length, although change of the growth length is little, SiO$_2$-covered NWs have decreasing trend for narrower NW width as is the case with Fig. 3.2. On the other hand, one may observe a slight increasing trend for narrower Fin width. This dependency is in agreement with the previous report showing a wide diameter dependent lateral growth of Ni silicide in refs. 2-4.
Figure 3.2 Width dependent growth length of Ni silicide for the case of deposited Ni with thickness of 20 nm.

Figure 3.3 Width dependent growth length of Ni silicide for the case of deposited Ni with thickness of 80 nm.
3.1.3 RTA temperature dependent lateral growth of Ni silicide

In order to circumstantially investigate the difference of width dependent the lateral growth in Fin and SiO₂-covered NW structures, the dependence on the annealing temperature was investigated. The deposited Ni film thickness was set to be 80 nm for all samples in this section. Figure 3.4 shows the growth length of Ni silicide as a function of the width of the SiO₂-covered NW. Annealing temperature is taken as a parameter in this figure. RTA duration was set to be 3 min. Figure 3.4 shows the suppression of the growth length for the lower reaction temperature, however, no change of the growth trend and the good uniformity of the growth length were observed.

Figure 3.5 shows the growth length of Ni silicide as a function of the width of the Si Fins. Annealing temperature is taken as a parameter also in this figure and RTA duration was also set to be 3 min. Figure 3.5 also indicates no change of the growth trend and the scattering in whole width range by the change of reaction temperature. Then, in order to characterize the dependence of the lateral growth on reaction temperature, an Arrhenius plot was derived from Fig. 3.5 and shown in Fig. 3.6. The values for Fins with width of 18-22 nm were plotted in Fig. 3.6. Activation energy $E_a$ can be derived from the Arrhenius relationship expressed as follows:

$$ k = A \exp \left( -\frac{E_a}{k_BT} \right) $$

(1)

where $k$ is rate constant, $A$ is temperature independent constant, $k_B$ is the Boltzmann constant, and $T$ is reaction temperature. The activation energy of the lateral growth of Ni silicide for Fin structures in this study is obtained as 0.93 eV from
Fig. 3.6. This value is smaller than the reported values of 1.5 eV and 1.4 eV for Ni$_2$Si and NiSi in bulk Si [5], and the obtained value of 1.4 eV for SiO$_2$-covered Si NW structures from previous work in this laboratory [6].

**Figure 3.4** Annealing temperature dependent growth length of Ni silicide for the case of SiO$_2$-covered NW structures.
Figure 3.5 Annealing temperature dependent growth length of Ni silicide for the case of Fin structures.

Figure 3.6 Arrhenius plot for the lateral growth of Ni silicide in Fin structures
3.1.4 RTA time dependent lateral growth of Ni silicide

In order to investigate the kinetics of the lateral growth of Ni silicide in Fin and SiO₂-covered NW structures and to understand the difference between two cases, the dependence on the annealing time was measured as shown in Fig 3.7. The RTA condition was set to be at 500 °C for 30 sec, 3 min, and 10 min. In Fig. 3.7, SiO₂-covered NWs with width of 8-12 nm and Fins with width of 18-22 nm are plotted. These measured width regions were determined because these regions are believed to represent the typical situation of both cases. The growth length of Ni silicide increased for longer annealing time, showing a linear relationship with the square root of the annealing time for both cases. This relationship is expressed as the diffusion law as follows:

\[ L \propto A\sqrt{t} \]  

where \( L \) is the growth length, \( A \) is constant, and \( t \) is reaction time i.e. annealing time. This result indicates that the lateral growth with Fin structure in this study is controlled by Ni atoms diffusion and may be same as in the case of SiO₂-covered NWs [5].

In order to clearly confirm the liner relationship of the growth length with the square root of the annealing time for SiO₂-covered NWs, the repeatability of the phenomenon was examined in other experiment, where deposited Ni film thickness was set to be 100 nm. The result is shown in Fig.3.8. The RTA temperature was 500°C and the RTA duration was varied from 30 sec, 3 min, 7 min, 10 min to 15 min. Since the clear liner relationship with the square root of time is also shown in Fig. 3.5, it is suggested that the lateral growth with SiO₂-covered NWs is also controlled by Ni atoms diffusion.
Fitted curves to calculate diffusion coefficients of Ni were drawn by least square method in Fig. 3.4 and Fig. 3.5. The diffusion coefficients $D$ were derived from following expression,

$$D = \frac{L^2}{t}$$  \hspace{1cm} (3)

where $L$ is the growth length, $t$ is reaction time. The estimated diffusion coefficients from these fitted curves are $6.6 \times 10^{-11}$ cm$^2$/s for Fin structure, $1.6 \times 10^{-11}$ and $1.2 \times 10^{-11}$ cm$^2$/s for SiO$_2$-covered NW structures shown in Fig. 3.4 and Fig. 3.5, respectively. For SiO$_2$-covered NW structures, the derived diffusion coefficients are almost the same to each other.

![Graph showing growth length vs. annealing time for different structures](image)

**Figure 3.7** Annealing time dependent growth length of Ni silicide for the case of deposited Ni with thickness of 80 nm.
3.1.5 Consideration for the mechanisms of Ni atoms diffusion

In order to investigate the reason why Fins have large scattering of the growth length, the lateral growth of Ni silicide for Fin-structures with large width ranging from 140 nm to 2000 nm (2.0 μm) was observed and shown in Fig. 3.9. Ni silicidation was performed at 500 °C for 3 min with deposited 80-nm-thick Ni film. The Fins can be considered to be much the same as SOI structures. Figures 3.9 indicate that the rough Ni silicide/Si interfaces and large difference of the growth length in narrow and wide Fin-structures. It is suggested that this large difference revealed as the scattering of growth length for narrow Fin-structures in Figs.3.3 as well as 3.5.

Figures 3.9 also show the contrast changes of Ni silicide at middle of the growth. These can be considered as the continuous change of Ni silicide phase for the growth direction as shown in Fig. 3.10 and previously reported in ref. 1,4,7-9. In lateral growth system of Ni silicide, there are some reports indicating the complex kinetics
and phases of the lateral growth from Si-Ni binary system. As examples, Fig. 3.11 show result of X-ray analysis of the continuous phase change in 50-nm-thick Si case [8], and Fig. 3.12 shows TEM observation of the phase in Si NW case with diameter of 50 nm with or without SiO₂ coverage [1]. Moreover, Fig. 3.10 show SEM image and the result from energy dispersive X-ray spectroscopy (EDS, EDX) analysis for the lateral growth in Fin (SOI) with width of 10.0 µm. Figures 3.10 and the previous reports indicated that the phase of silicide which is close to Ni supply source is Ni-rich, in contrast, the phase of silicide which is close to Ni silicide/Si interface is Si-rich. It is expected that this phenomenon is occurred for narrow Fin and SiO₂-covered NW structures.

Using the experimental results mentioned above, especially the diffusion coefficients, the main mechanisms can be discussed as follows; According to a model of surface diffusion of Ni atoms for NWs without thick SiO₂ coverage, which Katsman et al. considered in ref. 3, the diffusion coefficient of Ni in Fins, \( D \) can be transformed to surface diffusion coefficient which is normalized for NW radius using the following equation:

\[
D = 4 \frac{\delta}{R} D_{sy}
\]

where, \( R \) is NW radius, \( \delta \) and \( D_{sy} \) are assumed thickness of high-diffusivity surface layer and effective diffusion coefficient which is normalized for NW radius, respectively. In this case, the surface layer thickness is assumed to be \( \delta = 0.5 \) nm. The surface diffusion is considered that the high-diffusivity surface layer is main path of Ni atoms in this model. From the diffusion coefficient for Fins derived from Eq. (3), the
normalized diffusion coefficients is obtained as $D_{sy} = 3.3 \times 10^{-10} \text{ cm}^2/\text{s}$. This result of Fins is comparable to the reported values for the surface diffusion coefficient ranging from $D_{sy} = 5 \times 10^{-11} \text{ cm}^2/\text{s}$ to $3 \times 10^{-10} \text{ cm}^2/\text{s}$ in ref. 3. Provided that the difference in diffusion mechanism of Ni atoms is caused by structures with or without SiO$_2$ coverage, the reason for the difference can be proposed as follows: For Fin structures, the diffusion of Ni atoms at surface of Si Fins can mainly appear. On the other hand, in the case of SiO$_2$-covered NW structures, thick SiO$_2$ layer covered the surface of Si core, retarding the surface diffusion. The main diffusion path for this case could not be identified, however first of all, the diffusion at Si/SiO$_2$ interface can be considered. The change of the main diffusion mechanism from surface diffusion to grain boundary (GB) diffusion and volume diffusion which have lower diffusion coefficients by the effect of thick SiO$_2$ coverage may be also considered. The effect of compressive stress by SiO$_2$ coverage [10-12] could not be eliminated, however anyway further investigations are necessary for the identification of the main diffusion mechanism for the SiO$_2$-covered NW case.
Figures 3.9 Over view SEM images of lateral growth of Ni silicide for Fins with large width ranging from 140 nm to 2.0 \( \mu \text{m} \) (SOI).
Figures 3.10 (a) Over view SEM image and (b) result of EDS analysis for the lateral growth of Ni silicide in Fin (SOI) with width of 10.0 µm.
Figure 3.11 Composition profile and schematics of lateral growth of Ni silicide in 50-nm-thick Si on Al₂O₃. Deposited Ni thickness is 120 nm [8].

Figures 3.12 Over view TEM images of lateral growth of Ni silicide into Si NWs (a) without and (b) with SiO₂ coverage [1].
3.2 Conclusion of this section

In this section, in order to investigate the physical insight of the lateral growth of Ni silicide for NW structures with respect to the influence of SiO₂ cover on the nano-structure, dependence of the lateral growth of Ni silicide on wire-size and annealing conditions for Fin and SiO₂-covered NW structures has been studied and discussed.

At first, the dependence of the lateral growth of Ni silicide on Fin and SiO₂-covered NW width was observed. The lateral growth with large length for Fin structures has been suppressed dramatically with SiO₂ coverage. And, the good uniformity of the growth length is also observed for the entire range of SiO₂-covered NW width. Regarding dependence of the lateral growth on wire width, it may be observed a slight increasing trend for narrower Fin width. On the other hand, the dependence with decreasing trend for narrower SiO₂-covered NW width is confirmed.

Secondly, the annealing temperature dependent lateral growths have been summarized. The lateral growths were increased without trend change for wire width for higher temperature in both NW cases. In case of Fin structures, activation energy was derived from Arrhenius plot and obtained as 0.93 eV. This value was less than the reported values for Ni silicides on bulk Si and the value which has been obtained in previous work in this laboratory for SiO₂-covered NW structure. This result indicates the lateral growth of Ni silicide for Si Fin structure is more active compared to bulk Si and SiO₂-covered NW cases.

Thirdly, the annealing time dependence of the lateral growth has been investigated. It was revealed that the lateral growth is controlled by Ni atoms diffusion in both NW cases, but the difference between diffusion coefficients was also observed for each structure. Moreover, it is suggested that surface diffusion with diffusion coefficient of
6.6 \times 10^{-11} \text{ cm}^2/\text{s} is mainly appeared for Fin structures, while the SiO$_2$ coverage retards the diffusion or changes the main diffusion mechanism, resulting the smaller diffusion coefficients of $1.6 \times 10^{-11}$ and $1.2 \times 10^{-11}$ cm$^2$/s for SiO$_2$-covered NW structure is obtained.

Finally, the continuous phase changes of the laterally grown Ni silicide for the growth direction were confirmed for wider Fin structures. And, it can be assumed that the complex and partial phase change is also occurred in cases of narrow Fin and SiO$_2$-covered NW structures. As a result, it is suggested that the suppression of Ni diffusion and the resulting Si consumption is essentially important to suppress the lateral growth of Ni silicide in SiO$_2$-covered NW structures.

**Reference**

Chapter 4

A Proposal for Complete Suppression of Ni silicide lateral growth into Si nanowires

4.1 Introduction

4.1.1 Concept of using NiSi$_2$ source

4.1.2 Experiment

4.2 Result and Discussion

4.2.1 SEM and TEM images of Ni silicides formed in Si Fin and NW structures using NiSi$_2$ source

4.2.2 Consideration for mechanism of the complete suppression

4.3 Conclusion of this section

Reference
4.1 Introduction

4.1.1 Concept of using NiSi₂ source

The well known model of Ni silicidation with the conventional Ni source on Si substrate [1-2] and the model with NiSi₂ source proposed in this study are shown in Fig. 4.1. In the case of using the conventional Ni source, the deposited films react with Si substrate to form Ni silicide by annealing. During the silicidation, Ni atoms mainly diffuse from the films into the substrate, resulting in the consumption of Si substrate. Therefore, the consumption causes the full silicidation and excessive lateral growth for one- and two-dimension structures such as thin Si NW and SOI.

On the other hand, in case of NiSi₂ source, it is considered that the deposited films including Ni and Si atoms form Ni silicide by annealing because Ni and Si is already mixed in the films. Therefore, it is expected that Ni silicide/Si interface without the consumption of Si substrate can be formed in this method. And, this formation method is very convenient, because the NiSi₂, whose Ni-Si ratio is precisely controlled, is deposited from a composite NiSi₂ target by sputtering.

NiSi₂ has similar crystal structure and lattice constant to Si. NiSi₂ and Si are both cubic structure and have the lattice constants of 5.416 Å and 5.4309 Å, respectively [3,4]. And, NiSi₂ is the most thermodynamically stable phase with the highest Si ratio among all Ni silicides.
4.2.1 Experiment

NiSi$_2$ films with thickness of 20 nm were deposited on Fin and SiO$_2$-covered NW structures. The films were deposited by RF magnetron-sputtering with composite NiSi$_2$ target and lift-off technique was used to etch a part of the film selectively as in the case of Ni source mentioned above. Ni silicidation was performed at 500 °C for 10 min.
4.2 Result and Discussion

4.2.1 SEM and TEM images of Ni silicides formed on Fin and NW structures using NiSi\textsubscript{2} source

Figures 4.2 show SEM images of Ni silicides formed on Si Fin structures by using (a) Ni source and (b) NiSi\textsubscript{2} source. The width of Fins is 30 nm for both cases. Figure 4.2(a) shows the lateral growth of Ni silicide occurs and the length varied from about 1300 to 1600 nm in case of Ni source. On the other hand, Fig. 4.2(b) shows complete suppression of the lateral growth of Ni silicide in case of NiSi\textsubscript{2} source.

Figures 4.3 and 4.4 show SEM and TEM images of Ni silicidation for SiO\textsubscript{2}-covered Si NW structures. Fig. 4.3(a) is SEM image and Fig. 4.3(b) is cross sectional TEM image in the case of Ni source. On the other hand, Figs. 4.4(a) and (b) show the SEM and TEM images in case of NiSi\textsubscript{2} source. The cross sections observed in TEM images are indicated by lines crossing NWs in SEM images for both cases.

![SEM images of Ni silicides](image)

**Figures 4.2** SEM images of (a) laterally formed Ni silicides with Ni source and (b) complete suppression of the lateral growth of silicide in case of NiSi\textsubscript{2} source for Fin structures.
Figures 4.3 Lateral growth of Ni silicide for SiO₂-covered NW in case of Ni source.
(a) SEM image and (b) cross sectional TEM image.

Figures 4.4 Ni silicidation for SiO₂-covered NW in case of NiSi₂ source.
(a) SEM image and (b) cross sectional TEM image.
4.2.2 Consideration for mechanism of the complete suppression of the lateral growth of Ni silicide

Figure 4.5 shows cross sectional SEM images of Ni silicide/Si interfaces which were formed from 50-nm-thick Ni and NiSi$_2$ source at high temperature annealing for 1 min on Si substrates. It is indicated that the flat interfaces without consumption of Si substrate were achieved at high temperature in NiSi$_2$ case, while the rough interfaces are observed in Ni case where large Si substrate consumption occurs. Figure 4.6 shows cross sectional TEM image of Ni silicide/Si interface formed from 10-nm-thick NiSi$_2$ source on Si substrate after annealing at 500 $^\circ$C for 1 min. It is revealed that an about 1-nm-thick thin layer of epitaxially grown NiSi$_2$ was formed on Si surface at low temperature. It should be mentioned that NiSi is usually formed in this annealing condition in the conventional silicidation with Ni films [2,5-7]. And, it can be also considered the thin epitaxially grown NiSi$_2$ layer completely prevented the diffusion of Ni atoms.

Therefore, as proposed in Fig.4.1, it is confirmed that the NiSi$_2$ film deposition method is effective to completely suppress the lateral growth of silicide into Fin and NW structures, while the large growth was occurred with the conventional Ni source method. Figure 4.7 indicates the models of Ni silicidation for Fin structure with conventional Ni source and NiSi$_2$ source proposed in this study.
Figure 4.5 Cross sectional SEM images of Ni silicide/Si interfaces which were formed from 50-nm-thick Ni and NiSi$_2$ source on Si substrates.

Figure 4.6 Cross sectional TEM image of flat Ni silicide/Si interface which was formed from 10-nm-thick NiSi$_2$ source on Si substrate.
4.3 Conclusion of this section

As suppression method of the lateral growth of Ni silicide, the process, which uses the deposition of NiSi$_2$ source, instead of the conventional Ni source, was proposed. NiSi$_2$ films with thickness of 20 nm were deposited by sputtering on Fin and SiO$_2$-covered NW structures. Ni silicidation was performed at 500 °C for 10 min. The complete suppression of the lateral growth was achieved for both Fin and SiO$_2$-covered NW structures in the new method. It can be considered that the complete suppression of the lateral growth of Ni silicide for Fins and SiO$_2$-covered NWs was obtained from the direct formation of thin NiSi$_2$ layer on Si NW surfaces without Si NW consumption and the diffusion of Ni atoms from Ni silicide layer. In order to apply this method to a self-aligned silicide process of NW FETs in LSIs, further studies such as NiSi$_2$ epitaxial growth optimization as well as selective etching process of amorphous films of Ni and Si mixture to NiSi$_2$ epitaxial layers should be developed.
Reference


Chapter 5

Conclusion of This Study

5.1 Conclusion

Si nanowires field-effect-transistors (Si NW FETs) have been expected as future high performance devices and actively investigated. One of the issues is the degradation in the performance due to parasitic resistance located at source and drain (S/D) contact. To effectively reduce the S/D resistance, Ni silicide technology has been investigated intensively. However, the problem that excessive lateral growth of Ni silicide into Si NWs is occurred has been reported and the growth mechanism has been yet understood. Therefore, in this study, it has been purposed to obtain physical insight of the lateral growth and propose new suppression method with good controllability for the lateral growth. The wire-size dependent lateral growth of Ni silicide for SiO₂-covered Si NW structure with width ranging from sub-10 to 50 nm has been studied and discussed compared to the case of bare Si NW (Fin) structure.

At first, the wire-size dependent lateral growth of Ni silicide was investigated. The large lateral growth for Fin structures has been suppressed dramatically with SiO₂ coverage. And, the good uniformity of the growth length is also observed for the entire range of SiO₂-covered NW width. Regarding dependence of the lateral growth on wire width, it may be observed a slight increasing trend for narrower Fin width. On the other hand, the dependence with decreasing trend for narrower SiO₂-covered NW width is confirmed.
Secondly, dependence of the lateral growth on annealing conditions was observed. The lateral growths were increased without trend change for wire width at higher temperature in both NW cases. In case of Fin structures, activation energy was obtained as 0.93 eV from Arrhenius plot. This value was less than the previously reported values for Ni silicides on bulk Si and in SiO$_2$-covered NW structure. This result indicates the lateral growth for Si Fins is more active compared to bulk Si and SiO$_2$-covered NWs. Moreover, it was revealed that the lateral growth is controlled by Ni atoms diffusion in both NW cases from the annealing-time-dependence. And, it is suggested that surface diffusion with diffusion coefficient of $6.6 \times 10^{-11}$ cm$^2$/s is mainly appeared for Fin structures, while the SiO$_2$ coverage retards the diffusion or changes the dominant diffusion mechanism, resulting the smaller diffusion coefficients of $1.2-1.6 \times 10^{-11}$ for SiO$_2$-covered NW structure.

Thirdly, the continuous phase change of Ni silicide for the growth direction was observed for wider Fin structures. It can be assumed that the complex and partial phase change is also occurred in cases of narrow Fin and SiO$_2$-covered NW structures. As a result, it is suggested that the suppression of Ni diffusion and the resulting Si consumption is essentially important to suppress the lateral growth of Ni silicide in NW structures.

Based on theses and obtained results, as suppression method of the lateral growth of Ni silicide, the process which uses deposition of NiSi$_2$ source was proposed. The complete suppression of the lateral growth was achieved for both Fin and SiO$_2$-covered NW structures in the new method. It can be assumed that the complete suppression was obtained from the direct formation of thin NiSi$_2$ layer which prevents the diffusion of Ni into NWs on Si NW surface. In order to apply this method to a self-aligned silicide process of NW FETs, further process optimization is necessary.
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