Effect of Thin Si Insertion at Metal Gate/High-k Interface on Electrical Characteristics of MOS Device with $\text{La}_2\text{O}_3$

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Introduction of high-k Gate Dielectrics

EOT of 0.5 nm is required in the near future.

Hf-based oxides are currently in practical use.

SiO$_2$-IL would eventually limit the scaling.

High-k/Si direct contact without SiO$_2$-IL is necessary.
Reports on Direct Contact of HfO$_2$/Si

Selection of metal gate material is the key factor to achieve direct HfO$_2$/Si structure
Direct Contact of High-k/Si with La$_2$O$_3$

Advantages of La$_2$O$_3$

- High permittivity ($\varepsilon_r = 23.4$)
- Wide band-gap ($E_g = 5.6\text{eV}$)
- Direct contact with Si by forming La-silicate

500 °C, 30 min

Peak $\mu_{\text{eff}} = 312 \text{ cm}^2/\text{Vs}$
$\mu_{\text{eff}}@0.8\text{MV/cm} = 280 \text{ cm}^2/\text{Vs}$

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Fairly nice interfacial property with a peak $\mu_{\text{eff}}$ of over 300 cm$^2$/Vs has been reported.

La$_2$O$_3$ is expected to be one of the gate dielectrics for next generation devices

Remote charge scattering induced by fixed charges might degrade mobility.

Fixed charges induced by gate metal

Grain boundaries with oxygen vacancies

Formation of amorphous silicate layer by Si deposition.

Improving mobility by preventing generation of fixed charges
Experimental Procedure

**capacitor**

- n-Si Substrate
- SPM, HF-last treatment
- La$_2$O$_3$ e-beam evaporation @ 300°C under ~10$^{-6}$ Pa
- Si deposition by RF-sputtering
- W deposition by RF-sputtering
- TiN deposition by RF-sputtering
- Metal dry etching
- Post metallization annealing (PMA) with F. G. for 2 s
- Contact hole formation
- Al wiring for S/D
- Backside contact formation (Al)

**transistor**

- Source/Drain pre-formed Substrate
- La$_2$O$_3$ e-beam evaporation @ 300°C under ~10$^{-6}$ Pa
- Si deposition by RF-sputtering
- W deposition by RF-sputtering, *in-situ*
- TiN deposition by RF-sputtering
- Metal dry etching
- Post metallization annealing (PMA) with F. G. for 2 s
- Contact hole formation
- Al wiring for S/D
- Backside contact formation (Al)
Electrical characteristics of capacitors
Smaller EOT is obtained with Si inserted capacitor.
Annealing Temperature Dependence of EOT

Oxygen diffusion from gate metal might be reduced by La-silicate at metal/high-k interface.
$V_{fb}$ shift indicates reduction of positive fixed charges with Si insertion.
Electrical characteristics of transistors
The $V_{th}$ shift and suppression of EOT increase is consistent with capacitors.
Mobility Comparison

EOT=0.58 nm

EOT=0.66 nm

Effective mobility is improved with Si inserted FETs.
Fixed charges such as oxygen vacancies or metal induced defects are reduced by forming La-silicate at metal/high-k interface.
Mobility at High Electric Field

La rich-silicate is formed at La$_2$O$_3$/Si interface with Si inserted FETs.
A fairly nice $J_g$ of $\sim 10^3$ times smaller with respect to the ITRS requirement is achieved.
Conclusions

The effect of Si insertion at metal/La$_2$O$_3$ interface has been investigated.

- Smaller EOT is obtained with Si insertion possibly owing to the reduction of oxygen diffusion.
- The negative $V_{fb}$ and $V_{th}$ shift has been suppressed by the reduction of positive fixed charges with Si insertion.
- Mobility improvement at low electric field might be due to suppression of remote charge scattering induced by oxygen vacancies or metal induced defects.
- Mobility improvement at high electric field might be due to formation of La-silicate with high permittivity at high-k/Si interface.

Si insertion technique is effective to improve FET property with EOT of sub 0.6 nm.
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Thank you for your attention