17th INFOS 2011

Effect of Thin Si Insertion at Metal Gate/High-k Interface on Electrical Characteristics of MOS Device with La_2O_3

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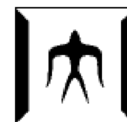
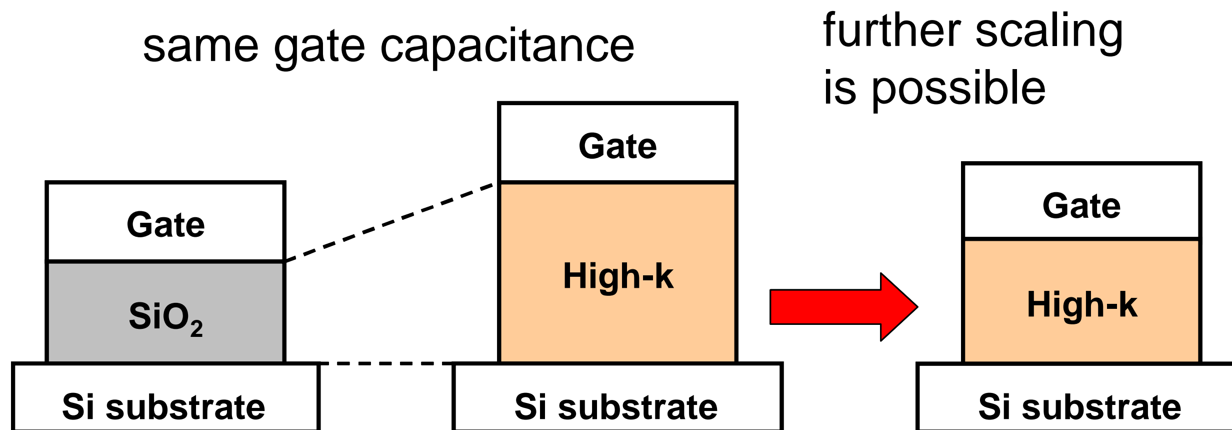
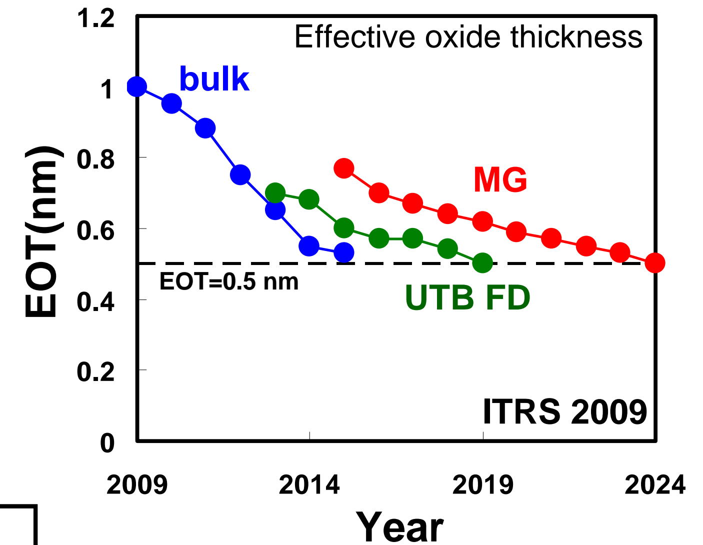


Tokyo Institute of Technology

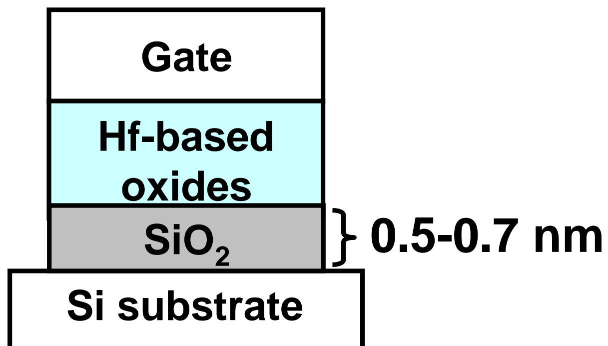
Introduction of high-k Gate Dielectrics





EOT of 0.5 nm is required in the near future

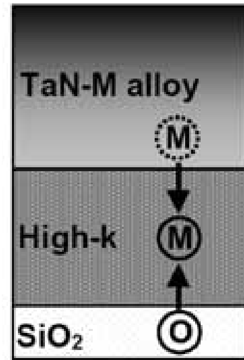
Hf-based oxides are currently in practical use

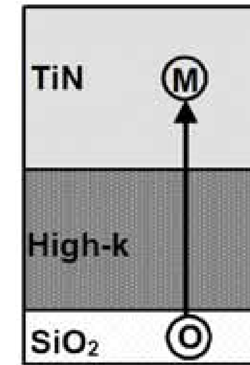


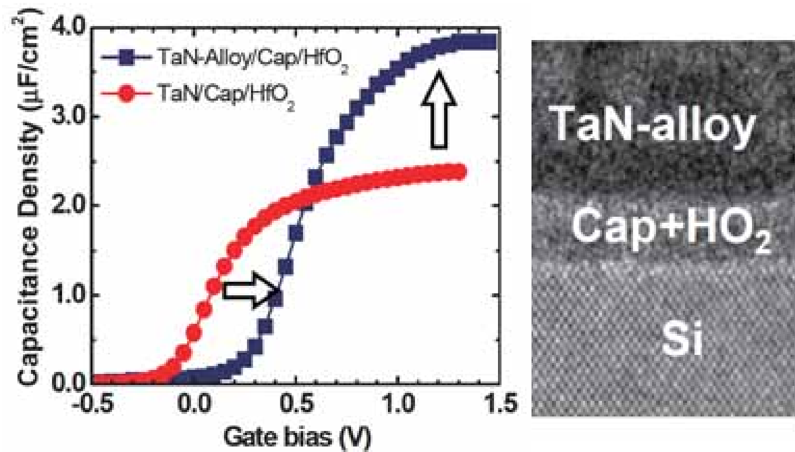
SiO_2-IL would eventually limit the scaling

high-k/Si direct contact without SiO_2-IL is necessary

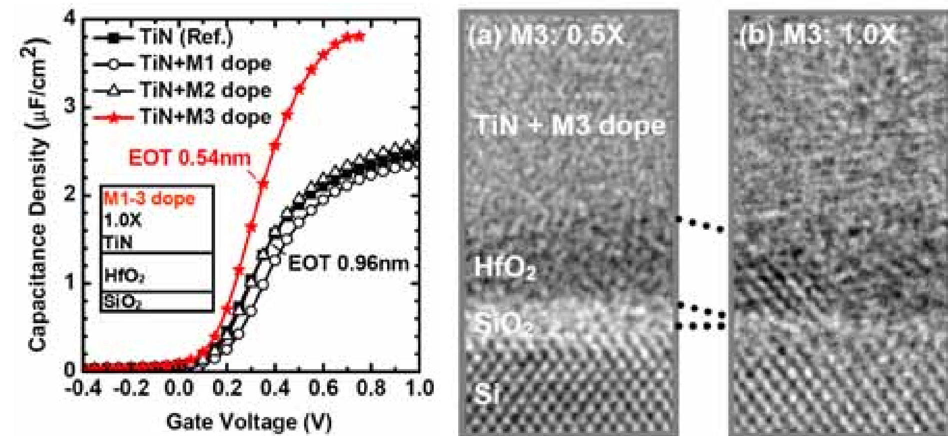
Reports on Direct Contact of HfO_2/Si







K. Choi, et al., VLSI symp. Tech. p.138 (2009).



T. Ando, et al., IEDM, Tech. p.423 (2009).

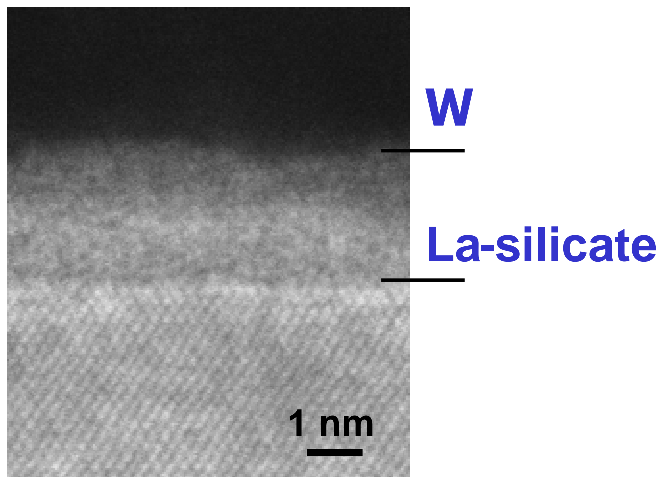
Selection of metal gate material
is the key factor to achieve direct HfO_2/Si structure

Direct Contact of High-k/Si with La_2O_3

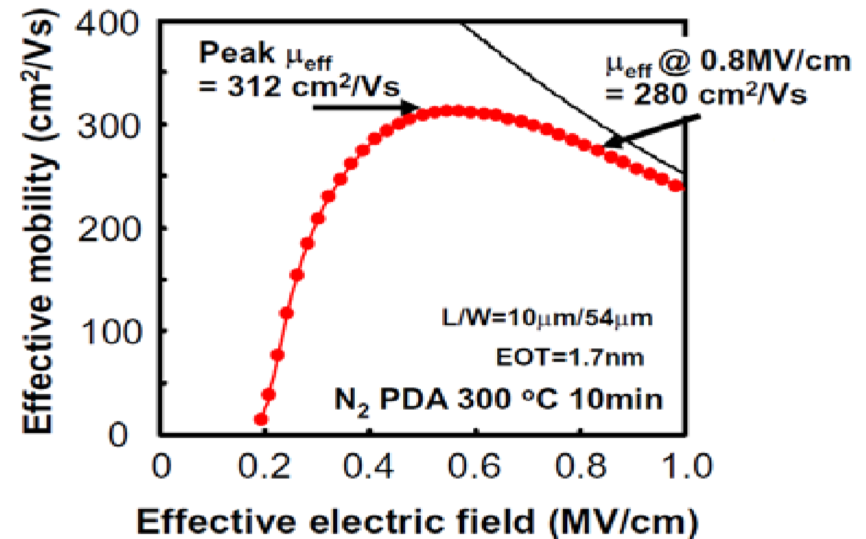
Advantages of La_2O_3

- High permittivity (ε_r=23.4)
- Wide band-gap (E_g=5.6eV)
- Direct contact with Si by forming La-silicate

500 ^{o}C, 30 min



K. Kakushima, et. al.: IWDTF(2008)

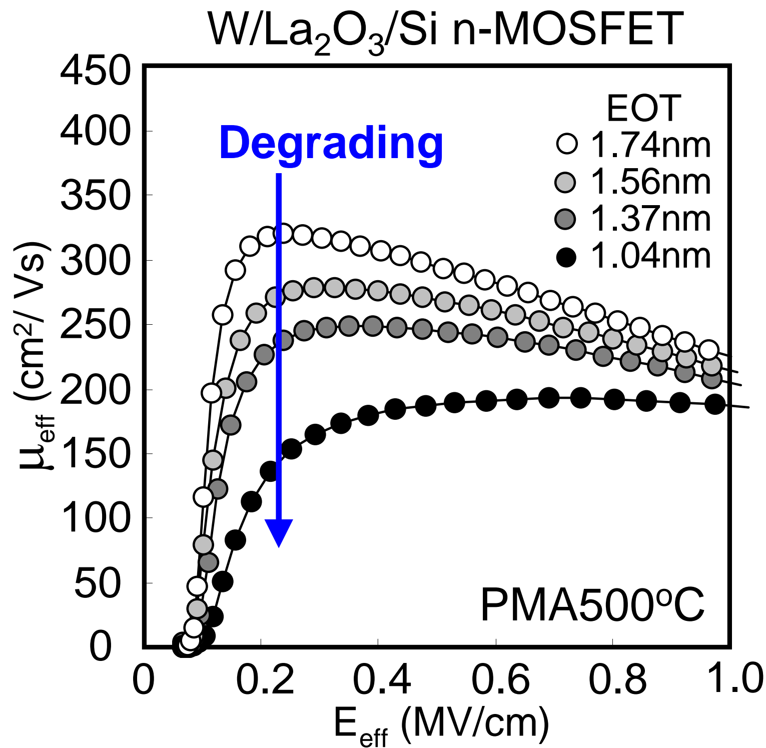


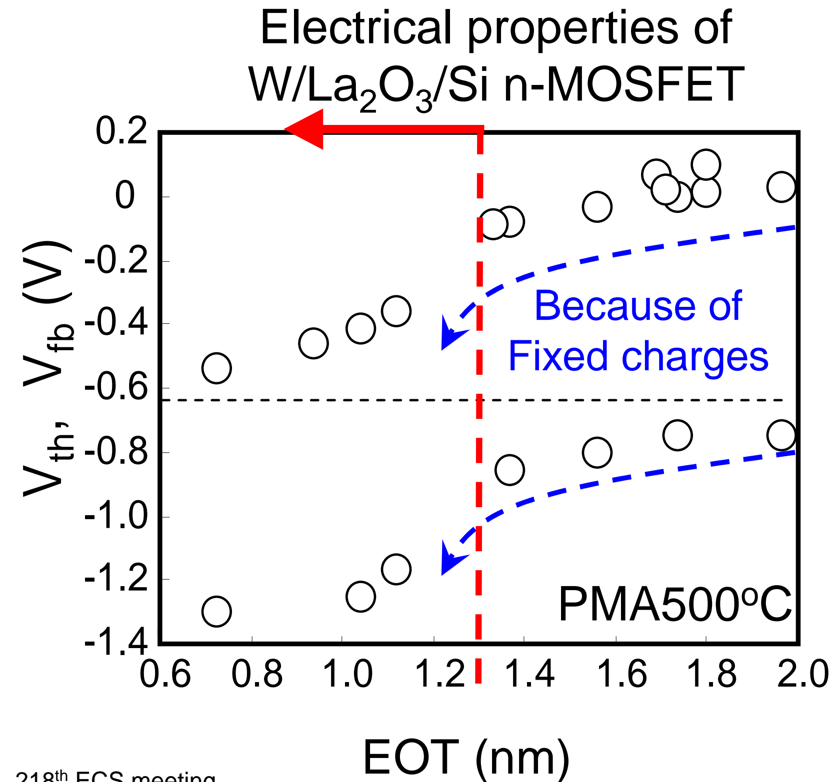
J. A. Ng et al.: IEICE Electronics Express 3 (2006) 316

Fairly nice interfacial property with a peak μ_{eff} of over 300 cm^2/Vs has been reported.

La_2O_3 is expected to be one of the gate dielectrics for next generation devices

Issues for EOT Scaling

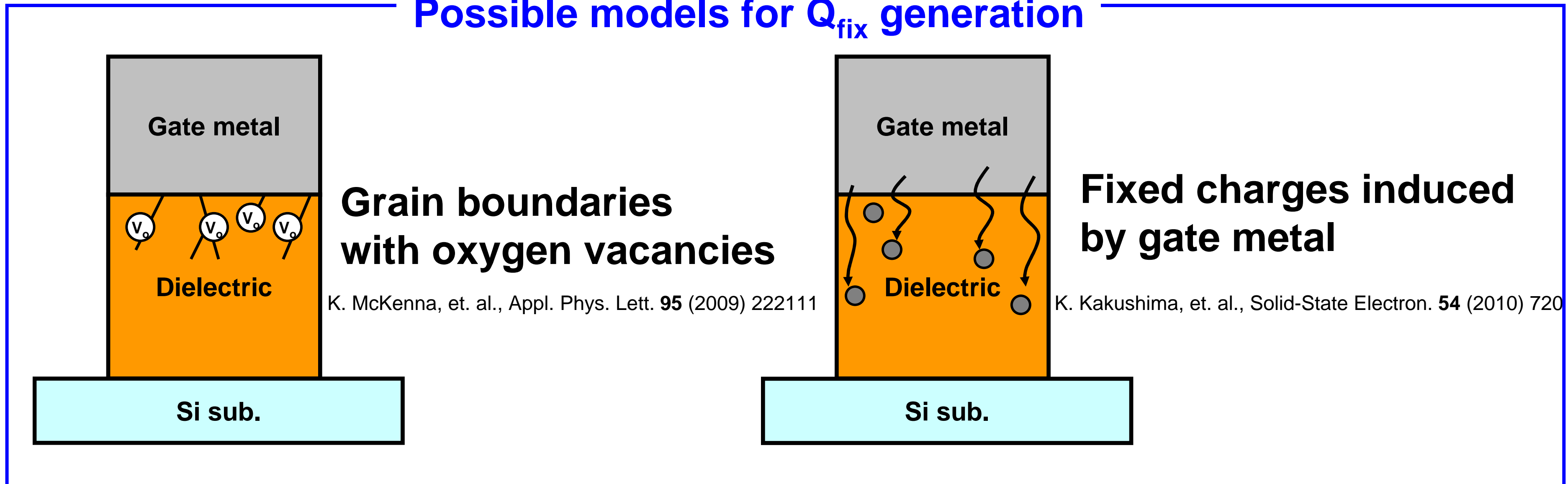




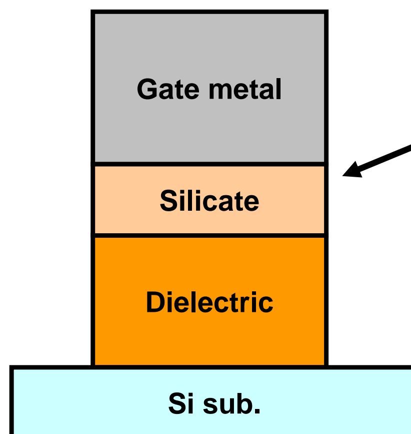
T. Koyanagi, et. al., 218th ECS meeting

Remote charge scattering induced by fixed charges might degrade mobility.

Si Insertion Technique



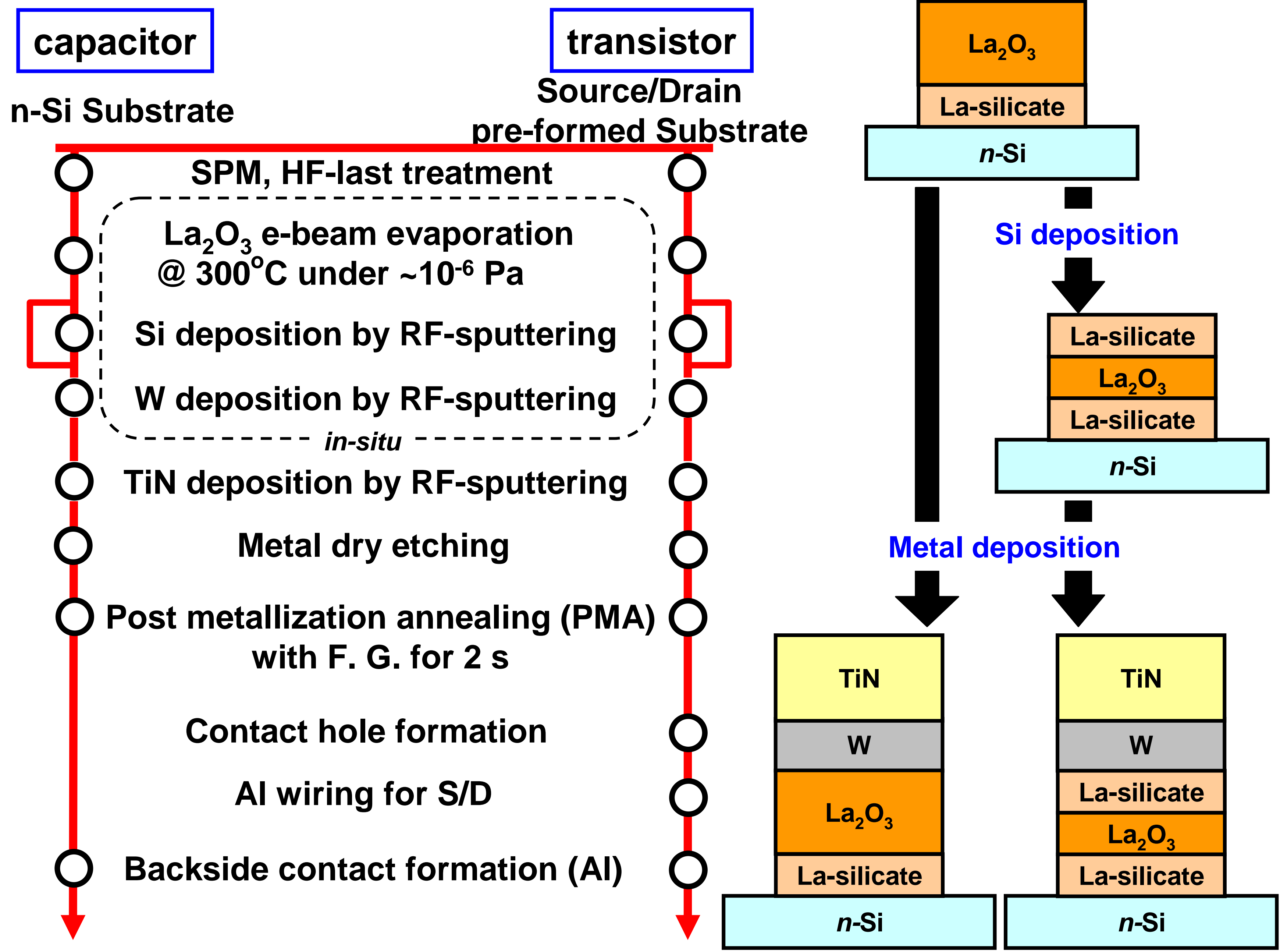
Purpose of this work



Formation of amorphous silicate layer by Si deposition.

Improving mobility by preventing generation of fixed charges

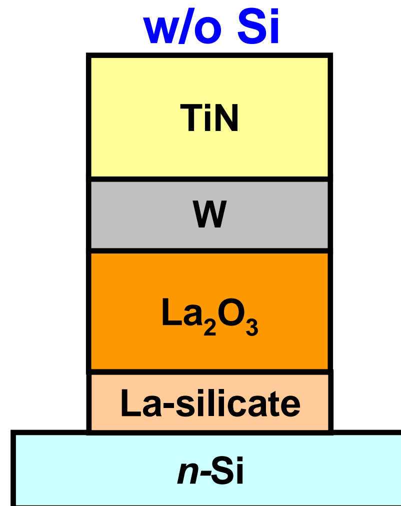
Experimental Procedure



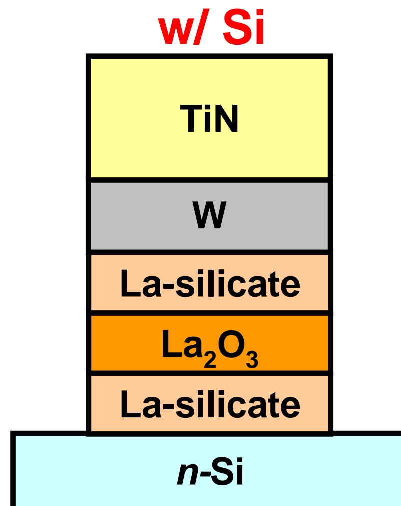
Electrical characteristics of capacitors

C-V Characteristics

w/o Si



w/ Si



TiN/W/Si(0 or 0.3 nm)/La_2O_3(3 nm)

Capacitance ($\mu F/cm^2$)

4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0

w/ Si
EOT=0.62 nm

w/o Si
EOT=0.71 nm

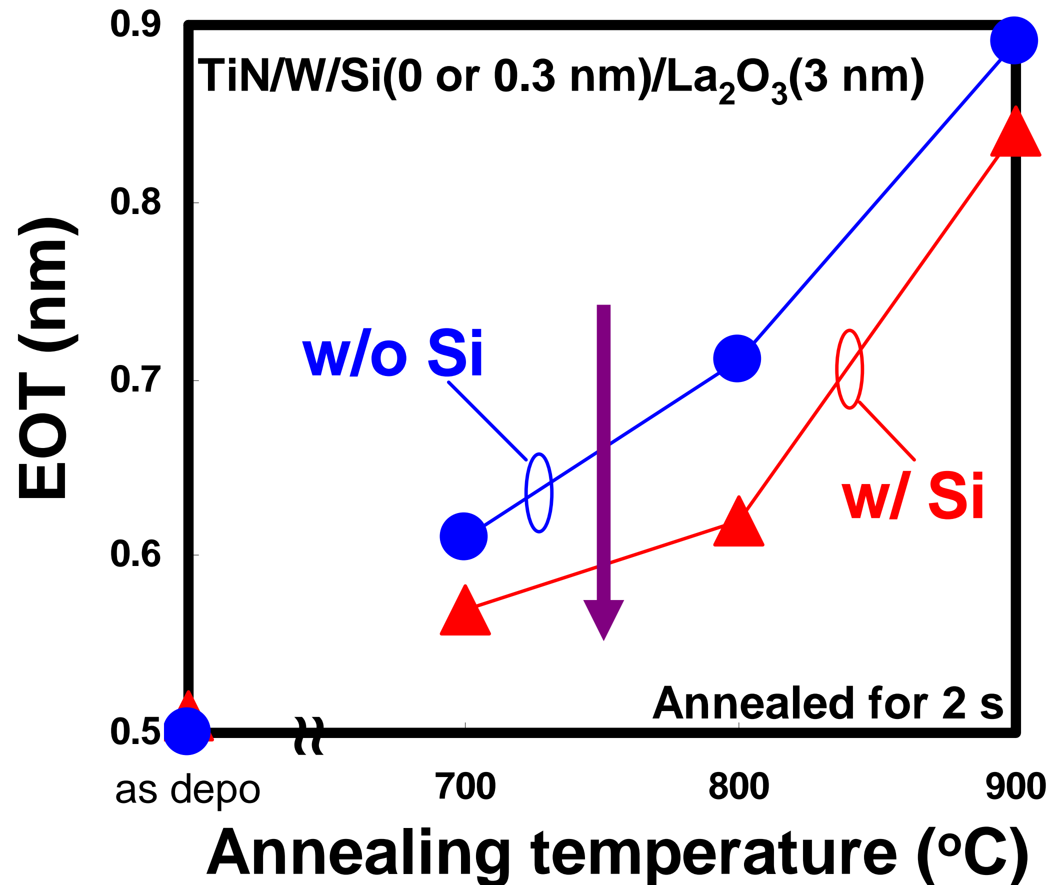
800 °C, 2 s
100 kHz

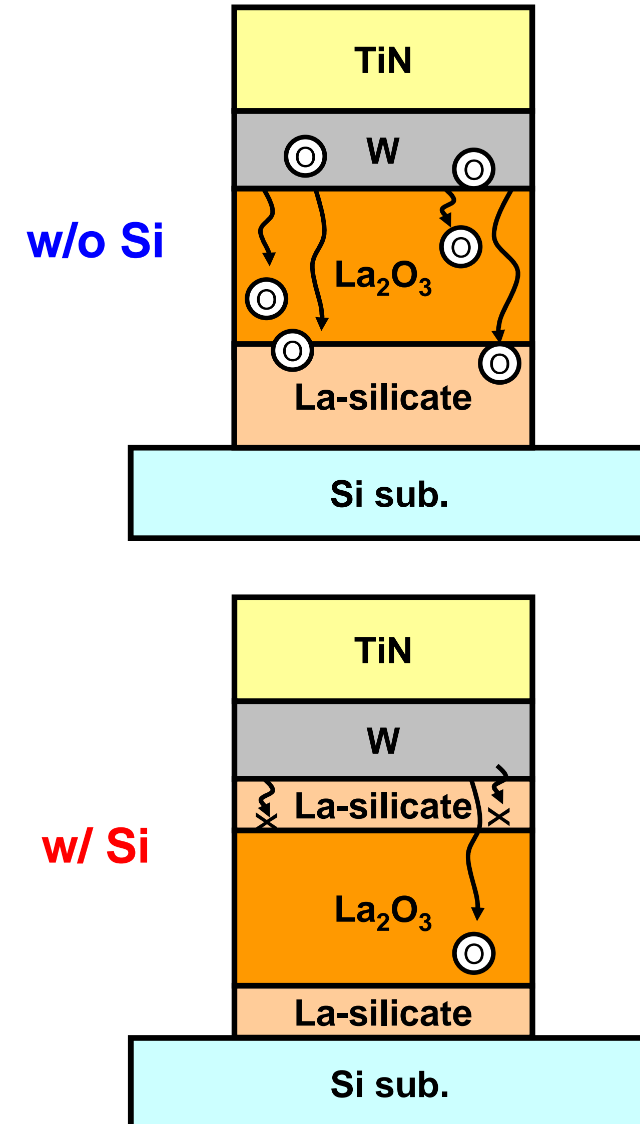
-1.5 -1.0 -0.5 0.0 0.5 1.0

Voltage (V)

Smaller EOT is obtained with Si inserted capacitor

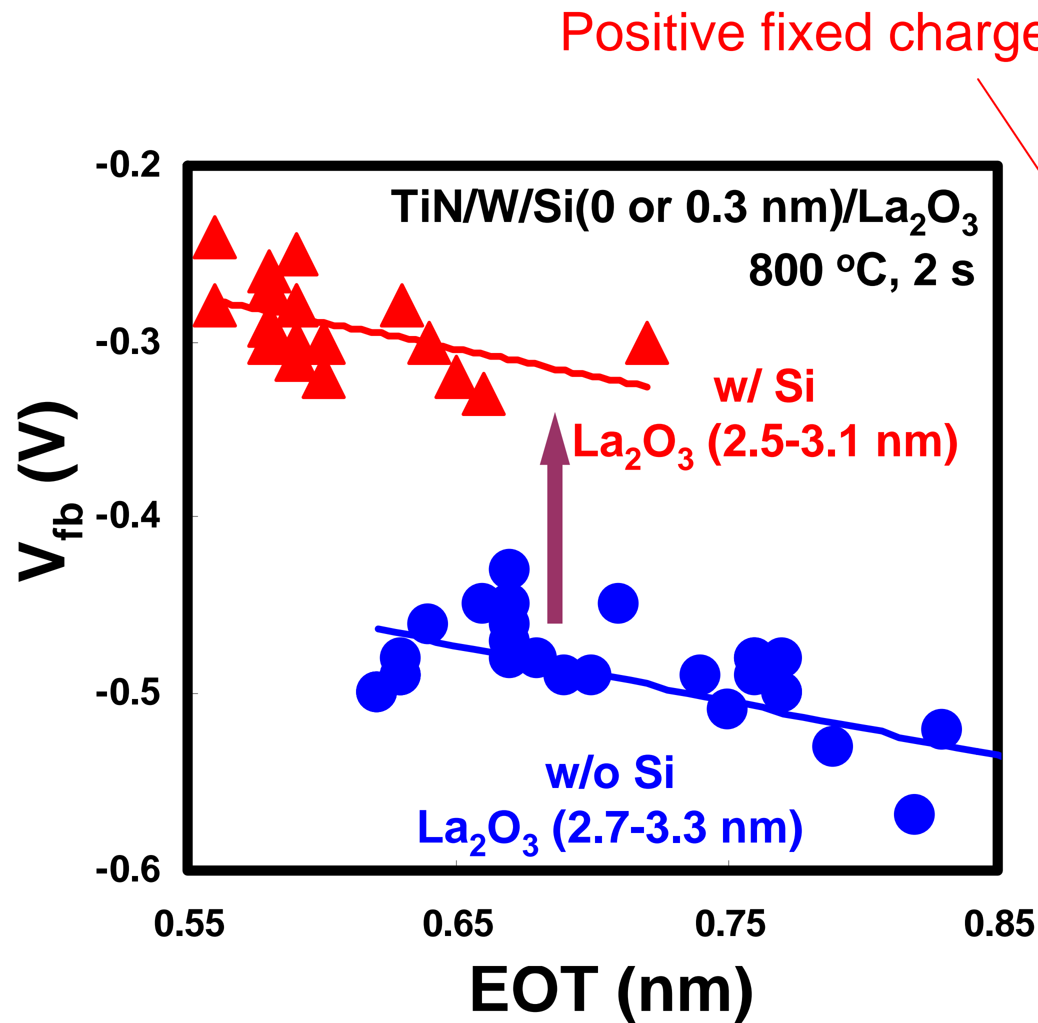
Annealing Temperature Dependence of EOT

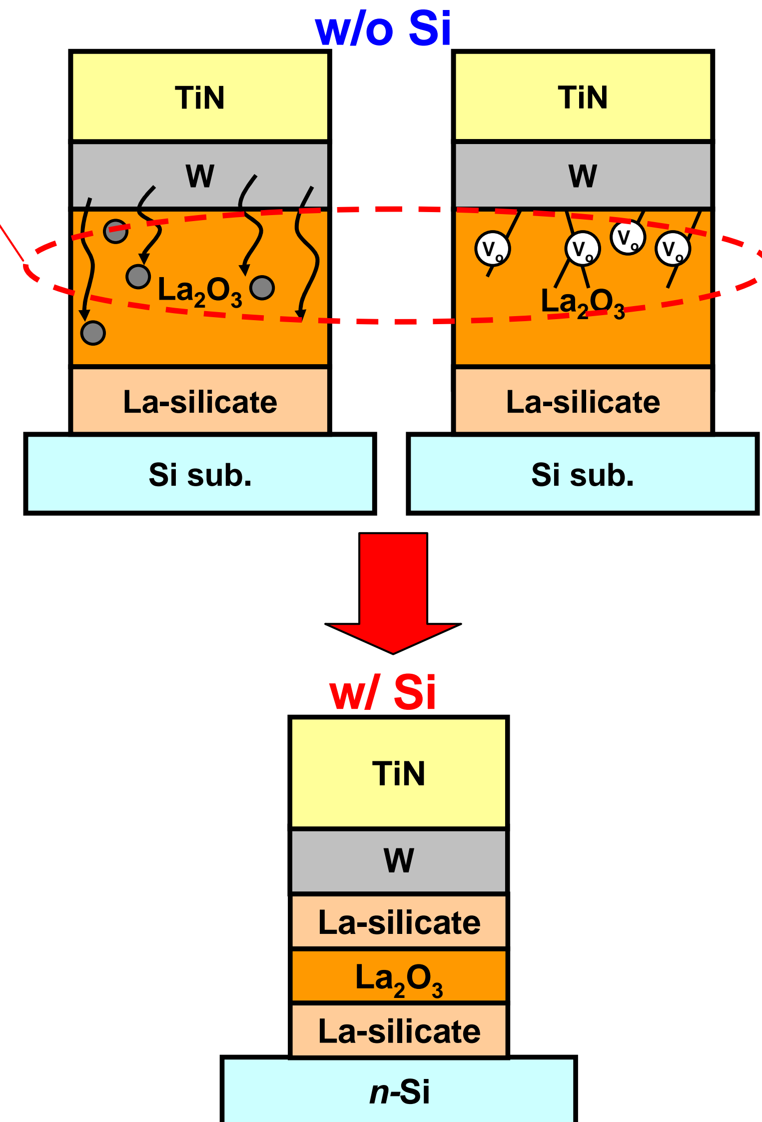




Oxygen diffusion from gate metal might be reduced by La-silicate at metal/high-k interface

V_{fb} Shift Induced by Si Insertion

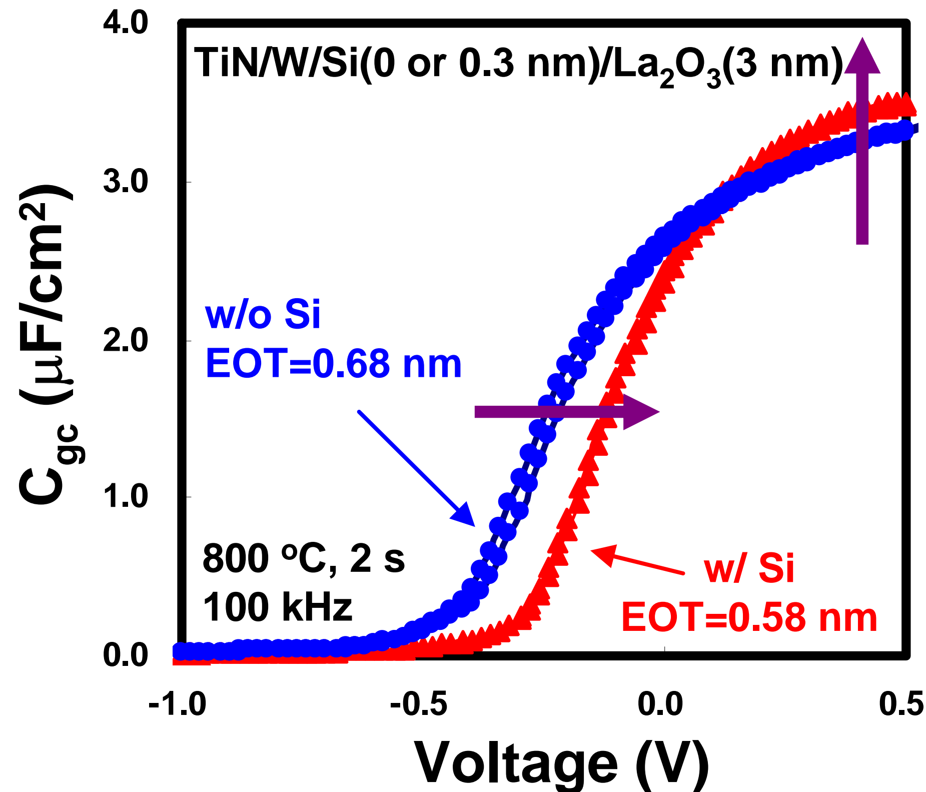


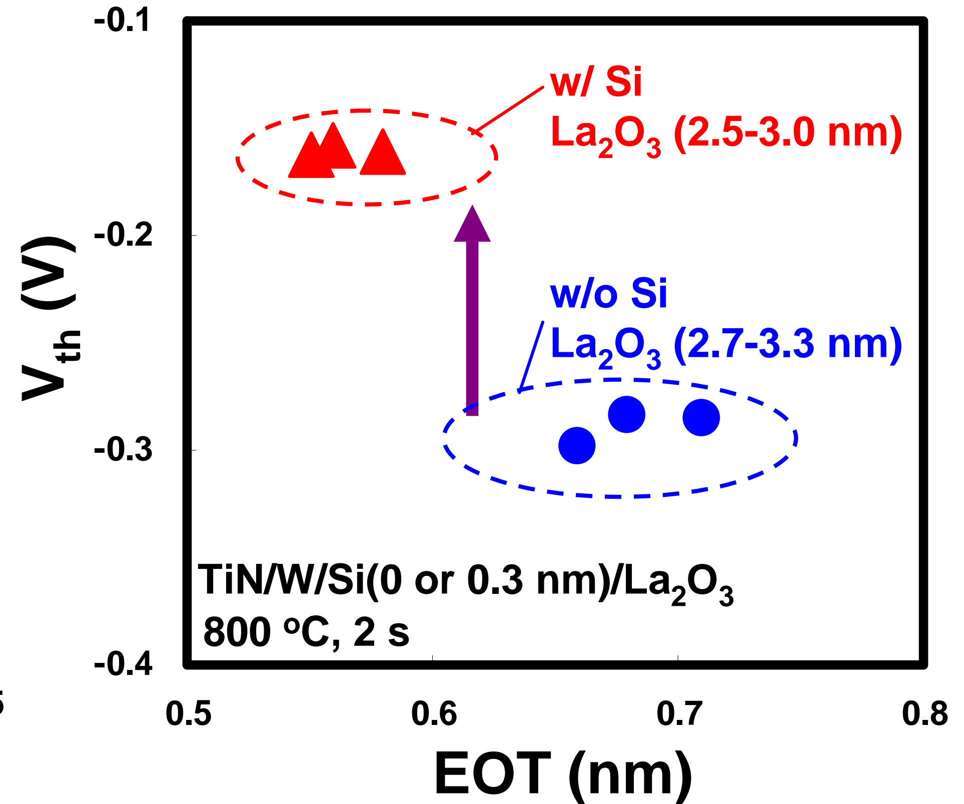


V_{fb} shift indicates reduction of positive fixed charges with Si insertion.

Electrical characteristics of transistors

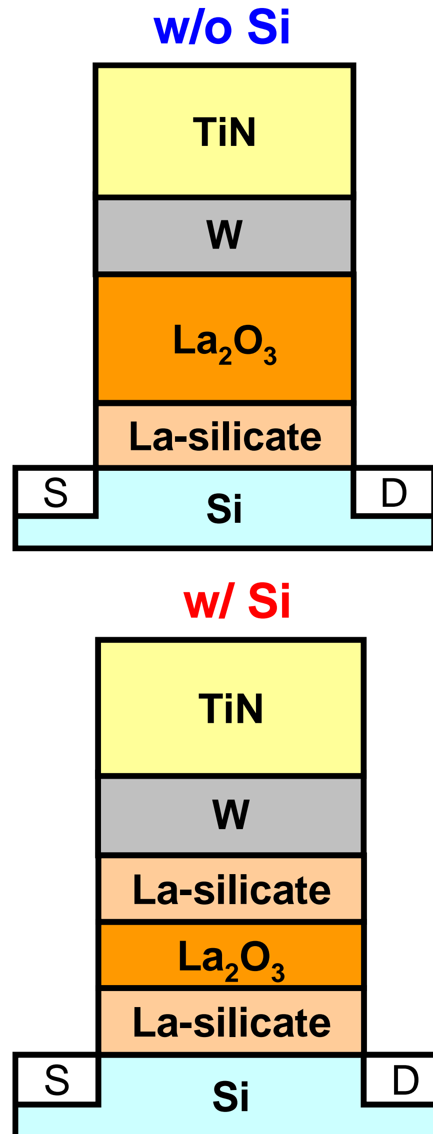
Electrical Characteristics of FETs

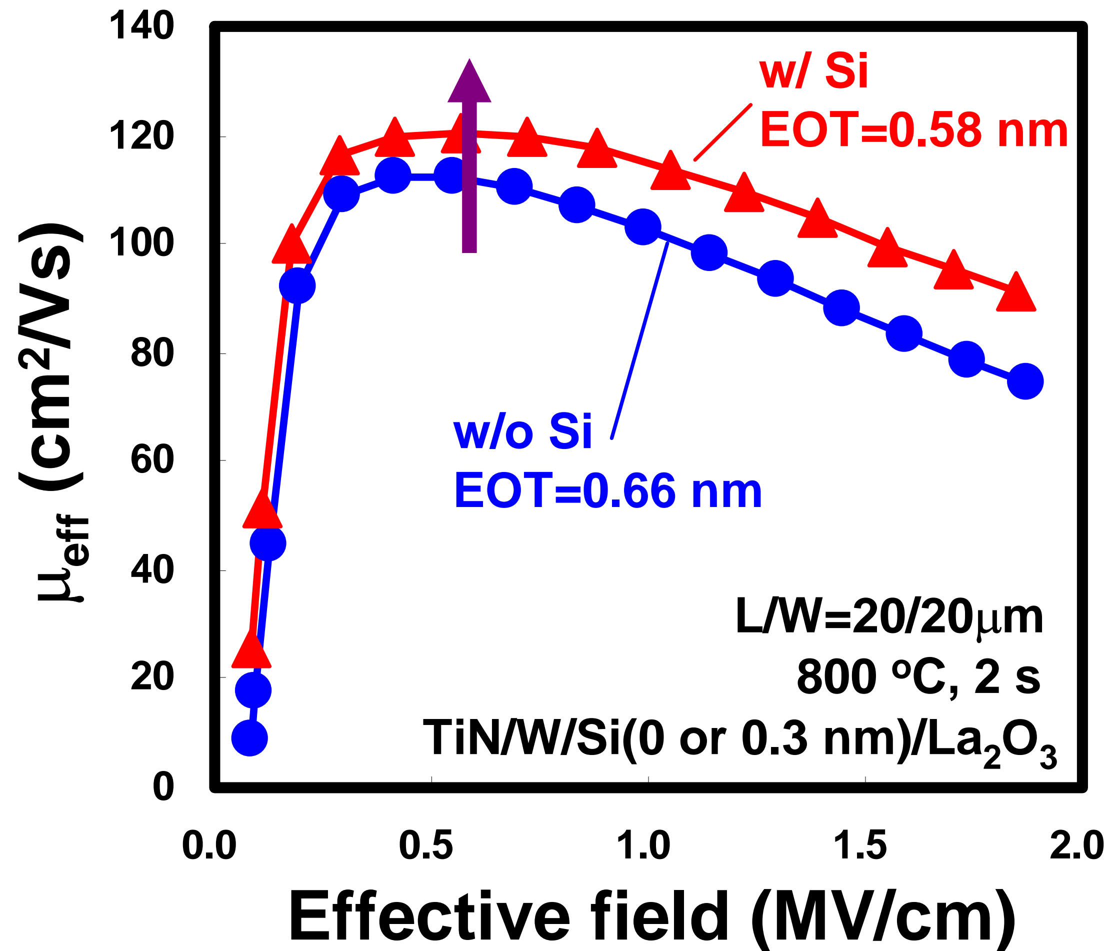




The V_{th} shift and suppression of EOT increase is consistent with capacitors.

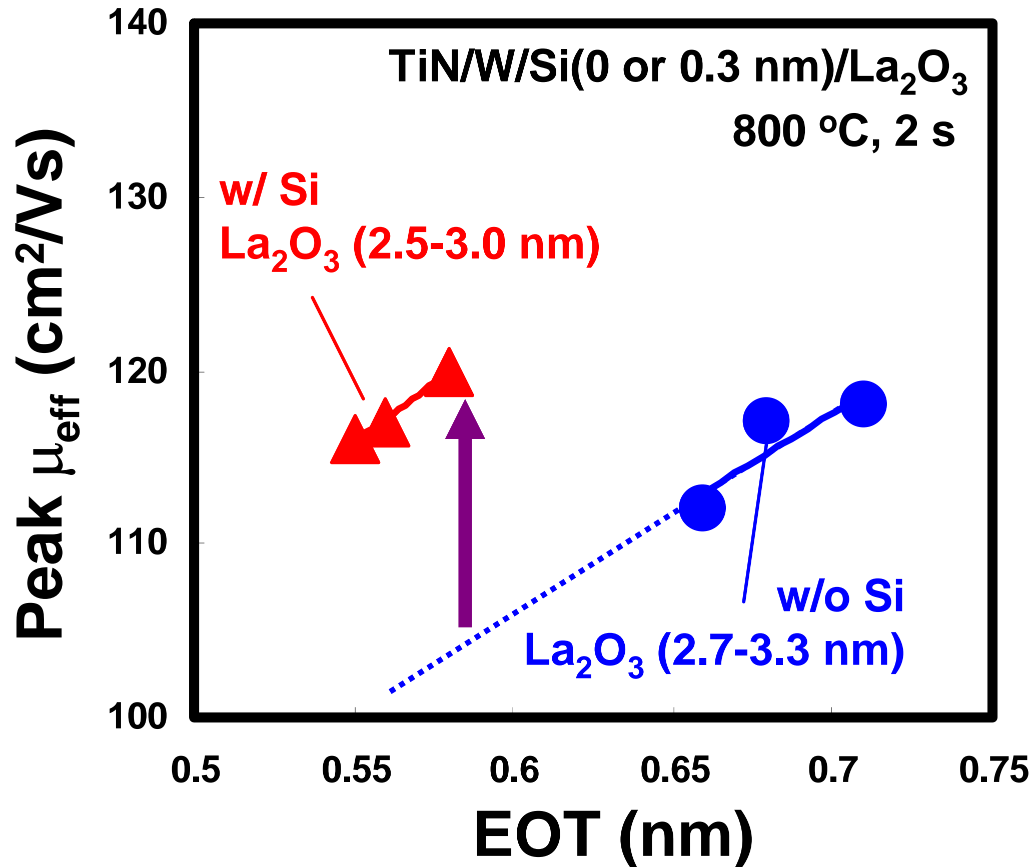
Mobility Comparison

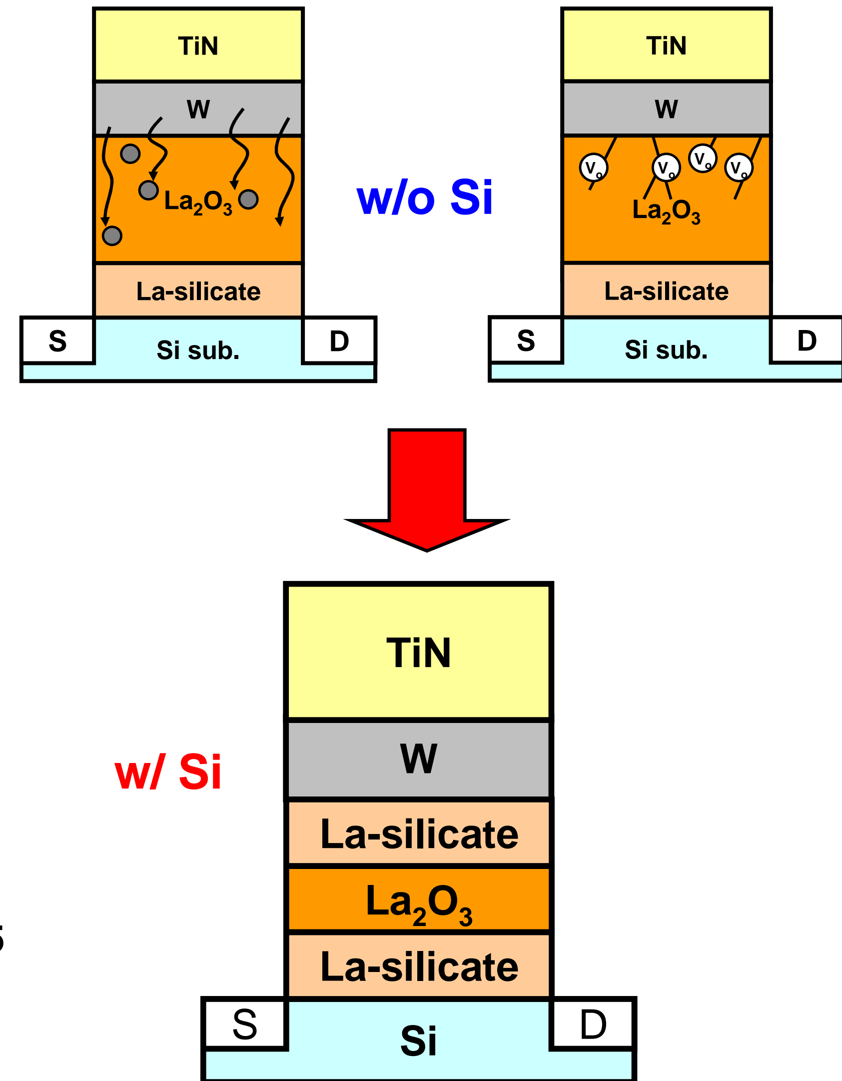




Effective mobility is improved with Si inserted FETs.

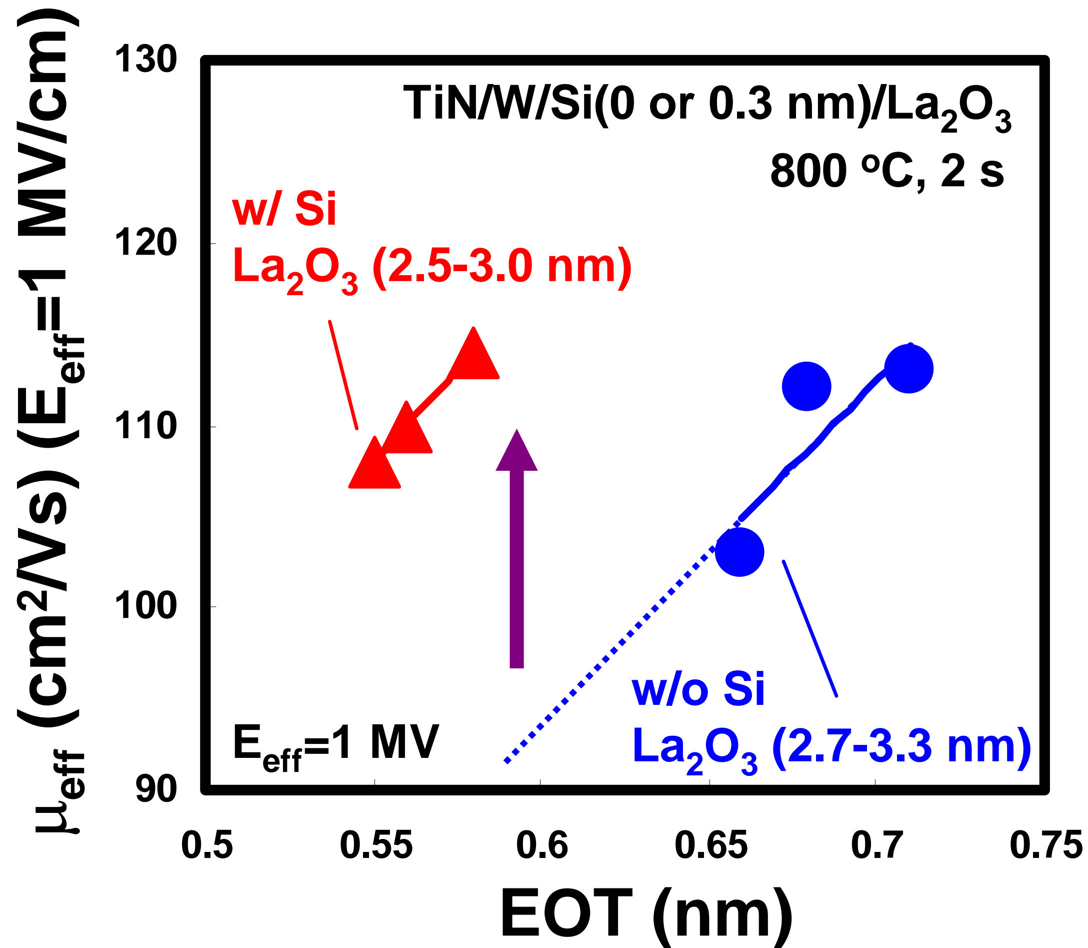
Mobility at Low Electric Field

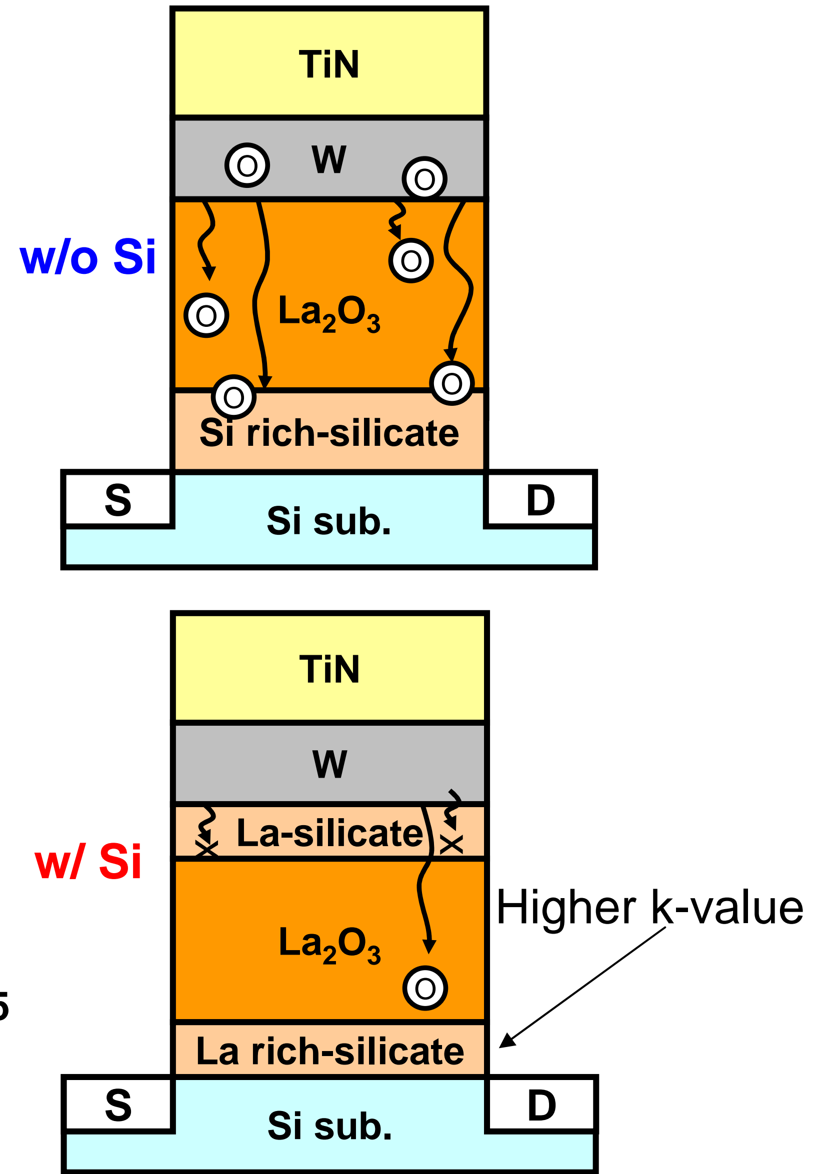




Fixed charges such as oxygen vacancies or metal induced defects are reduced by forming La-silicate at metal/high-k interface.

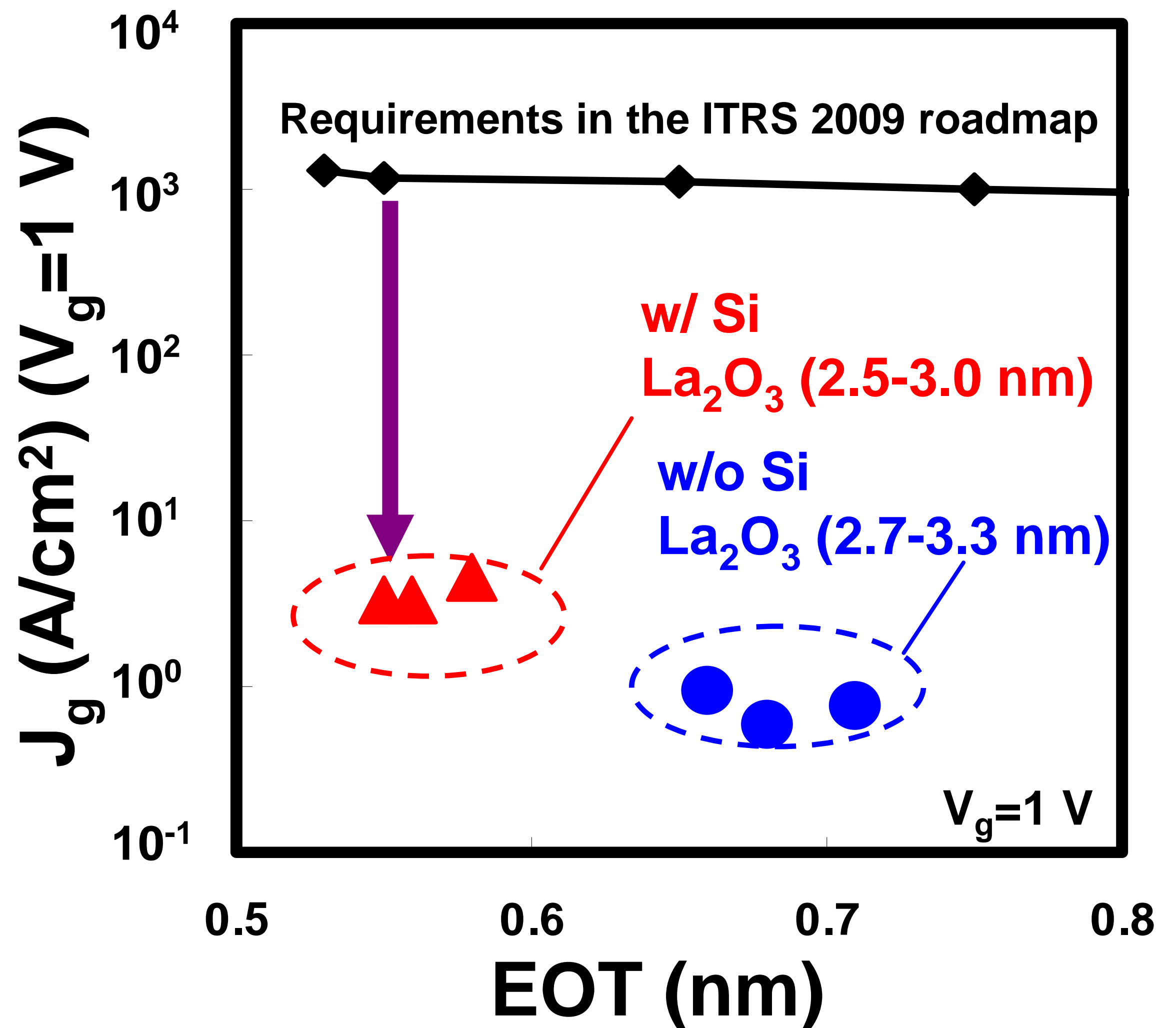
Mobility at High Electric Field





La rich-silicate is formed at La$_2$O$_3$/Si interface with Si inserted FETs.

Leakage Current



A fairly nice J_g of ~10^3 times smaller with respect to the ITRS requirement is achieved.

Conclusions

The effect of Si insertion at metal/La_2O_3 interface has been investigated.

- **Smaller EOT is obtained with Si insertion possibly owing to the reduction of oxygen diffusion.**
- **The negative V_{fb} and V_{th} shift has been suppressed by the reduction of positive fixed charges with Si insertion.**
- **Mobility improvement at low electric field might be due to suppression of remote charge scattering induced by oxygen vacancies or metal induced defects.**
- **Mobility improvement at high electric field might be due to formation of La-silicate with high permittivity at high-k/Si interface.**

Si insertion technique is effective to improve FET property with EOT of sub 0.6 nm.

Acknowledgement

This work has been supported by NEDO.

Thank you for your attention