Effects of surface treatment on electric properties of W/high-*k*/$In_{0.53}Ga_{0.47}As$ capacitors

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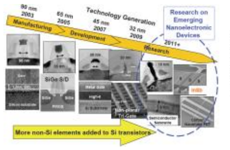
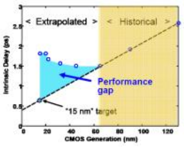
Background

Limits of Si





Points of Improvement:

1. Switching speed
2. Density
3. Power

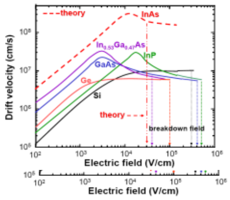
22nm node and below

Parasitic charge interference with channel charge → **Gate delay increases** $C_{ox}\cdot V_{CC}/I_{ON}$

Si replacements are considered for 15nm node and beyond

Increasing carrier mobility can increase the drive current at low bias voltage to reduce the gate delay

High Mobility Material



		Material				
Parameter	Units	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
μ_e at n_s=1E12 cm^{-2}	$cm^2/V.s$	300	7,000	10,000	15,000	30,000
bulk μ_h	$cm^2/V.s$	450	400	200	460	1,250
E_g	eV	1.11	1.43	0.7	0.36	0.17

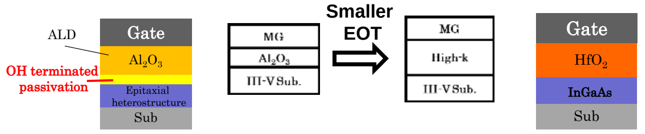
$In_{0.53}Ga_{0.47}As$ ⇒

Carrier transport
Low electron effective mass

Off current
Relatively large Band-gap

Potentially faster and less power consuming

Adopting high-k to III-V



Al_2O_3 suitable but needs to re Replaced with high-k to allow for scaling

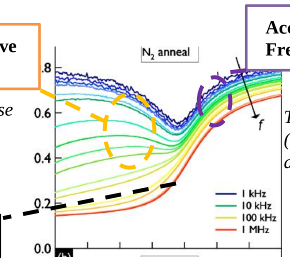
high-k gate stack requirements →

- **Sufficient band offset with semiconductor conduction band**
- **Thermal stability**
- **Low interface trap density**

capacitance at negative biases

Interface trap response is the main reason

Accumulation and flatband Frequency Dispersion



Thermally activated trapping (both conduction band and mid-gap fast traps)

High C_{dep}

Inefficient fermi level bending around mid-gap

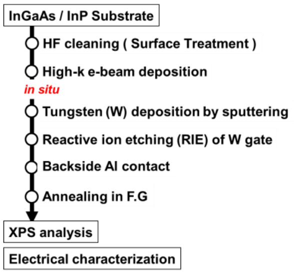
Purpose

Optimizing high-k/$In_{0.53}Ga_{0.47}As$ interface for improved electrical properties

Surface treatment prior to high-k deposition → Monolayer Si coating

Deposition and annealing condition investigation → Depo/pre-depo heating

Experimental Method

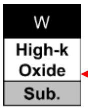


InGaAs / InP Substrate
- HF cleaning (Surface Treatment)
- High-k e-beam deposition

in situ
- Tungsten (W) deposition by sputtering
- Reactive ion etching (RIE) of W gate
- Backside Al contact
- Annealing in F.G

XPS analysis

Electrical characterization



Surface treatments (thermal / chemical)

Results and discussion

Surface chemical treatment

1-Concentrated HF treatment

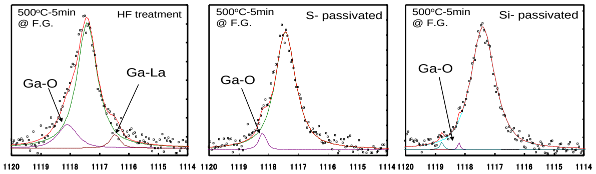
Native oxide removal

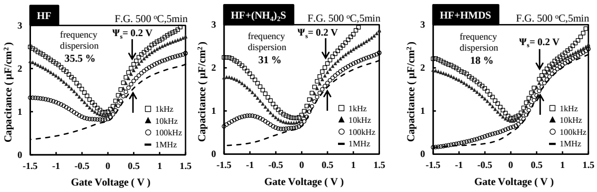
2-$(NH_4)_2S$ treatment

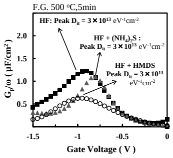
S-terminate Prevent re-oxidation

3-HMDS vapor coating

Mono-layer Si coating

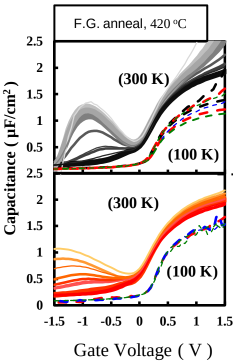






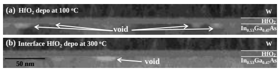
Mono-layer Si insertion results in native oxide & frequency dispersion reduction

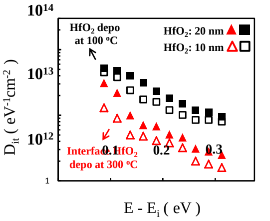
Surface thermal treatment



Surface treatment with concentrated HF
↓
Vacuum anneal at 450 °C (30min)
↓
Depo at 100 °C

Surface treatment with concentrated HF
↓
Vacuum anneal at 450 °C (30min)
↓
Depo at 300 °C (0.5nm)
↓
Depo at 100 °C





By depositing the interface at high temperature, D_{it} is monotonically Decreased along the InGaAs bandgap

Conclusion

III-V Semiconductor strong candidate for high performance devices

-high electron mobility (injection velocity)
-low power dissipation

Careful surface treatment can significantly improve CV characteristics of the high-k/InGaAs capacitors.

Further investigation to systematically diagnose the mechanism of interface state suppression by surface treatment methods is needed.